TEXAS INSTRUMENTS
DCR021205, DCR022405
SBVS028D – DECEMBER 2000 – REVISED AUGUST 2021

DCR02 Series, 2-W, 1000-V_{RMS} Isolated, Regulated DC/DC Converter Modules

1 Features

- 1-kV isolation (operational): 1-second test
- Continuous voltage applied across isolation barrier: 60 VDC / 42.5 VAC
- UL1950 recognized component
- 10-pin PDIP and SOP packages
- Input voltage: 12 V or 24 V
- 5-V output voltage
- Device-to-device synchronization
- 400-kHz switching frequency
- Short-circuit protection
- Thermal protection
- High efficiency
- 125 FITS at 55°C

2 Applications

- Point-of-use power conversion
- Digital interface power
- Ground loop elimination
- Power-supply noise reduction

3 Description

The DCR02 family is a series of high-efficiency, input-isolated, output-regulated DC/DC converters. In addition to 2-W nominal, galvanically-isolated output power capability, this range of converters offers very low output noise and high accuracy.

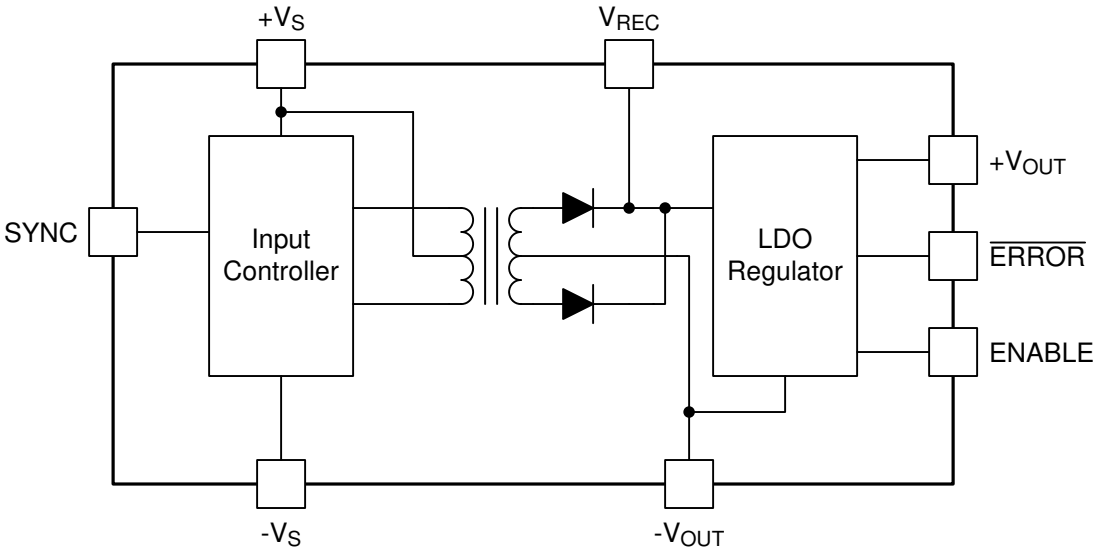
The DCR02 family is implemented in standard molded device packaging, providing standard JEDEC outlines suitable for high-volume assembly. They are manufactured using the same technology as standard device packages, thereby achieving very high reliability.

WARNING: This product has operational isolation and is intended for signal isolation only. It must not be used as a part of a safety isolation circuit requiring reinforced isolation. See definitions in *Section 7.3*.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DCR02xxxx	PDIP (10)	22.86 mm × 6.61 mm
	SOP (10)	22.86 mm × 6.61 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



DCR02 Block Diagram

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4 Revision History

Changes from Revision C (November 2016) to Revision D (August 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1
• Updated *Section 1*	1
• Added links to *Section 2*	1
• Added Load Regulation plots to *Section 6.6*	6
• Added sentence to *Section 7.3.1.3*	8

Changes from Revision B (December 2007) to Revision C (November 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table and *Supplemental Ordering Information* image; see *Package Option Addendum* at the end of the data sheet	1
• Changed *DCR02 PinOut* image in *Pin Configuration and Functions*	3
• Changed Pin 1 From: V_S To: $+V_S$	3
• Changed Pin 8 From: $0V_{OUT}$ To: $–V_{OUT}$	3
• Changed Pin 9 From: V_O To: $+V_{OUT}$	3
• Changed Pin 17 From: $0V_{IN}$ To: $–V_S$	3
• Deleted Lead temperature (PDIP package), 270°C maximum, from *Absolute Maximum Ratings* table	4
• Added *Isolation* subsection to the *Feature Description*	7

5 Pin Configuration and Functions

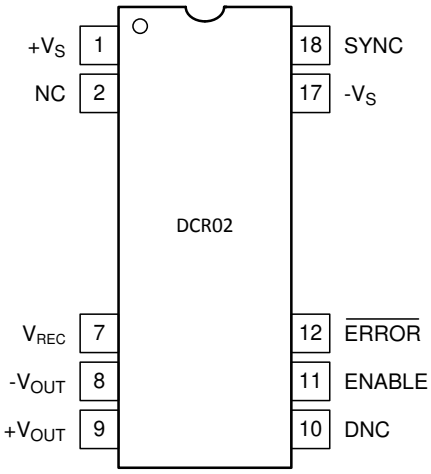


Figure 5-1. NVE or DVS Package 10-Pin PDIP or SOP Top View

Table 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	$+V_S$	I	Voltage input
2	NC	—	No connection
7	V_{REC}	O	Rectified output
8	$–V_{OUT}$	O	Output ground
9	$+V_{OUT}$	O	Voltage output
10	DNC	—	Do not connect
11	ENABLE	I	Output voltage enable
12	$\overline{ERROR}$	O	Error flag active low
17	$–V_S$	I	Input ground
18	SYNC	I	Synchronization input

(1) I = input and O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	DCR021205		15	V
	DCR022405		29	
Reflow solder temperature	SOP package (surface temperature of device body or pins)		260	°C
Storage temperature, T_{stg}		–60	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	DCR021205	10.8	12	13.2	V
	DCR022405	21.6	24	26.4	
Operating temperature		–40		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		DCR02		UNIT
		NVE (PDIP)	DVS (SOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24	24	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7	7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24	24	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At T_A = +25°C, V_S = nominal, I_{OUT} = 10 mA, C_{OUT} = 0.1-µF ceramic, and C_{IN} = 2.2-µF ceramic, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT						
Nominal output voltage (+V_{OUT})				5		V
Setpoint accuracy				0.5%	2%	
Maximum output current					400	mA
Output short-circuit protected	Duration			Infinite		
Line regulation				1		mV/V
Over line and load	10-mA to 400-mA load, over +V_S range			1%	2.5%	
Temperature variation	–40°C to 70°C			1%		
Ripple and noise	DCR0212 ripple, 20−MHz bandwidth, 50% load(1)			18		mV_{PP}
	DCR0212 noise, 100−MHz bandwidth, 50% load(1)			20		
	DCR0224 ripple, 20−MHz bandwidth, 50% load(1)			18		
	DCR0224 noise, 100−MHz bandwidth, 50% load(1)			25		
INPUT						
Nominal voltage (+V_S)	DCR022405			12		V
	DCR021205			24		
Voltage range			–10%		10%	
Supply current	DCR021205	I_O = 0 mA		15		mA
		I_O = 10 mA		23		
		I_O = 400 mA		250		
	DCR022405	I_O = 0 mA		15		
		I_O = 10 mA		17		
		I_O = 400 mA		129		
Reflected ripple current	20−MHz bandwidth, 100% load(1)			8		mA_{PP}
ISOLATION						
Voltage	1-s flash test	Voltage	1			kVrms
		dV/dt			500	V/s
		Leakage current			30	nA
	Continuous working voltage across isolation barrier	DC			60	VDC
		AC			42.5	VAC
Barrier capacitance				25		pF
OUTPUT ENABLE CONTROL						
Logic high input voltage			2		V_{REC}	V
Logic high input current	2 < V_{ENABLE} < V_{REG}			100		nA
Logic low input voltage			–0.2		0.5	V
Logic low input current	0 < V_{ENABLE} < 0.5			100		nA
ERROR FLAG						
Logic high open collector leakage	V_{ERROR} = 5 V				10	µA
Logic low output voltage	Sinking 2 mA				0.4	V
THERMAL SHUTDOWN						
Junction temperature	Temp activated			150		°C
	Temp deactivated			130		
SYNCHRONIZATION PIN						
Internal oscillator frequency			720	800	880	kHz
External synchronization frequency			720		880	kHz

At T_A = +25°C, V_S = nominal, I_{OUT} = 10 mA, C_{OUT} = 0.1-µF ceramic, and C_{IN} = 2.2-µF ceramic, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External synchronization signal high		2.5		3	V
External synchronization signal low		0		0.4	V
External capacitance on SYNC pin				3	pF

(1) Ceramic capacitors, C_{IN} = 2.2 µF, C_{FILTER} = 1 µF, and C_{OUT} = 0.1 µF.

6.6 Typical Characteristics

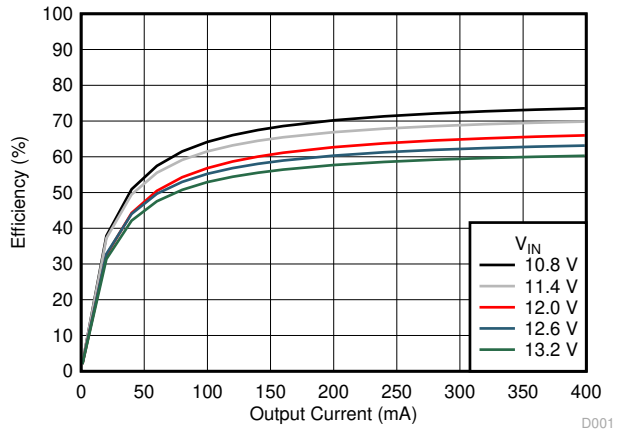


Figure 6-1. DCR021205 Efficiency versus Output Current

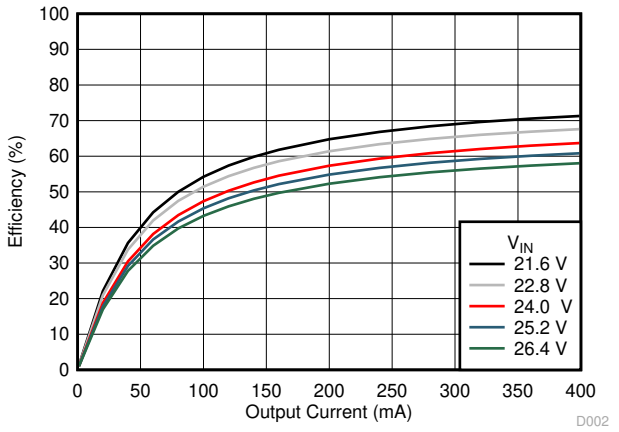


Figure 6-2. DCR022405 Efficiency vs Output Current

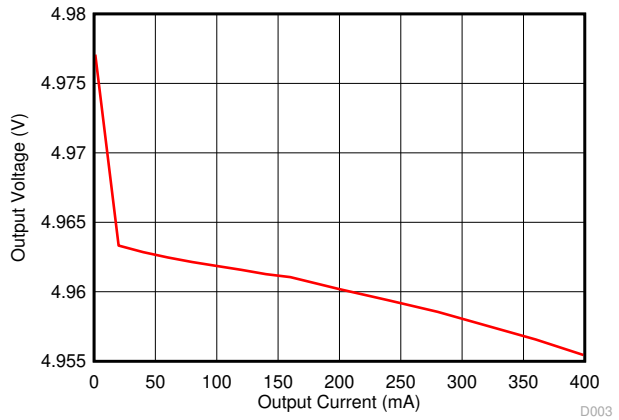


Figure 6-3. DCR021205 Load Regulation

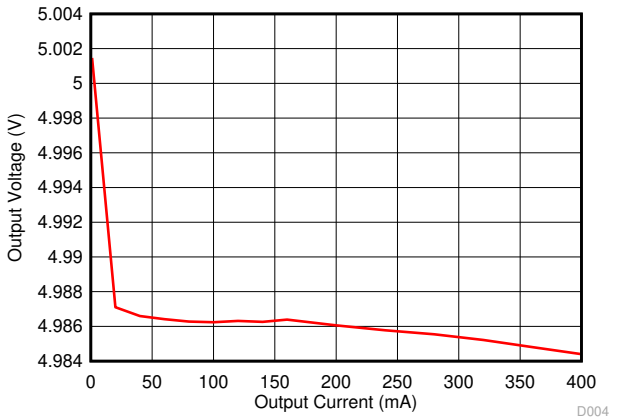


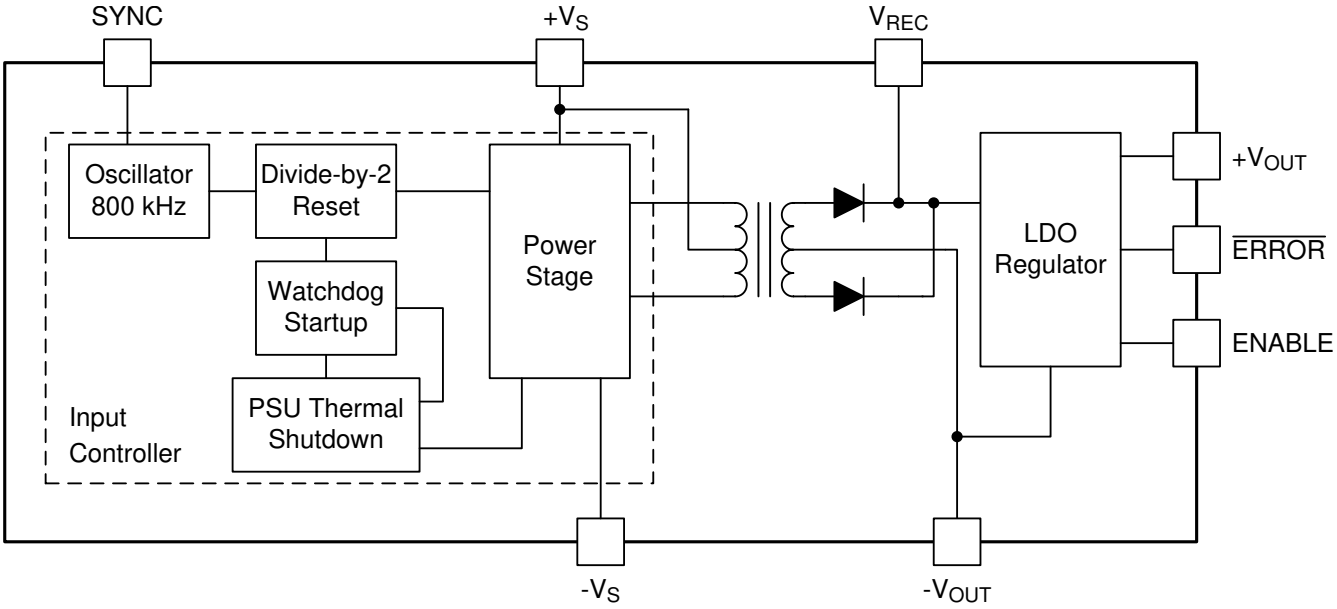
Figure 6-4. DCR022405 Load Regulation

7 Detailed Description

7.1 Overview

The DCR02 series of power modules offer isolation from a regulated power supply operating from 12-V or 24-V inputs. The DCR02s provide a regulated 5-V output voltage at a nominal output power of 2 W. The DCR02 devices include a low dropout linear regulator internal to the device to achieve a well-regulated output voltage. The DCR02 devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS and DMOS process.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Isolation

Underwriters Laboratories (UL)™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42.5 V_{RMS} or 60 V_{DC} peak.

7.3.1.1 Operation or Functional Isolation

The type of isolation used in the DCR02 products is referred to as operational or functional isolation. Insulated wire used in the construction of the transformer acts as the primary isolation barrier. A high-potential (hipot), one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation must never be used as an element in a safety-isolation system.

7.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

Note

The DCR02 products do not provide basic or enhanced isolation.

7.3.1.3 Working Voltage

For a device with operational isolation, the continuous working voltage that can be applied across the device in normal operation must be less than 42.5 V_{RMS} or 60 V_{DC}. Ensure that both input and output voltages maintain normal SELV limits.

WARNING

Do not use the device as an element of a safety isolation system that exceeds the SELV limit.

If the device is expected to function correctly with more than 42.5 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

7.3.1.4 Isolation Voltage Rating

The terms *Hipot test*, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* all relate to the same thing; a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCR02 series of DC/DC converters are all 100% production tested at 1.0 kV_{AC} for one second.

7.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCR02 series of DC/DC converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

7.3.2 Power Stage

The DCR02 series of devices use a push-pull, center-tapped topology. The DCR02 devices switch at 400 kHz (divide-by-2 from an 800-kHz oscillator). The internal transformer's output is full wave rectified and filtered by the external 1-µF ceramic capacitor connected to the V_{REC} pin. An internal low-dropout regulator provides a well-regulated output voltage over the operating range of the device.

7.3.3 Oscillator and Watchdog

The onboard, 800-kHz oscillator generates the switching frequency through a divide-by-2 circuit. The oscillator can be synchronized to other DCR02 device circuits or an external source, and is used to minimize system noise.

A watchdog circuit monitors the operation of the oscillator circuit. The oscillator can be disabled by pulling the SYNC pin low. When the SYNC pin goes low, the output pins transition into tri-state mode, which occurs within 2 µs.

7.3.4 $\overline{\text{ERROR}}$ Flag

The DCR02 has an $\overline{\text{ERROR}}$ pin which provides a *power good* flag, as long as the internal regulator is in regulation. If the $\overline{\text{ERROR}}$ output is required, place a 10-kΩ resistor between the $\overline{\text{ERROR}}$ pin and the output voltage.

7.3.5 Synchronization

When more than one DC/DC converter is switching in an application, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCR02 series of devices overcome this interference by allowing devices to be synchronized to one another. Synchronize up to eight devices by connecting the SYNC pins of each device, taking care to minimize the capacitance of tracking. Stray capacitance (greater than 3 pF) reduces the switching frequency, or can sometimes stop the oscillator circuit. The maximum recommended voltage applied to the SYNC pin is 3 V.

For an application that uses more than eight synchronized devices use an external device to drive the SYNC pins. The *External Synchronization of the DCP01/02 Series of DC/DC Converters Application Report* (SBAA035) describes this configuration.

Note

During the start-up period, all synchronized devices draw maximum current from the input simultaneously. A ceramic capacitor must be connected close to each device's input pin. A 2.2-µF ceramic capacitor is required.

7.3.6 Construction

The basic construction of the DCR02 series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCR02 series of devices are constructed using an IC, low dropout linear regulator, rectifier diodes, and a wound magnetic toroid on a leadframe. Because the package contains no solder, the devices do not require any special printed-circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

7.3.7 Decoupling – Ripple Reduction

Due to the very low forward resistance of the DMOS switching transistors, high current demands are placed upon the input supply for a short time. By using a high-quality, low Equivalent Series Resistance (ESR) ceramic input capacitor of 2.2-µF, placed close to the IC supply input pins, the effects on the power supply can be minimized.

The high switching frequency of 400 kHz allows relatively small values of capacitors to be used for filtering the rectified output voltage. A good-quality, low-ESR, 1-µF ceramic capacitor placed close to the V_{REC} pin and output ground is required and reduces the ripple. The output at V_{REC} is full wave rectified and produces a ripple of 800 kHz.

TI recommends that a 0.1-µF, low-ESR ceramic capacitor is connected close to the output pin and ground to reduce noise on the output. The capacitor values listed are minimum values. If lower ripple is required, the filter capacitor must be increased in value to 2.2 µF.

As with all switching power supplies, the best performance is obtained with low ESR ceramic capacitors connected close to the device pins. If low-ESR ceramic capacitors are not used, the ESR generates a voltage drop when the capacitor is supplying the load power. Often a larger capacitor is chosen for this purpose, when a low ESR, smaller capacitor would perform as well.

Note

TI does not recommend that the DCR02 be fitted using an IC socket, as this degrades performance.

7.4 Device Functional Modes

7.4.1 Device Disable and Enable

Each of the DCR02 series devices can be disabled or enabled by driving the SYNC pin using an open-drain CMOS gate. If the SYNC pin is pulled low, the DCR02 becomes disabled. The disable time depends upon the

external loading. The internal disable function is implemented in 2 µs. Removal of the pulldown causes the DCR02 to be enabled.

Capacitive loading on the SYNC pin must be minimized (≤ 3 pF) to prevent a reduction in the oscillator frequency. The *External Synchronization of the DCP01/02 Series of DC/DC Converters Application Report* (SBAA035) describes disable and enable control circuitry. This document contains information on how to null the effects of additional capacitance on the SYNC pin. The oscillator's frequency can be measured at V_{REC}, as this is the fundamental frequency of the ripple component.

7.4.2 Regulated Output Disable and Enable

The regulated output of the DCR02 can be disabled by pulling the ENABLE pin LOW. Disabling the output voltage this way still produces a voltage on the V_{REC} pin. When using the ENABLE control, TI recommends placing a 10-kΩ resistor between the V_{REC} and ENABLE pins. The ENABLE pin only controls the internal linear regulator.

If disabling the regulated output is not required, pull the ENABLE pin HIGH by shorting it directly to the V_{REC} pin. This enables the regulated output voltage, thus allowing the output to be controlled from the isolated side.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

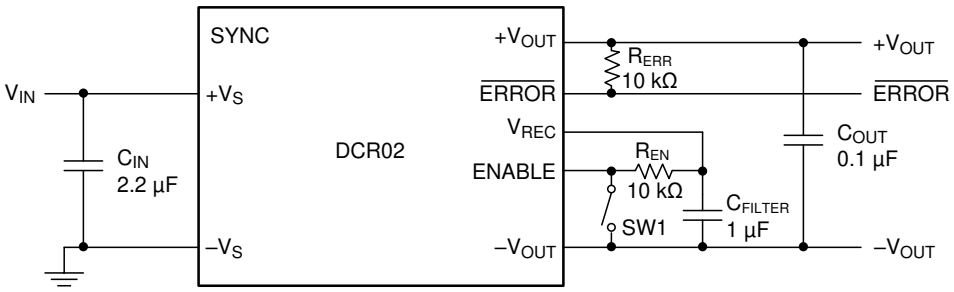
8.1 Application Information

The DCR02 devices offer up to 2 W of isolated, 5-V regulated output power from a 12-V or 24-V input supply. Applications requiring up to 1-kVrms of operational isolation benefits from the small size and ease-of-use of the DCR02 family of devices.

8.1.1 DCR02 Single Voltage Output

The DCR02 can be used to provide a single voltage output by connecting the circuit as shown in Figure 8-1. The $\overline{\text{ERROR}}$ output signal is pulled up to the value of V_{OUT} for the particular DCR02 being used. The value of R_{ERR} depends on the loading on the $\overline{\text{ERROR}}$ line; however, the total load on the $\overline{\text{ERROR}}$ line must not exceed the value given in the *Section 6.5*.

The output can be permanently enabled by connecting the ENABLE pin to the V_{REC} pin. The DCR02 can be enabled remotely by connecting the ENABLE pin to V_{REC} through a pull-up resistor (R_{EN}); the value of this resistor is not critical for the DCR02, because only a small current flows. Switch SW1 can be used to pull the ENABLE pin low, thus disabling the output. The switching devices can be a bipolar transistor, FET, or a mechanical device; the main load that it senses is R_{EN}.

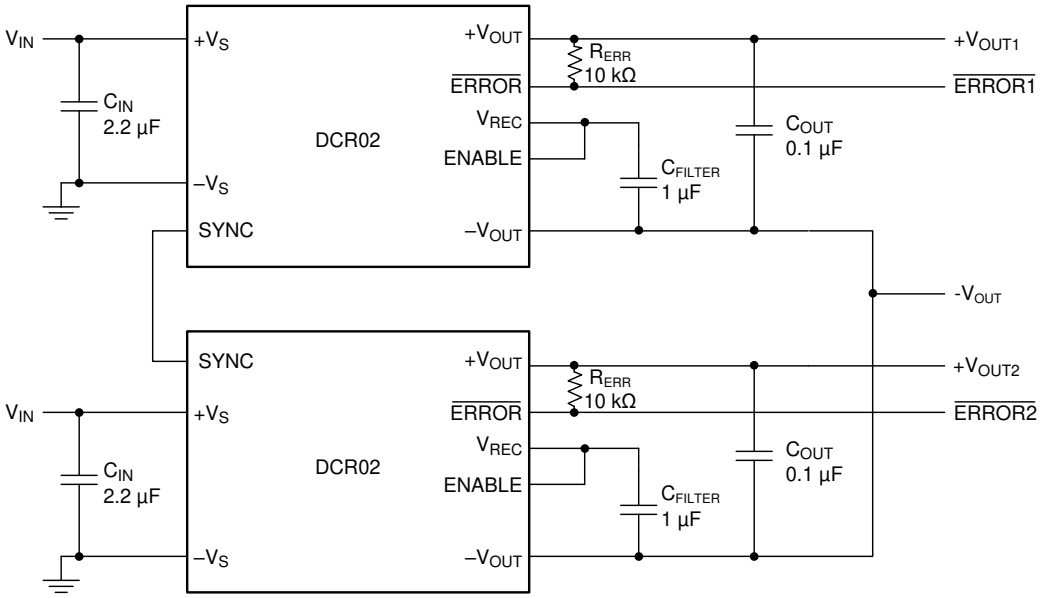


Low-ESR, ceramic capacitors are required for C_{IN}, C_{OUT}, and C_{FILTER}.

Figure 8-1. DCR02 Single Output Voltage

8.1.2 Generating Two Positive Output Voltages

Two DCR02s can be used to create two +5-V output voltages, as shown in Figure 8-2. The two DCR02s are connected in self-synchronization, thus locking the oscillators of both devices to a single frequency. The $\overline{\text{ERROR}}$ and ENABLE facilities can be used in a similar configuration for a single DCR02. The filter capacitors connected to the V_{REC} pins (C_{FILTER}) must be kept separate from each other and connected in close proximity to the respective DCR02. If similar output voltages are being used, TI does not recommend that a single filter capacitor (with an increased capacitance) be used with both V_{REC} pins connected together, because this could result in the overloading of one of the devices.



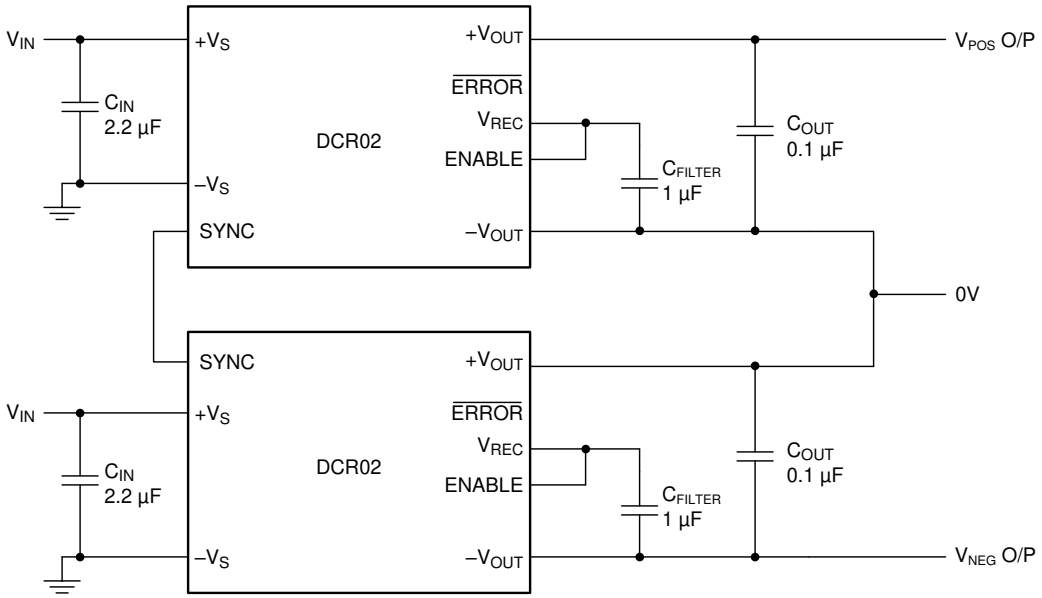
Low-ESR, ceramic capacitors are required for C_{IN}, C_{OUT}, and C_{FILTER}.

Figure 8-2. Generating Two Positive Voltages from Self-Synchronized DCR02s

8.1.3 Generation of Dual Polarity Voltages from Two Self-Synchronized DCR02s

Two DCR02s can be configured to produce a dual polarity supply (that is, ±5 V); the circuit must be connected as shown in Figure 8-3.

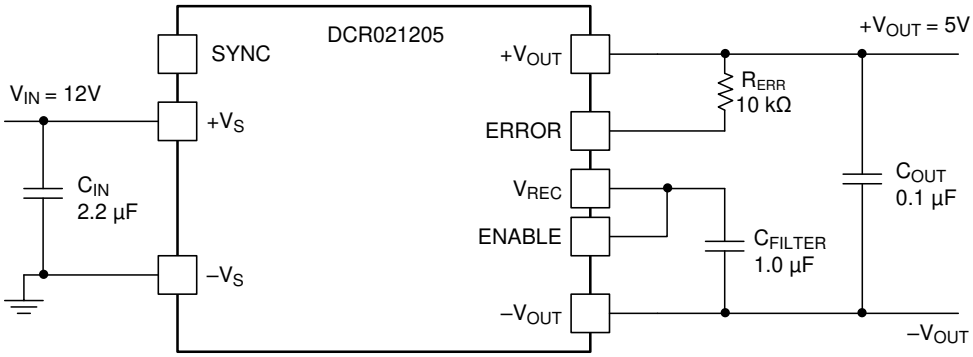
It must be observed that both DCR02s are positive voltage regulators; therefore the $\overline{\text{ERROR}}$, ENABLE, and V_{REC} pins are relative to their respective devices, 0 V, and must not be connected together.



Low-ESR, ceramic capacitors are required for C_{IN}, C_{OUT}, and C_{FILTER}.

Figure 8-3. Dual Polarity Voltage Generation from Two Self-Synchronized DCR02s

8.2 Typical Application



Low-ESR, ceramic capacitors are required for C_{IN}, C_{OUT}, and C_{FILTER}.

Figure 8-4. DCR02 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 and follow the design procedure.

Table 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage, V_{IN}	12 V typical
Output voltage, V_{OUT}	5 V regulated
Output current rating	400 mA
Isolation	1000-V operational

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

For this design, a 2.2-µF, ceramic capacitor is required for the input decoupling capacitor.

8.2.2.2 Output Capacitor

For this design, a 0.1-µF, ceramic capacitor is required for between $+V_{OUT}$ and $–V_{OUT}$.

8.2.2.3 Filter Capacitor

A high-quality, low-ESR, 1-µF, ceramic capacitor placed close to the V_{REC} pin and output ground is required to reduce output voltage ripple.

8.2.2.4 $\overline{\text{ERROR}}$ Flag

Place a 10-kΩ resistor between the $\overline{\text{ERROR}}$ pin and the output voltage to provide a *power good* signal when the internal regulator is in regulation.

8.2.3 Application Curves

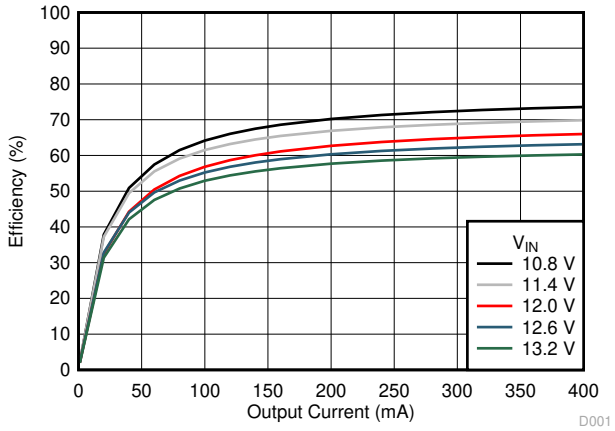


Figure 8-5. DCR021205 Efficiency versus Output Current

9 Power Supply Recommendations

The DCR02 is a switching power supply, and as such can place high peak current demands on the input supply. To avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCR02. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

10 Layout

10.1 Layout Guidelines

Carefully consider the layout of the PCB in order for the best results to be obtained.

Input and output power and ground planes provide a low-impedance path for the input and output power. For the output, the positive and negative voltage outputs conduct through wide traces to minimize losses.

A good-quality, low-ESR, ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensure a smooth start-up.

A good-quality, low-ESR, ceramic capacitor placed as close as practical across the rectifier output terminal and output ground gives the best ripple and noise performance.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

If the SYNC pin is being used, the tracking between device SYNC pins must be short to avoid stray capacitance. Never connect a capacitor to the SYNC pin. If the SYNC pin is not being used it is advisable to place a guard ring (connected to input ground) around this pin to avoid any noise pickup. Ensure that no other trace is in close proximity to this trace SYNC trace to decrease the stray capacitance on this pin. The stray capacitance affects the performance of the oscillator.

Figure 10-1 and Figure 10-2 show a typical layout for the SOP package DCR02 device. The layout shows proper placement of capacitors and power planes. Figure 10-3 shows a schematic for a single DCR02, SOP package device.

10.2 Layout Examples

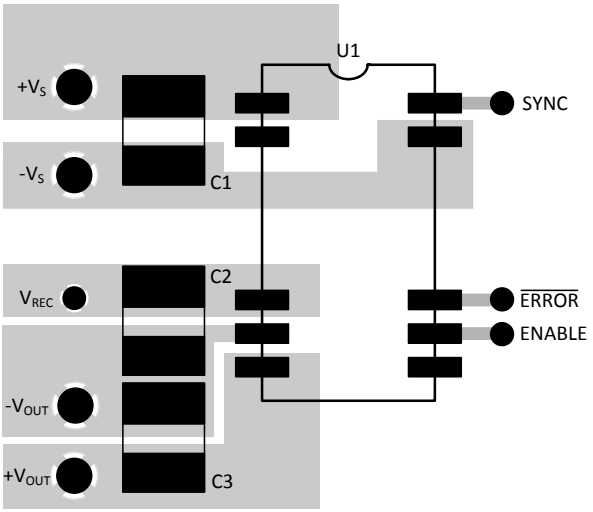


Figure 10-1. PCB Layout Example, Component-Side View

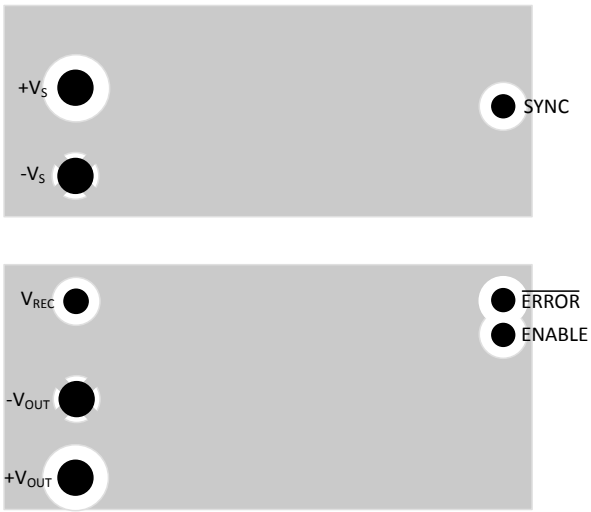


Figure 10-2. PCB Layout Example, Non-Component-Side View

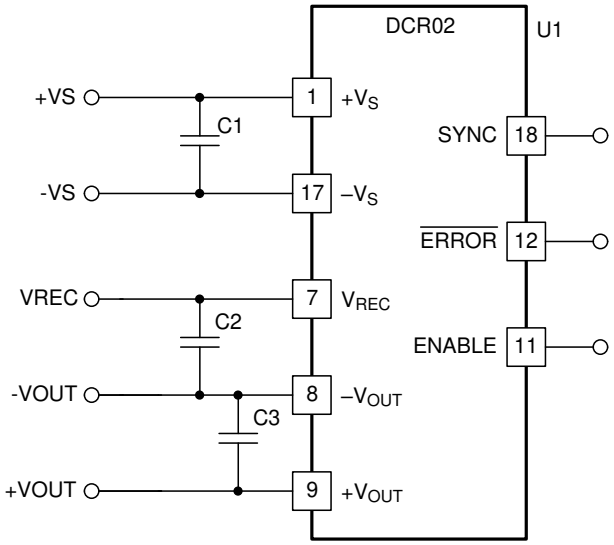


Figure 10-3. DCR02 PCB Schematic, U Package

10.3 Thermal Consideration

Due to the high power density of this device, it is advisable to provide a ground plane on the output. The output regulator is mounted on a copper leadframe, and a ground plane serves as an efficient heatsink.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *External Synchronization of the DCP01/02 Series of DC/DC Converters* (SBAA035)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCR021205P	ACTIVE	PDIP	NVE	10	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 70	DCR021205P	Samples
DCR021205P-U	ACTIVE	SOP	DVS	10	20	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 70	DCR021205P-U	Samples
DCR022405P	ACTIVE	PDIP	NVE	10	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 70	DCR022405P	Samples
DCR022405P-U	ACTIVE	SOP	DVS	10	20	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 70	DCR022405P-U	Samples
DCR022405P-U/700	LIFEBUY	SOP	DVS	10	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	0 to 0	DCR022405P-U	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

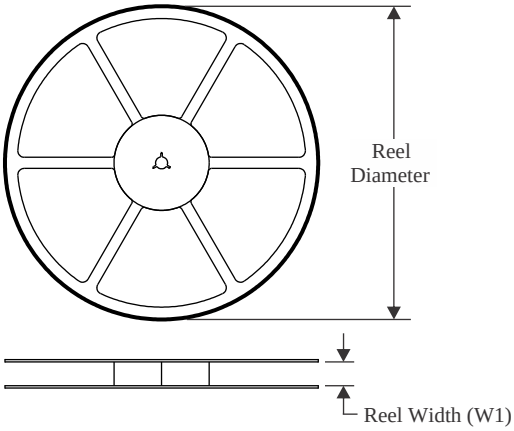
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

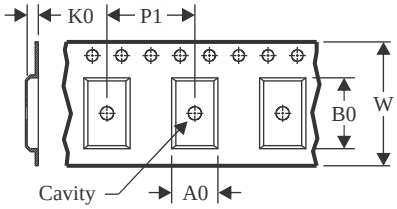
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

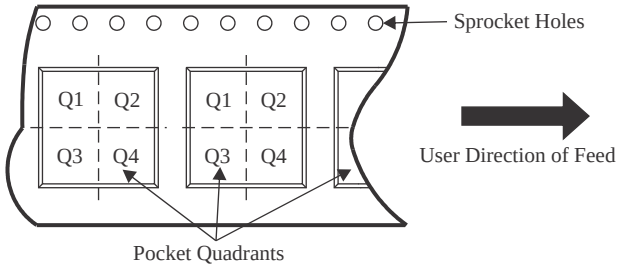


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

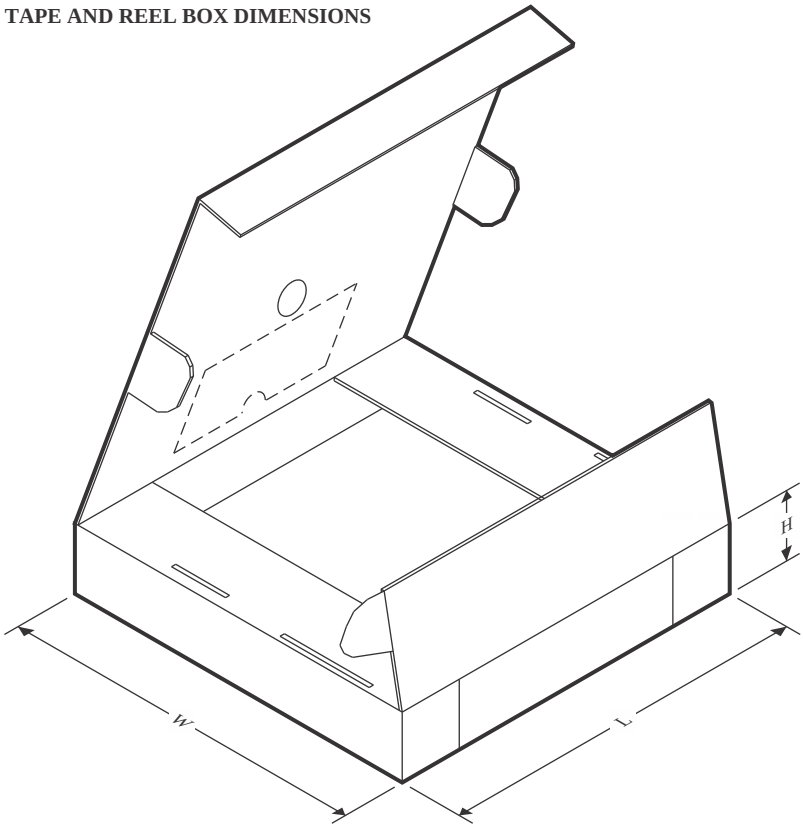
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DCR022405P-U/700	SOP	DVS	10	700	330.0	44.4	10.85	23.5	5.25	16.0	44.0	Q1

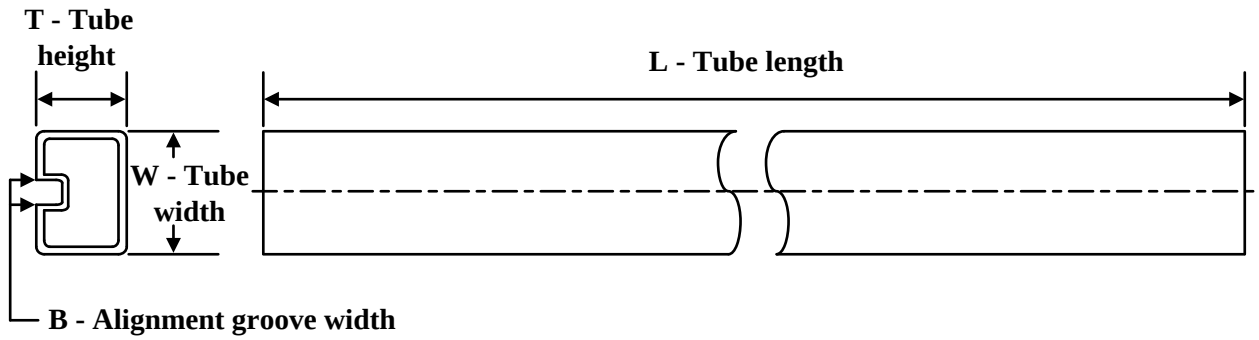
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DCR022405P-U/700	SOP	DVS	10	700	346.0	346.0	61.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DCR021205P	NVE	PDIP	10	20	533.4	14.33	13.03	8.07
DCR021205P-U	DVS	SOP	10	20	532.13	13.51	7.36	6.91
DCR022405P	NVE	PDIP	10	20	533.4	14.33	13.03	8.07
DCR022405P-U	DVS	SOP	10	20	532.13	13.51	7.36	6.91

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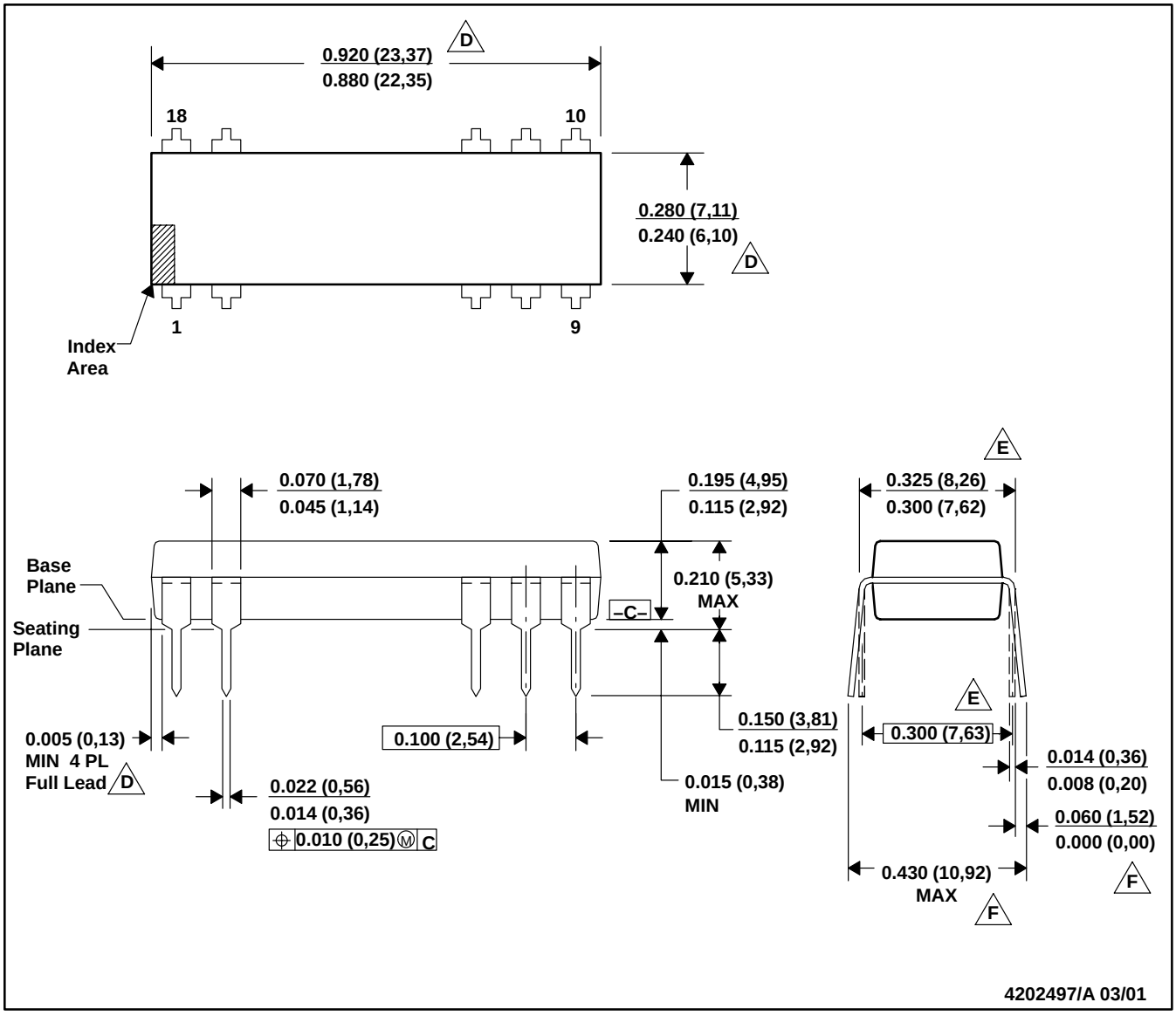
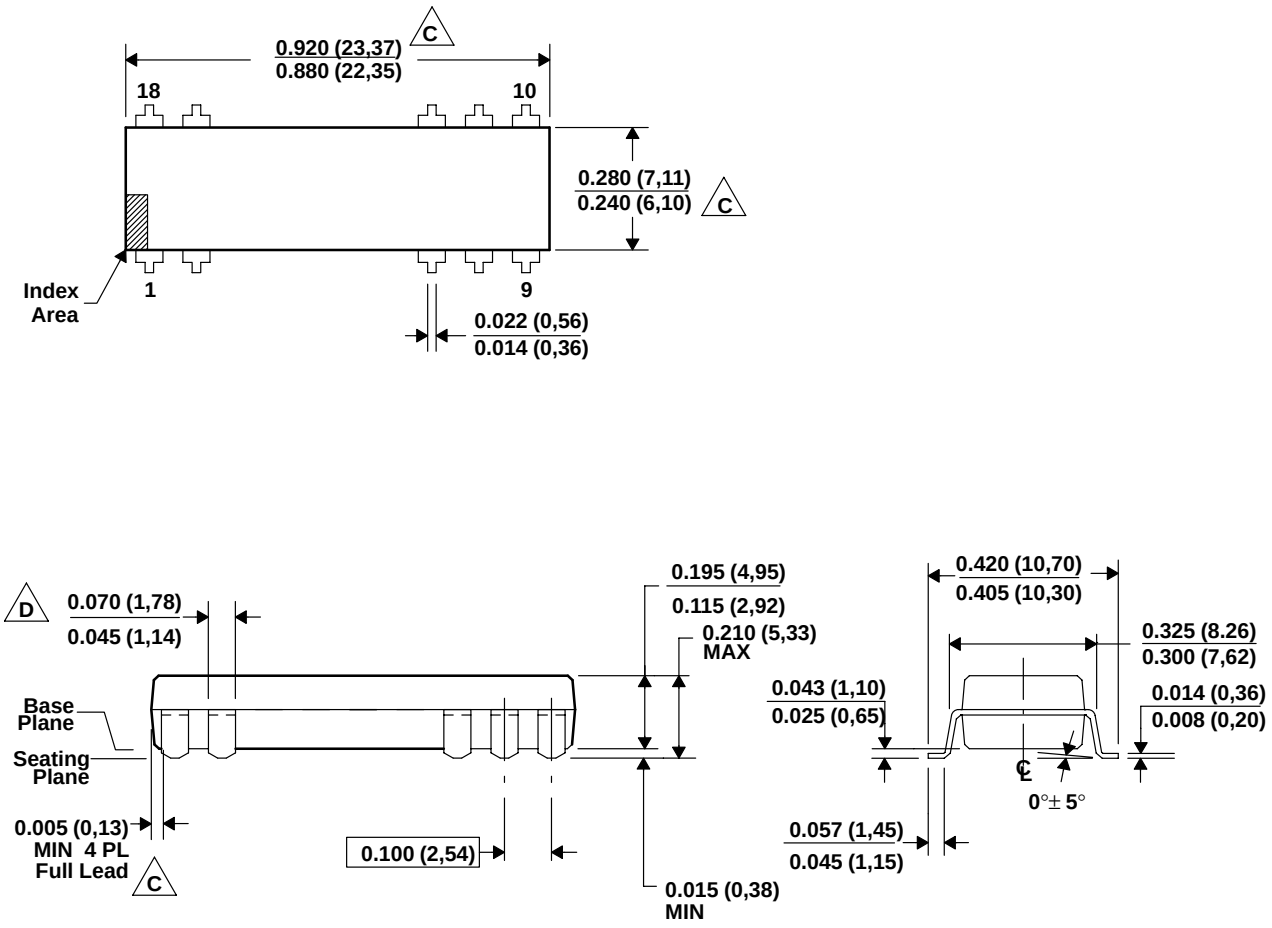
NVE (R-PDIP-T10/18) **PLASTIC DUAL-IN-LINE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-AC with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

DVS (R-PDSO-G10/18) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
D. Maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25)
E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
F. A visual index feature must be located within the cross–hatched area.
G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

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