2nd-Order Delta-Sigma Modulator with Excitation for Hall Elements

FEATURES

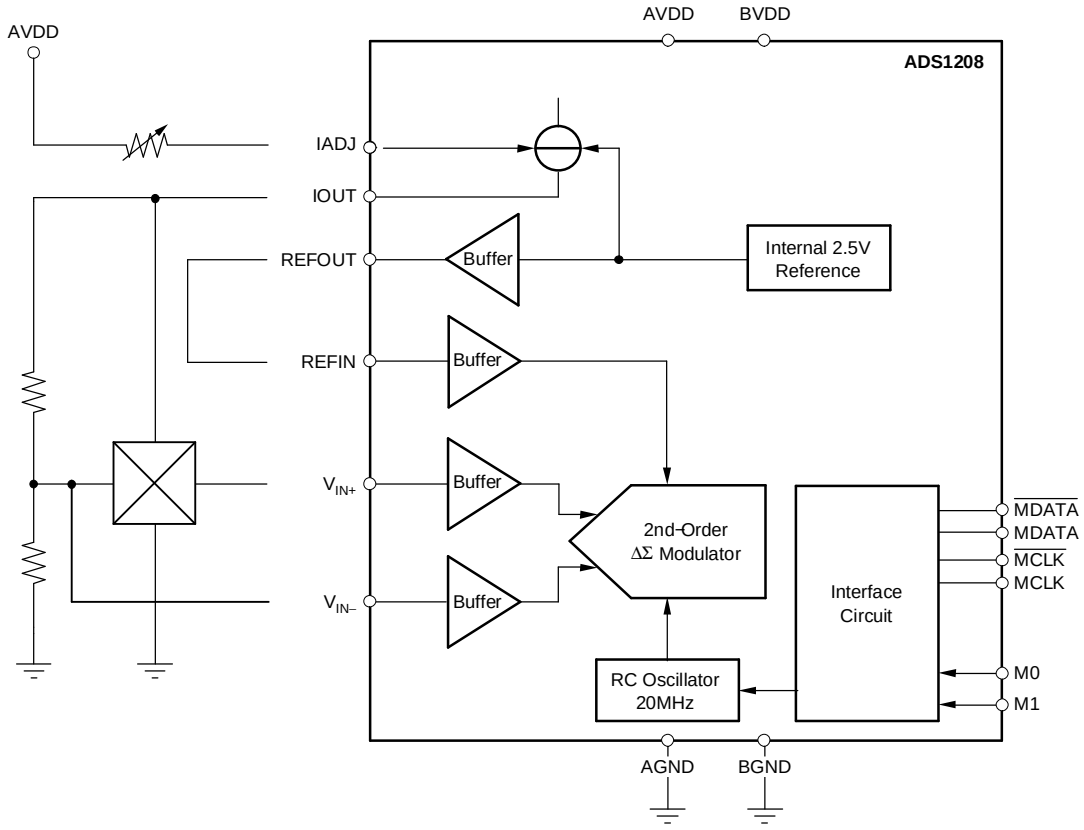
- **±100mV Specified Input Range**
- **±125mV Full-Scale Range**
- **95dB typ. CMR, 82dB typ. SNR**
- **Adjustable Current Output for Sensor Biasing**
- **Digital Output Compatible to ADS1202/03**
- **Differential Digital Outputs**
- **Separate 2.7V to 5.5V Digital Supply Pin**

APPLICATIONS

- **Motor Control**
- **Current Measurement**
- **Hall Sensors**
- **Bridge Sensors**
- **Instrumentation**

DESCRIPTION

The ADS1208 is a 2nd-order ΔΣ (delta-sigma) modulator operating at a 10MHz clock rate. The specified input range is ±100mV, optimized for current measurement with a Hall sensor, especially in motor control applications. The ADS1208 contains a programmable current source for sensor biasing and has integrated input buffers for fast settling of the sample capacitors; it also requires only a minimum of external components. The differential analog input offers low noise and excellent common-mode rejection.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Package/Ordering Information

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	ADS1208I	UNIT
Supply voltage, AGND to AV_{DD}	–0.3 to +6	V
Supply voltage, BGND to BV_{DD}	–0.3 to +6	V
Analog input voltage with respect to AGND	AGND – 0.3 to AV_{DD} + 0.3	V
Reference input voltage with respect to AGND	AGND – 0.3 to AV_{DD} + 0.3	V
Digital input voltage with respect to BGND	BGND – 0.3 to BV_{DD} + 0.3	V
Ground voltage difference AGND to BGND	±0.3	V
Input current to any pin except supply	±10	mA
Power dissipation	See Dissipation Ratings Table	
Operating virtual junction temperature range, T_J	–40 to +150	°C
Operating free-air temperature range, T_A	–40 to +85	°C
Storage temperature range, T_{STG}	–65 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, AGND to AV_{DD}		4.5	5.0	5.5	V
Supply voltage, BGND to BV_{DD}	Low-voltage levels	2.7		3.6	V
	5V logic levels	4.5	5.0	5.5	V
Reference input voltage		0.5	2.5	3.0	V
Analog inputs	$V_{IN+} – V_{IN-}$	$–V_{REFIN}$ /20		$+V_{REFIN}$ /20	V

DISSIPATION RATINGS TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	PW	35°C/W	147°C/W	6.8mW/°C	850mW	544mW	442mW
High-K(2)	PW	33.6°C/W	108.4°C	9.225W/°C	1150mW	738mW	600mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in x 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit $Sinc^3$ filter with OSR = 256, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1208I			UNIT
		MIN	TYP(1)	MAX	
Resolution		16			Bits
DC Accuracy					
Integral nonlinearity(2)	16-bit resolution	–8	1.6	8	LSB
Integral nonlinearity		–0.012	0.0025	0.012	%
Differential nonlinearity(3)	16-bit resolution	–1.0		1.0	LSB
Input offset(4)		–2.0	–1.4	0	mV
Input offset drift			2.0	8.0	µV/°C
Gain error(4)	Referenced to voltage at REFIN	–1.25	–0.7	1.25	%
Gain error drift	Referenced to voltage at REFIN		15		ppm/°C
Power-supply rejection ratio			66		dB
Analog Input					
Full-scale range	$V_{IN+} – V_{IN–}$	–125		125	mV
Operating common-mode signal		0.8	1.4	2.5	V
Input capacitance			5.0		pF
Common-mode rejection			95		dB
Current Source (IOUT)					
Output current(5)	I_{OUT}	1.0	5.0	8.0	mA
Voltage at IOUT pin	V_{OUT}	0		AVDD – 1.0	V
Voltage between AVDD pin and IADJ	V_{ADJ} at I_{OUT} = 1mA to 8mA	480	500	520	mV
Internal Voltage Reference					
Reference output voltage	REFOUT	2.45	2.5	2.55	V
Reference temperature drift			20		ppm/°C
Output resistance			0.3		Ω
Output source current				3.0	mA
Power-supply rejection ratio			60		dB
Startup time			0.1		ms
Voltage Reference Input					
Reference voltage input	REFIN	0.5		3.0	V
Reference input capacitance			5		pF
Reference input current		-50		+50	nA
Internal Clock for Modes 0, 1 and 2					
Clock frequency		8.0	10.1	12.0	MHz
External Clock for Mode 3					
Clock frequency		1.0		24.0	MHz

(1) All values are at T_A = 25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for $V_{IN+} – V_{IN–}$ = –100mV to +100mV, expressed either as the number of LSBs or as a percent of the measured input range (200mV).
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) It is possible to leave pin IOUT unconnected (I_{OUT} = 0mA).

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit Sinc^3 filter with OSR = 256, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1208I			UNIT
		MIN	TYP(1)	MAX	
AC Accuracy					
SNR	V_{IN} = 200mV_{PP} at 1kHz	80	82		dB
SINAD	V_{IN} = 200mV_{PP} at 1kHz	77	81.5		dB
THD	V_{IN} = 200mV_{PP} at 1kHz		–91	–80	dB
SFDR	V_{IN} = 200mV_{PP} at 1kHz	80	93		dB
Digital Inputs(6)					
Logic family			CMOS		
V_{IH} High-level input voltage		0.7 x BV_{DD}		BV_{DD} + 0.3	V
V_{IL} Low-level input voltage		–0.3		0.3 x BV_{DD}	V
I_{IN} Input current	V_{IN} = BV_{DD} or GND	–50		50	nA
C_I Input capacitance			5		pF
Digital Outputs(6)					
Logic family			CMOS		
V_{OH} High-level output voltage	BV_{DD} = 4.5V, I_{OH} = –100µA	4.44			V
V_{OL} Low-level output voltage	BV_{DD} = 4.5V, I_{OL} = +100µA			0.5	V
C_L Load capacitance				30	pF
Data format			Bit stream		
Digital Inputs(7)					
Logic family			LVCMOS		
V_{IH} High-level input voltage	BV_{DD} = 3.6V	2		BV_{DD} + 0.3	V
V_{IL} Low-level input voltage	BV_{DD} = 2.7V	–0.3		0.8	V
I_{IN} Input current	V_{IN} = BV_{DD} or GND	–50		50	nA
C_I Input capacitance			5		pF
Digital Outputs(7)					
Logic family			LVCMOS		
V_{OH} High-level output voltage	BV_{DD} = 2.7, I_{OH} = –100µA	BV_{DD} – 0.2			V
V_{OL} Low-level output voltage	BV_{DD} = 2.7, I_{OL} = +100µA			0.2	V
C_L Load capacitance				30	pF
Data format			Bit stream		
Power Supply					
Analog supply voltage, AV_{DD}		4.5	5.0	5.5	V
Digital interface supply voltage, BV_{DD}		2.7	5	5.5	V
Operating supply current, AI_{DD}	Modes 0, 1 and 2		11.9	15.0	mA
Operating supply current, AI_{DD}	Mode 3		11.5	14.5	mA
Operating supply current, BI_{DD}	Modes 0, 1 and 2		2.3	3.0	mA
Operating supply current, BI_{DD}	Mode 3		1.3	2.0	mA
Power dissipation	Modes 0, 1 and 2		71	90	mW
Power dissipation	Mode 3		64	82.5	mW

(6) Applicable for 5.0V nominal supply; BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(7) Applicable for 3.0V nominal supply; BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V

PARAMETER MEASUREMENT INFORMATION

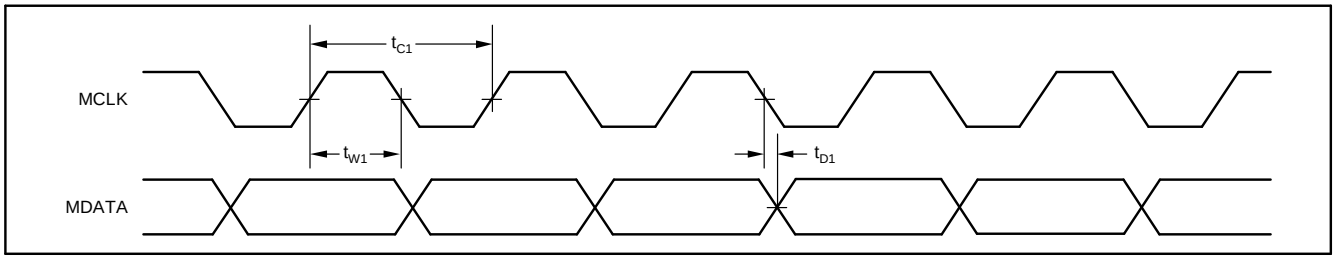


Figure 1. Mode 0 Operation

TIMING CHARACTERISTICS: MODE 0

Over recommended operating free-air temperature range at –40°C to +85°C, and AV_{DD} = +5V, BV_{DD} = +2.7 to +5.5V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{C1}	Clock period	83	125	ns
t_{W1}	Clock high time	(t_{C1} /2) – 5	(t_{C1} /2) + 5	ns
t_{D1}	Data delay after rising edge of clock	–2	+2	ns

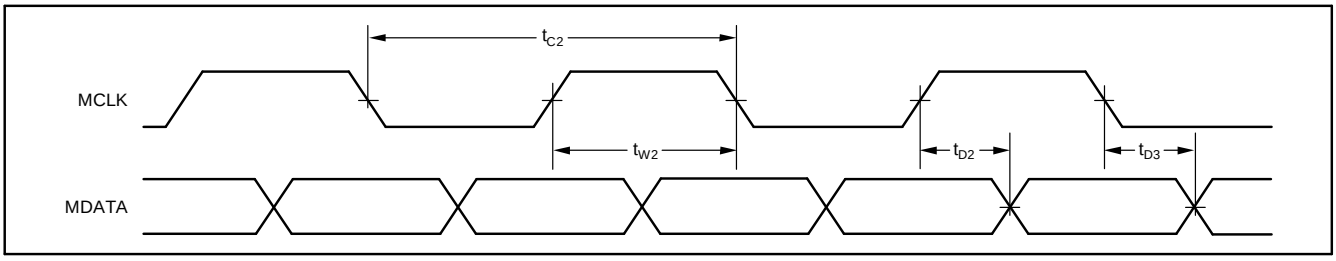


Figure 2. Mode 1 Operation

TIMING CHARACTERISTICS: MODE 1

Over recommended operating free-air temperature range at –40°C to +85°C, and AV_{DD} = +5V, BV_{DD} = +2.7 to +5.5V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{C1}	Clock period	166	250	ns
t_{W2}	Clock high time	(t_{C2} /2) – 5	(t_{C2} /2) + 5	ns
t_{D2}	Data delay after rising edge of clock	(t_{W2} /2) – 2	(t_{W2} /2) + 2	ns
t_{D3}	Data delay after falling edge of clock	(t_{W2} /2) – 2	(t_{W2} /2) + 2	ns

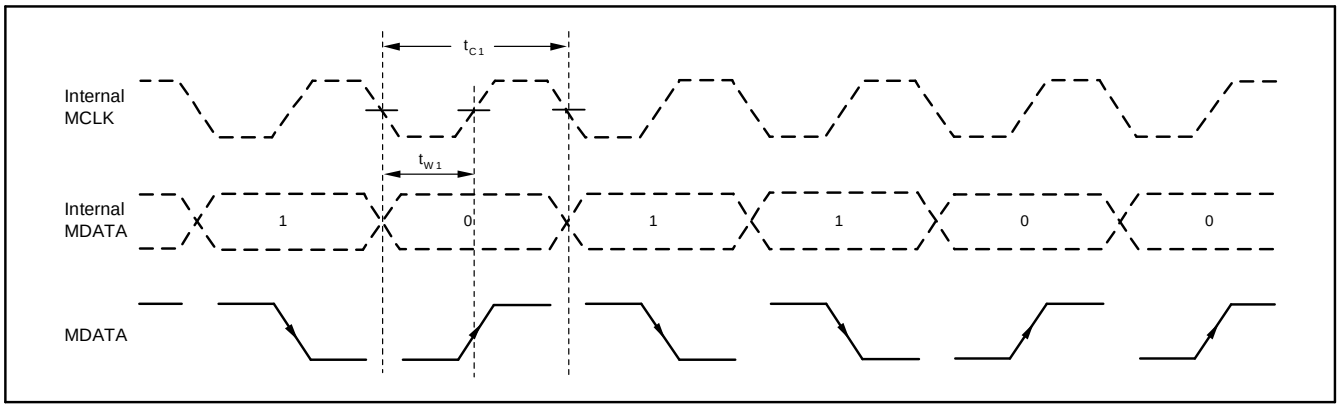
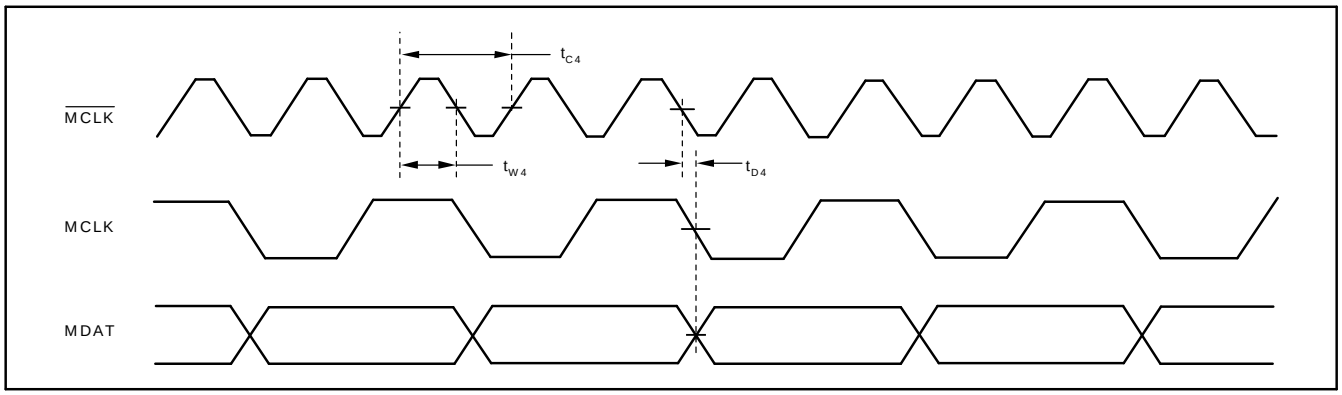


Figure 3. Mode 2 Operation

TIMING CHARACTERISTICS: MODE 2

Over recommended operating free-air temperature range at –40°C to +85°C, and AV_{DD} = +5V, BV_{DD} = +2.7 to +5.5V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{C1}	Clock period	83	125	ns
t_{W1}	Clock high time	(t_{C1} /2) – 5	(t_{C1} /2) + 5	ns



note: $\overline{MCLK}$ is system clock input. MCLK is modulator clock output. Modulator clock frequency is half of system clock frequency.

Figure 4. Mode 3 Operation

TIMING CHARACTERISTICS: MODE 3

Over recommended operating free-air temperature range at –40°C to +85°C, and AV_{DD} = +5V, BV_{DD} = +2.7 to +5.5V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{C4}	Clock period	41	1000	ns
t_{W4}	Clock high time	10	t_{C4} – 10	ns
t_{D4}	Data and output clock delay after falling edge of input clock	0	10	ns
t_R	Rise time of clock (10% to 90% of BV_{DD})	0	10	ns
t_F	Fall time of clock (90% to 10% of BV_{DD})	0	10	ns

DEVICE INFORMATION

16-LEAD TSSOP PACKAGE
(TOP VIEW)

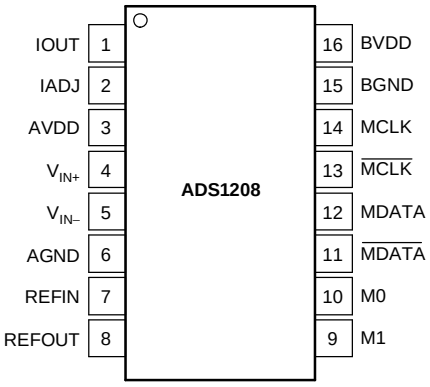
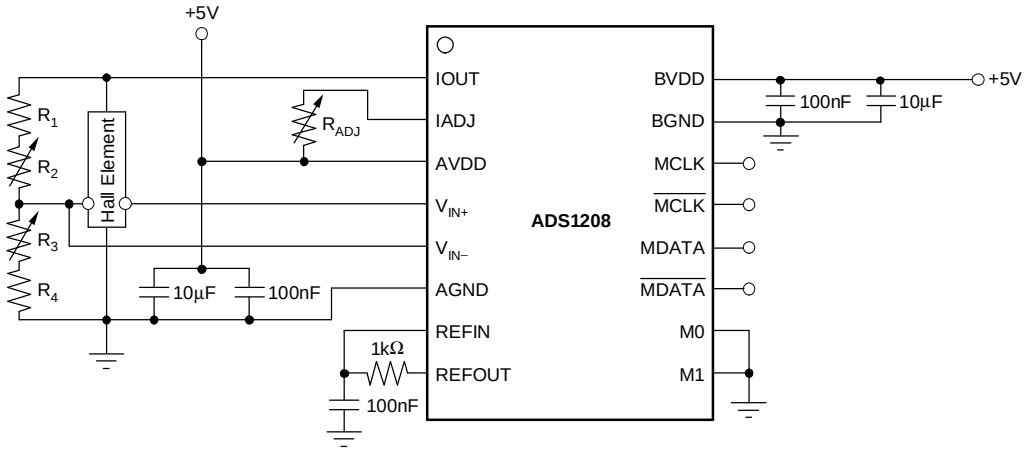


Table 1. TERMINAL FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1	IOUT	Current output for sensor
2	IADJ	Output current adjustment
3	AVDD	Analog supply
4	V_{IN+}	Positive input
5	V_{IN-}	Negative input
6	AGND	Analog ground
7	REFIN	Reference input
8	REFOUT	Reference output
9	M1	Mode selection input
10	M0	Mode selection input
11	$\overline{MDATA}$	Inverted data output
12	MDATA	Noninverted data output
13	$\overline{MCLK}$	Inverted clock output (Modes 0, 1); Clock input (Mode 3)
14	MCLK	Noninverted clock output
15	BGND	Digital interface ground
16	BVDD	Digital interface supply (2.7V to 5.5V)

FUNCTIONAL BLOCK DIAGRAM



A. For Functional configuration (Mode 0), possible Hall elements include the Toshiba THS119 and the Philips KMZ10.

Figure 5. Functional Configuration (Mode 0)

TYPICAL CHARACTERISTICS

At 25°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit Sinc^3 filter with OSR = 256, unless otherwise noted.

INTEGRAL NONLINEARITY vs INPUT SIGNAL (Mode 0)

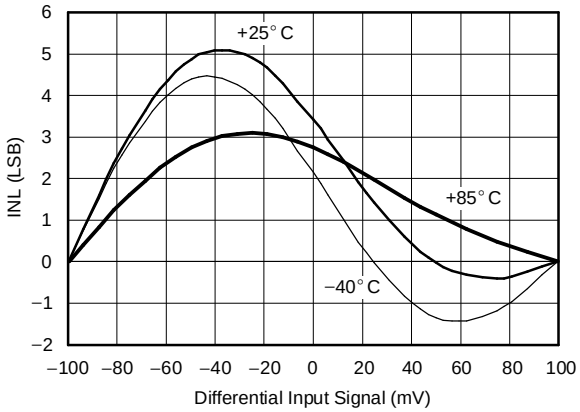


Figure 6.

INTEGRAL NONLINEARITY vs INPUT SIGNAL (Mode 3, MCLK = 20MHZ)

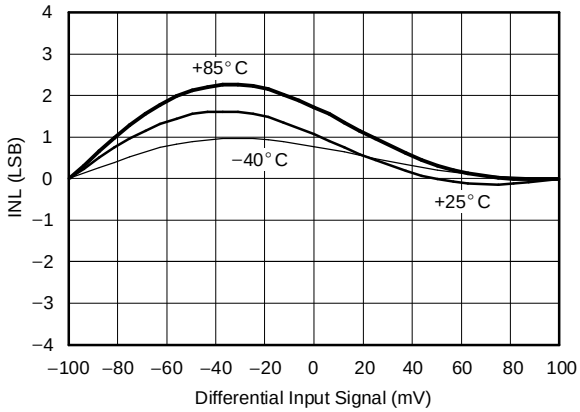


Figure 7.

INTEGRAL NONLINEARITY vs TEMPERATURE

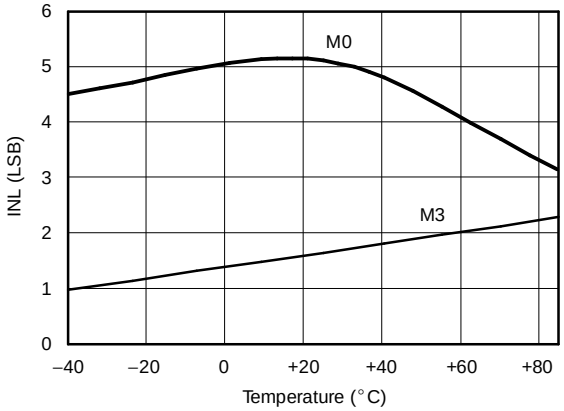


Figure 8.

GAIN ERROR vs TEMPERATURE

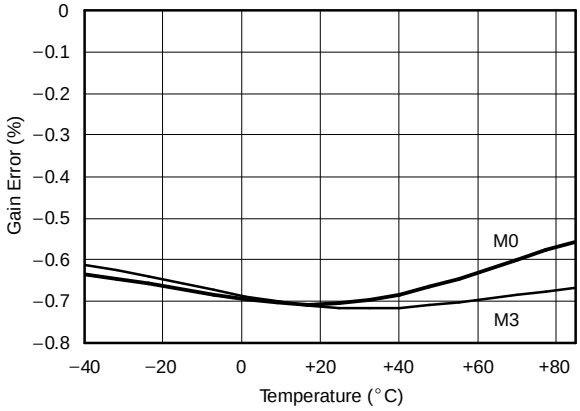


Figure 9.

OFFSET vs TEMPERATURE

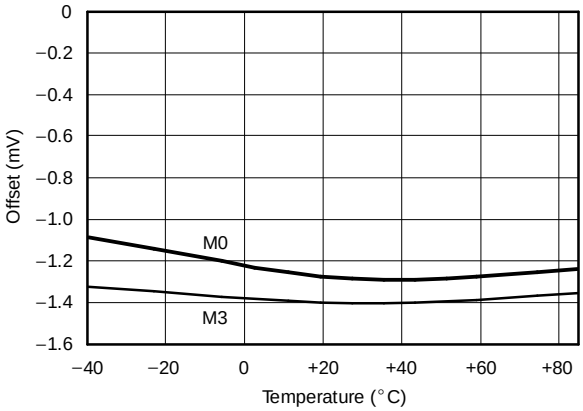


Figure 10.

OFFSET vs POWER SUPPLY

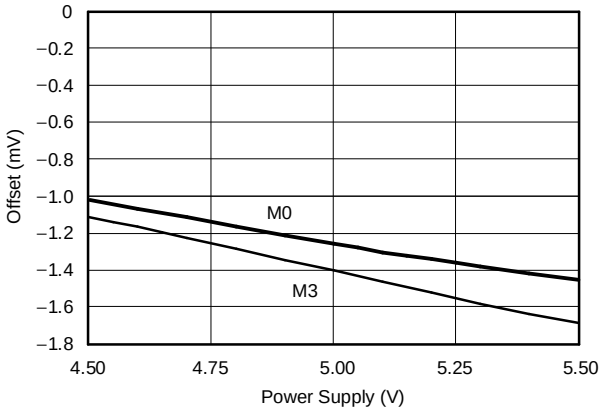


Figure 11.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit $Sinc^3$ filter with OSR = 256, unless otherwise noted.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

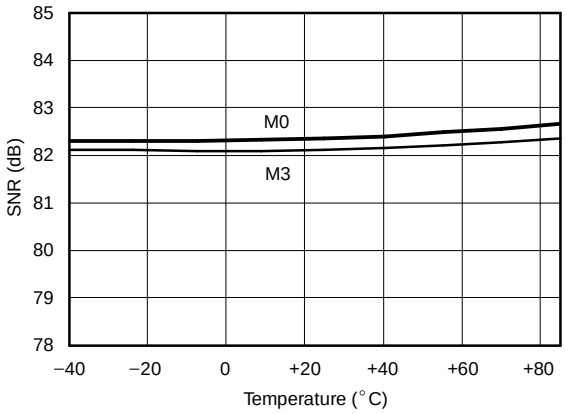


Figure 12.

SIGNAL-TO-NOISE AND DISTORTION vs TEMPERATURE

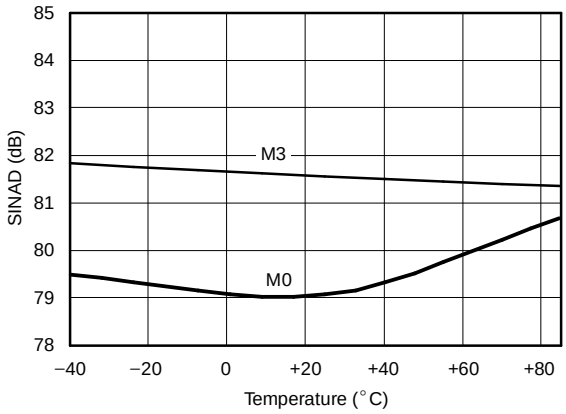


Figure 13.

SIGNAL-TO-NOISE RATIO vs DECIMATION RATIO

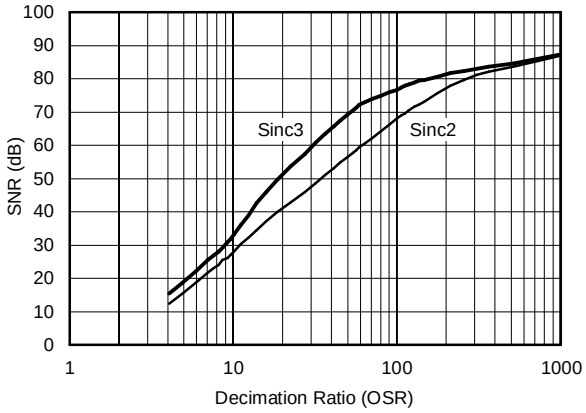


Figure 14.

EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO

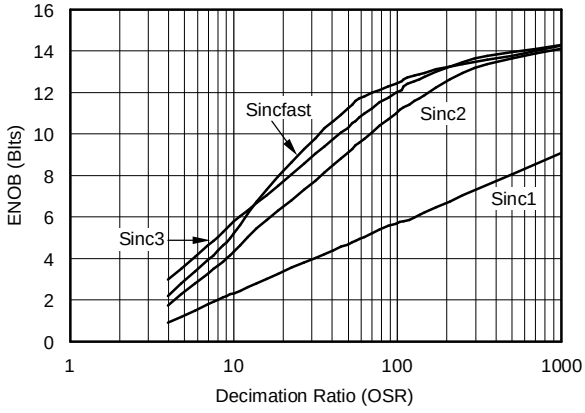


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit $Sinc^3$ filter with OSR = 256, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs FREQUENCY (Mode 1)

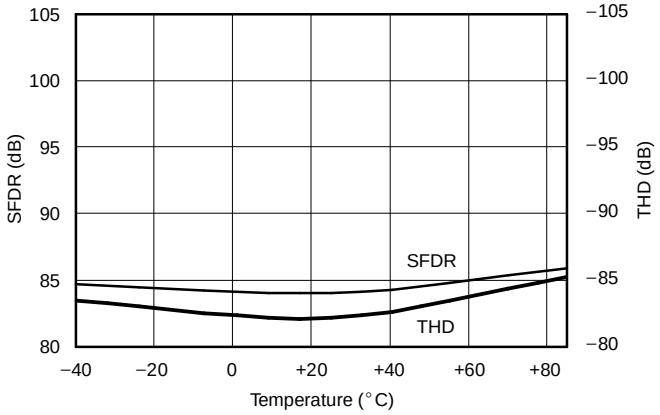


Figure 16.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs TEMPERATURE (Mode 3)

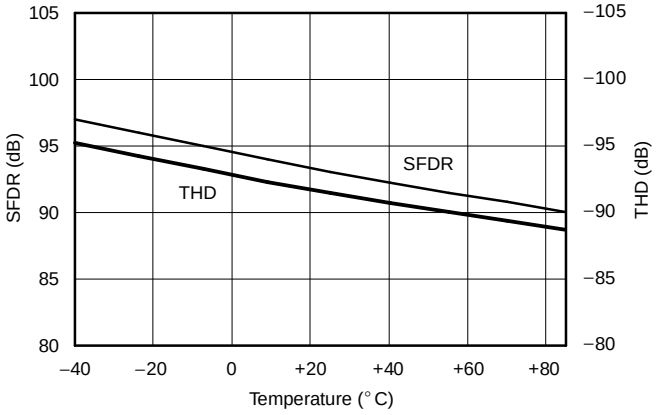


Figure 17.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs FREQUENCY (Mode 1)

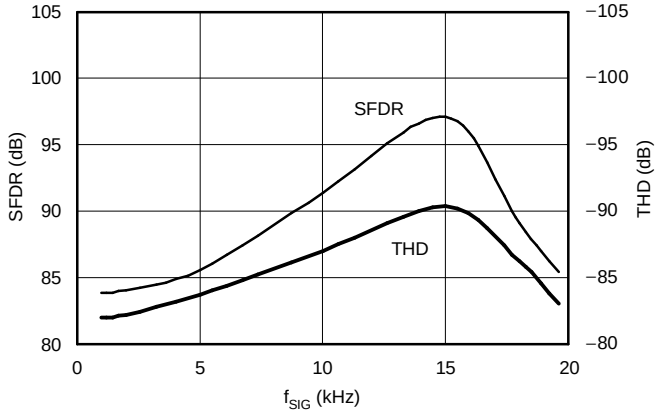


Figure 18.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs TEMPERATURE (Mode 3)

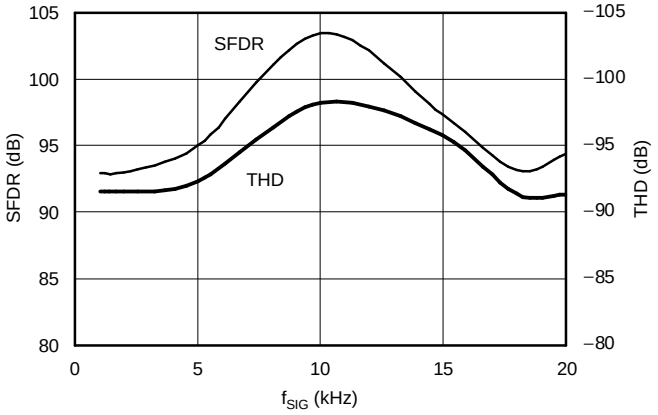


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit $Sinc^3$ filter with OSR = 256, unless otherwise noted.

FREQUENCY SPECTRUM (4096 POINT FFT, f_{IN} = 1kHz)

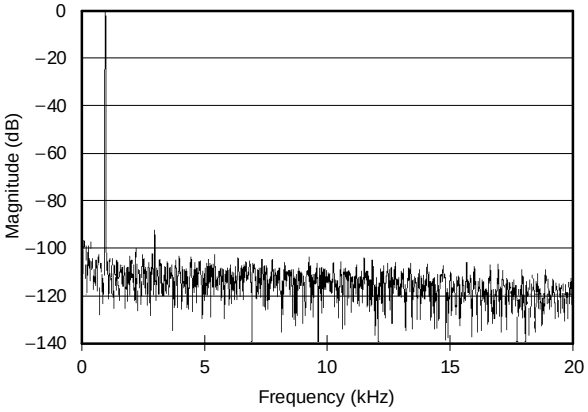


Figure 20.

FREQUENCY SPECTRUM (4096 POINT FFT, f_{IN} = 5kHz)

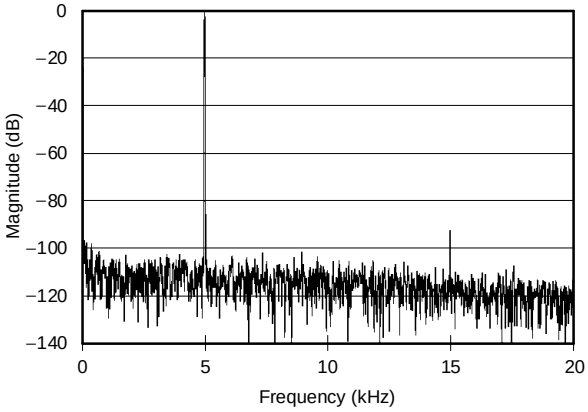


Figure 21.

COMMON-MODE REJECTION RATIO vs FREQUENCY

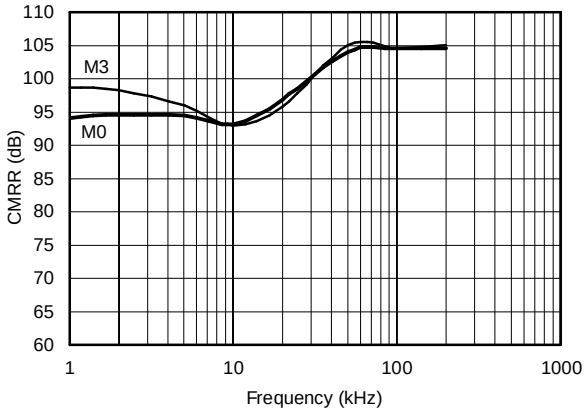


Figure 22.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

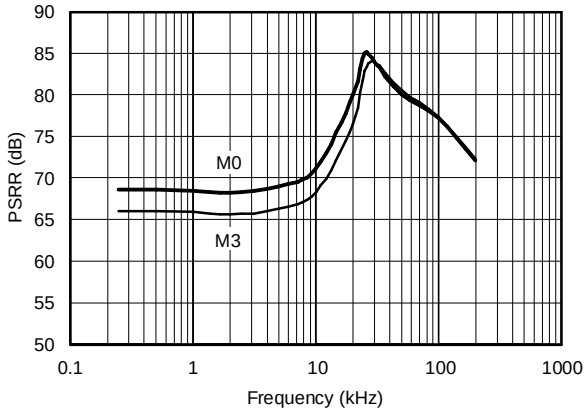


Figure 23.

CLOCK FREQUENCY vs TEMPERATURE

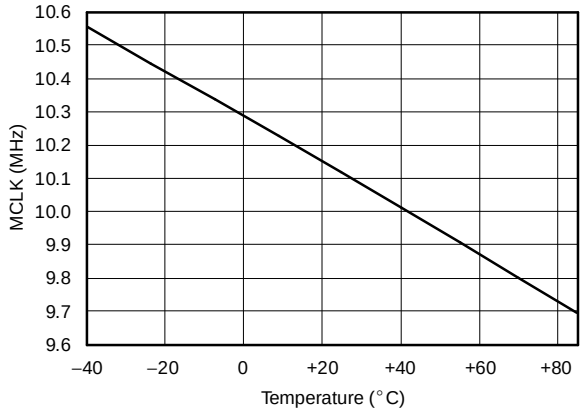


Figure 24.

CLOCK FREQUENCY vs POWER SUPPLY

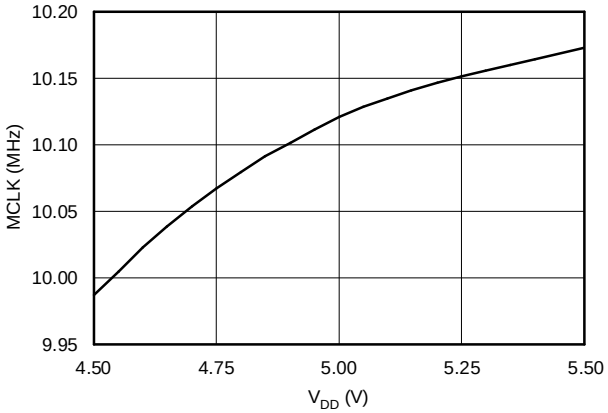


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit $Sinc^3$ filter with OSR = 256, unless otherwise noted.

ANALOG POWER SUPPLY CURRENT vs TEMPERATURE

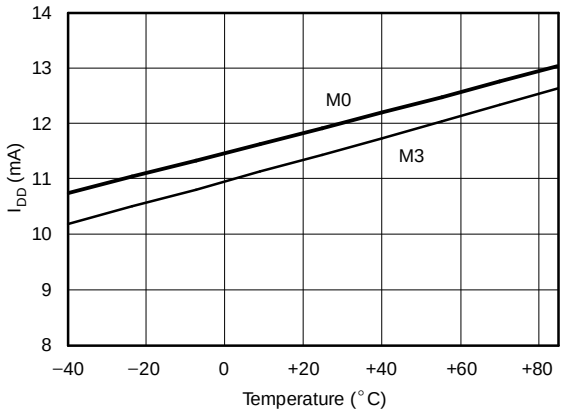


Figure 26.

DIGITAL POWER SUPPLY CURRENT vs TEMPERATURE

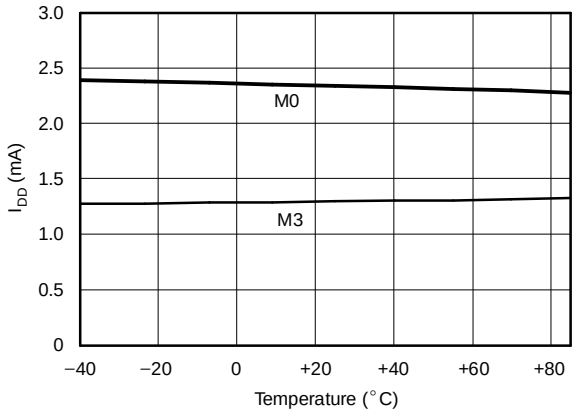


Figure 27.

REFERENCE OUTPUT VOLTAGE vs TEMPERATURE

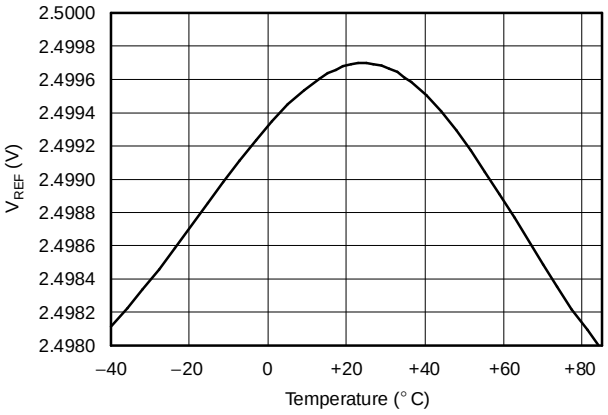


Figure 28.

REFERENCE OUTPUT VOLTAGE vs POWER SUPPLY

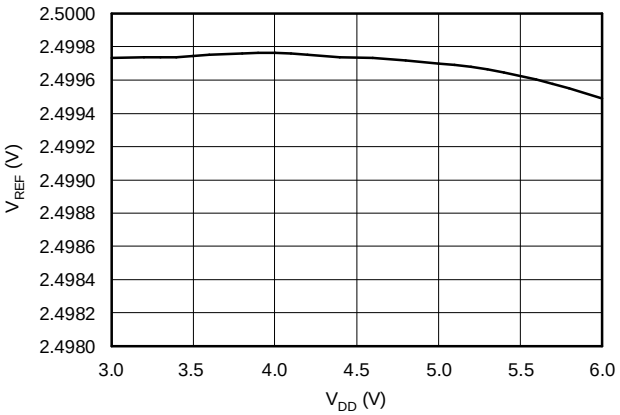


Figure 29.

REFERENCE OUTPUT VOLTAGE vs LOAD CURRENT

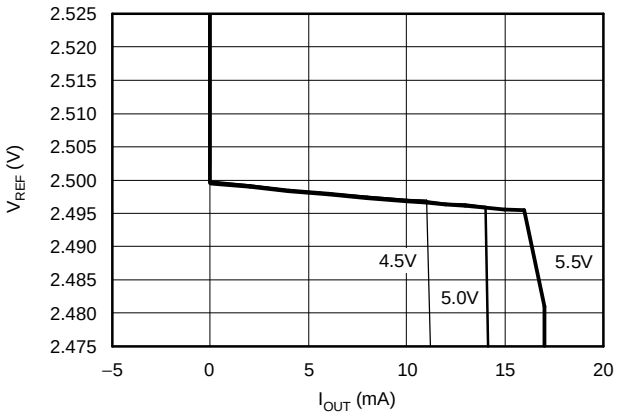


Figure 30.

CURRENT SOURCE REFERENCE VOLTAGE vs LOAD VOLTAGE (I = 8mA)

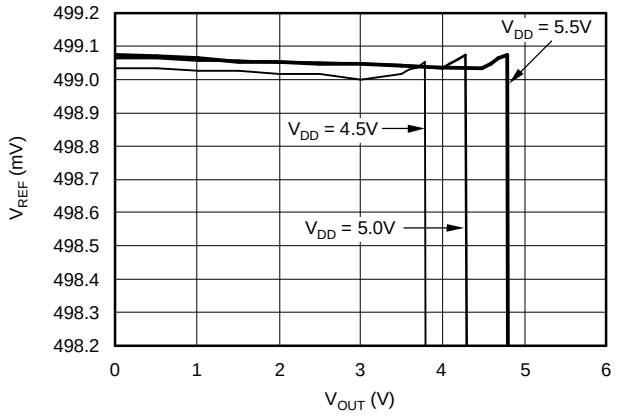


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At 25°C, AV_{DD} = BV_{DD} = +5V, V_{REF} = internal +2.5V, Mode 3, MCLK input = 20MHz, differential input voltage = 200mV_{PP}, common-mode voltage = 1.4V, and 16-bit $Sinc^3$ filter with OSR = 256, unless otherwise noted.

CURRENT SOURCE REFERENCE VOLTAGE vs TEMPERATURE (I = 8mA)

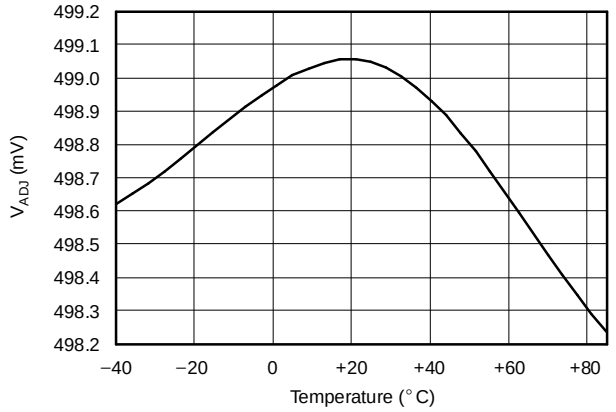


Figure 32.

CURRENT SOURCE REFERENCE VOLTAGE vs POWER SUPPLY (I = 8mA)

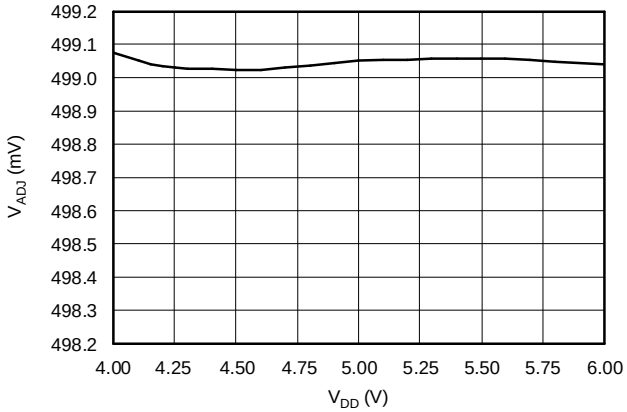


Figure 33.

RMS NOISE vs INPUT VOLTAGE LEVEL

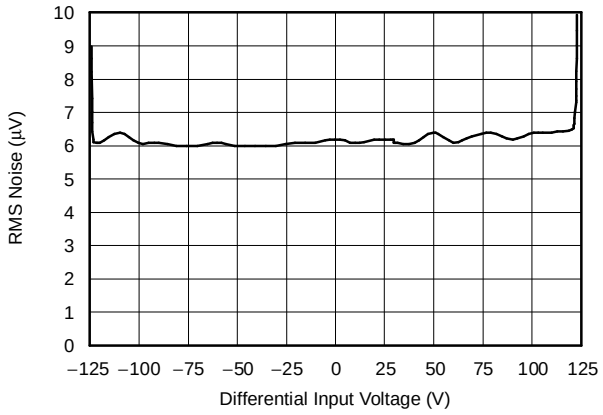


Figure 34.

APPLICATION INFORMATION

GENERAL DESCRIPTION

The ADS1208 is a 2nd-order delta-sigma modulator, which is implemented with a switched capacitor circuit. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital bit stream, which accurately represents the analog input voltage over time, appears at the output of the converter.

The ADS1208 is optimized for Hall sensors and similar applications. As a result, the full-scale input range is $\pm V_{REFIN}/20$, which is typically ±125mV. However, to achieve good noise and linearity, only 80% of this range should be used (±100mV). The analog input pins (V_{IN+} and V_{IN-}) are internally buffered with two low-noise, high bandwidth, low offset amplifiers.

A current source is also integrated into the ADS1208 that can be used for biasing a Hall element or bridge sensor. This current can be programmed with a resistor that must be placed between AVDD and IADJ.

Additionally, the ADS1208 includes a reference voltage source with a buffered output. A reference input pin is provided as well. The voltage at the REFIN pin sets the analog input range.

The device digital interface is fully compatible with the ADS1202 and ADS1203. The ADS1208 also provides inverted outputs of MCLK and MDATA ($\overline{MCLK}$ and $\overline{MDATA}$, respectively) to increase noise immunity for the digital data transmission.

The clock source can be internal as well as external. Different clock frequencies in combination with an optional digital filter enable a variety of solutions and signal bandwidths.

Figure 5 (page 8) shows the functional block diagram with external circuitry. The Hall element is biased from the internal current source. The current is set by resistor R_{ADJ}. An offset compensation of the Hall element is enabled by the optional resistors R1 to R4. The analog inputs V_{IN+} and V_{IN-} are directly connected with the Hall element outputs. The reference input REFIN is connected to the reference output REFOUT with an optional RC low-pass filter, for additional noise filtering. For both power-supply pairs, AVDD and BVDD, decoupling capacitors of 100nF and 10µF (respectively) are recommended.

ANALOG SECTION

Modulator

The 2nd-order modulator acts as a filter. The input signal is low-passed while the quantization noise is shifted to higher frequencies. A digital low-pass filter should be used at the output of the delta-sigma modulator. The primary purpose of the digital filter is to remove high-frequency noise. The secondary purpose is to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (that is, decimation). A digital signal processor (DSP), microcontroller (µC), or field programmable gate array (FPGA) could be used to implement the digital filter.

Analog Inputs

The internal sampling capacitors present a very significant load that needs to be recharged within 50ns. The ADS1208 provides two input buffers to decouple the sampling capacitors from the pins (V_{IN+}, V_{IN-}). These buffers provide a high bandwidth (typically, 50MHz) at a low noise and low offset. This configuration improves the system performance significantly, if the input source has a high impedance in the kΩ range. A source impedance in this range without buffers would decrease THD and linearity significantly, and would also cause a gain error that changes with supply or temperature.

The input buffers have an auto zero function to reduce the input offset. The auto zero switches of the input buffers may apply a glitch of 10fC to 50fC to the signal source in each clock cycle. For this reason, placing a 1nF capacitor between the inputs is recommended, if the source impedance is larger than 500Ω. See Figure 35 for the equivalent input circuit, including the protection diodes.

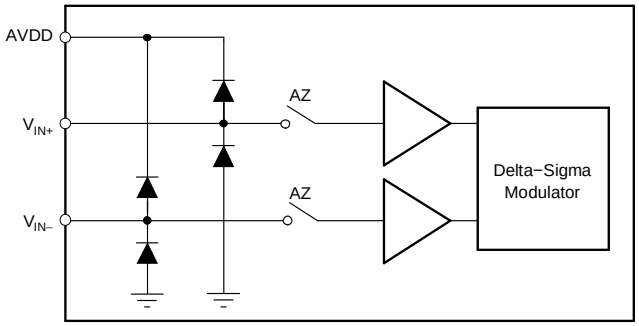


Figure 35. Equivalent Input Circuit

Internal Reference

The ADS1208 includes a 2.5V reference. The reference output is connected to the REFOUT pin via an output buffer that can source 3mA. The sink current is limited to 50µA. The output resistance of this buffer is 0.3Ω. The internal reference is also used to control the current source at the IOUT pin.

The ADS1208 additionally provides a REFIN pin. The applied voltage V_{REFIN} sets the gain of the internal

modulator. An external reference could vary from 0.5V to 3V. The modulator input range is defined to $\pm V_{REFIN}/20$. For a 2.5V reference, the full-scale range is ±125mV. The REFIN pin is decoupled from the modulator with a buffer.

Current Source for the Hall Element

Internal circuitry (see Figure 36) forces the IADJ pin to a potential of:

$$V_{IADJ} = AVDD - \frac{V_{REFOUT}}{5}$$

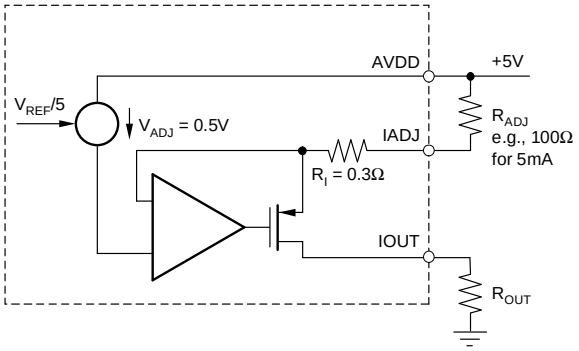


Figure 36. Current Source

This means that the voltage drop of the resistor R_{ADJ} is equal to the current source reference V_{ADJ}.

$$V_{ADJ} = \frac{V_{REFOUT}}{5} = 0.5\ V$$

With resistor R_{ADJ} placed between AVDD and IADJ, a current of:

$$I_{OUT} = \frac{V_{REFOUT}}{5 \cdot (R_{ADJ} + 0.3\Omega)}$$

is sourced out of the IOUT pin. The current should be set between 1mA and 8mA. However, it is also possible to leave the pin open. As the Hall voltage is directly proportional to this current, the input voltage to the modulator V_{IN} is directly proportional to the internal reference voltage V_{REFOUT}. As the filtered digital output data word Y_{OUT} from the modulator is also directly proportional to the reference voltage, the drift of the reference is actually cancelled out. Be aware that this is only the case if the application is using IOUT to drive the Hall sensor and if REFIN is connected to REFOUT.

$$Y_{OUT} \sim \frac{1}{R_{ADJ}}$$

This means that trimming the resistor can calibrate the gain of the entire system. The resistor can be chosen to be stable over temperature, or to compensate any temperature behavior of the Hall sensor.

DIGITAL OUTPUT

A differential analog input signal of 0V ideally produces a stream of 1s and 0s that are high 50% of the time and low 50% of the time. A differential analog input of +100mV produces a stream of 1s and 0s that are high 80% of the time. A differential analog input of –100mV produces a stream of 1s and 0s that are high 20% of the time. The input voltage versus the output modulator signal is shown in Figure 37.

DIGITAL INTERFACE

Introduction

The analog signal that is connected to the input of the delta-sigma modulator is converted using the clock signal that is applied to the modulator. The result of the conversion, or modulation, is the output signal MDATA from the delta-sigma modulator. In most applications, the two standard signals (MCLK and MDATA) are provided from the modulator to an ASIC, FPGA, DSP, or µC (each with an implemented filter, respectively). A single wire interface is provided in Mode 2, where the data stream is Manchester encoded. This configuration reduces the costs for galvanic isolation.

The interface also provides the inverted outputs $\overline{\text{MDATA}}$ and $\overline{\text{MCLK}}$ for the signals MDATA and MCLK, respectively. These inverted outputs are useful for systems with high common-mode noise at the digital data transmission. The digital interface is specified for the voltage range of 2.7V to 5.5V.

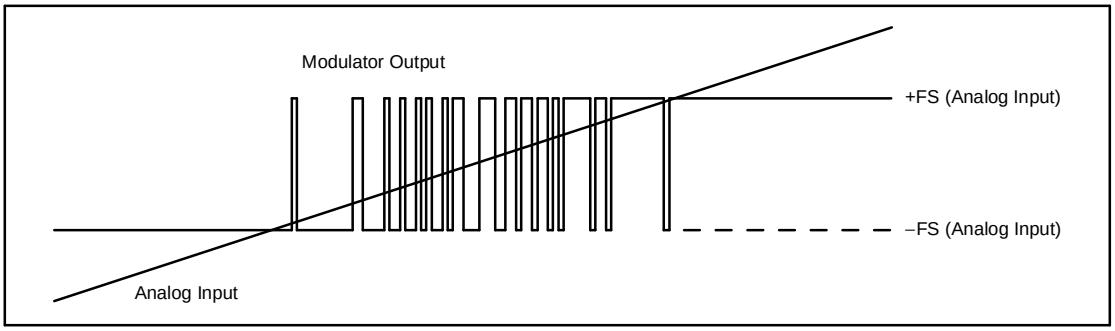


Figure 37. Analog Input vs Modulator Output of the ADS1208

Different Modes of Operation

The typical system clock of the ADS1208 is 20MHz. The system clock can be provided either from the internal 20MHz RC oscillator or from an external clock source. For this reason, the $\overline{\text{MCLK}}$ pin is bidirectional and is controlled by the mode setting. The system clock is divided by two for the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 24MHz, the modulator operates between 500kHz and 12MHz. The four modes of operation for the digital data interface are shown in Table 2.

Mode 0

In Mode 0, the internal RC oscillator is running. The data is provided at the MDATA and $\overline{\text{MDATA}}$ output pins, and the modulator clock at the MCLK and $\overline{\text{MCLK}}$ pins. The data changes at the falling edge of MCLK. Therefore, it can safely be strobed with the rising edge. See Figure 1 on page 5.

Mode 1

In Mode 1, the internal RC oscillator is running. The data is provided at the MDATA and $\overline{\text{MDATA}}$ output pins. The frequency at the MCLK and $\overline{\text{MCLK}}$ pins is equivalent to the modulator clock frequency divided by two. The data must be strobed at both the rising and falling edges of MCLK. The data at MDATA changes in the middle, between the rising and falling edge. In this mode, the frequency of both MCLK and MDATA is only 5MHz. See Figure 2 on page 5.

Mode 2

In Mode 2, the internal RC oscillator is running. The data is Manchester encoded and is provided at the MDATA and $\overline{\text{MDATA}}$ pins. There is no clock output in this mode. The MCLK and $\overline{\text{MCLK}}$ outputs are set to low. The Manchester coding allows the data transfer with only a single wire. See Figure 3 on page 6.

Mode 3

In Mode 3, the internal RC oscillator is disabled. The system clock must be provided externally at the input $\overline{\text{MCLK}}$. The system clock must have twice the frequency of the chosen modulator clock. The data is provided at the MDATA and $\overline{\text{MDATA}}$ output pins. Since the modulator runs with half the frequency of the system clock, the data changes at every other falling edge of the external clock. The data can be safely strobed at every rising edge of the MCLK output, which provides half the frequency of the system clock. This mode allows synchronous operation to any digital system or the use of modulator clocks different from 10MHz. See Figure 4 on page 6.

Filter Usage

The modulator generates only a bitstream, which is different from the digital word of an analog-to-digital converter (ADC). In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter. A very simple filter built with minimal effort and hardware is the Sinc^3 filter, shown in Equation 1:

$$H(z) = \left(\frac{1 - z^{-\text{OSR}}}{1 - z^{-1}}\right)^3 \quad (1)$$

Table 2. Operating Mode Definition and Description

MODE DEFINITION		M1	M0
Mode 0	Internal clock, synchronous data output	Low	Low
Mode 1	Internal clock, synchronous data output, half output clock frequency	Low	High
Mode 2	Internal clock, Manchester encoded data output, no clock output	High	Low
Mode 3	External clock, synchronous data output	High	High

This filter provides the best output performance at the lowest hardware size (for example, a count of digital gates). For oversampling ratios in the range of 16 to 256, the Sinc^3 filter is a good choice. All characterizations in this datasheet were obtained using a Sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word length of 16 bits. In a Sinc^3 filter response (shown in Figure 38 and Figure 39), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3dB point is located at half the Nyquist frequency, or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type for better frequency response. Device performance can be improved, for example, by using a cascaded filter structure. The first decimation stage can be a Sinc^3 filter with a low OSR and a second stage, high-order filter.

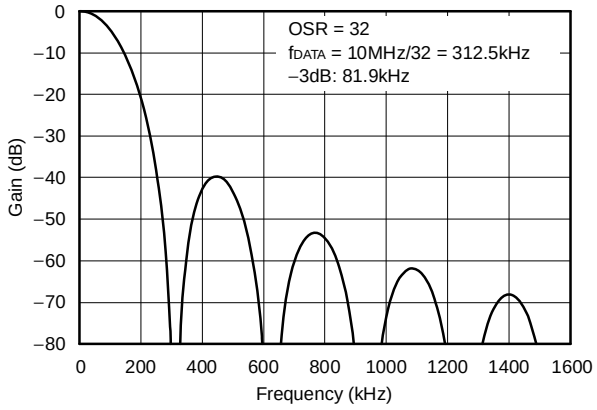


Figure 38. Frequency Response of Sinc^3 Filter

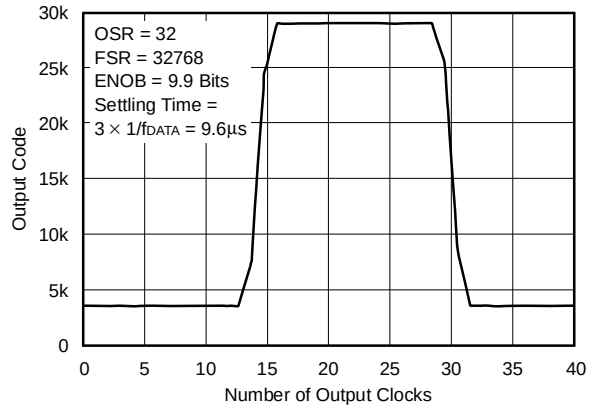


Figure 39. Pulse Response of Sinc^3 Filter (f_{MOD} = 10MHz)

The effective number of bits (ENOB) can be used to compare the performance of ADCs and delta-sigma modulators. Figure 40 shows the ENOB of the ADS1208 with different filter types. In this datasheet, the ENOB is calculated from the SNR:

SNR = 1.76dB + 6.02dB × ENOB

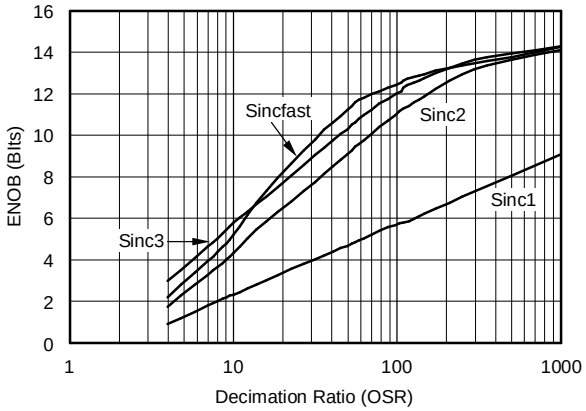


Figure 40. Measured ENOB vs OSR

In motor control applications, a very fast response time for overcurrent detection is required. There is a constraint between 1µs and 5µs with 3 bits to 7 bits of resolution. The time for full settling depends on the filter order. Therefore, the full settling of the Sinc^3 filter needs three data clocks and the Sinc^2 filter needs two data clocks. The data clock is equal to the modulator clock divided by the OSR. For overcurrent protection, filter types other than Sinc^3 might be a better choice. A good example is a Sinc^2 filter. Figure 41 compares the settling time of different filter types. The Sincfast is a modified Sinc^2 filter, as shown in Equation 2:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 \left(1 + z^{-2 \cdot OSR}\right) \quad (2)$$

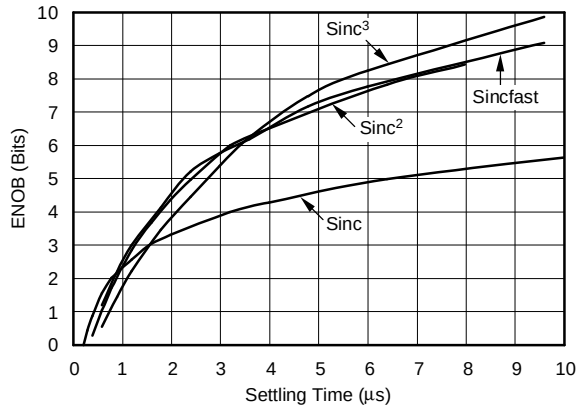


Figure 41. Measured ENOB vs Settling Time

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

LAYOUT CONSIDERATIONS

Power Supplies

The ADS1208 has two power supplies, AVDD and BVDD. If there are separate analog and digital power supplies on the board, a good design approach is to have AVDD connected to the analog and BVDD to the digital power supply. Another possible approach to control noise is the use of a resistor on the power supply. The connection can be made between the ADS1208 power supply pins via a 5Ω resistor. The combination of this resistor and the decoupling capacitors between the power supply pins AVDD and AGND provides some filtering. The analog supply must be well-regulated and offer low noise. For designs requiring higher resolution from the ADS1208, power-supply rejection will be a concern. The digital power supply has high-frequency noise that can be coupled into the analog portion of the ADS1208. This noise can originate from switching power supplies, microprocessors, or DSPs. High-frequency noise will generally be rejected by the external digital filter at integer multiples of MCLK. Just below and above these frequencies, noise will alias back into the passband of the digital filter, affecting the conversion result. Inputs to the ADS1208, such as V_{IN+}, V_{IN-} and MCLK should not be present before the power supply is turned on. Violating this condition could cause latch-up. If these signals are present before the supply is turned on, series resistors should be used to limit the input current. Additional user testing may be necessary in order to determine the appropriate connection between the ADS1208 and different power supplies.

Grounding

Analog and digital sections of the system design must be carefully and cleanly partitioned. Each section should have its own ground plane, with no overlap between them. Do not join the ground planes. Instead, connect the two planes with a moderate signal trace underneath the modulator. For multiple modulators, connect the two ground planes as close as possible to one central location for all of the modulators. In some cases, experimentation may be required to find the best point to connect the two planes together.

Decoupling

Good decoupling practices must be used for the ADS1208 and for all components in the system design. All decoupling capacitors, specifically the 0.1µF ceramic capacitors, must be placed as close as possible to the respective pin being decoupled. A 1µF and 10µF capacitor, in parallel with the 0.1µF ceramic capacitor, can be used to decouple AVDD to AGND. At least one 0.1µF ceramic capacitor must be used to decouple BVDD to BGND, as well as for the digital supply on each digital component

It is highly recommended to place the 100nF compensation capacitor, which is connected between AVDD and AGND, directly at pins 3 and 6. Otherwise, current glitches from the internal circuitry can cause glitches in the supply, which again causes jitter on the internal clock signal. This jitter degrades the noise performance of the ADS1208. The input signals V_{IN+} and V_{IN-} can be routed underneath this capacitor.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1208IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AZ1208I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

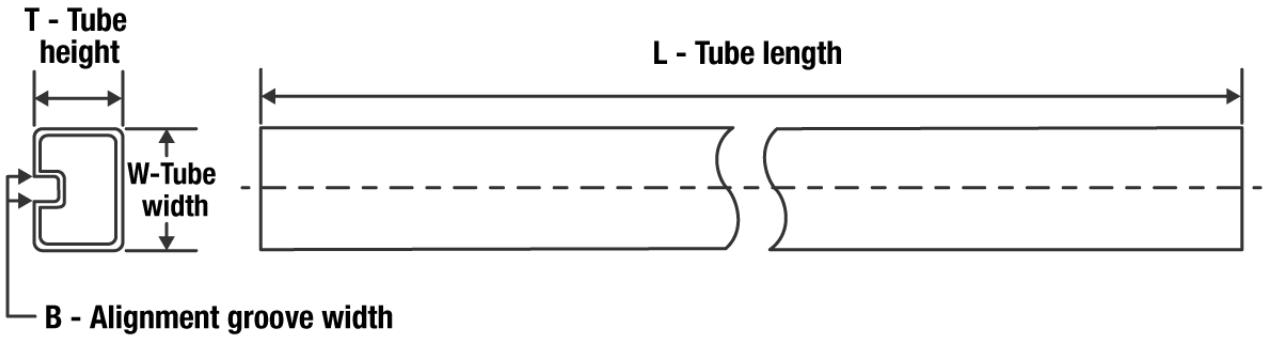
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE

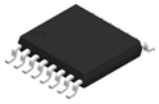


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1208IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

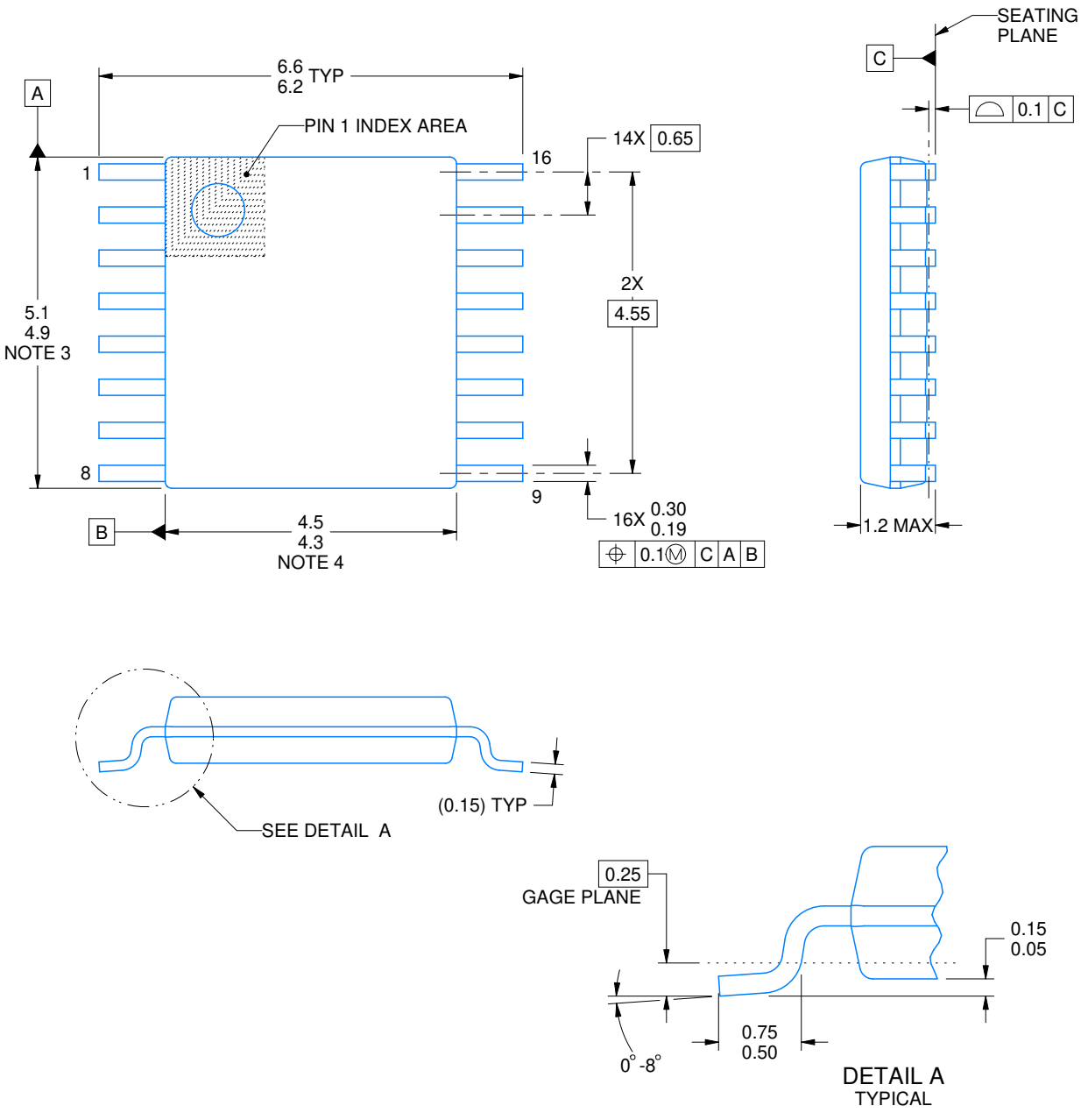
PACKAGE OUTLINE

PW0016A



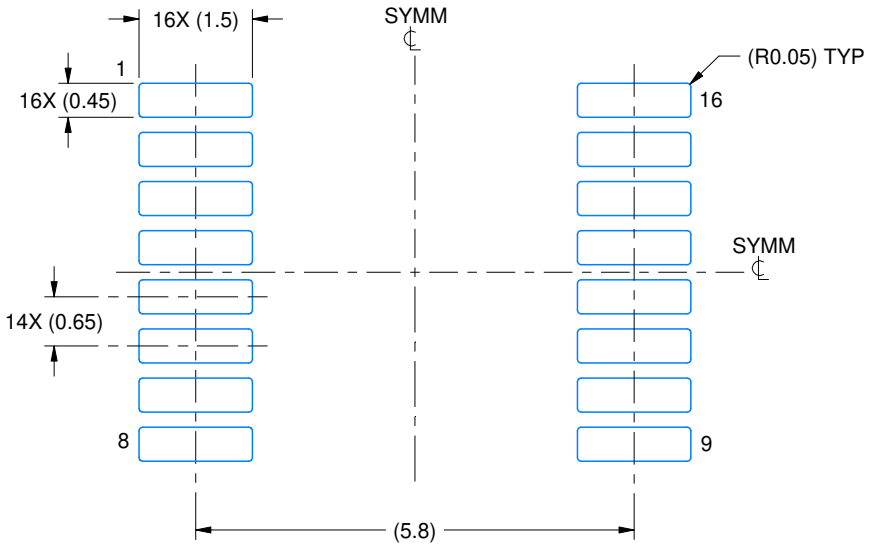
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

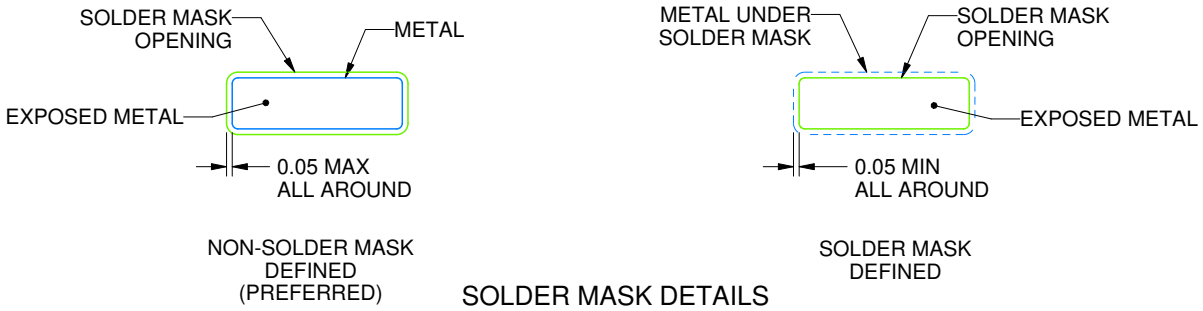


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

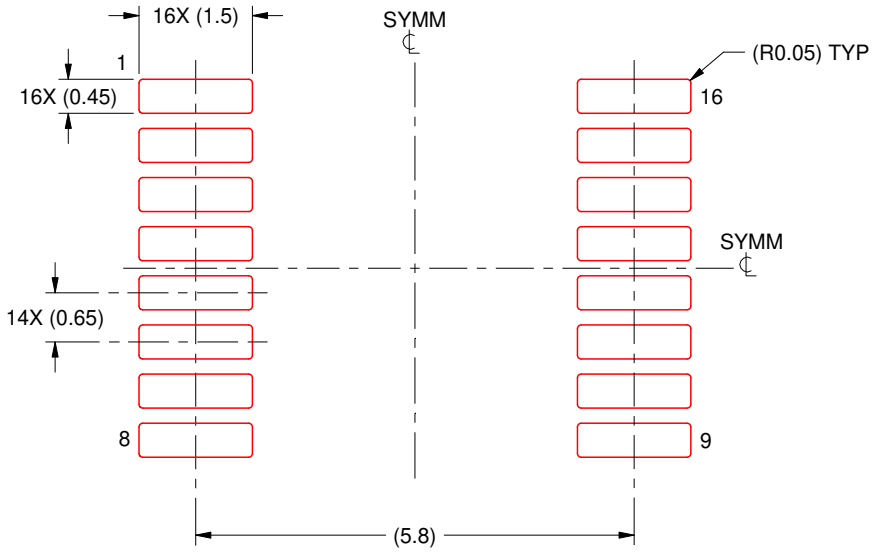


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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