PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

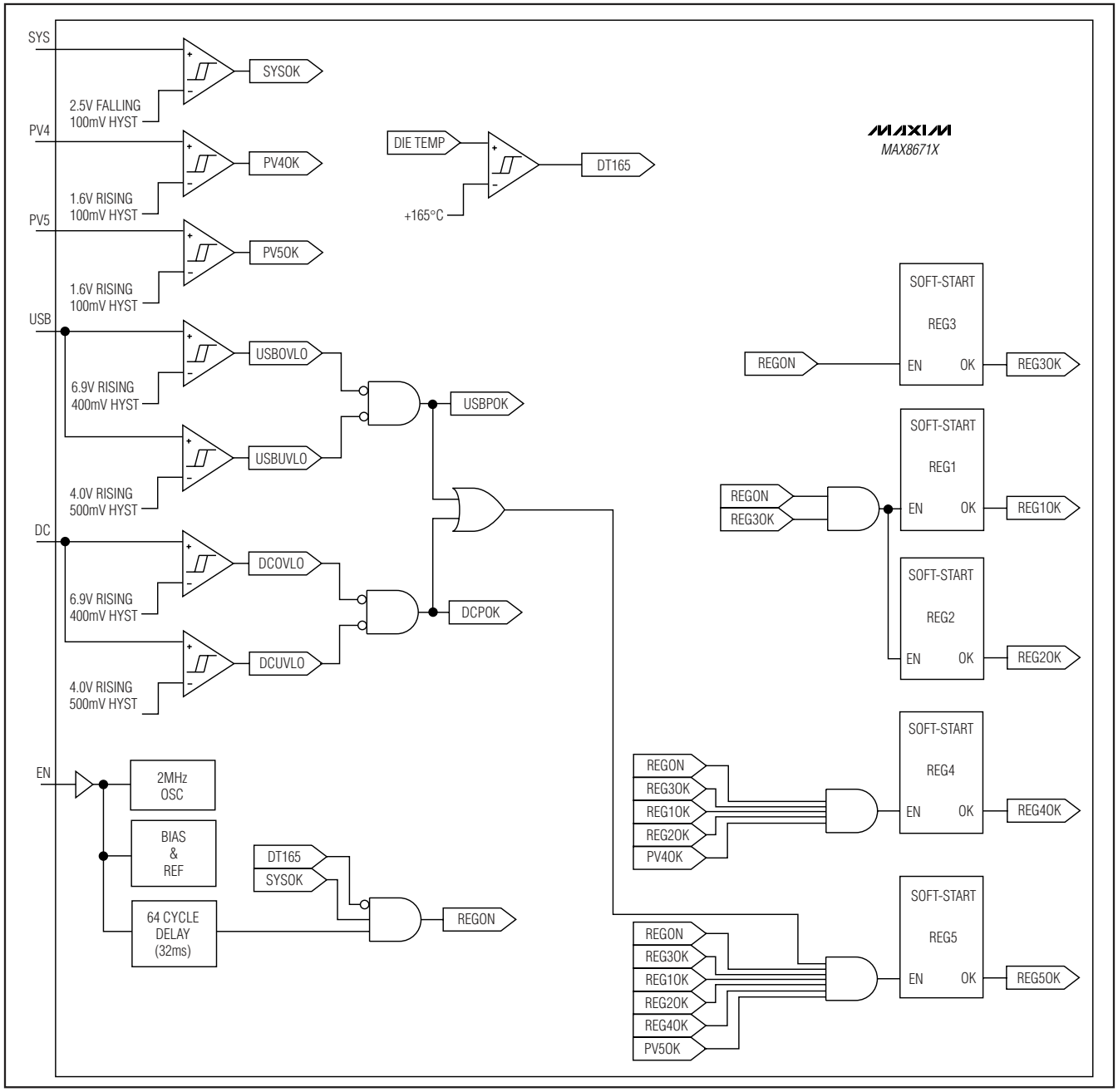

Figure 11. Enable/Disable Logic

Enable/Disable (EN) and Sequencing

Figures 11, 12, and 13 show how the five MAX8671X regulators are enabled and disabled. With a valid SYS voltage and die temperature, asserting EN high enables REG1–REG4. Pulling EN low disables REG1–REG5. REG5 is intended to power the system USB transceiver circuitry, which is only active when USB power is available. Therefore, a valid source must be on either the USB or DC input for REG5 to enable.

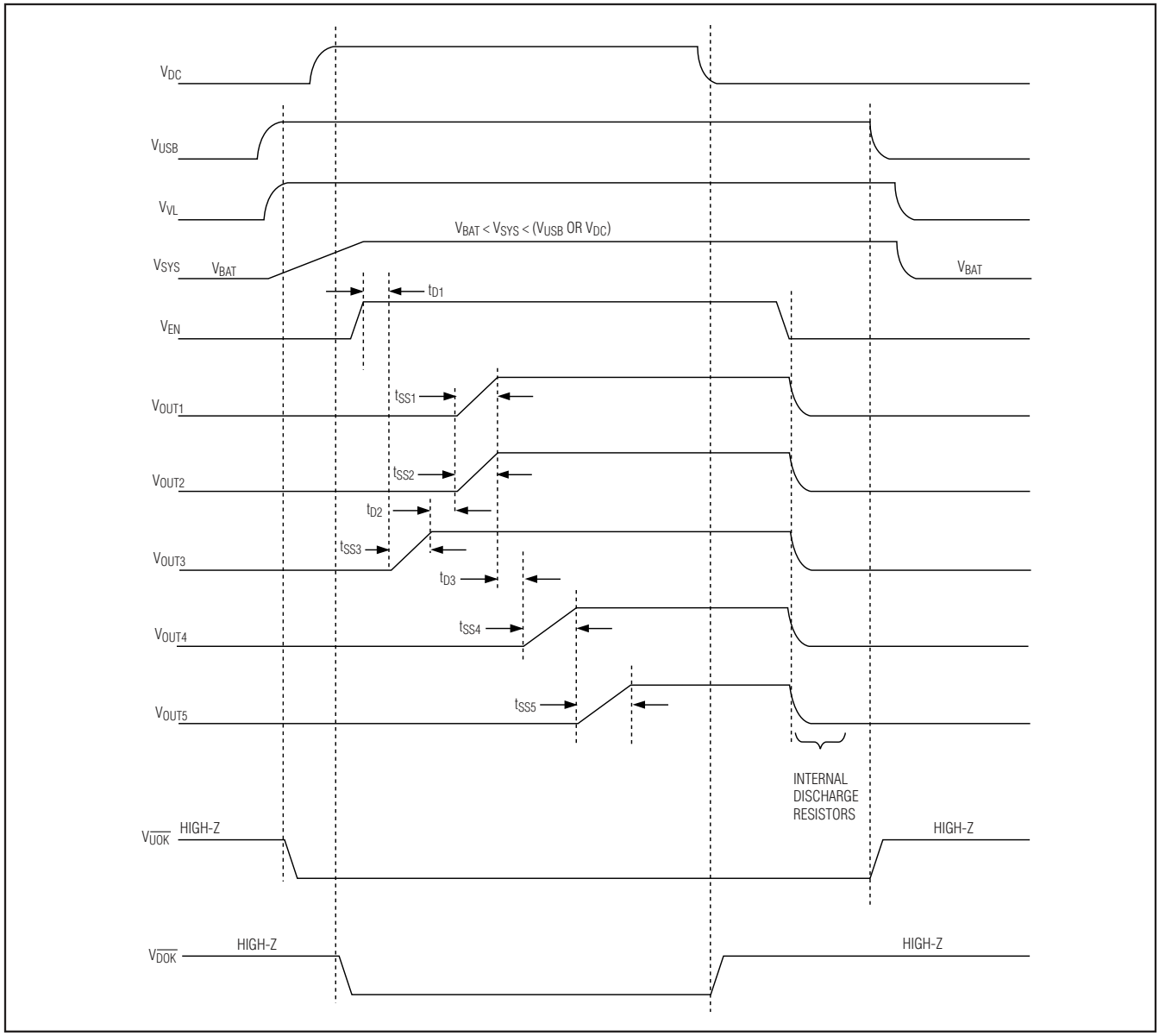

Figure 12. Enable and Disable Waveforms

The VL regulator is not controlled by EN. It is powered from the higher of USB or DC and automatically powers up when either of the power inputs exceeds approximately 1.5V. Similarly, VL automatically powers down when both the USB and DC power inputs are removed.

Soft-Start/Inrush Current

The MAX8671X implements soft-start on many levels to control inrush current, to avoid collapsing supply voltages, and to fully comply with the USB 2.0 specifications. All USB, DC, and charging functions implement soft-start. The USB and DC nodes only require 4.7µF of input capacitance. Furthermore, all regulators implement soft-start to avoid transient overload of power inputs (Figure 12).

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Active Discharge in Shutdown

Each MAX8671X regulator (REG1–REG5) has an internal 1kΩ resistor that discharges the output capacitor when the regulator is off. The discharge resistors ensure that the load circuitry powers down completely. The internal discharge resistors are connected when a regulator is disabled and when the device is in UVLO with an input voltage greater than 1.0V. With an input voltage less than 1.0V, the internal discharge resistors are not activated.

Undervoltage and Overvoltage Lockout

USB/DC UVLO

Undervoltage lockout (UVLO) prevents an input supply from being used when its voltage is below the operating range. When the USB voltage is less than the USB UVLO threshold (4.0V typ), the USB input is disconnected from SYS, and $\overline{UOK}$ goes high impedance. When the DC voltage is less than the DC UVLO threshold (4.0V typ), the DC input is disconnected from SYS, and $\overline{DOK}$ goes high impedance. In addition, when both USB and DC are in UVLO, the battery charger is disabled, and BAT is connected to SYS through the internal system load switch. REG1–REG4 are allowed to operate from the battery without power at USB or DC. REG5 is intended to power the system USB transceiver circuitry, which is only active when USB power is available. Therefore, a valid source must be present on either the USB or DC input for REG5 to enable.

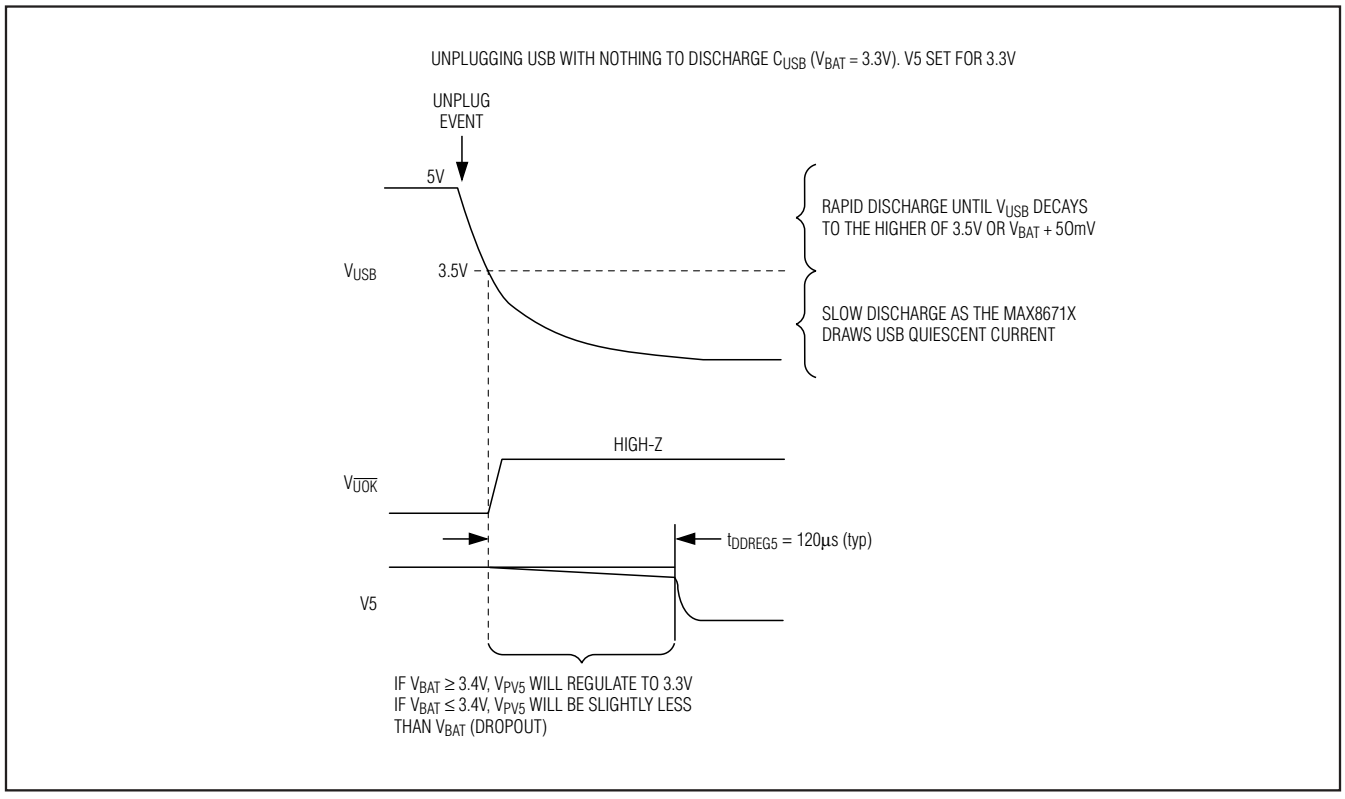


Figure 13. REG5 Disable Detail

USB/DC OVLO

Overvoltage lockout (OVLO) prevents an input supply from being used when its voltage exceeds the operating range. Both USB and DC withstand input voltages up to 14V. When the USB voltage is greater than the USB OVLO threshold (6.9V typ), the USB input is disconnected from SYS, and $\overline{UOK}$ goes high impedance. When the DC voltage is greater than the DC OVLO threshold (6.9V typ), the DC input is disconnected from SYS, and $\overline{DOK}$ goes high impedance. In addition, when both DC and USB are in OVLO, the battery charger is disabled, and BAT is connected to SYS through the internal system load switch. REG1–REG4 are allowed to operate from the battery when USB and DC are in overvoltage lockout. The VL supply remains active in OVLO. REG5 is intended to power the system USB transceiver circuitry, which is only active when USB power is available. A valid source must be present on either the USB or DC input for REG5 to enable.

SYS UVLO

A UVLO circuit monitors the voltage from SYS to ground (V_{SYS}). When V_{SYS} falls below V_{UVLO_SYS} (2.5V typ), REG1–REG5 are disabled. V_{UVLO_SYS} has a 100mV hysteresis. The VL supply remains active in SYS UVLO.

REG4/REG5 UVLO

A UVLO circuit monitors the PV4 and PV5 LDO power inputs. When the PV_ voltage is below 1.6V, it is invalid and the LDO is disabled.

Thermal Limiting and Overload Protection

The MAX8671X is packaged in a 5mm x 5mm x 0.8mm 40-pin thin QFN. Table 7 shows the thermal characteristics of this package. The MAX8671X has several mechanisms to control junction temperature in the event of a thermal overload.

Table 7. 5mm x 5mm x 0.8mm Thin QFN Thermal Characteristics

	SINGLE-LAYER PCB	MULTILAYER PCB
Continuous Power Dissipation	1777.8mW Derate 22.2mW/°C above +70°C	2857.1mW Derate 35.7mW/°C above +70°C
*θ_{JA}	45°C/W	28°C/W
θ_{JC}	1.7°C/W	1.7°C/W

θ_{JA} is specified according to the JESD51 standard.

Smart Power Selector Thermal-Overload Protection

The MAX8671X reduces the USB and DC current limits by 5%/°C when the die temperature exceeds +100°C. The system load (I_{SYS}) has priority over the charger current, so input current is first reduced by lowering charge current. If the junction temperature still reaches +120°C in spite of charge-current reduction, no input current is drawn from USB and DC; the battery supplies the entire load and SYS is regulated 82mV (V_{BSREG}) below BAT. Note that this on-chip thermal-limiting circuit is not related to and operates independently from the thermistor input.

Regulator Thermal-Overload Shutdown

The MAX8671X disables all regulator outputs (except VL) when the junction temperature rises above +165°C, allowing the device to cool. When the junction temperature cools by approximately 15°C, the regulators resume the state indicated by the enable input (EN) by repeating their soft-start sequence. Note that this thermal-overload shutdown is a fail-safe mechanism; proper thermal design should ensure that the junction temperature of the MAX8671X never exceeds the absolute maximum rating of +150°C.

Battery Charger Thermistor Input (THM)

The THM input connects to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature. Charging is suspended when the thermistor temperature is out of range. Additionally, the charge timers are suspended and charge status indicators report that the charger is in thermistor suspend (CST[1:2] = 01). When the thermistor comes back into range, charging resumes and the charge timer continues from where it left off. Table 8 shows THM temperature limits for various thermistor material constants. If the battery temperature monitor is not required, bias THM midway between V_L and AGND with a resistive divider—100kΩ ±5% resistors are recommended. Biasing THM midway between V_L and AGND bypasses this function.

Table 8. Trip Temperatures for Different Thermistors

THERMISTOR BETA (ß [K])	3000	3250	3500	3750	4250	4250
R_{TB} (kΩ)	10	10	10	10	10	10
R_{TP} (kΩ)	Open	Open	Open	Open	Open	120
R_{TS} (kΩ)	Short	Short	Short	Short	Short	Short
Resistance at +25°C [kΩ]	10	10	10	10	10	10
Resistance at +50°C [kΩ]	4.59	4.30	4.03	3.78	3.32	3.32
Resistance at 0°C [kΩ]	25.14	27.15	29.32	31.66	36.91	36.91
Nominal Hot Trip Temperature [°C]	55	53	51	49	46	45
Nominal Cold Trip Temperature [°C]	-3	-1	0	2	5	0

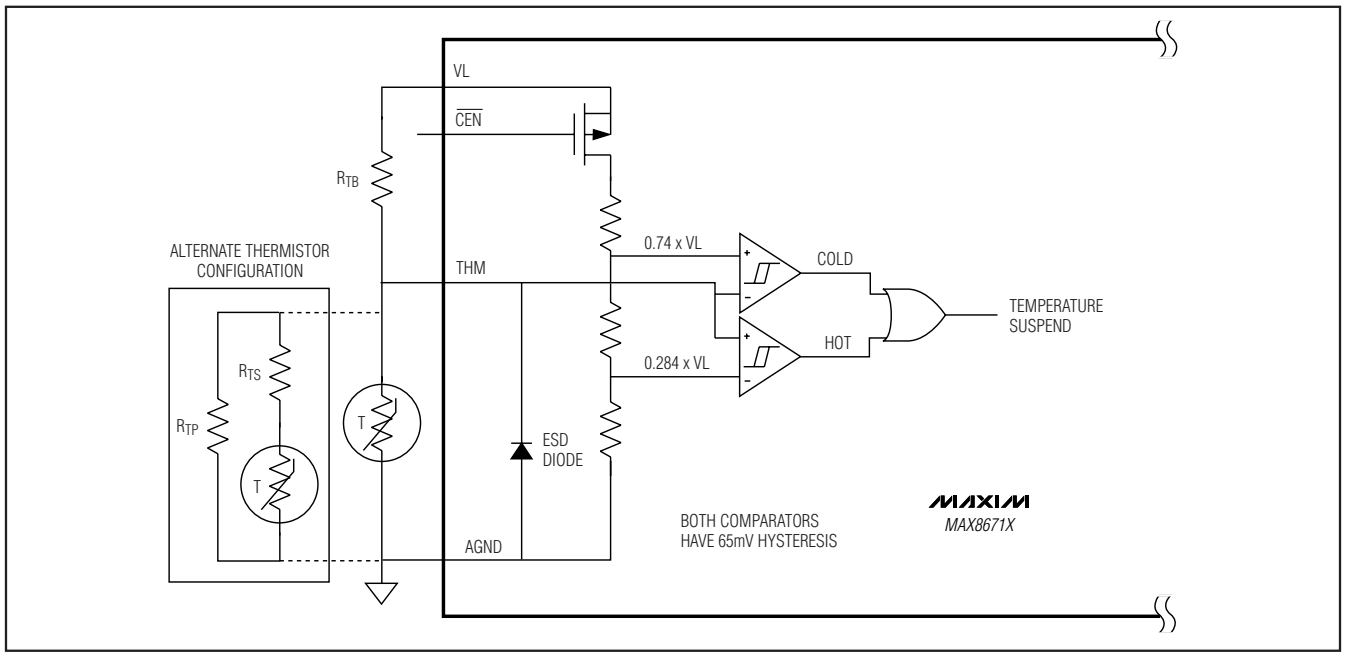


Figure 14. Thermistor Input

Since the thermistor monitoring circuit employs an external bias resistor from THM to VL (R_{TB} in Figure 14), any resistance thermistor can be used as long as the value of R_{TB} is equivalent to the thermistor's +25°C resistance. For example, with a 10kΩ at +25°C thermistor, use 10kΩ at R_{TB}, and with a 100kΩ at +25°C thermistor, use 100kΩ at R_{TB}. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{\left\{\beta\left(\frac{1}{T+273}-\frac{1}{298}\right)\right\}}$$

where:

R_T = The resistance in ohms of the thermistor at temperature T in Celsius

R_{25} = The resistance in ohms of the thermistor at +25°C

β = The material constant of the thermistor that typically ranges from 3000K to 5000K

T = The temperature of the thermistor in °C that corresponds to R_T

THM threshold adjustment can be accommodated by changing R_{TB}, connecting a resistor in series and/or in parallel with the thermistor, or using a thermistor with different material constant (β). For example, a +45°C hot threshold and 0°C cold threshold can be realized by using a 10kΩ thermistor with a β of 4250K and connecting 120kΩ in parallel. Since the thermistor resistance near 0°C is much higher than it is near +50°C, a large parallel resistance lowers the cold threshold, while only slightly lowering the hot threshold. Conversely, a small series resistance raises the cold threshold, while only slightly raising the hot threshold. Raising R_{TB} lowers both the hot and cold thresholds, while lowering R_{TB} raises both thresholds.

PCB Layout and Routing

Good printed circuit board (PCB) layout is necessary to achieve optimal performance. Refer to the MAX8671 evaluation kit for Maxim's recommended layout.

Use the following guidelines for the best results:

- Use short and wide traces for high-current and discontinuous current paths.
- The step-down regulator power inputs are critical discontinuous current paths that require careful bypassing. Place the step-down regulator input bypass capacitors as close as possible to each switching regulator power input pair (PV_ to PG_).
- Minimize the area of the loops formed by the step-down converters' dynamic switching currents.
- The exposed paddle (EP) is the main path for heat to exit the IC. Connect EP to the ground plane with thermal vias to allow heat to dissipate from the device.
- The MAX8671X regulator feedback nodes are sensitive high-impedance nodes. Keep these nodes as short as possible and away from the inductors.
- The thermistor node is high impedance and should be routed with care.
- Make power ground connections to a power ground plane. Make analog ground connections to an analog ground plane. Connect the ground planes at a single point.

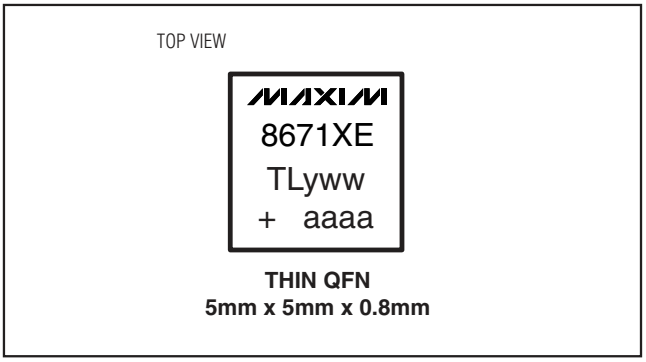


Figure 15. Package Marking Example

- The REG4 LDO is a high-performance LDO with high PSRR and low noise and care should be used in the layout to obtain the high performance. Generally, the REG4 LDO is powered from a step-down regulator output, and therefore, its input capacitor should be bypassed to the power ground plane. However, its output capacitor should be bypassed to the analog ground plane.
- BP is a high impedance node and leakage current into or out of BP can affect the LDO output accuracy.

Package Marking

The top of the MAX8671X package is laser etched as shown in Figure 15:

- "8671XETL" is the product identification code. The full part number is MAX8671XETL; however, in this case, the "MAX" prefix is omitted due to space limitations.
- "yww" is a date code. "y" is the last number in the Gregorian calendar year. "ww" is the week number in the Gregorian calendar. For example:

  "801" is the first week of 2008; the week of January 1st, 2008

  "052" is the fifty-second week of 2010; the week of December 27th, 2010.

  "aaaa" is an assembly code and lot code.

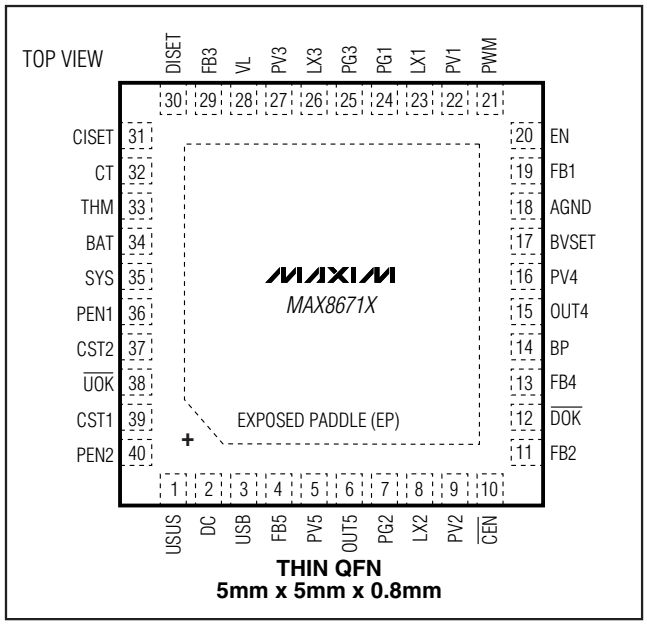
  "+" denotes lead-free packaging and marks the pin 1 location.

Chip Information

PROCESS: BiCMOS

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

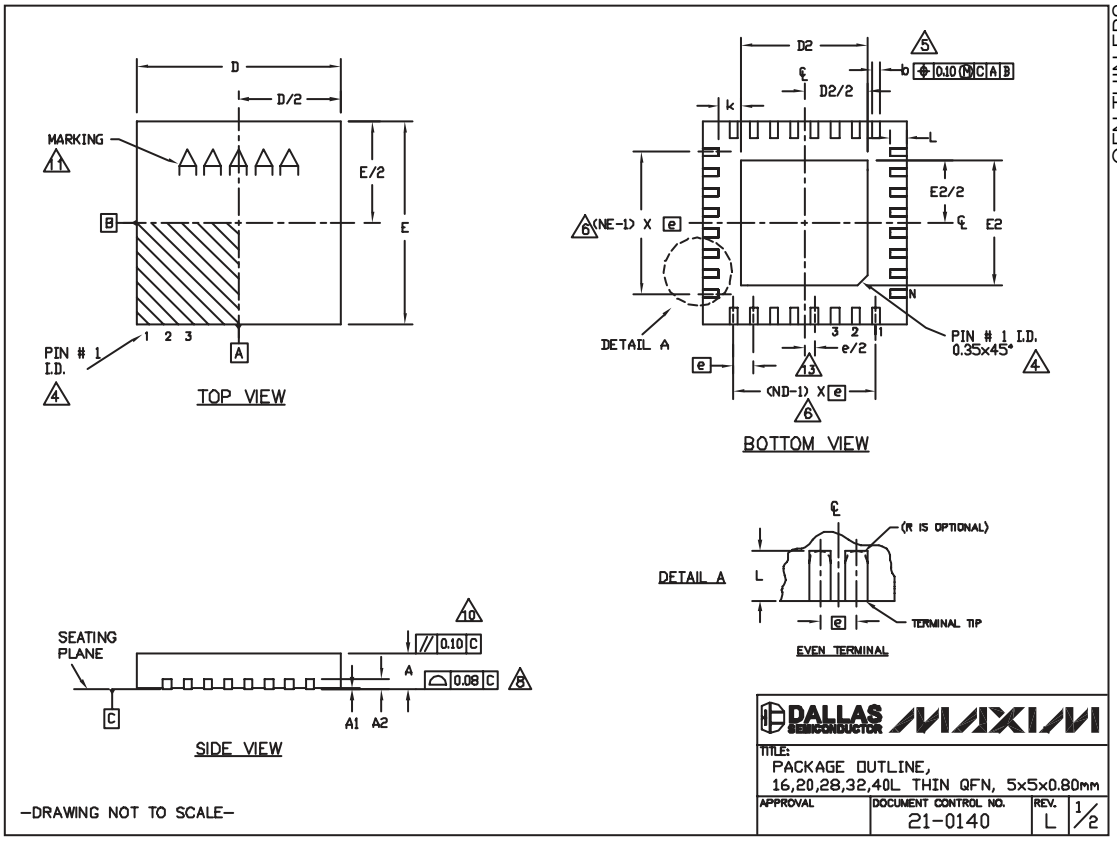
Pin Configuration



THIN QFN
5mm x 5mm x 0.8mm

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	L	2/2