

## QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

 Check for Samples: [SN65LBC174A](#) [SN75LBC174A](#)

### FEATURES

- Designed for TIA/EIA-485, TIA/EIA-422 and ISO 8482 Applications
- Signaling Rates <sup>(1)</sup> up to 30 Mbps
- Propagation Delay Times < 11 ns
- Low Standby Power Consumption 1.5-mA Max

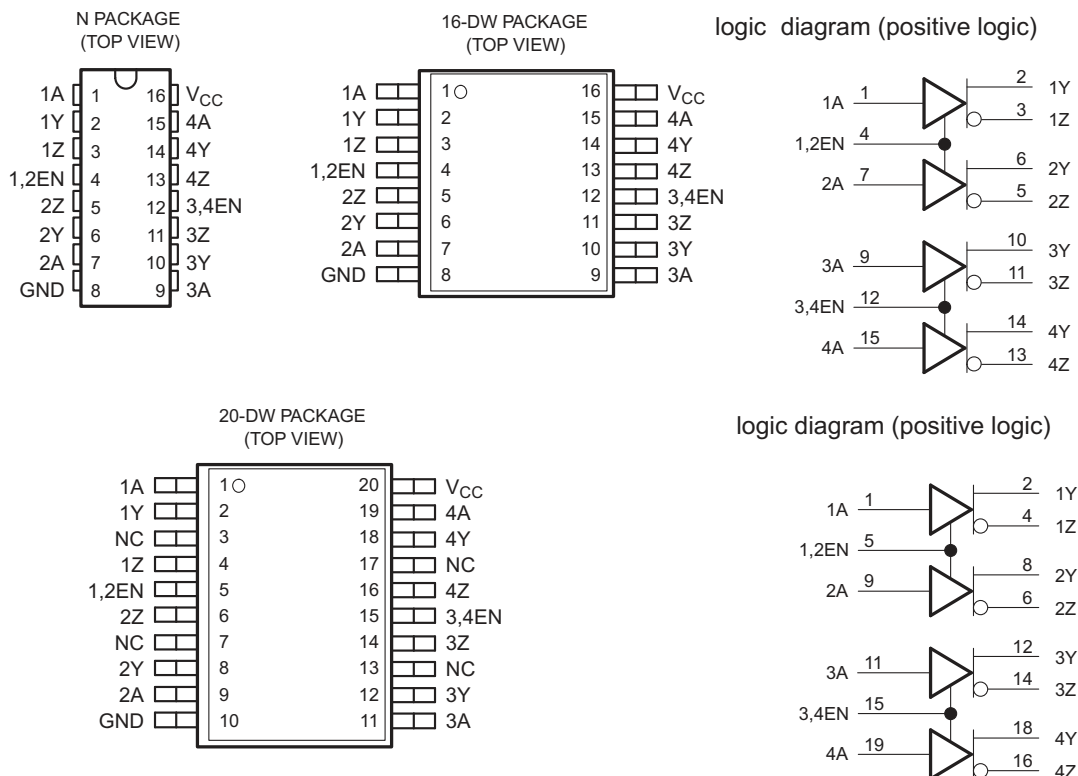
(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

- Output ESD Protection: 12 kV
- Driver Positive- and Negative-Current Limiting
- Power-Up and Power-Down Glitch-Free for Line Insertion Applications
- Thermal Shutdown Protection
- Industry Standard Pin-Out, Compatible With SN75174, MC3487, DS96174, LTC487, and MAX3042

### DESCRIPTION

The SN65LBC174A and SN75LBC174A are quadruple differential line drivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.

These devices are optimized for balanced multipoint bus transmission at signaling rates up to 30 million bits per second. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DESCRIPTION (CONTINUED)

Each driver features current limiting and thermal-shutdown circuitry making it suitable for high-speed multipoint applications in noisy environments. These devices are designed using LinBiCMOS<sup>®</sup>, facilitating low power consumption and robustness.

The two EN inputs provide pair-wise driver enabling, or can be externally tied together to provide enable control of all four drivers with one signal. When disabled or powered off, the driver outputs present a high-impedance to the bus for reduced system loading.

The SN75LBC174A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC174A is characterized for operation over the temperature range of –40°C to 85°C.

**Table 1. AVAILABLE OPTIONS**

T <sub>A</sub>	PACKAGE		
	16-PIN PLASTIC SMALL OUTLINE <sup>(1)</sup> (JEDEC MS-013)	20-PIN PLASTIC SMALL OUTLINE <sup>(1)</sup> (JEDEC MS-013)	16-PIN PLASTIC THROUGH-HOLE (JEDEC MS-001)
0°C to 70°C	SN75LBC174A16DW	SN75LBC174ADW	SN75LBC174AN
	MARKED AS 75LBC174A		
–40°C to 85°C	SN65LBC174A16DW	SN65LBC174DW	SN65LBC174AN
	MARKED AS 65LBC174A		

(1) Add R suffix for taped and reeled version.

**Table 2. FUNCTION TABLE (EACH DRIVER)<sup>(1)</sup>**

INPUT A	ENABLE EN	OUTPUT Y	OUTPUT Z
L	H	L	H
H	H	H	L
OPEN	H	H	L
L	OPEN	L	H
H	OPEN	H	L
OPEN	OPEN	H	L
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			VALUE / UNIT
Supply voltage range, $V_{CC}$ <sup>(2)</sup>			–0.3 V to 6 V
Voltage range at any bus (DC)			–10 V to 15 V
Voltage range at any bus (transient pulse through 100 $\Omega$ , see <a href="#">Figure 8</a> )			–30 V to 30 V
Input voltage range at any A or EN terminal, $V_I$			–0.5 V to $V_{CC} + 0.5$ V
Electrostatic discharge	Human body model <sup>(3)</sup>	Y, Z, and GND	$\pm 12$ kV
		All pins	$\pm 5$ kV
	Charged-device model <sup>(4)</sup>	All pins	$\pm 1$ kV
Storage temperature range, $T_{stg}$			–65°C to 150°C
Continuous power dissipation			See Dissipation Rating Table

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to GND.
- (3) Tested in accordance with JEDEC standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC standard 22, Test Method C101.

**Table 3. DISSIPATION RATING TABLE**

PACKAGE <sup>(1)</sup>	JEDEC BOARD MODEL	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(2)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
16 DW	LOW K	1200 mW	9.6 mW/°C	769 mW	625 mW
	HIGH K	2240 mW	17.9 mW/°C	1434 mW	1165 mW
20 DW	LOW K	1483 mW	11.86 mW/°C	949 mW	771 mW
	HIGH K	2753 mW	22 mW/°C	1762 mW	1432 mW
16 N	LOW K	1150 mW	9.2 mW/°C	736 mW	598 mW

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal	Y, Z	–7		12	V
High-level input voltage, $V_{IH}$	A, EN	2		$V_{CC}$	V
Low-level input voltage, $V_{IL}$		0		0.8	
Output current		–60		60	mA
Operating free-air temperature, $T_A$	SN75LBC174A	0		70	°C
	SN65LBC174A	–40		85	

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18 mA	-1.5	-0.77		V
V <sub>O</sub>	Open-circuit output voltage	Y or Z, No load	0		V <sub>CC</sub>	V
V <sub>OD(SS)</sub>	Steady-state differential output voltage magnitude <sup>(2)</sup>	No load (open circuit)	3		V <sub>CC</sub>	V
		R <sub>L</sub> = 54 Ω, See <a href="#">Figure 1</a>	1	1.6	2.5	
		With common-mode loading, See <a href="#">Figure 2</a>	1	1.6	2.5	
ΔV <sub>OD(SS)</sub>	Change in steady-state differential output voltage between logic states	See <a href="#">Figure 1</a>	-0.1		0.1	V
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	See <a href="#">Figure 3</a>	2	2.4	2.8	V
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage between logic states	See <a href="#">Figure 3</a>	-0.02		0.02	V
I <sub>I</sub>	Input current	A, EN	-50		50	μA
I <sub>OS</sub>	Short-circuit output current	V <sub>TEST</sub> = -7 V to 12 V, See <a href="#">Figure 7</a>	-200	V <sub>I</sub> = 0 V	200	mA
I <sub>OZ</sub>	High-impedance-state output current			V <sub>I</sub> = V <sub>CC</sub>		
I <sub>O(OFF)</sub>	Output current with power off	EN at 0 V	-50		50	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = 0 V or V <sub>CC</sub> , No load		V <sub>CC</sub> = 0 V	10	mA
				All drivers enabled	23	
C <sub>IN</sub>	Input Capacitance	A inputs		13		pF
		EN inputs		21		pF

(1) All typical values are at V<sub>CC</sub> = 5 V and 25°C.

(2) The minimum V<sub>OD</sub> may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.

## SWITCHING CHARACTERISTICS

over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high level output	5.5	8	11	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low level output	5.5	8	11	ns
t <sub>r</sub>	Differential output voltage rise time	3	7.5	11	ns
t <sub>f</sub>	Differential output voltage fall time	3	7.5	11	ns
t <sub>sk(p)</sub>	Pulse skew  t <sub>PLH</sub> - t <sub>PHL</sub>		0.6	2	ns
t <sub>sk(o)</sub>	Output skew <sup>(1)</sup>		0.6	2	
t <sub>sk(pp)</sub>	Part-to-part skew <sup>(2)</sup>			2	ns
t <sub>PZH</sub>	Propagation delay time, high-impedance-to-high-level output			25	ns
t <sub>PHZ</sub>	Propagation delay time, high-level-output-to-high impedance			25	
t <sub>PZL</sub>	Propagation delay time, high-impedance-to-low-level output			30	ns
t <sub>PLZ</sub>	Propagation delay time, low-level-output-to-high impedance			20	

(1) Output skew (t<sub>sk(o)</sub>) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

(2) Part-to-part skew (t<sub>sk(pp)</sub>) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

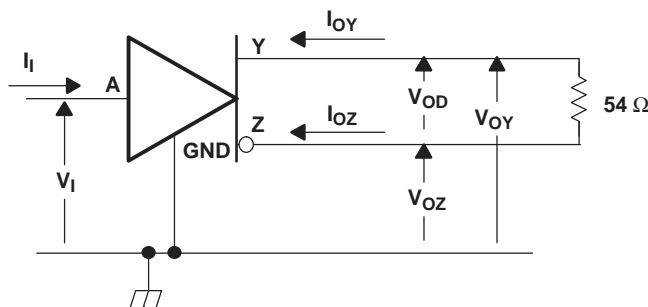


Figure 1. Test Circuit,  $V_{OD}$  Without Common-Mode Loading

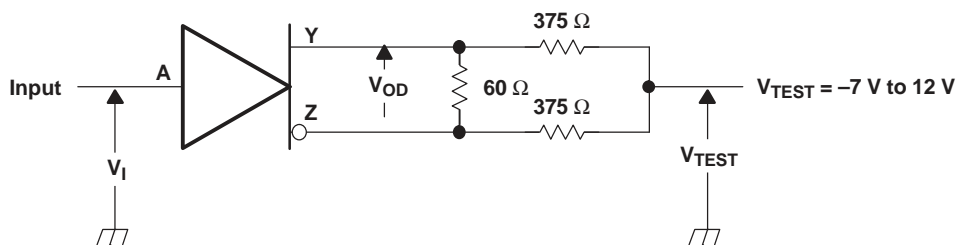
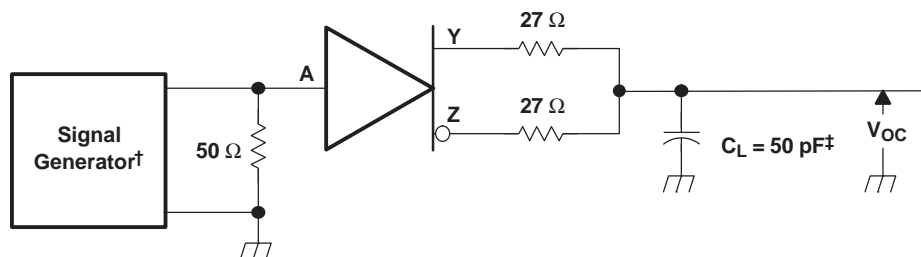


Figure 2. Test Circuit,  $V_{OD}$  With Common-Mode Loading

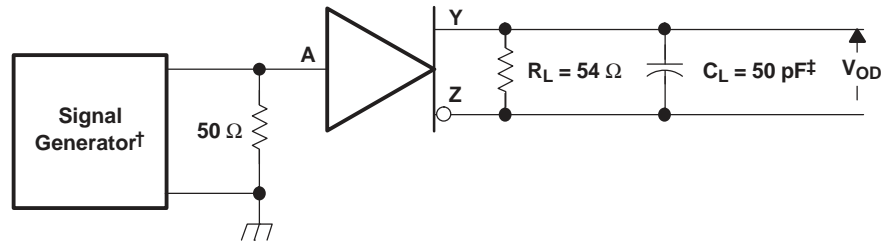


† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

‡ Includes probe and jig capacitance

Figure 3.  $V_{OC}$  Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

‡ Includes probe and jig capacitance

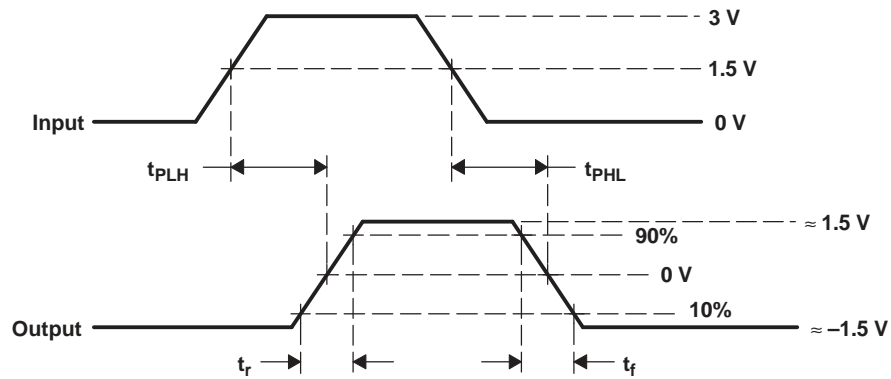
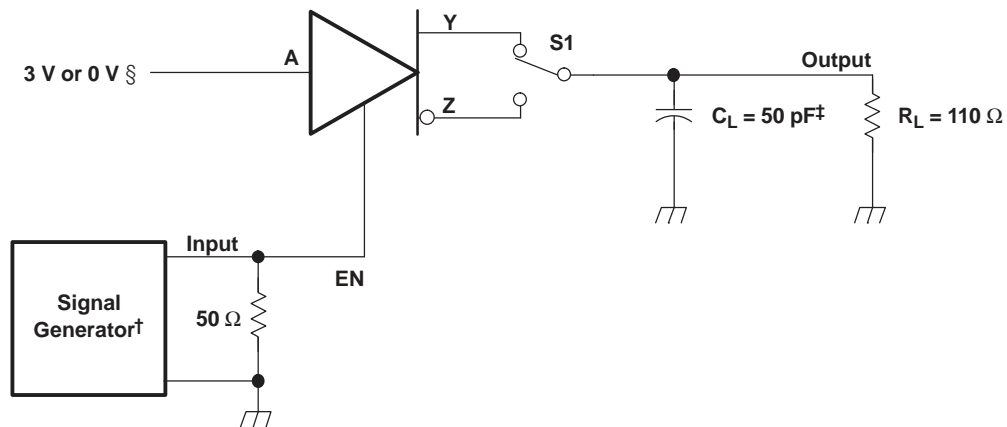


Figure 4. Output Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

‡ Includes probe and jig capacitance

§ 3 V if testing Y output, 0 V if testing Z output

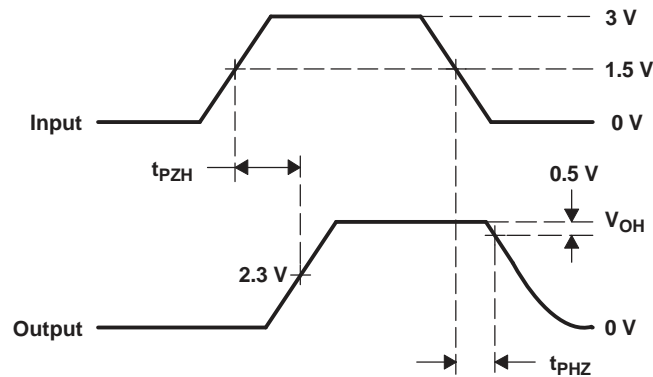
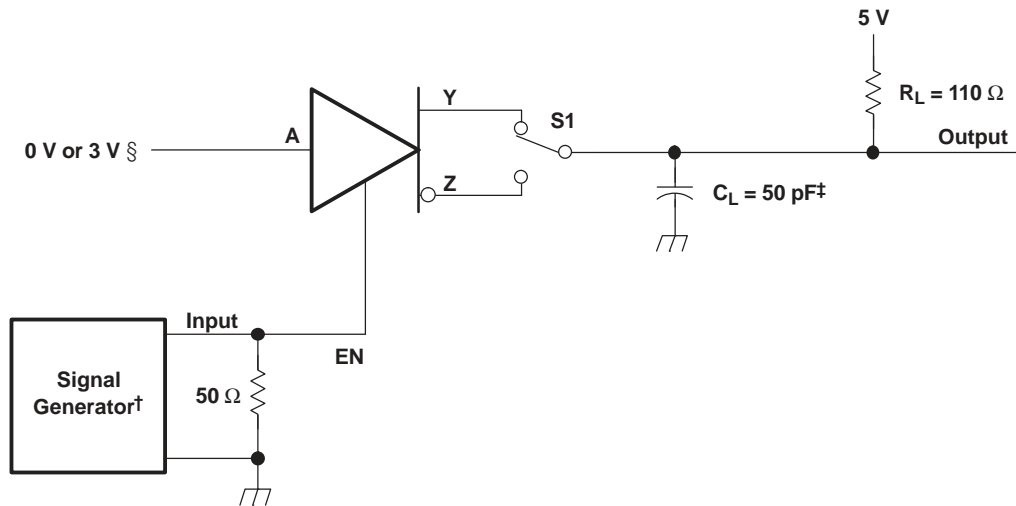


Figure 5. Enable Timing Test Circuit and Waveforms,  $t_{PZH}$  and  $t_{PHZ}$

PARAMETER MEASUREMENT INFORMATION (continued)



† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$   
 ‡ Includes probe and jig capacitance  
 § 3 V if testing Y output, 0 V if testing Z output

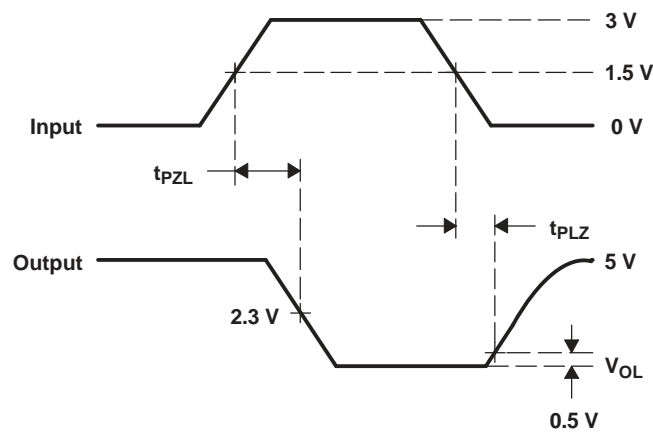


Figure 6. Enable Timing Test Circuit and Waveforms,  $t_{PZL}$  and  $t_{PLZ}$



PARAMETER MEASUREMENT INFORMATION (continued)

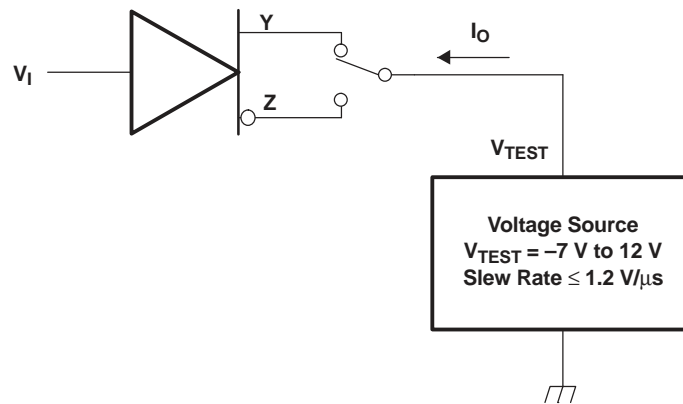


Figure 7. Test Circuit, Short-Circuit Output Current

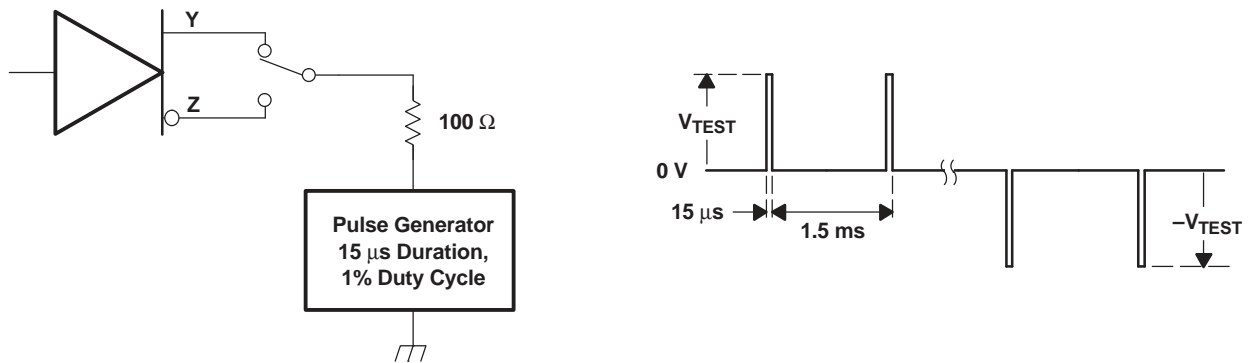
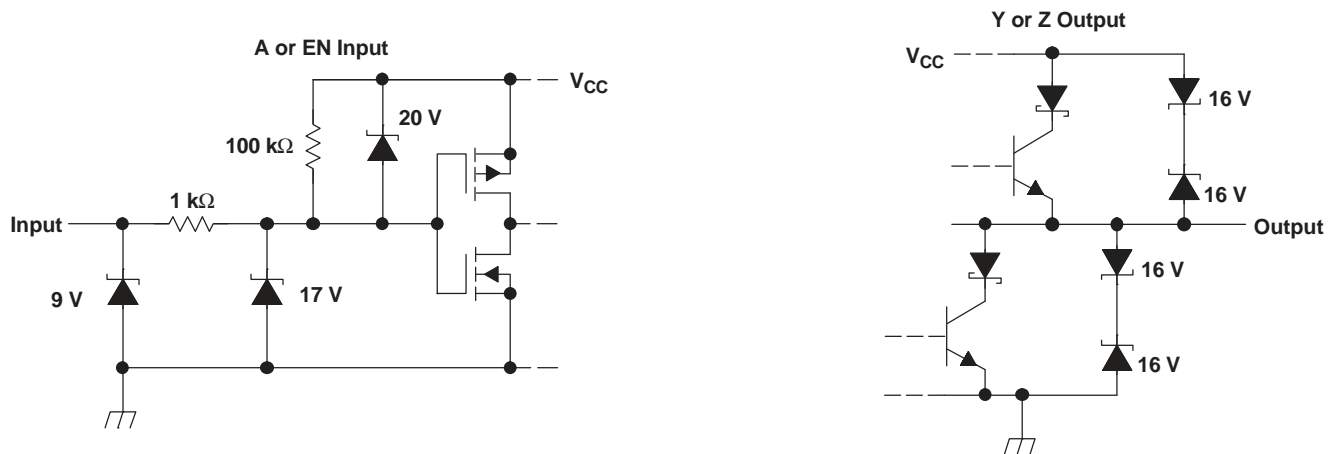


Figure 8. Test Circuit Waveform, Transient Overvoltage Test

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

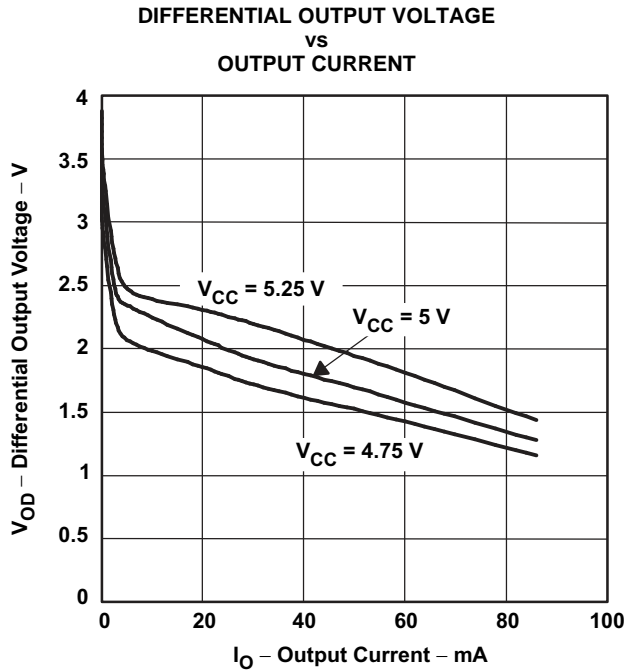


Figure 9.

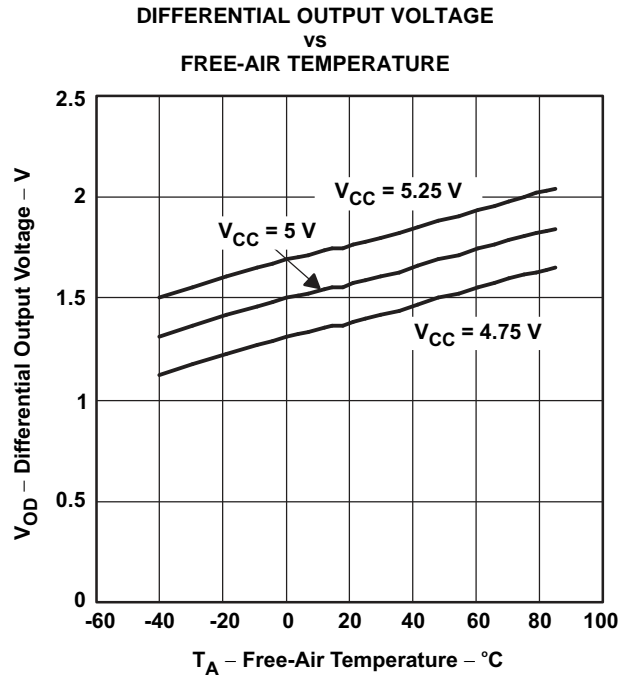


Figure 10.

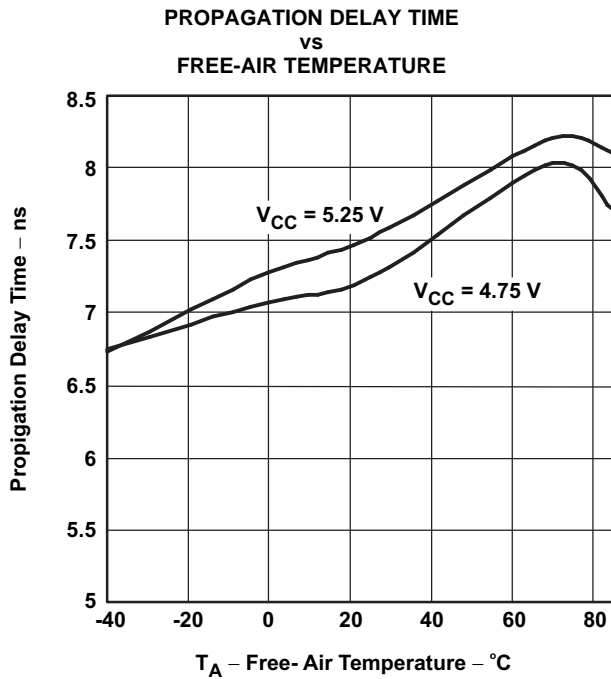


Figure 11.

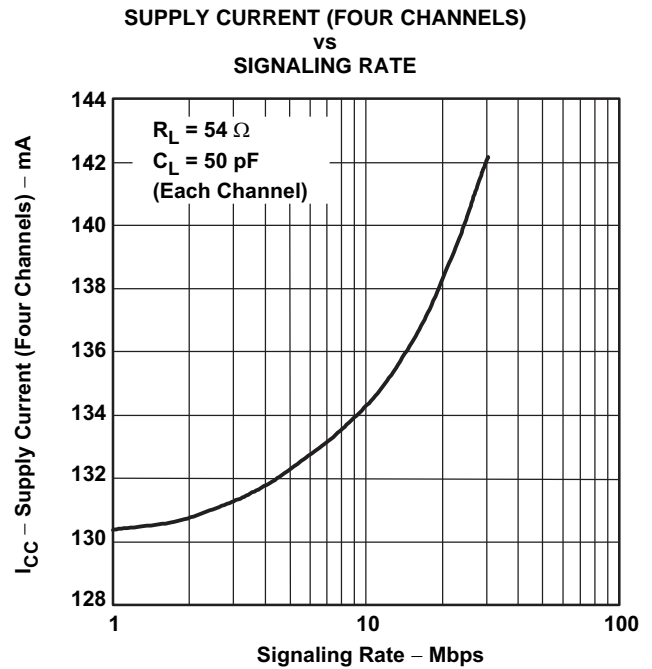


Figure 12.

TYPICAL CHARACTERISTICS (continued)

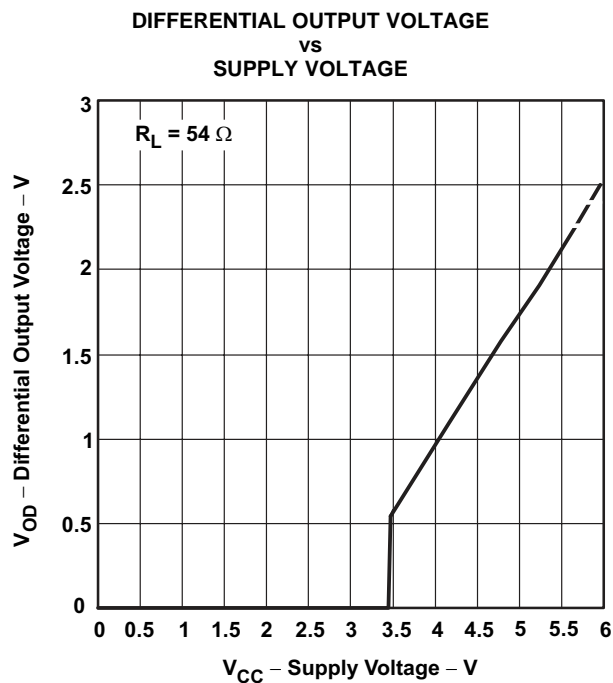


Figure 13.

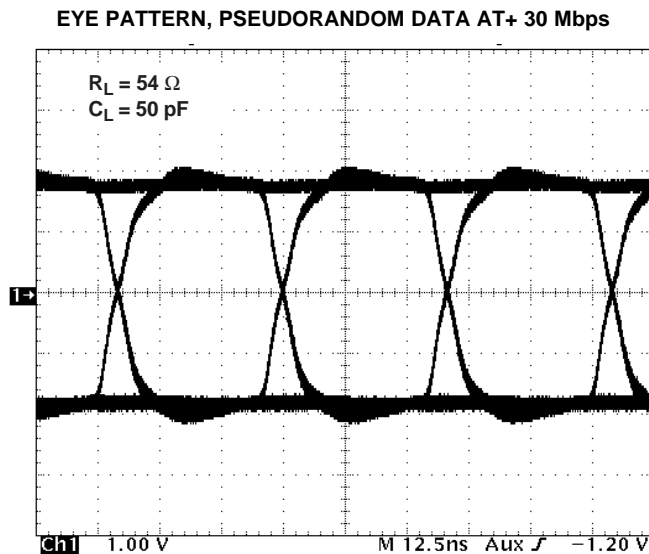
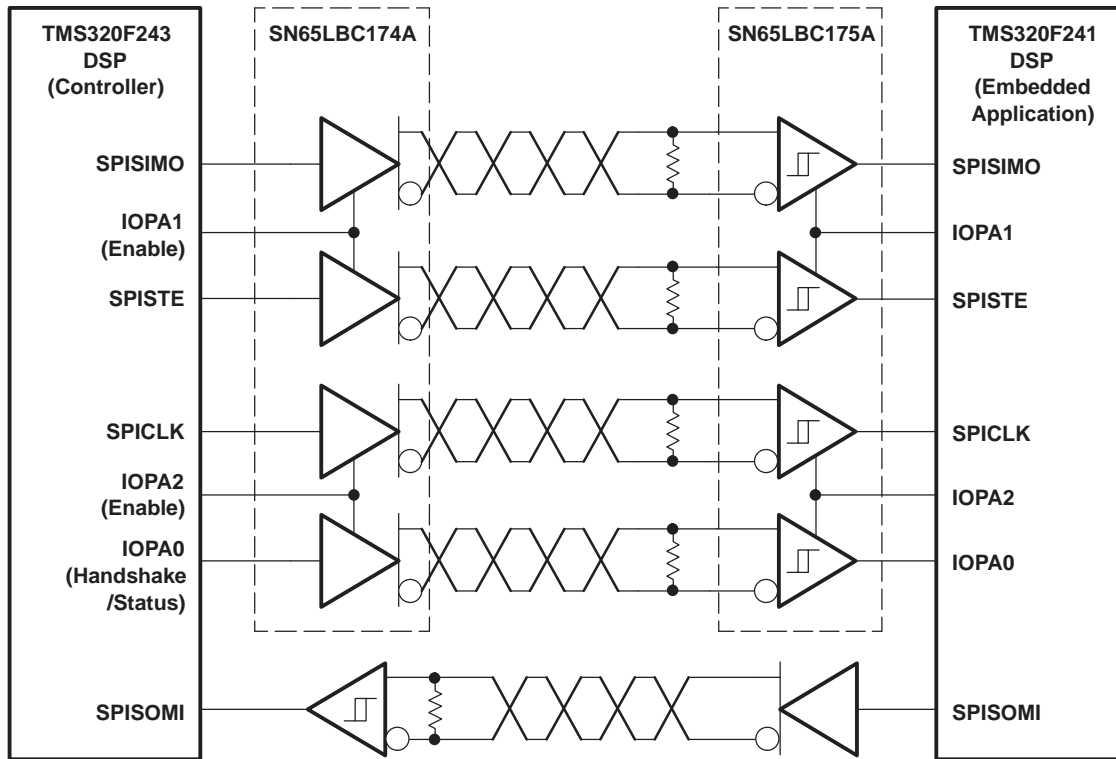


Figure 14.

**APPLICATION INFORMATION**



**Figure 15. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface**

**REVISION HISTORY**

**Changes from Original (October 2000) to Revision A Page**

- Changed multiple items through the data sheet. .... 1

**Changes from Revision A (February 2001) to Revision B Page**

- Changed DW Package appearance ..... 1
- Added [Figure 13](#) ..... 11

**Changes from Revision B (June 2001) to Revision C Page**

- Changed Features bullet From: Output ESD Protection Exceeds 13 kV To: Output ESD Protection: 11 kV ..... 1
- Changed Features bullet for Industry Standard From: Compatible With SN75174, MC3487, and DS96174 To: Compatible With SN75174, MC3487, DS96174, LTC487, and MAX3042 ..... 1

**Changes from Revision C (May 2003) to Revision D Page**

- Changed the AVAILABLE OPTIONS table ..... 2
- Changed Electrostatic discharge-Human body model-Y, Z, and GND From: 13kV To: 11kV ..... 3
- Changed the DISSIPATION RATING TABLE ..... 3

**Changes from Revision D (June 2008) to Revision E**
**Page**

- Changed Features bullet From: Output ESD Protection Exceeds 11 kV To: Output ESD Protection: 12 kV ..... 1
  - Changed Electrostatic discharge-Human body model-Y, Z, and GND From: 11kV To: 12kV ..... 3
  - From: A, G,  $\bar{G}$  To: A, EN ..... 4
- 

**Changes from Revision E (July 2008) to Revision F**
**Page**

- Changed FUNCTION TABLE header From: ENABLE G To: ENABLE EN ..... 2
  - Added  $C_{IN}$  - Input Capacitance to the Electrical Characteristics table ..... 4
  - Changed the location of the EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAM ..... 9
-

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC174A16DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	
SN65LBC174A16DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	Samples
SN65LBC174A16DWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	Samples
SN65LBC174ADW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	
SN65LBC174ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	Samples
SN65LBC174AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC174A	Samples
SN75LBC174A16DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC174A	
SN75LBC174A16DWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC174A	
SN75LBC174ADW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC174A	
SN75LBC174ADWR	LIFEBUY	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC174A	
SN75LBC174AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC174A	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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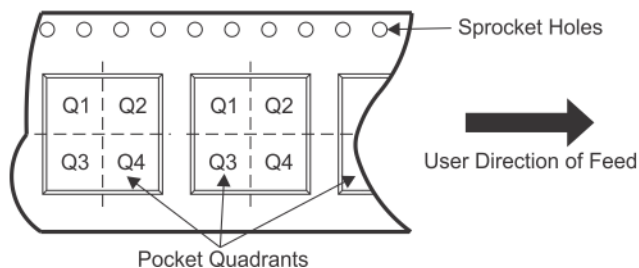
**OTHER QUALIFIED VERSIONS OF SN65LBC174A :**

- Enhanced Product : [SN65LBC174A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC174A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65LBC174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75LBC174A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN75LBC174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC174A16DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN65LBC174ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75LBC174A16DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN75LBC174ADWR	SOIC	DW	20	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC174A16DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN65LBC174ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN65LBC174ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN65LBC174AN	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC174A16DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN75LBC174ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75LBC174ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC174AN	N	PDIP	16	25	506	13.97	11230	4.32

## GENERIC PACKAGE VIEW

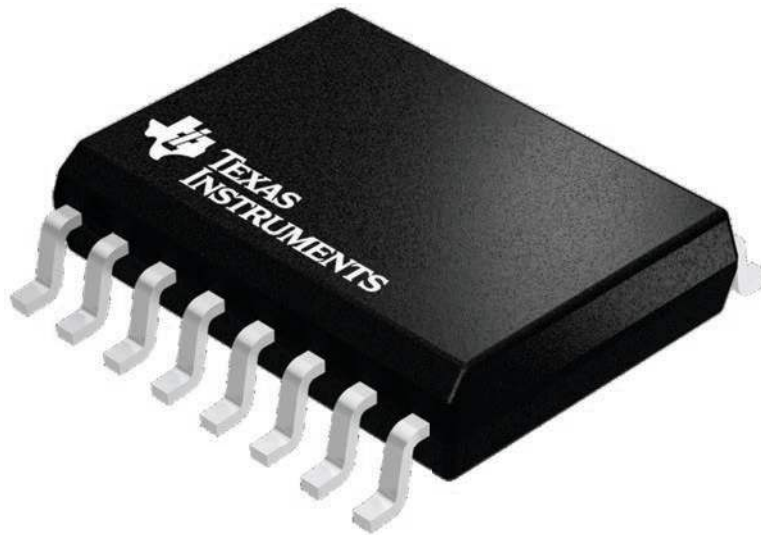
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

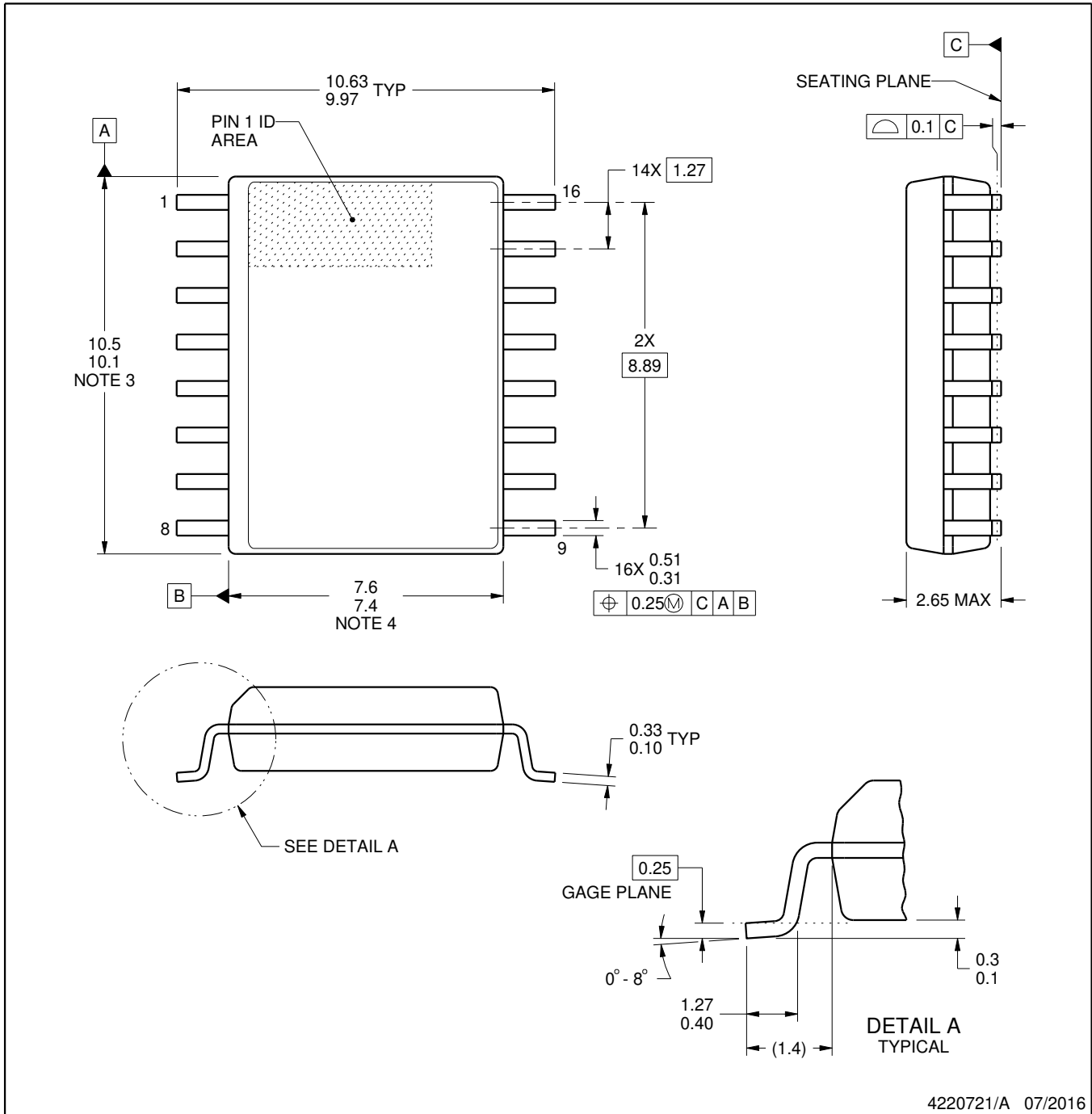


# DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

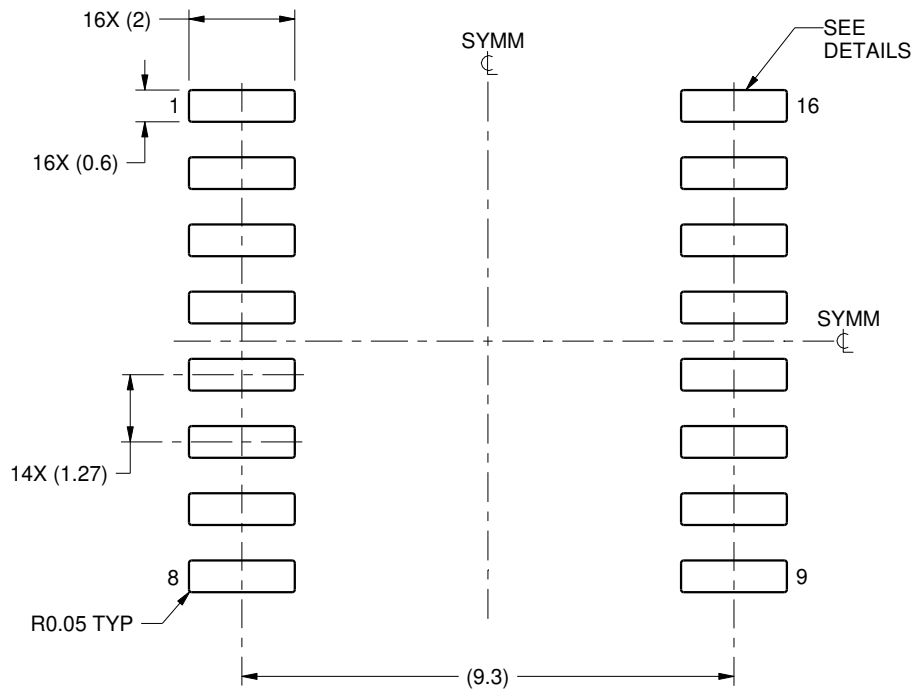
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

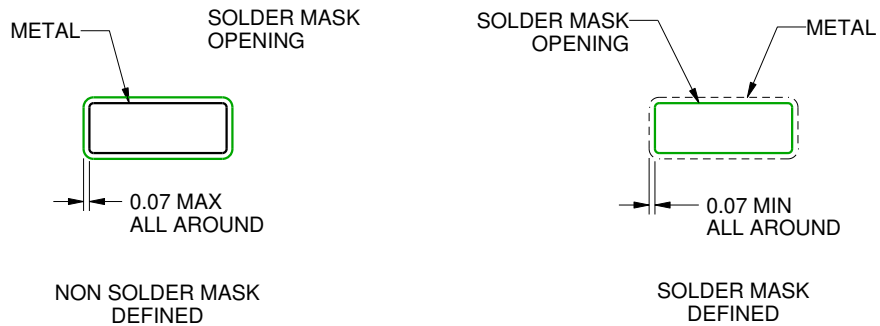
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

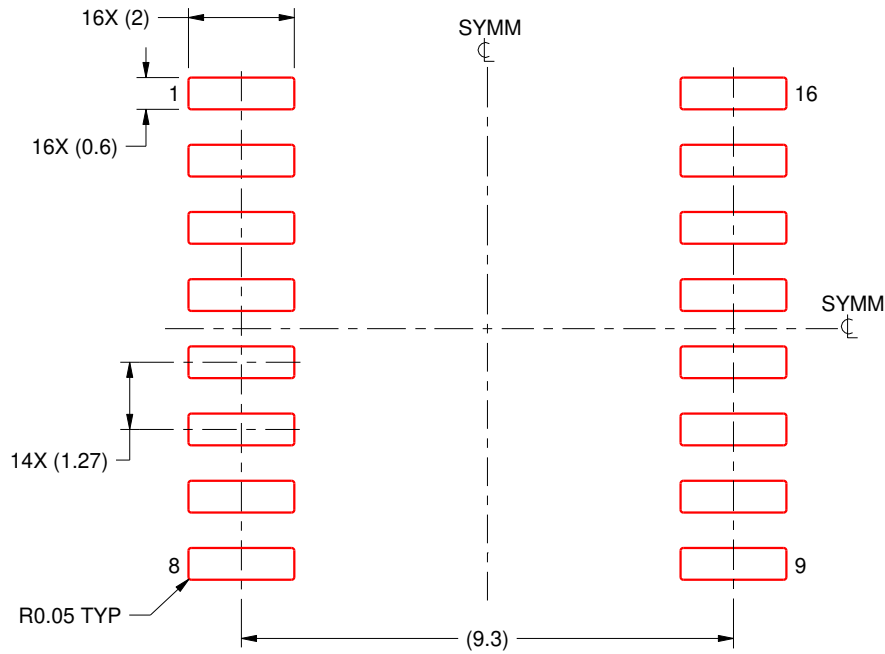
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

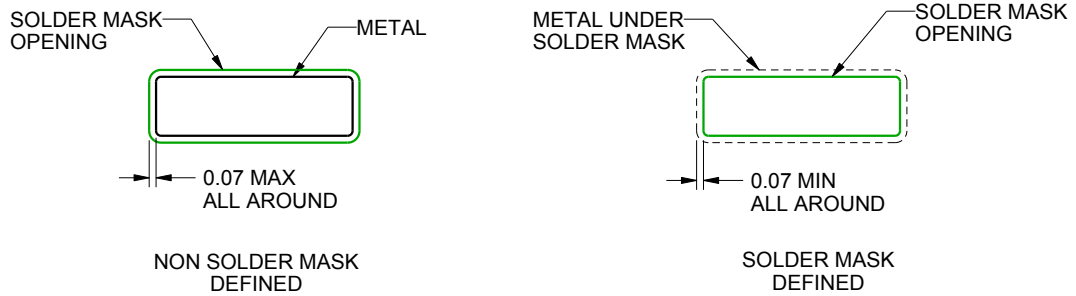
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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