User Guide for

# FEBFAN7688_I00250A
# Evaluation Board

# FAN7688, LLC Resonant, 250 W, 400 V to 12.5 V Converter, Evaluation Board

## Featured Fairchild Products:

## FAN7688

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# Table of Contents

The following user guide supports the FEBFAN7688_I00250A, FAN7688, 250 W, and 400 V to 12.5 V Evaluation Board (EVB). It should be used in conjunction with the FAN7688 datasheet, and FAN7688 Excel®-based Design Tool.

# 1. Introduction

This document describes the use and performance of the FAN7688, 250 W, and 400 V to 12.5 V EVB. The input voltage range is 300 $V_{DC}$<$V_{IN}$<450$V_{DC}$ and the output is a 12.5 V, regulated over an output current range of 0 A<$I_{OUT}$<20 A. The EVB allows ease of probing by making available numerous test points and options for installing current loops. Although the input voltage range is typical of the output voltage from a PFC boost power stage, the end application of this EVB is considered general purpose for the use of testing the many features of the FAN7688 LLC resonant controller. This document contains a general description of the FAN7688 LLC resonant controller, EVB specification, power-on and off procedure, schematic, Bill of Materials (BOM), and typical EVB performance characteristics.

## 1.1. General Description of FAN7688

The FAN7688 is a secondary-side, LLC resonant, Pulse Frequency Modulated (PFM) controller with dedicated Synchronous Rectification (SR) gate drive, offering best in class efficiency for isolated DC/DC converters. The primary resonant current is sensed and integrated to employ a type of peak current mode control known as charge control. The integrated resonant current is combined with a triangular waveform generated from an internal oscillator to determine the switching frequency. This provides a better control-to-output transfer function of the power stage making the feedback loop design easy and allows true input power limit capability. The FAN7688 also incorporates a closed loop soft-start function that uses an adaptive soft-start current to prevent saturation of the error amplifier which allows monotonic startup of the output voltage independent of load current. A dual edge tracking, adaptive SR drive technique minimizes body-diode conduction of the SR MOSFETs thereby maximizing overall efficiency.

## 1.2. FAN7688 Internal Block Diagram

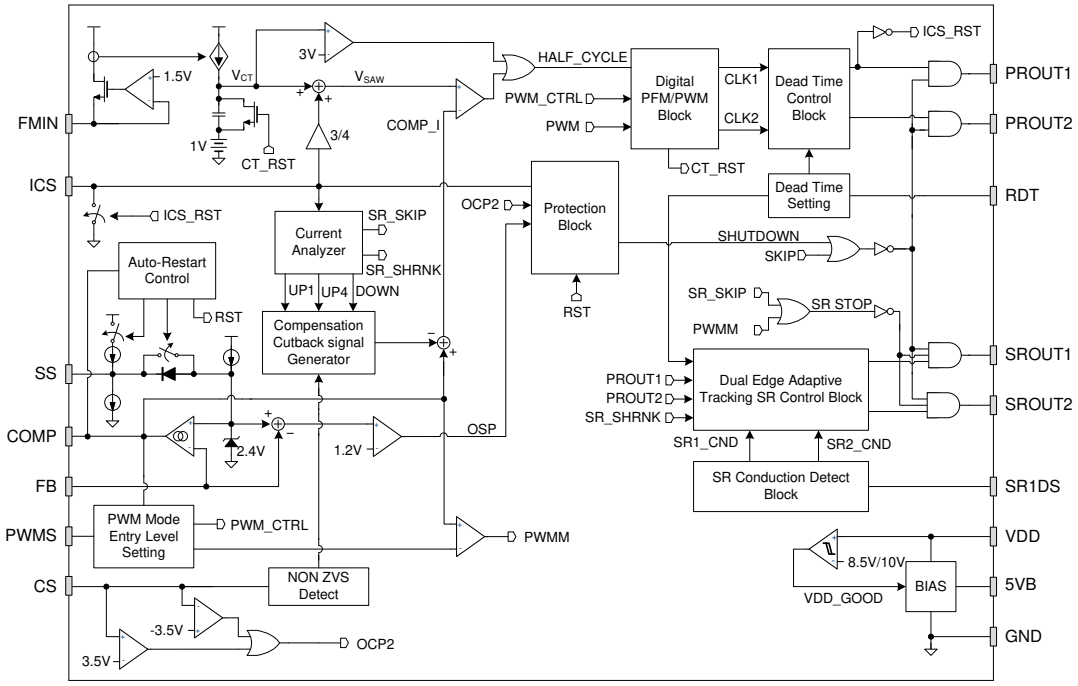



**Figure 1. FAN7688 Internal Block Diagram**

## 1.3. FAN7688 Controller Features

The FAN7688 is a secondary side controller designed to modulate the frequency to control a DC to DC isolated LLC converter. Secondary side control offers several unique advantages over primary side control. Direct sensing of the SR drain is necessary for accurate SR timing optimization and better SR reliability under all operating conditions. The output voltage is also directly sensed by the controller which allows accurate closed loop soft-start, direct interface to the load and output short circuit overload protection during startup. And since no optocoupler is required, there is no variation in loop gain due to the variation in optocoupler Current Transfer Ration (CTR).

The FAN7688 uses a hybrid control scheme where, depending upon line or load conditions (COMP voltage), operation can occur using either fixed frequency PWM mode or traditional PFM mode. PFM mode commands highest switching frequency during light load and startup. High frequency switching losses are dominant during light load. Light load efficiency is therefore improved when the power stage is controlled using fixed frequency, PWM mode. The transition between PWM and PFM is seamless and can be programmed as a function of load current via the PWMS pin. This allows custom efficiency tailoring around a particular light load efficiency point of interest.

Further light load efficiency improvements can be realized by disabling SR switching at a particular minimum load point. The FAN7688 SR_SKIP function is programmable through the ICS pin. When the peak value of the integrated current sense is less than the SR_SKIP enable threshold, SR switching is disabled. Whenever the SRs are disabled, load current will flow through the SR body diodes or parallel Schottky rectifiers can be used as an option for even higher light load efficiency.

A comprehensive set of auto-restart protection functions includes: pulse-by-pulse Over-Current Protection (OCP), Output Short Protection (OSP), non-Zero Voltage Switching (ZVS) Protection (NZP), Overload Protection (OLP) and Over-Temperature Protection (OTP). Capacitive region operation can be detrimental to an LLC converter. During light load PFM mode, the frequency decreases as the voltage gain is increasing to maintain output regulation. Inevitably, operation deep below resonance occurs where, at some minimum frequency, the maximum peak gain is obtained, pushing the converter into the capacitive region. Loss of ZVS, DC gain inversion and body diode reverse recovery are some of the problems associated with capacitive region operation. The FAN7688 FMIN pin allows the minimum frequency to be programmed. By setting a stop before the absolute maximum gain is obtained, capacitive region operation can easily be prevented.

## 2. Overview of the Evaluation Board

The FEBFAN7688_I00250A EVB uses a four-layer Printed Circuit Board (PCB) designed for 250 W (12.5 V / 20 A) rated power. The EVB dimensions are 163 mm x 89 mm x 25 mm (LxWxH). The maximum rated power is designed for 250 W but the maximum power limit is set to 375 W. The EVB is a DC to DC converter and operates from a 400 V input, typical of the voltage produced from an off-line PFC boost converter. The output voltage is set to regulate at 12.5 V. An input bulk capacitor, C1, is included but in the case of operating from a PFC output, C1 would be redundant since the PFC output would include a similar size bulk capacitor necessary for hold up. The EVB also requires an external 12 V bias supply voltage for operation. Connections for the DC input voltage, DC output voltage and DC bias supply voltage are made possible through J9, J6, J15 and J16. Remote sense connections (J7, J26) are also available for accurately monitoring output voltage. Control loop measurements can easily be made by injecting a perturbation signal across a 49.9 Ω (R6) resistor through +Loop (J8) and –Loop (J10). Primary resonant current can be measured by removing R4 and soldering a loop of wire (minimum AWG#22) into the plated through holes located on each R4 conductive pad. Similarly, secondary AC current can be measured by removing R5 and soldering a loop of wire (minimum AWG#16) onto the conductive R4 SMD pads. Primary side gate drive can be monitored for the high-side MOSFET (floating) between J5 and the source lead of Q1 and for the low-side MOSFET (GND referenced) between J13 and J17. On the secondary side, the SR MOSFET gate drives can be monitored between J11 and J14 for Q3 and between J12 and J14 for Q4. All 16 pins of the FAN7688 can easily be probed at J18-J36 and there are five secondary side ground pins (J14, J26-7, J35-6). In summary, the EVB allows ease of probing at the signals most important for understanding the FAN7688 operation and allows additional board space for ease of soldering external components or circuit modifications.

## 2.1. Photographs

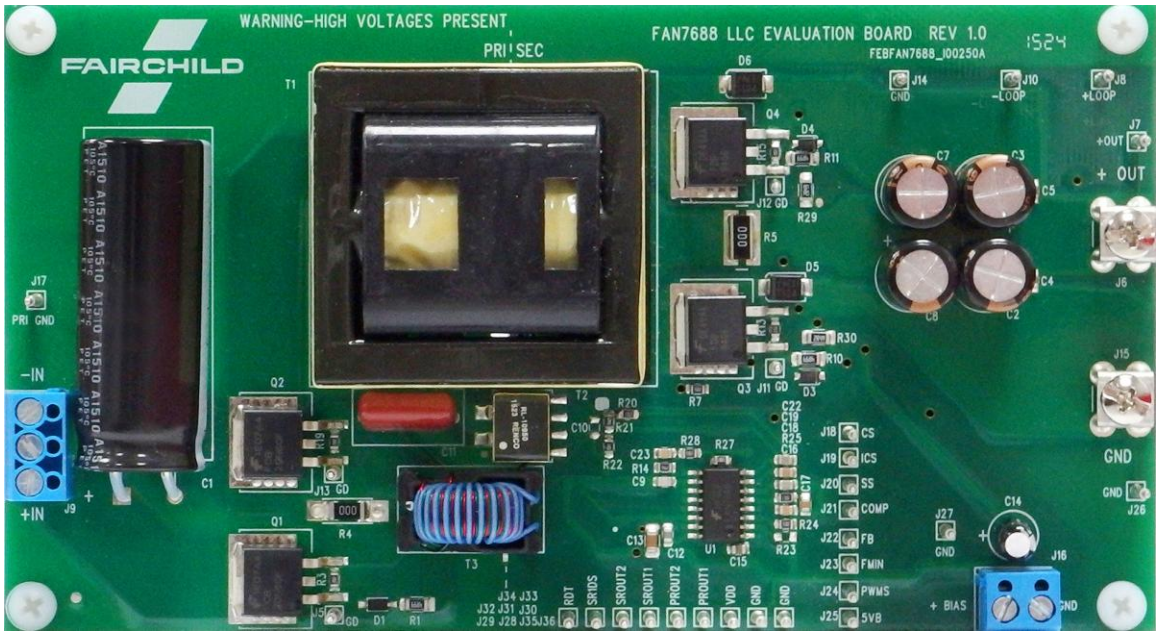



**Figure 2. Top View, 163 mm x 89 mm**

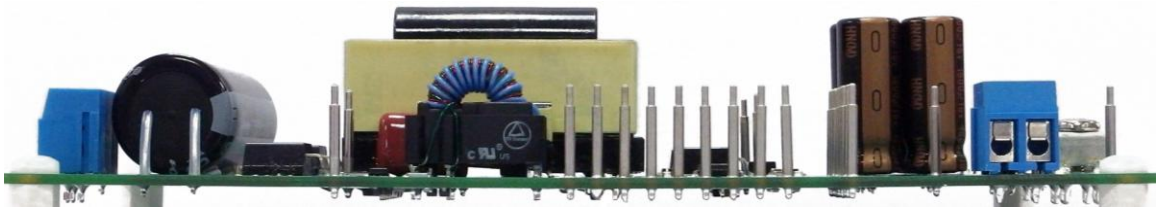


**Figure 3. Side View, Cross Section, 30 mm**

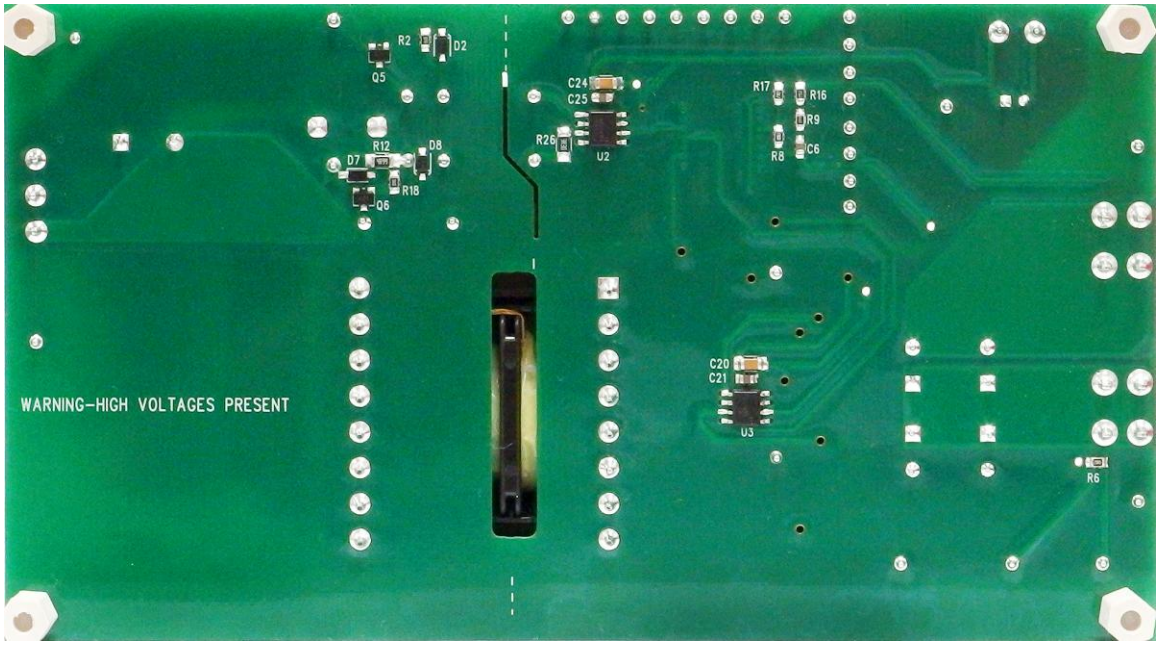



**Figure 4. Bottom View, 163 mm x 89 mm**

# 3. Specifications

The evaluation board has been designed and optimized for the conditions in Table 1.

**Table 1. Electrical and Mechanical Specifications**

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $V_{IN}$ | 300 | 400 | 450 | $V_{DC}$ |
| $V_{OUT}$ | 12.4 | 12.5 | 12.6 | $V_{DC}$ |
| $I_{OUT}$ | 0 | | 20 | A |
| $P_{OUT\_MAX}$ | | | 250 | W |
| $F_{RES}$ $V_{IN}$=375 V | | 105 | | kHz |
| $f_{PWM}$ | | 250 | | kHz |
| $f_{SW(PFM)}$ 300 V<$V_{IN}$<450 V | 80 | | 140 | kHz |
| $SR_{SHRINK}$ 10% $P_{OUT\_MAX}$ | | 25 | | W |
| $SR_{ENABLE}$ 25% $P_{OUT\_MAX}$ | | 60 | | W |
| $I_{OUT\_OCP}$ Below Res $V_{IN}$=300 V | | | 22 | A |
| $I_{OUT\_OCP}$ Above Res $V_{IN}$=425 V | | | 30 | A |
| $t_{SS}$ 400 V, 20 A | | 55 | 60 | ms |
| $t_{HU}$ 400 V, 20 A | 16 | 75 | | ms |
| η_400 V $P_{OUT}$=50 W 20% $P_{OUT\_MAX}$ | | 95 | | % |
| η_400 V $P_{OUT}$=125 W 50% $P_{OUT\_MAX}$ | | 97 | | % |
| η_400V $P_{OUT}$=250 W 100% $P_{OUT\_MAX}$ | | 96 | | % |
| **Mechanical and Thermal** | | | | |
| Height | | | 25 mm | |
| $\theta_{JC}$ Use of Fan for $I_{OUT}$>20 A | | | 80°C | |

# 4. Test Procedure

Before applying power to the FEBFAN7688_I00250A EVB; the DC bias supply voltage, DC source input voltage and DC electronic load should be connected to the board as shown in Figure 5. Optionally a Digital Volt Meter (DVM1) (set to measure DC voltage) can be connected to J7 and J26 to measure the output voltage and a second DVM (DVM2, set to measure ≤2.5 $V_{DC}$) can be connected across an external current sensing shunt ($R_{SHUNT}$=100 mΩ) to measure DC output current. Note that most ammeter settings are limited to 10 $A_{DC}$. Measuring the DC output current using a direct connection into a DVM ammeter can damage the DVM and/or blow the fuse.

## 4.1. Safety Precautions

The FEBFAN7688_I00250A EVB operates from a high voltage DC supply and the bulk input capacitor stores significant charge. Please be extra careful when probing and handling the module and observe the following safety precautions:

- Start with a clean working surface, clear of any conductive material.
- Never probe or move a probe on the EVB while the DC supply voltage is present.
- Ensure the input and output capacitors are fully discharged before disconnecting the test leads.


### Power-On Procedure

1. Connect an electronic load (12.5 V, 0-30 A) to J6 and J15. Set the electronic load to Constant Current (CC) with an initial setting of 0-1A.
2. Connect DVM1to Kelvin connections, J7 and J26.
3. As shown in Figure 5, connect a resistive shunt in series with the electronic load + or electronic load -. If efficiency is not being measured, the shunt can be omitted.
4. Connect DVM2 across the resistive shunt.
5. Connect a 400 V, DC power supply (300~450 V) to J9, pins 1 and 3.
6. Connect an optional power meter between the 400 V, DC power supply and J9. If a power meter is not available, 2 DVMs can also be used to measure input current and input voltage.
7. Connect a 12 V bias DC power supply to J16, pins 1 and 2.
8. Set the input voltage source to 400 V and turn on the input voltage source.
9. Set the electronic load to draw 1 A of CC and turn on the electronic load.
10. Set the 12 V bias DC power supply to 12 V and turn on the bias power supply.
11. Verify the output voltage reading on DVM1 is now 12.5 V.
12. Vary the load current (0~20 A) as desired and verify normal output voltage regulation.
13. **Prolonged operation near or above 20 A requires use of fan.**
14. Vary the input voltage as desired (300 V~450 V) and verify normal output voltage regulation.

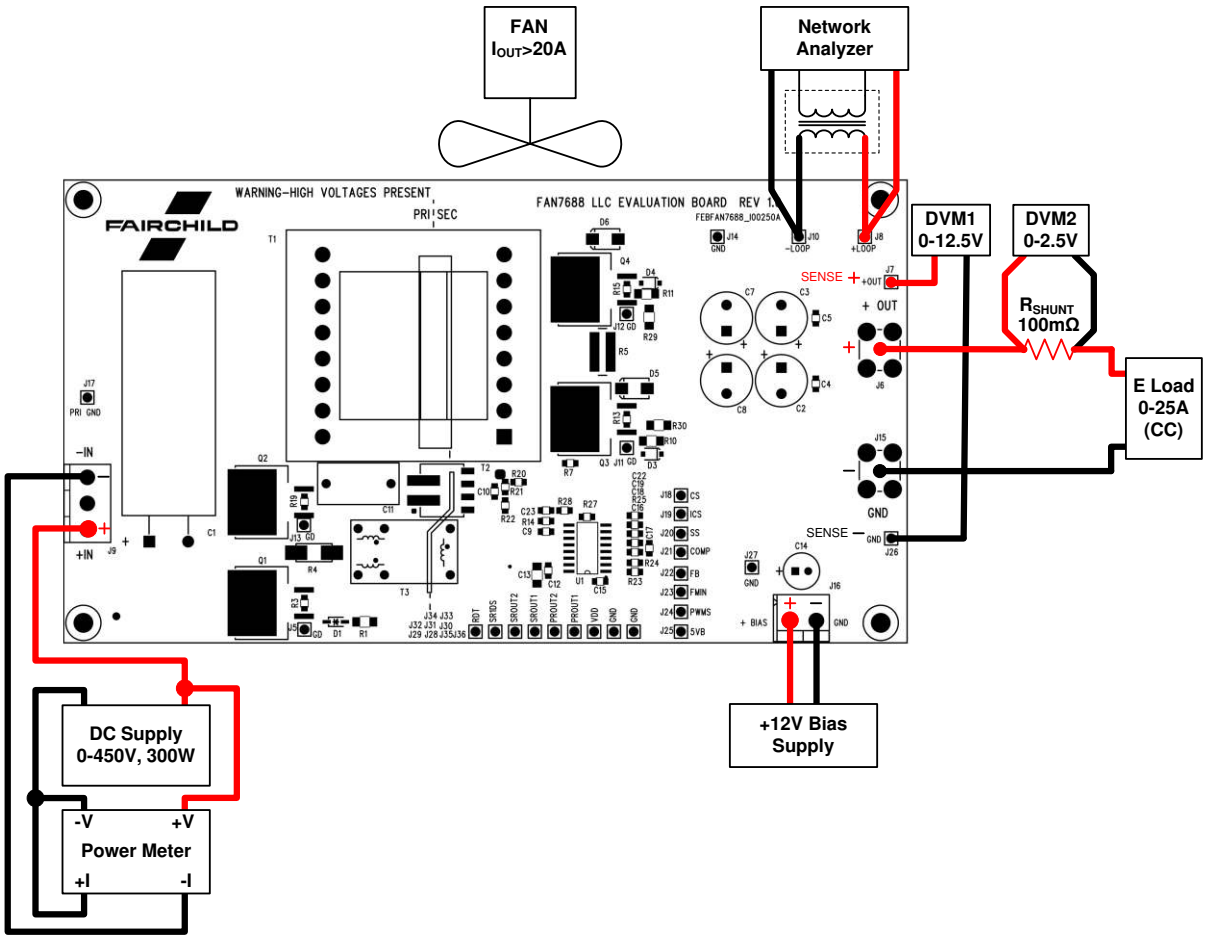



**Figure 5. Recommended EVB Test Configuration**

All efficiency data shown was taken using the test set up shown in Figure 5.

## Power-Off Procedure

1. Make sure the electronic load is ON and set to draw at least 5 A of CC.
2. Disconnect (shutdown) the 400 V DC supply voltage.
3. Disconnect (shutdown) the 12 V bias DC power supply.
4. Disconnect (shutdown) DC electronic load last to ensure the output capacitors are fully discharged before handling the evaluation module.
5. Verify that DVM1 reads 0 V.
6. Verify that the power meter (or DVM measuring input voltage) reads 0 V. If not, wait until the input capacitor (C1) is fully discharged or manually discharge C1 using an appropriate sized low value (~200 Ω) power resistor (>10 W).

# 5. Schematic

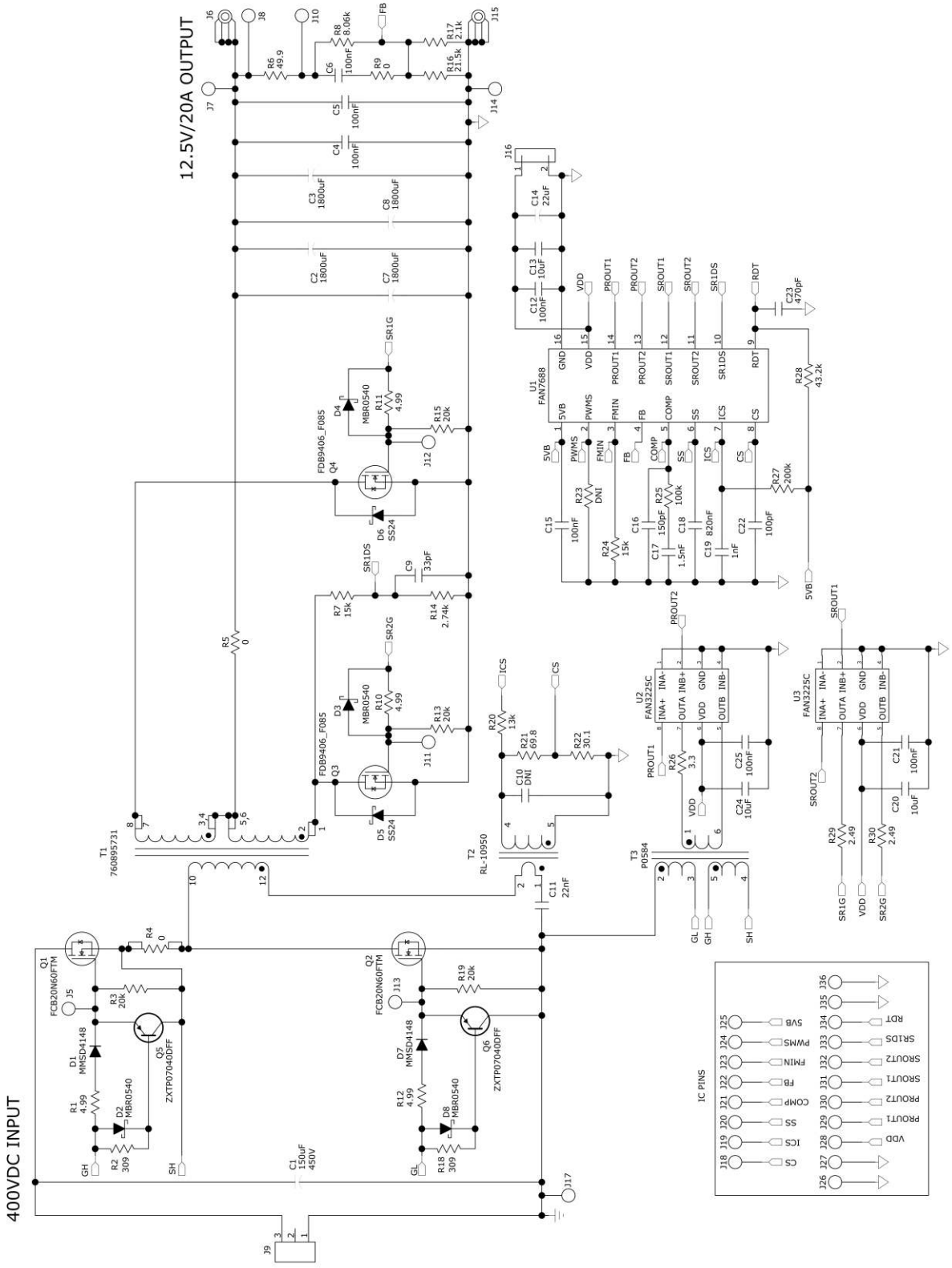



**Figure 6. Evaluation Board Schematic**

# 6. List of Test Points

**Table 2. List of Test Points**

| Test Point | Name | Description |
|---|---|---|
| J5 | GD | Primary upper MOSFET, Q1, floating gate |
| J7 | +OUT | +12.5 V output Kelvin sense |
| J8 | +Loop | Network analyzer perturbation loop injection + |
| J10 | -Loop | Network analyzer perturbation loop injection - |
| J11 | GD | SR, Q3, gate, secondary ground referenced |
| J12 | GD | SR, Q4, gate, secondary ground referenced |
| J13 | GD | Primary lower MOSFET, Q1, gate, primary ground referenced |
| J14 | GND | Secondary ground, use for J11-2 gate drive |
| J17 | PRI GND | Primary ground, use for J13 gate drive |
| J18 | CS | FAN7688 CS pin, current sensing for OCP |
| J19 | ICS | FAN7688 ICS pin, integrated current sense for charge control |
| J20 | SS | FAN7688 SS pin, soft-start |
| J21 | COMP | FAN7688 COMP pin, error amplifier output |
| J22 | FB | FAN7688 FB pin, divided down sensed output voltage |
| J23 | FMIN | FAN7688 FMIN pin, minimum frequency setting |
| J24 | PWMS | FAN7688 PWMS pin, PWM entry point |
| J25 | 5VB | FAN7688 5VB pin, 5 V reference |
| J26 | GND | Secondary ground, +12.5 V output return Kelvin sense |
| J27 | GND | Secondary ground |
| J28 | VDD | FAN7688 VDD pin, VDD bias |
| J29 | PROUT1 | FAN7688 PROUT1 pin, PROUT1 gate drive |
| J30 | PROUT2 | FAN7688 PROUT2 pin, PROUT2 gate drive |
| J31 | SROUT1 | FAN7688 SROUT1 pin, SROUT1 gate drive |
| J32 | SROUT2 | FAN7688 SROUT2 pin, SROUT2 gate drive |
| J33 | SR1DS | FAN7688 SR1DS pin, SR, Q3, drain-to-source sense |
| J34 | RDT | FAN7688 RDT pin, PROUT and SROUT dead time setting |
| J35 | GND | Secondary ground |
| J36 | GND | Secondary ground |
| R4 | R4 | Option - remove R4, install primary drain current loop |
| R5 | R5 | Option - remove R5, install secondary AC current loop |

# 7. Transformer Specifications

## 7.1. LLC Power Transformer

760895731 from Wurth Elektronik (www.we-online.com) is a LLC transformer orderable from Digikey. A split bobbin is used to incorporate the resonant inductance (leakage inductance) and magnetizing inductance into a single magnetic component.

- Core: ETD44 ($A_e$=172mm$^2$)
- Bobbin: 16 pin TH
- Magnetizing Inductance : 475 µH, ±10%
- Leakage Inductance: 100 µH, ±10%

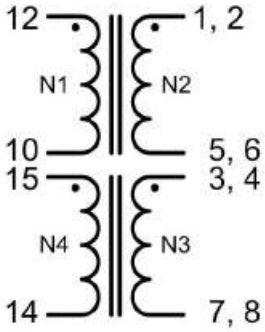



**Figure 7. LLC Power Transformer (T1) in the Evaluation Board**

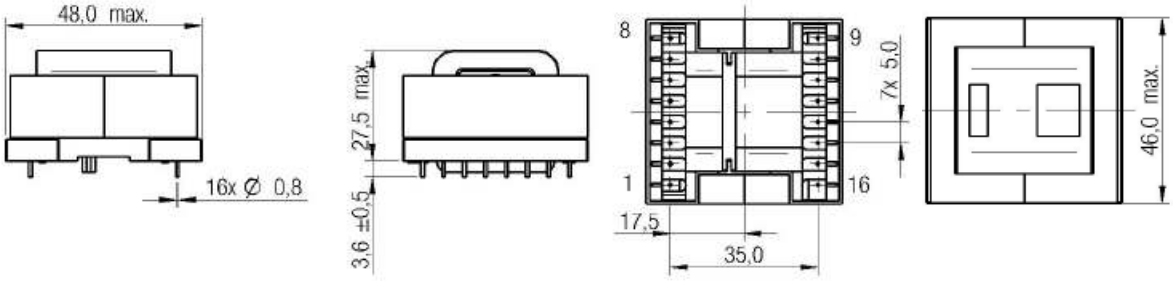



**Figure 8. Wurth 760895731 Mechanical Drawing (dimensions in mm)**

**Table 3. Wurth 760895731 Transformer Electrical Specifications**

| Properties | Test conditions | | Value | Unit | Tol. |
|---|---|---|---|---|---|
| **Inductance** | 100 kHz/ 100 mV | L | 475 | µH | ±10% |
| **Turns ratio** | | n | 35 : 2 : 2 : 3 | | ±3% |
| **Saturation current** | IΔL/LI < 20% | $I_{sat}$ | 5.0 | A | typ. |
| **DC Resistance 1** | @ 20°C | $R_{DC1}$ | 128 | mΩ | max. |
| **DC Resistance 2** | @ 20°C | $R_{DC2}$ | 4.0 | mΩ | max. |
| **DC Resistance 3** | @ 20°C | $R_{DC3}$ | 4.0 | mΩ | max. |
| **DC Resistance 4** | @ 20°C | $R_{DC4}$ | 192 | mΩ | max. |
| **Leakage inductance** | 100 kHz/ 100 mV | $L_S$ | 100 | µH | ±10% |
| **Insulation test voltage** | W1,4 => W2,3 | $U_T$ | 4000 | V (AC) | |

## 7.2. Current Sense Transformer

RL-10950 from Renco Electronics (www.rencousa.com) is a custom designed current sense transformer (CT). Most "off-the-shelf" CTs have primary to secondary isolation of <1000 V because they are not intended to operate across the isolation barrier. The RL-10950 is a 1:50 CT, specifically designed with 2500 V primary to secondary isolation which makes it more suitable for applcations such as the FAN7688 where the controller is on the secondary side and current sensing is coming from the primary side.

- Core: EP7 ($A_e$=9mm$^2$)
- Bobbin: 16 pin TH
- Magnetizing Inductance : 2.75mH, +40%/-20%

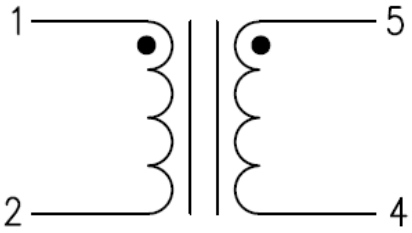



**Figure 9. Current Sense Transformer (T2) in the Evaluation Board**

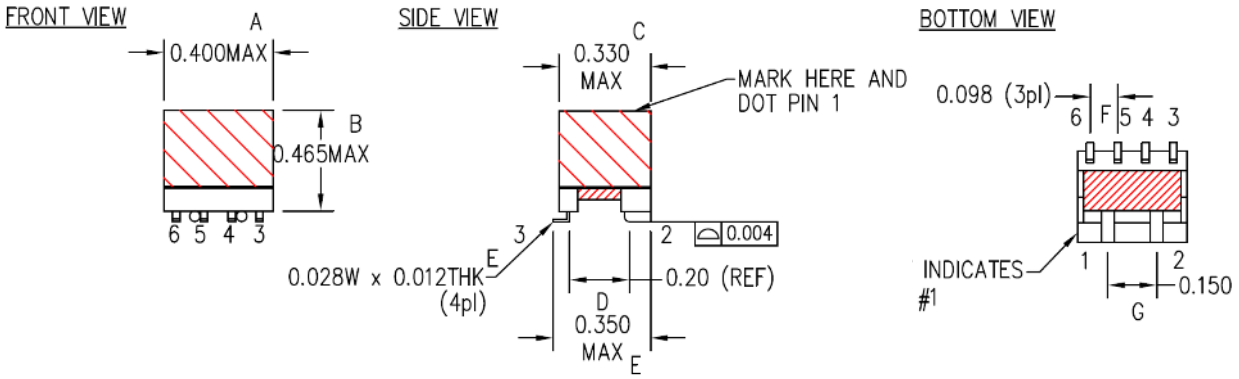



**Figure 10. Renco RL-10950 Mechanical Drawing (dimensions in inches)**

**Table 4. RL-10950 Transformer Electrical Specifications**

| Parameter | Test Conditions | Ref, | Value | Unit | Tolerance |
|---|---|---|---|---|---|
| Inductance | 100 kHz, 0,1 $V_{AC}$ | L | 2.75 | mH | +40% / -20% |
| Turns Ratio | | | 1:50 | | |
| DC Resistance 1 | Pins 1-2, @25°C | $R_{DC(1-2)}$ | 7.5 | mΩ | ±25% |
| DC Resistance 2 | Pins 5-4, @25°C | $R_{DC(5-4)}$ | 1.15 | Ω | Max. |
| Isolation | 2500 $V_{AC}$ @ 60 Hz for 2s, Pins 1-5 | | 2500 | $V_{AC}$ | Min. |

# 8. Four-Layer PCB and Assembly Images

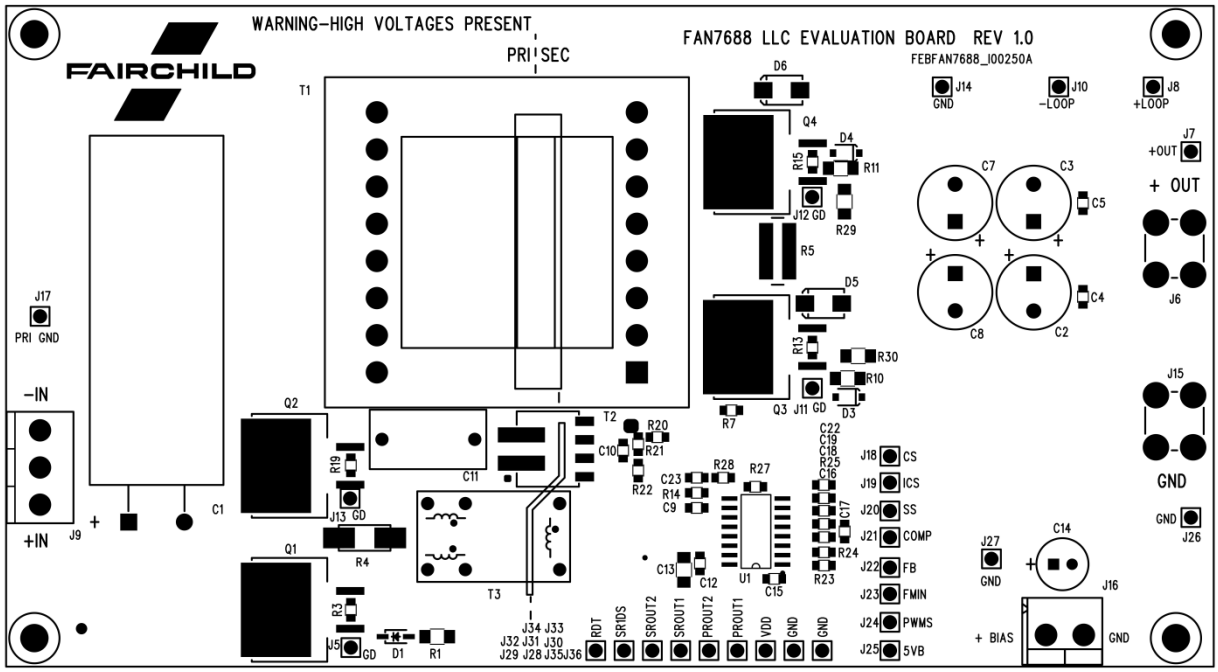



**Figure 11. Layer 1 – Top Assembly Layer**

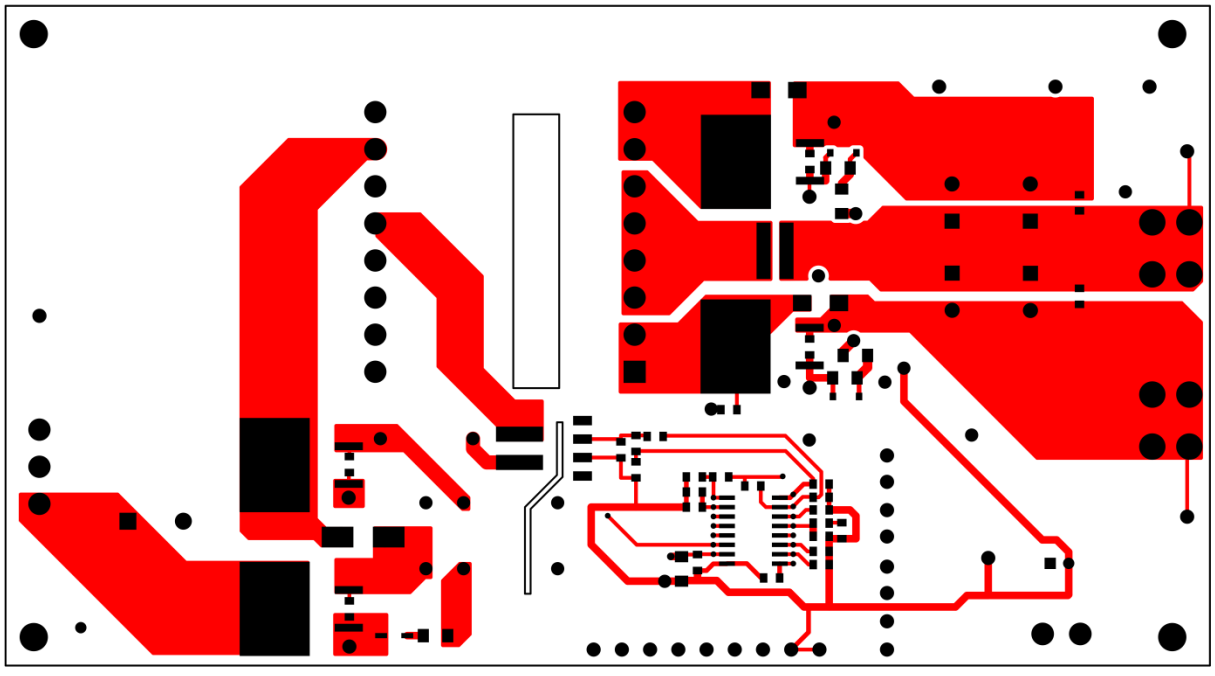


**Figure 12. Layer 1 – Top Copper Layer**

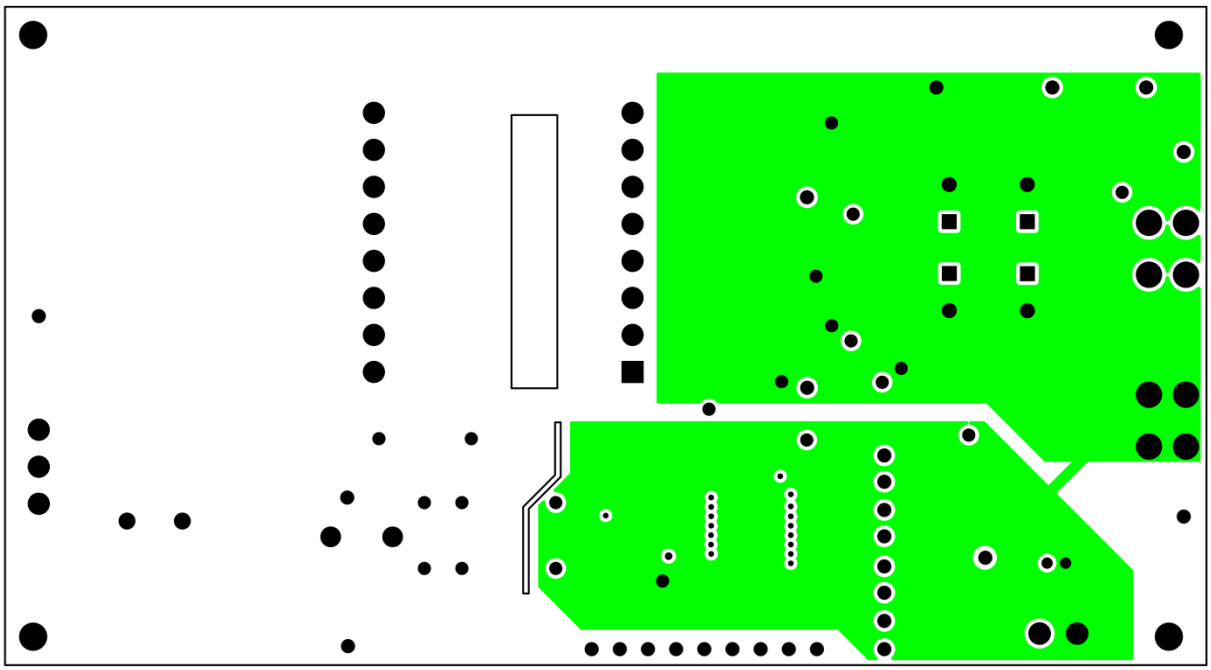


**Figure 13. Layer 2 – Internal Copper Layer**

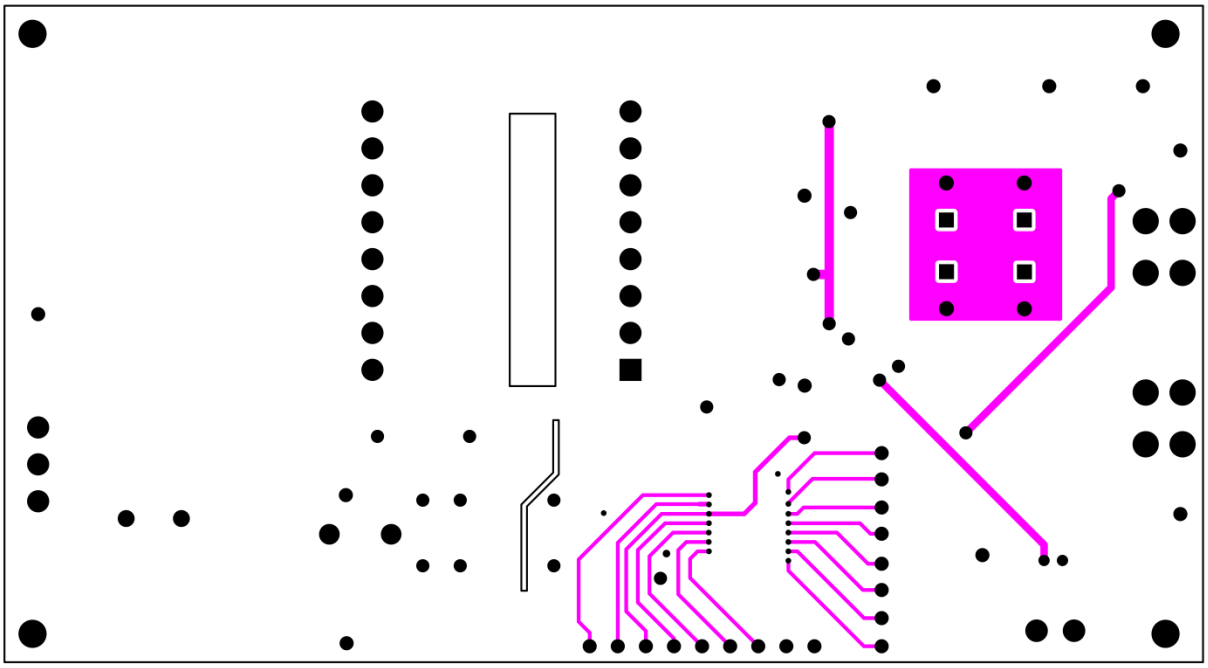


**Figure 14. Layer 3 – Internal Copper Layer**

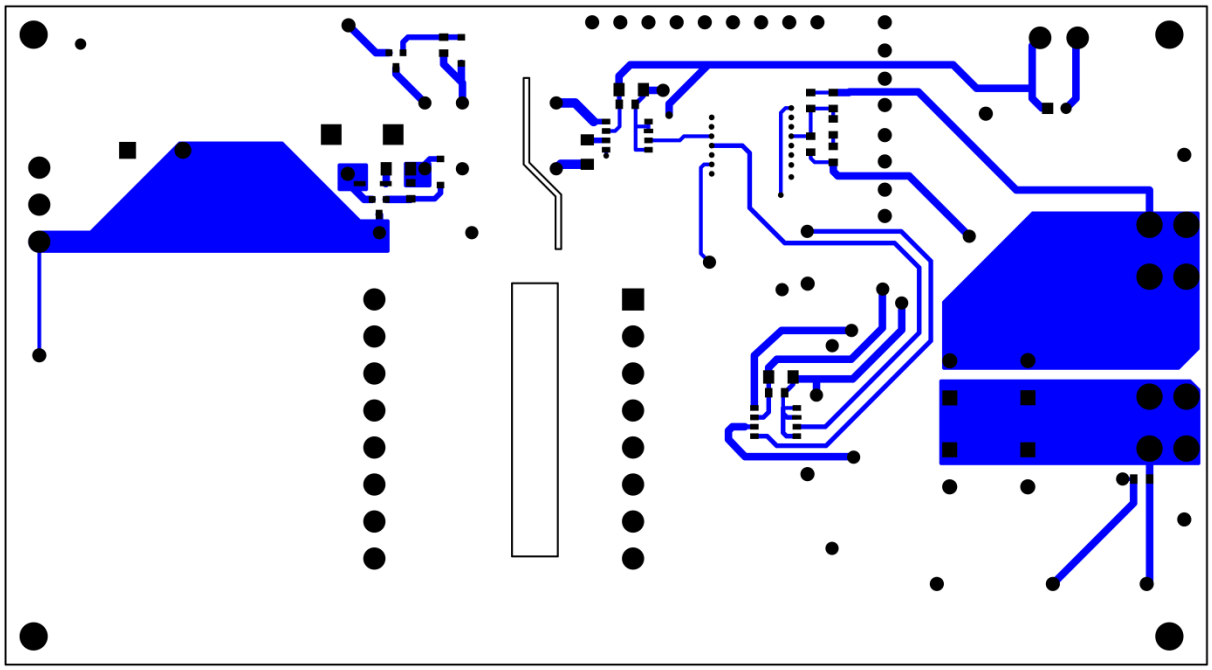


**Figure 15. Layer 4 – Bottom Copper Layer**

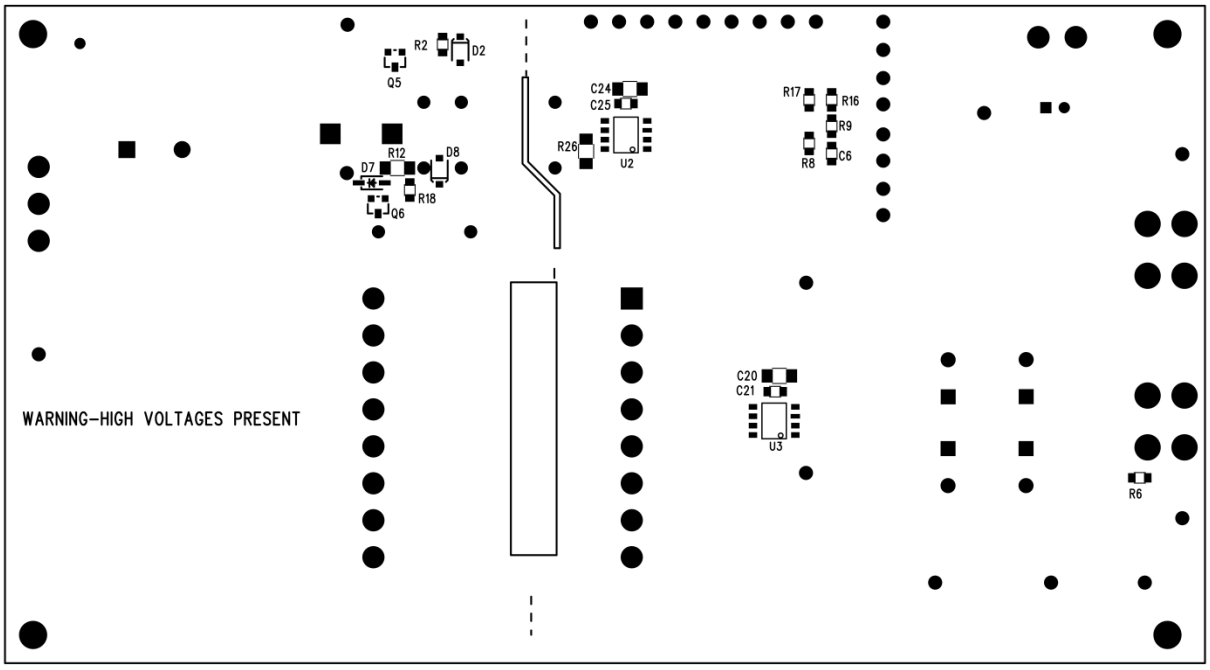



**Figure 16. Layer 4 – Bottom Assembly Layer**

# 9. Bill of Materials (BOM)

**Table 5. Bill of Materials**

| Item | Qty. | Reference | Value | Part Number | Description | Manufacturer | Package |
|---|---|---|---|---|---|---|---|
| 1 | 1 | C1 | 150 µF | 450BXW150MEFC18X45 | Cap, Alum, 450 V, 20% | Rubycon | Thru-Hole |
| 2 | 4 | C2-3, C7-8 | 1800 µF | UHN1C182MPD | Cap, Alum, 16 V, 20% | Nichicon | Thru-Hole |
| 3 | 7 | C4-6, C12, C15, C21, C25 | 100 nF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 4 | 1 | C9 | 33 pF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 5 | 0 | C10 | **DNI** | | CAP, SMD, CERAMIC | STD | 805 |
| 6 | 1 | C11 | 22 nF | ECW-H8223HA | Cap, 800VDC, Metal Poly Film, 3% | Panasonic | Radial |
| 7 | 3 | C13, C20, C24 | 10 µF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 1206 |
| 8 | 1 | C14 | 22 µF | EEA-GA1E220B | Cap, Alum, 25 V, 20% | Panasonic | Axial |
| 9 | 1 | C16 | 150 pF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 10 | 1 | C17 | 1.5 nF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 11 | 1 | C18 | 820 nF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 12 | 1 | C19 | 1 nF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 13 | 1 | C22 | 100 pF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 14 | 1 | C23 | 470 pF | | CAP, SMD, CERAMIC, 25 V, X7R | STD | 805 |
| 15 | 2 | D1, D7 | | MMSD4148 | Diode, 200 mA, 100 V, Signal Diode | Fairchild | SOD-123 |
| 16 | 4 | D2-4, D8 | | MBR0540 | Diode, Schottky, 40 V, 500 mA | Fairchild | SOD-123 |
| 17 | 2 | D5-6 | | SS24 | Diode, Schottky, 40 V, 2 A | Fairchild | SMB |
| 18 | 28 | J5, J7-8, J10-14, J17-36 | | 3103-2-00-21-00-00-08-0 | Test pin, Gold, 40 mil | Mill-Max | Thru-Hole |
| 19 | 2 | J6, J15 | | 7701 | Terminal, 15 A, Vertical, PC mount | Keystone | Thru-Hole |
| 20 | 1 | J9 | | ED100/3DS | Header, Vert. 3 pin, 5 mm Spacing | OST | Thru-Hole |
| 21 | 1 | J16 | | OSTTA024163 | Header, 2 pin, 100 mil Spacing, 15 A | OST | Thru-Hole |
| 22 | 2 | Q1-2 | | FCB20N60FTM | MOSFE, N-CH, 600 V, 20 A, 190 mΩ | Fairchild | D2PAK |
| 23 | 2 | Q3-4 | | FDB9406_F085 | MOSFE, N-CH, 40 V, 110 A, 1.8 mΩ | Fairchild | D2PAK |
| 24 | 2 | Q5-6 | | ZXTP07040DFF | Transistor, PNP, -40 V, -3 A | Diodes Inc. | SOT-23 |

| Item | Qty. | Reference | Value | Part Number | Description | Manufacturer | Package |
|---|---|---|---|---|---|---|---|
| 25 | 4 | R1, R10-12 | 4.99 Ω | | RES, SMD, 1/4W | STD | 1206 |
| 26 | 2 | R2 ,R18 | 309 Ω | | RES, SMD, 1/8W | STD | 805 |
| 27 | 4 | R3, R13, R15, R19 | 20 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 28 | 1 | R4 | 0 Ω | | RES, SMD, 1/2W | STD | 2010 |
| 29 | 1 | R5 | 0 Ω | 12250000Z0EG | RES, SMD, 1W | Vishay | 2512W |
| 30 | 1 | R6 | 20 Ω | | RES, SMD, 1/8W | STD | 805 |
| 31 | 2 | R7, R24 | 15 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 32 | 1 | R8 | 8.06 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 33 | 1 | R9 | 0 Ω | | RES, SMD, 1/8W | STD | 805 |
| 34 | 1 | R14 | 2.74 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 35 | 1 | R16 | 21.5 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 36 | 1 | R17 | 2.1 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 37 | 1 | R20 | 13 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 38 | 1 | R21 | 69.8 Ω | | RES, SMD, 1/8W | STD | 805 |
| 39 | 1 | R22 | 30.1 Ω | | RES, SMD, 1/8W | STD | 805 |
| 40 | 0 | R23 | **DNI** | | RES, SMD, 1/8W | STD | 805 |
| 41 | 1 | R25 | 100 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 42 | 1 | R26 | 3.3 Ω | | RES, SMD, 1/4W | STD | 1206 |
| 43 | 1 | R27 | 200 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 44 | 1 | R28 | 43.2 kΩ | | RES, SMD, 1/8W | STD | 805 |
| 45 | 2 | R29-30 | 2.49 Ω | | RES, SMD, 1/4W | STD | 1206 |
| 46 | 1 | T1 | | 760895731 | XFMR, LLC, 475 µH, 100 µH | Wurth Elektronik | Thru-Hole |
| 47 | 1 | T2 | | RL-10950 | XFMR, CT, 1:50, 35 A | Renco | SMD |
| 48 | 1 | T3 | | P0584 | XFMR, Gate Drive, 1:1:1, 450 µH | Pulse | Thru-Hole |
| 49 | 1 | U1 | | FAN7688 | LLC Resonant PFM Controller | Fairchild | SOIC-16DW |
| 50 | 2 | U2-3 | | FAN3225C | Driver, Low-Side, High-Speed, 4 A | Fairchild | SOIC-8 |
| 51 | 1 | PWB | | FEBFAN7688_100250A | PWB, 4-Layer, FR4, 0.062" | Custom | N/A |
| 52 | 2 | Sleeving,C1 HV leads | | TFT20018 NA005 | 1.02 mm x 1.78 mm x 13 mm (IDxODxL) | Alpha Wire | N/A |
| 53 | 1 | N/A | | | Silicone adhesive bonding for C1 | | N/A |
| 54 | 4 | N/A | | 8441B | Hex Standoff, 6-32, Nylon, 3/8" | Keystone | Nylon |
| 55 | 4 | N/A | | NY PMS 632 0038 PH | Machine Screw, Nylon, 6-32 x 3/8" | B&F Fastener | Nylon |

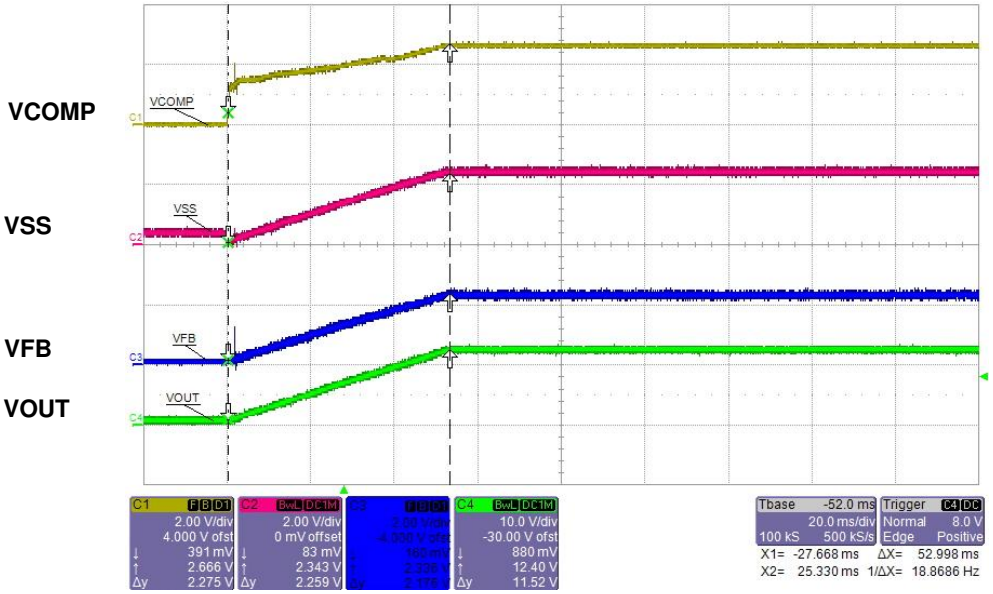
**Notes:**
1. STD = Standard Components
2. DNI = Do Not Install

# 10. Test Data

The following section shows measured wave forms, efficiency, control loop and thermal data for the EVB.

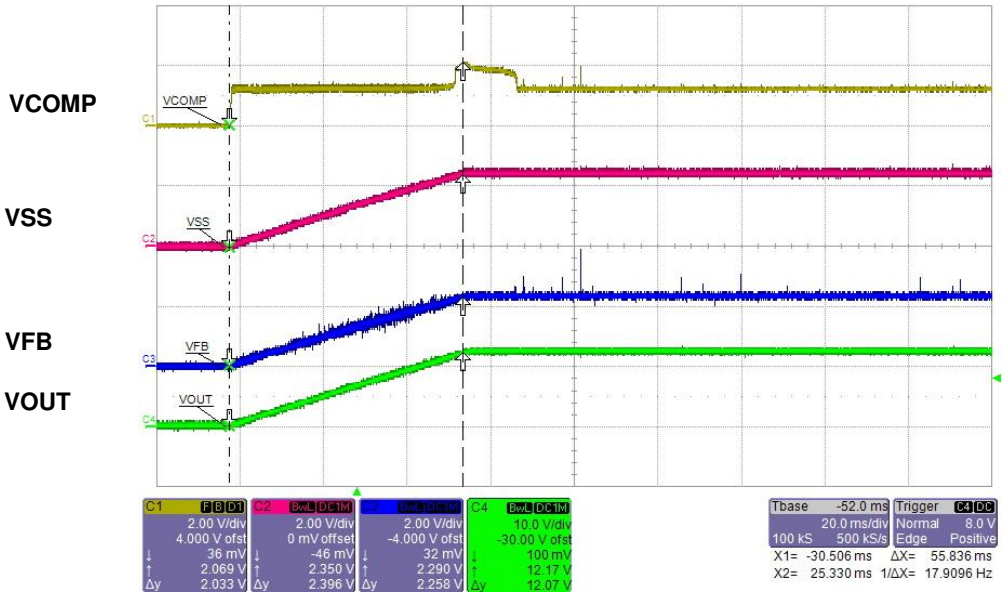
## 10.1. Startup

Figure 17 and Figure 18 show the monotonic soft-start operation at 400 $V_{DC}$ line for full-load and min-load condition, respectively.




CH1: COMP Voltage (2 V/div), CH2: Soft-start Voltage (2 V/div), CH3: Feedback Voltage (2 V/div), CH4: Output Voltage (10V/div), Time (20 ms/div)

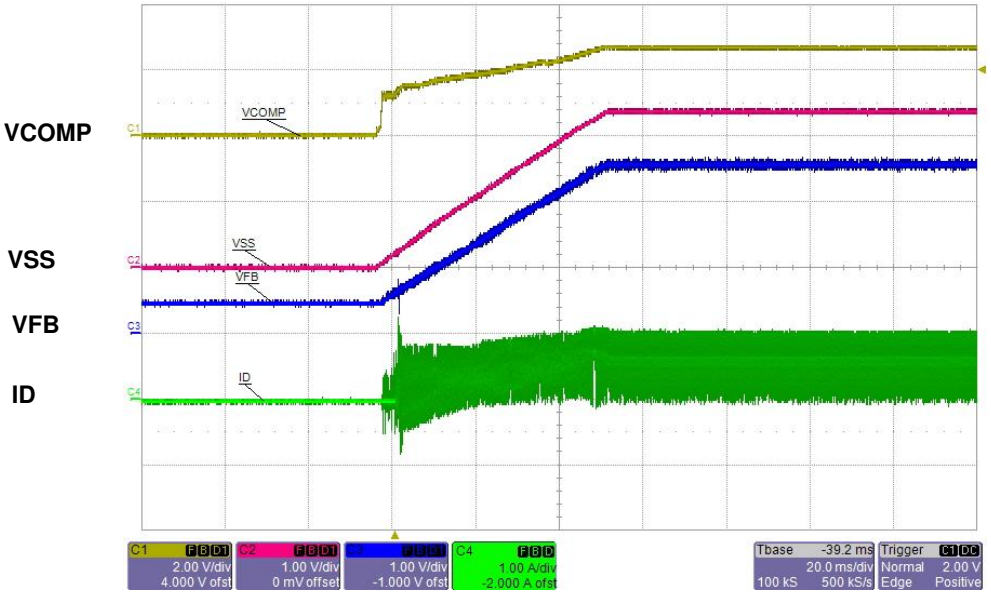
**Figure 17. Full-Load (20 A) Startup at 400 $V_{DC}$, $t_{SS}$ (Soft-start)=53 ms**




CH1: COMP Voltage (2 V/div), CH2: Soft-start Voltage (2 V/div), CH3: Feedback Voltage (2 V/div), CH4: Output Voltage (10 V/div), Time (20 ms/div)

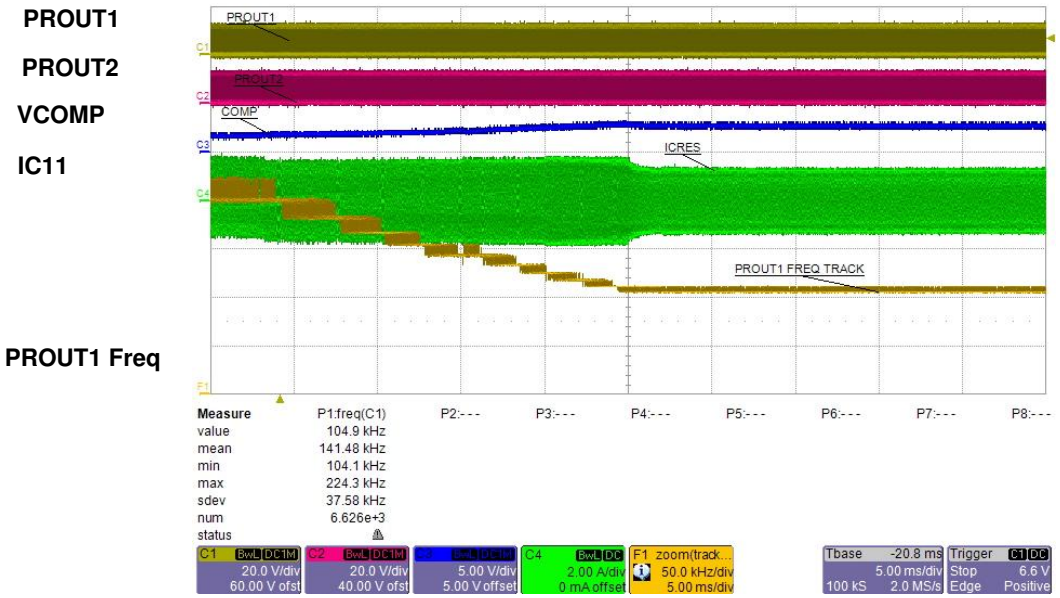
**Figure 18. No-Load (0 A) Startup at 400 $V_{DC}$, $t_{SS}$ (Soft-start)=55 ms**

Figure 19 shows the startup operation at 400 $V_{DC}$ for full-load. The primary drain current shows no current overshoot. No overshoot is observed for full load startup or minimum load startup. Figure 20 is captured 14 ms after startup is initiated. A frequency tracking function was used to show PROUT1 frequency variation from the initial frequency of 224 kHz (PWM mode) to steady state frequency (resonance) of 105 kHz (PFM mode). The frequency transition is smooth and shows no signs of oscillation or abnormal variation.




CH1: COMP Voltage (2 V/div), CH2: Soft-start Voltage (1 V/div), CH3: Feedback Voltage (1 V/div), CH4: Drain Current (1 A/div), Time (20 ms/div)

**Figure 19. Full-Load (20 A) Startup at 400 $V_{DC}$, Primary Drain Current, $I_{R4}$**

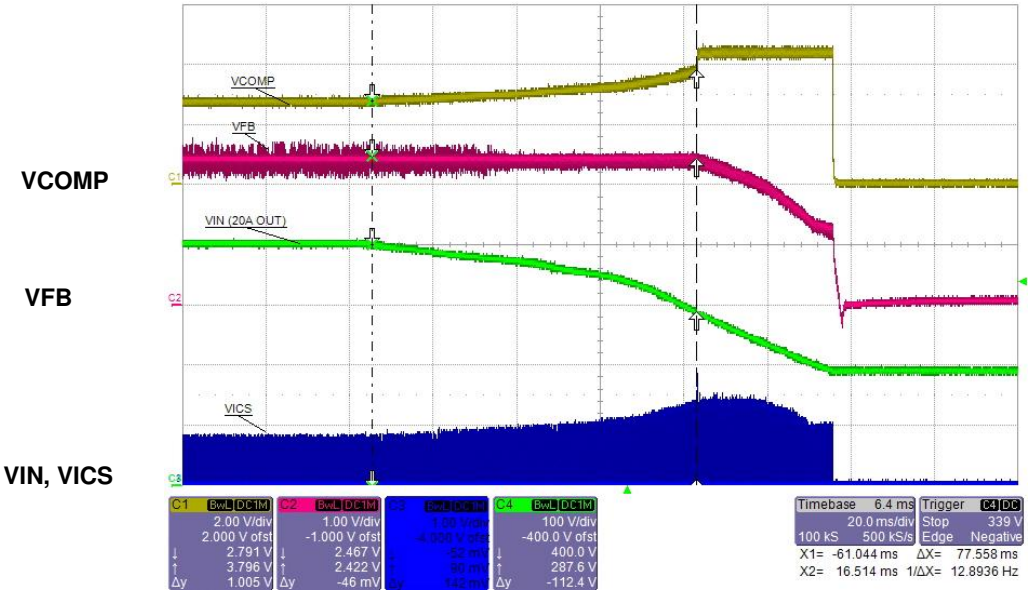



CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: COMP Voltage (5 V/div), CH4: Resonant Current (2 A/div), PROUT1 Freq Track (50 kHz/div), Time (5 ms/div)

**Figure 20. Full-Load (20 A) Startup at 375 $V_{DC}$, Frequency Track, 105 kHz<$F_{PROUT1}$<240 kHz**

## 10.2. Hold-Up

Hold-up time is measured at full load from the time that VIN is removed until VOUT drops out of regulation. The feedback voltage, VFB, is proportional to VOUT and as shown in Figure 21, stays in regulation for 77 ms for 287 $V_{DC}$<VIN<400 $V_{DC}$. As VIN is decreasing, the sensed primary ICS current, VICS, is increasing. Also during this time, the converter operation transitions from above resonance to below resonance. The FAN7688 ICS voltage threshold limit shifts accordingly from 1.2 V (above resonance) to 1.45 (below resonance). This shift in ICS voltage threshold permits operation down to a lower VIN level without causing an overload limit, thus increasing the amount of available hold-up time.

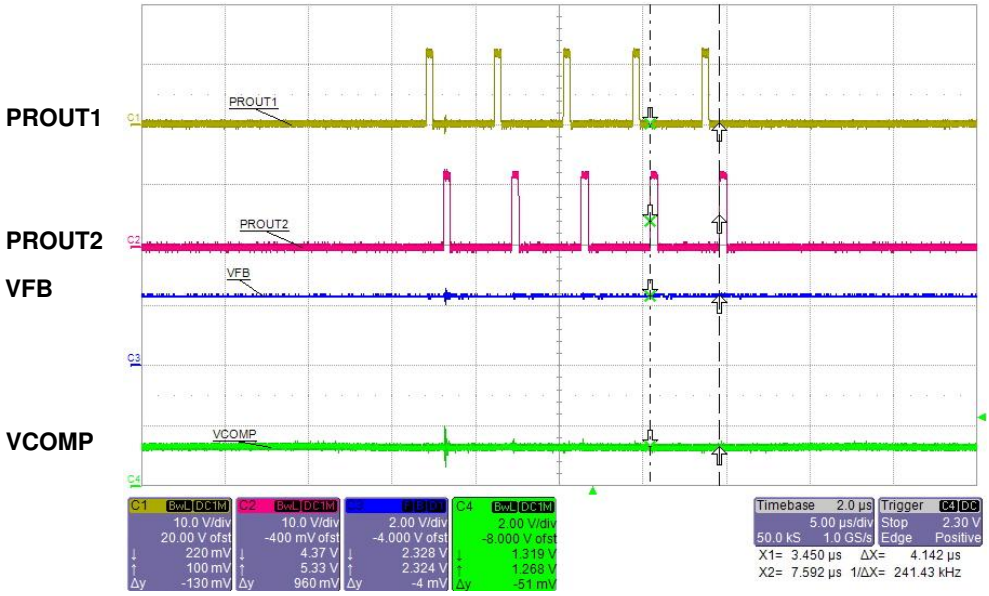



CH1: COMP Voltage (2 V/div), CH2: Feedback Voltage (1 V/div), CH3: ICS Voltage (1 V/div), CH4: Input Voltage (100 V/div), Time (20 ms/div)

**Figure 21. Full-Load (20 A), VIN=400 $V_{DC}$, Hold-Up Time, $t_{HU}$=77 ms**

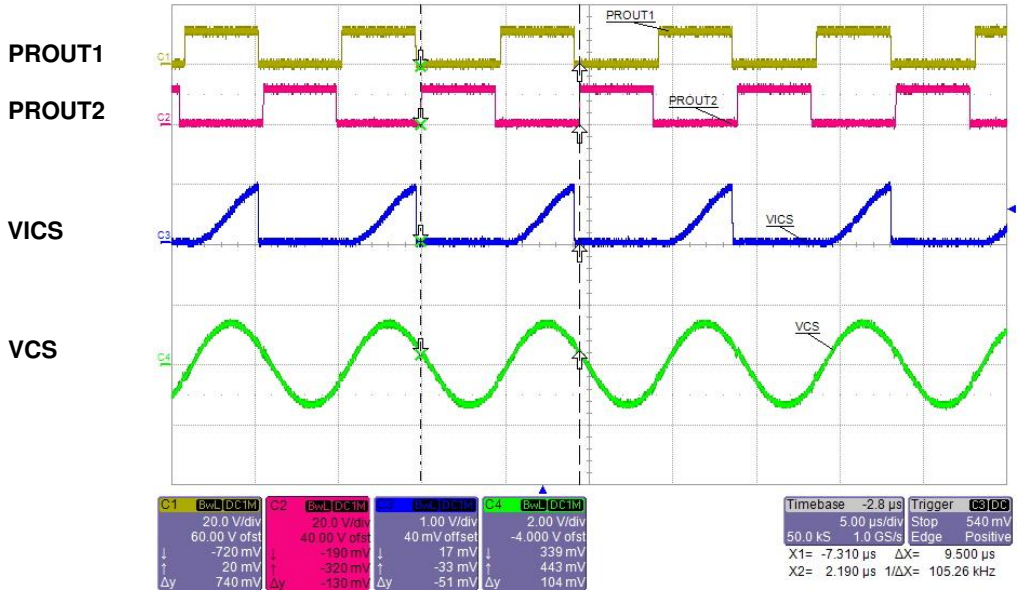
## 10.3. Steady-State Operation

Figure 22 through Figure 25 shows the full load, switching frequency variation for 300 $V_{DC}$<VIN<450 $V_{DC}$.



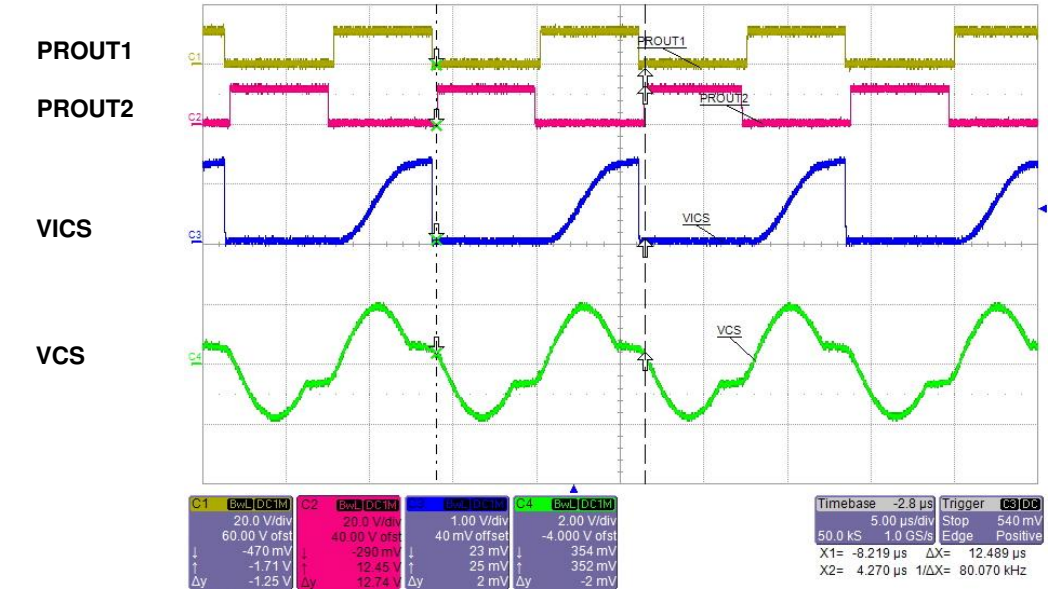

CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: COMP Voltage (2 V/div), Time (5 µs/div)

**Figure 22. PWM Burst Mode, $I_{OUT}$=250 mA, VIN=400 $V_{DC}$, $f_{PWM}$=240 kHz**



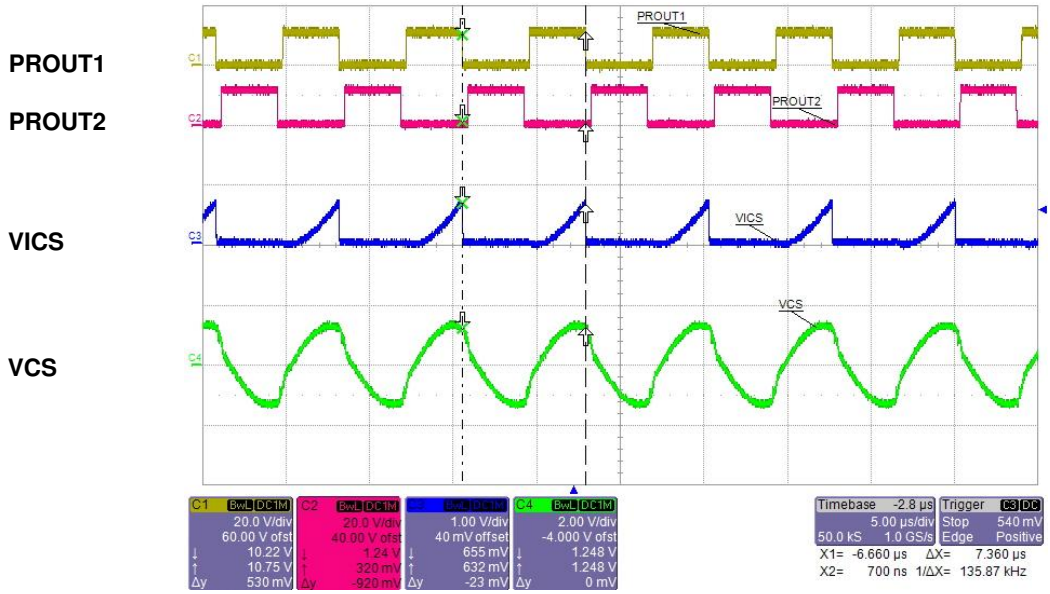

CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (5 µs/div)

**Figure 23. PFM Mode, at Resonance, $I_{OUT}$=20 A, VIN=375 $V_{DC}$, $f_{RES}$=105 kHz**




CH1: PROUT1 (20 V/div), CH2: PROUT2 (20V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (5 µs/div)

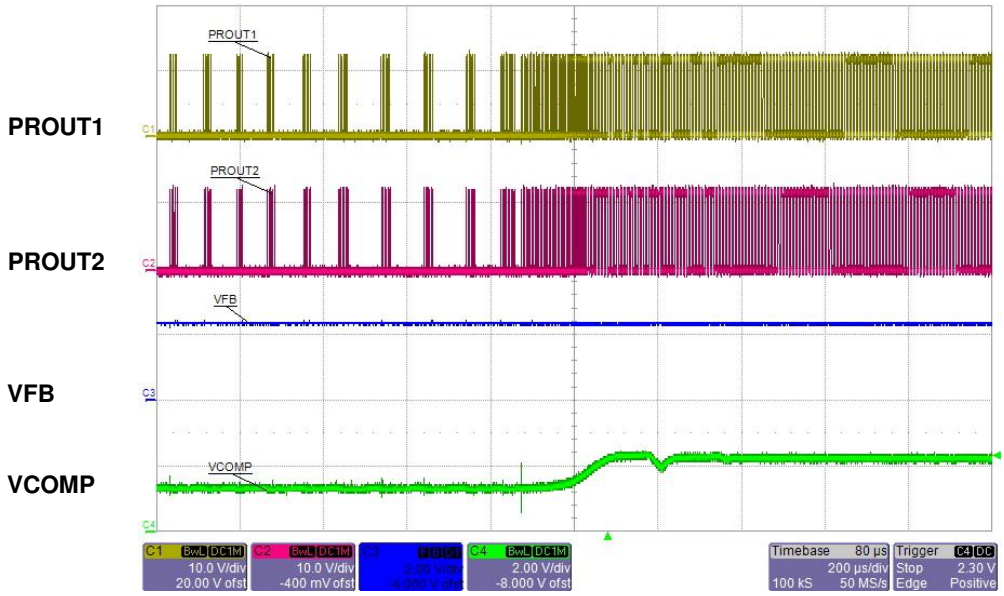
**Figure 24. PFM Mode, Below Resonance, $I_{OUT}$=20 A, VIN=300 $V_{DC}$, F=80 kHz**




CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (5 µs/div)

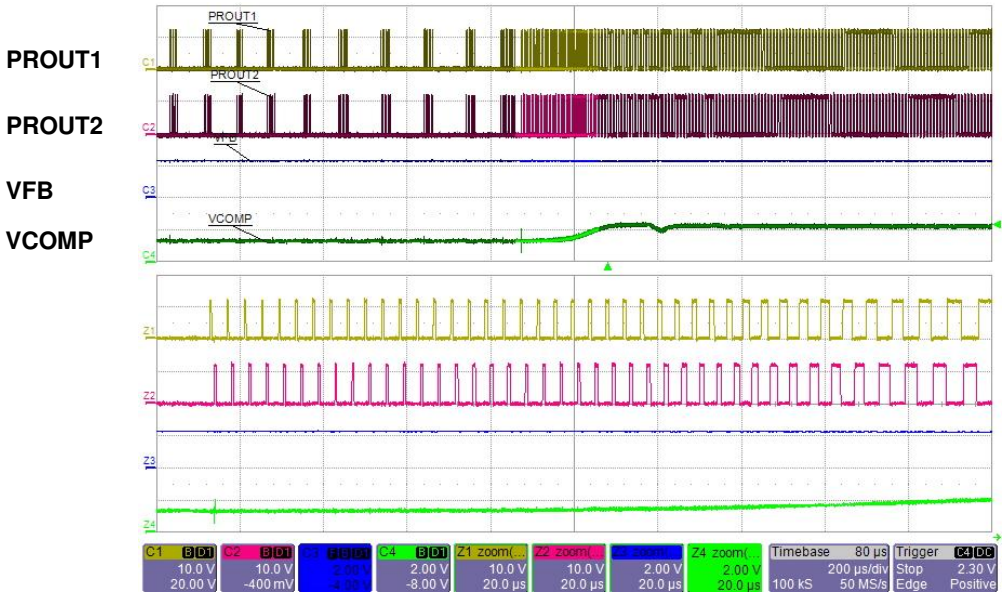
**Figure 25. PFM Mode, Above Resonance, $I_{OUT}$=20 A, VIN=450 $V_{DC}$, F=136 kHz**

Figure 26 shows the transition between PWM burst mode and PFM mode as a current load step from 250 mA to 5 A is introduced. Figure 27 is a zoom showing the smooth transition into the start of PFM mode. The duty cycle increases smoothly as the COMP voltage is increasing.




CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: COMP Voltage (2 V/div), Time (200 µs/div)

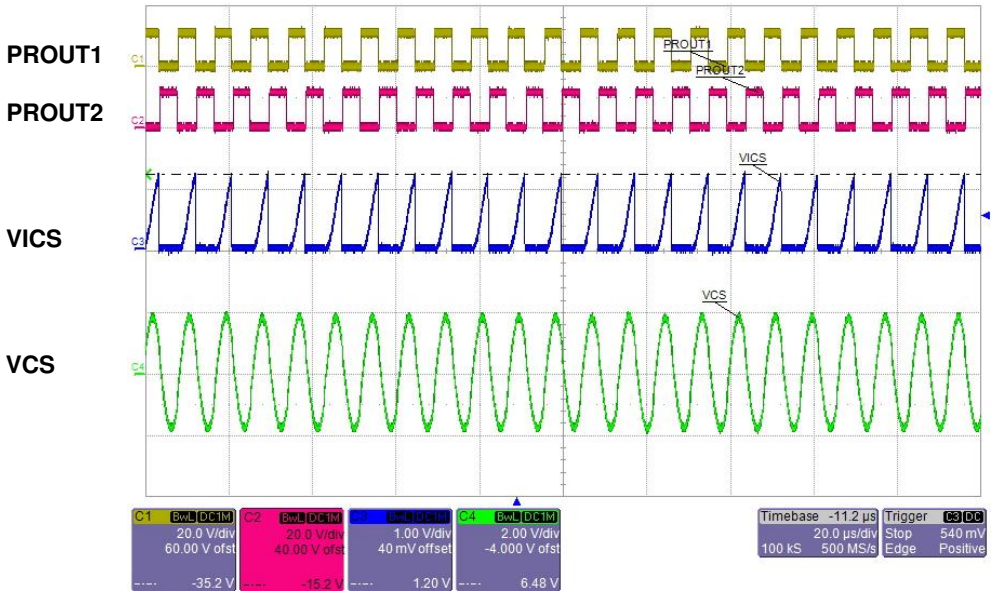
**Figure 26. PWM Burst to PFM Mode Change, $I_{OUT}$=250 mA to 5 A Step, VIN=400 $V_{DC}$**




CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: COMP Voltage (2 V/div), Time (200 µs/div), Zoom Time (20 µs/div)

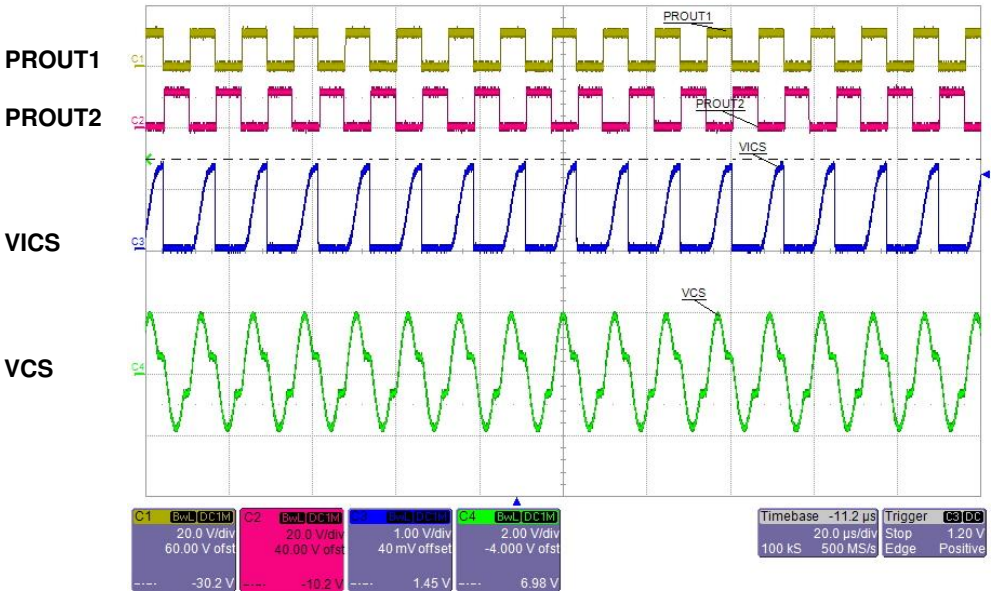
**Figure 27. PWM Burst to PFM Mode Change, $I_{OUT}$=250 mA to 5 A Step, VIN=400 $V_{DC}$**

Figure 28 shows the maximum load current (IOUT=29 A) just before over-current limit when operating above resonance where the VICS threshold limit ($V_{OCL1}$) is 1.2 V. Figure 29 shows the maximum load current (IOUT=21 A) just before over-current limit when operating below resonance where the VICS threshold limit ($V_{OCL2}$) is 1.45 V.




CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (20 µs/div)

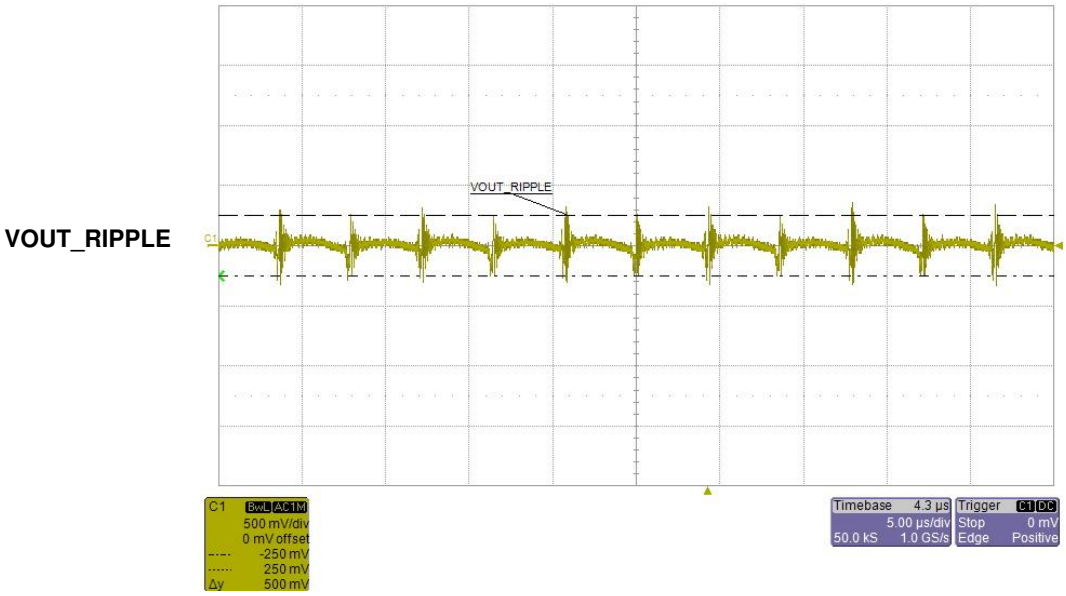
**Figure 28. Just Before Over-Current Limit, Above Resonance, $I_{OUT}$=29 A, VIN=400 $V_{DC}$, VICS=1.2 V**




CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (20 µs/div)

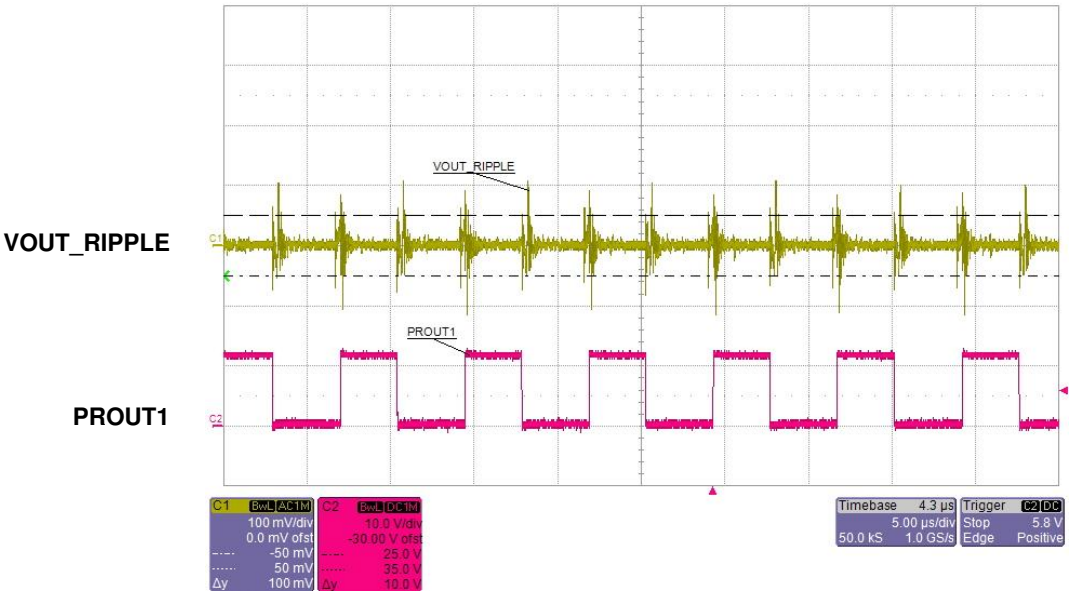
**Figure 29. Just Before Over-Current Limit, Below Resonance, $I_{OUT}$=21 A, VIN=300 $V_{DC}$, VICS=1.45 V**

The maximum, full load, output AC ripple voltage is about 500 $mV_{PP}$ as shown in Figure 30. Setting the load current to the minimum value that will sustain PFM operation (1A) at 400 $V_{DC}$ input, the output AC ripple voltage is measured as 100 mVpp, and is shown in Figure 31.




CH1: Output AC Ripple Voltage (500 mV/div), Time (5 µs/div)

**Figure 30. Output, AC Ripple Voltage, Full Load, $I_{OUT}$=20 A, VIN=400 $V_{DC}$, $V_{OUT\_PP}$=500 $mV_{PP}$**

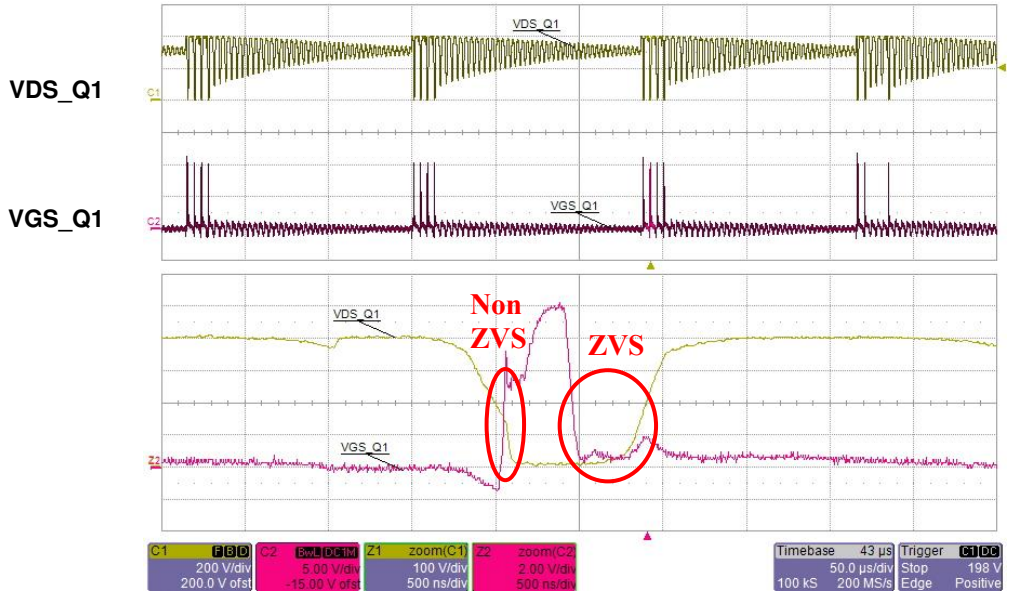



CH1: Output AC Ripple Voltage (100 mV/div), CH2: PROUT1 (10 V/div), Time (5 µs/div)

**Figure 31. Output, AC Ripple Voltage, PFM, $I_{OUT}$=1 A, VIN=400 $V_{DC}$, $V_{OUT\_PP}$=100 $mV_{PP}$**

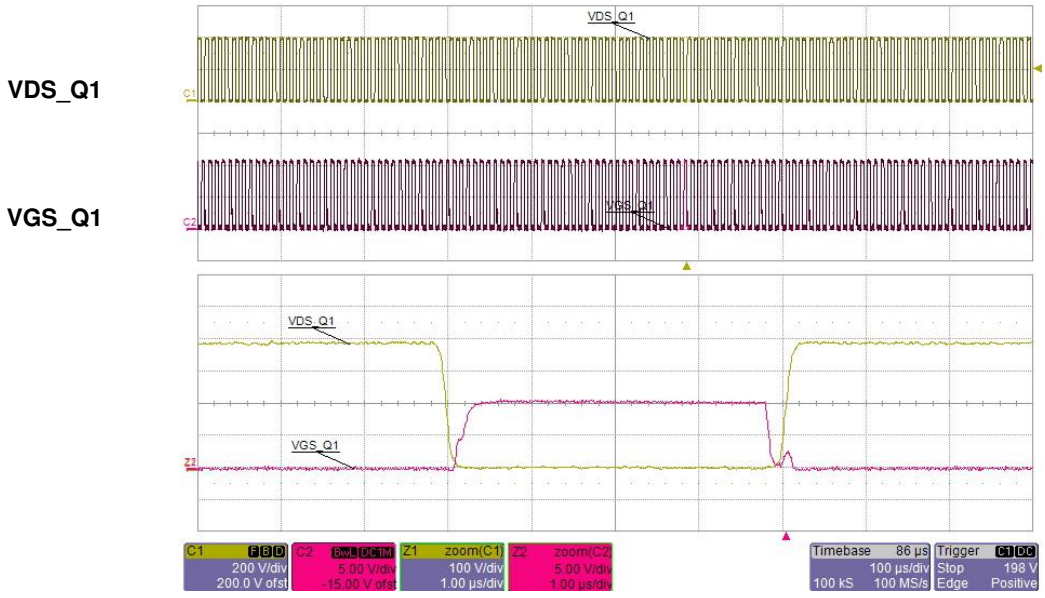
## 10.4. Zero-Voltage Switching (ZVS)

Using traditional PWM mode operation, ZVS is lost on both edges. However, the unique burst mode, PWM pattern of the FAN7688, highlighted in Figure 22, allows for partial ZVS (turn-off only), as shown in Figure 32. High line, light load operation is the worst case condition where ZVS could possibly be lost. Figure 33 and Figure 34 shows full ZVS during PFM mode at turn-on and turn-off for 400 $V_{DC}$, 1 A<IOUT<20 A operation and Figure 35 shows that ZVS is fully retained down to 300 $V_{DC}$ input.



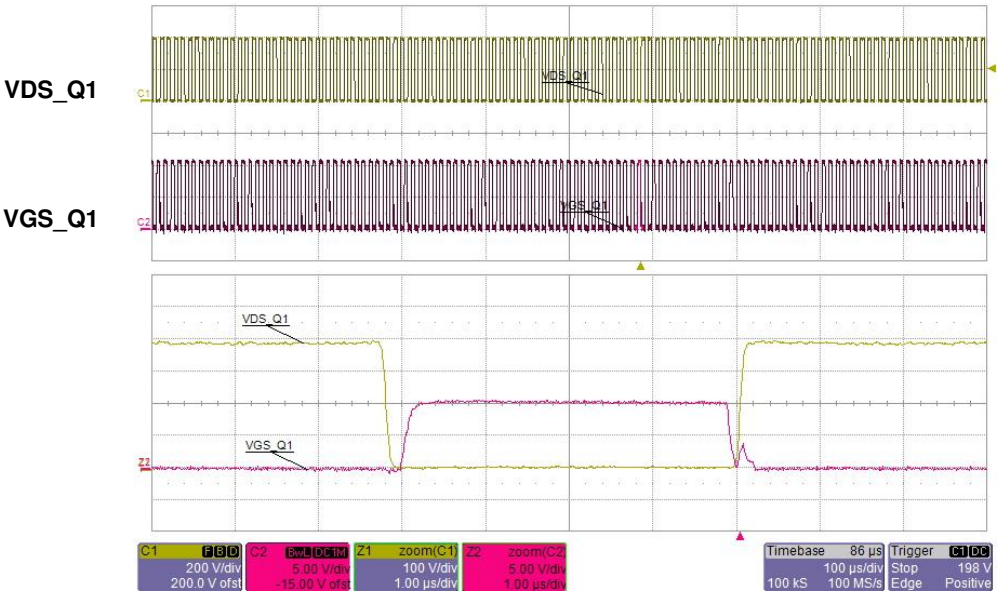

CH1: VDS_Q1 (200 V/div), CH2: VGS_Q1 (5 V/div), CH3: VDS_Q1(zoom) (100 V/div), CH4: VGS_Q1(zoom) (2 V/div), Time (50 µs/div), Zoom Time (500 ns/div)

**Figure 32. Turn-Off ZVS Only, PWM Burst, $I_{OUT}$=120 mA, VIN=400 $V_{DC}$**



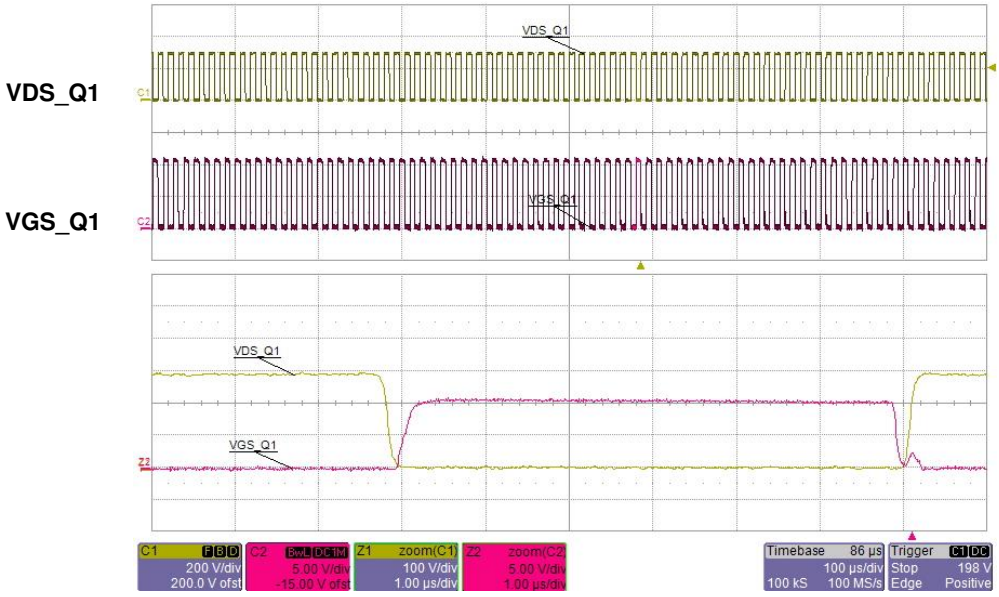

CH1: VDS_Q1 (200 V/div), CH2: VGS_Q1 (5 V/div), CH3: VDS_Q1(zoom) (100 V/div), CH4: VGS_Q1(zoom) (5 V/div), Time (100 µs/div), Zoom Time (1 µs/div)

**Figure 33. Full ZVS, PFM Light- Load, $I_{OUT}$=1 A, VIN=400 $V_{DC}$**




CH1: VDS_Q1 (200 V/div), CH2: VGS_Q1 (5 V/div), CH3: VDS_Q1 (Zoom) (100 V/div), CH4: VGS_Q1 (Zoom) (5 V/div), Time (100 µs/div), Zoom Time (1 µs/div)

**Figure 34. Full ZVS, PFM Full Load, $I_{OUT}$=20 A, VIN=400 $V_{DC}$**

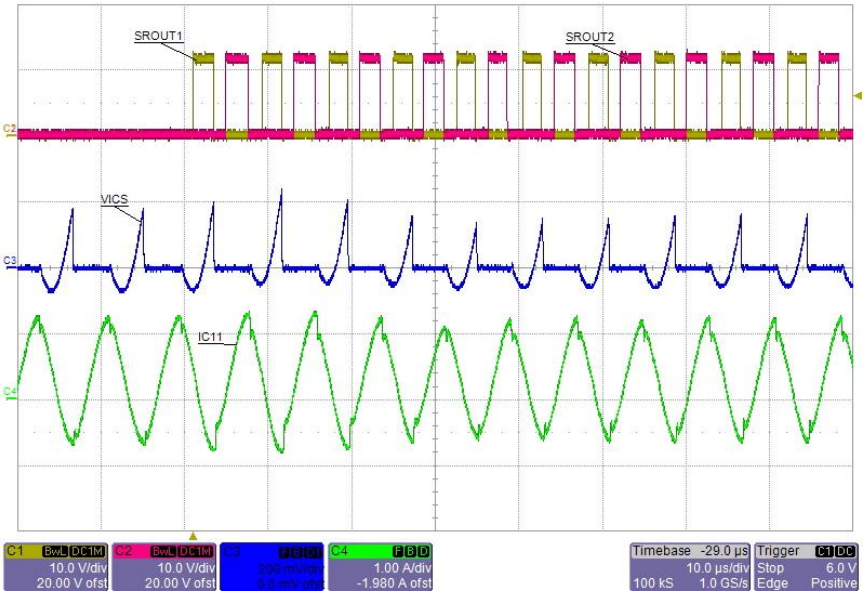



CH1: VDS_Q1 (200 V/div), CH2: VGS_Q1 (5 V/div), CH3: VDS_Q1 (Zoom) (100 V/div), CH4: VGS_Q1 (Zoom) (5 V/div), Time (100 µs/div), Zoom Time (1 µs/div)

**Figure 35. Full ZVS, PFM Full Load, $I_{OUT}$=20 A, VIN=300 $V_{DC}$**

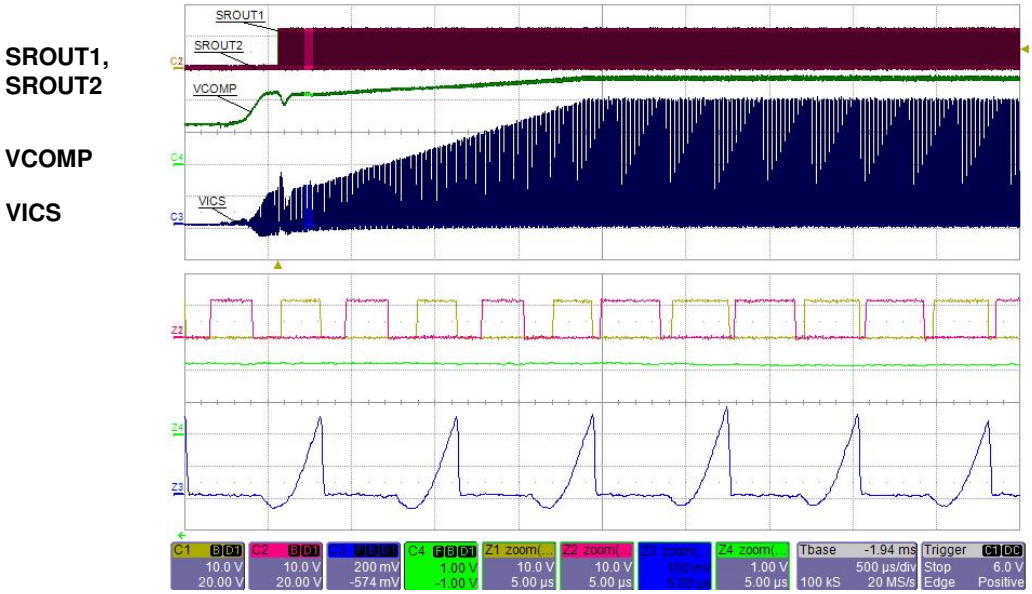
## 10.5. SR Performance

Figure 36 shows the moment both SRs initially turn on in SHRINK mode as a result of a load step from 0 A to 2 A. Figure 37 highlights the smooth transition from SR SHRINK to full SR ENABLE mode as a result of a 0 A to 20 A load step.




CH1: SROUT1 (10 V/div), CH2: SROUT2 (10 V/div), CH3: ICS Voltage (200 mV/div), CH4: Primary Resonant Current (1 A/div), Time (10 µs/div)

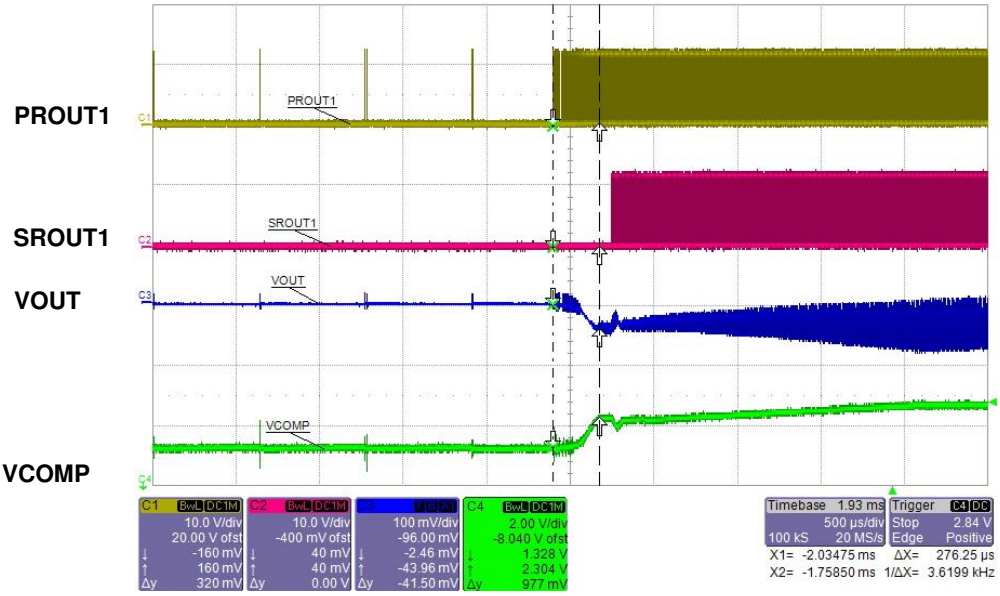
**Figure 36. SR Shrink, $I_{OUT}$=0 A to 2 A Step, VIN=400 $V_{DC}$**




CH1: SROUT1 (10 V/div), CH2: SROUT2 (10 V/div), CH3: ICS Voltage (200 mV/div), CH4: COMP Voltage (1 V/div), Time (500 µs/div), Zoom Time (5 µs/div)

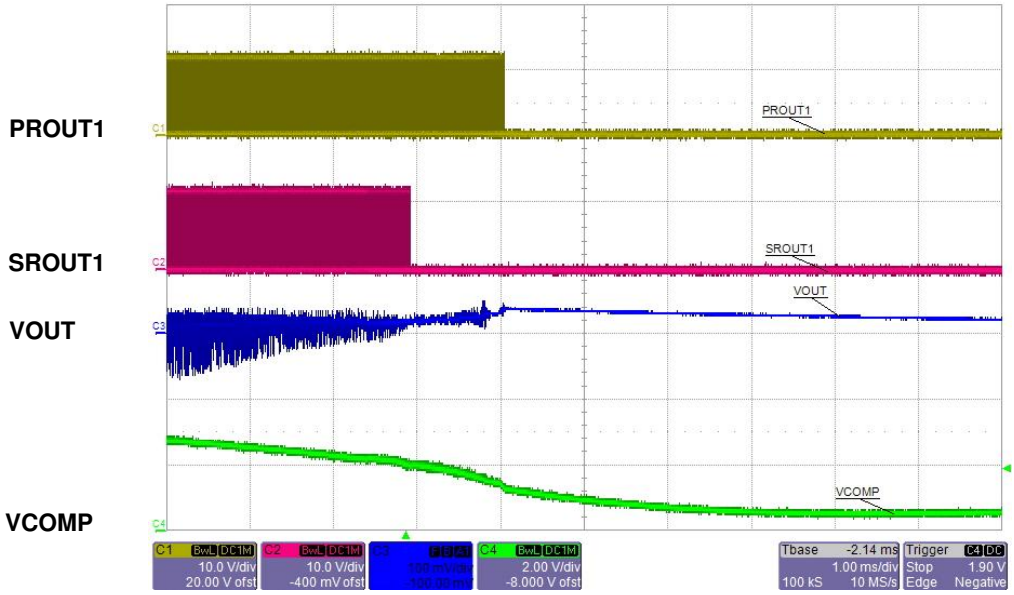
**Figure 37. Shrink to SR EN Mode, $I_{OUT}$=0 A to 20 A Step, VIN=400 $V_{DC}$**

During a 0 A to 20 A current load step, the converter is initially operating in PWM burst mode as indicated by PROUT1 in Figure 38. In response to the 20 A load step, the COMP voltage increases and PROUT1 transitions to PFM mode. SROUT1 is enabled according to VICS (not shown). The VOUT deviation is about 50 mV. Figure 39 shows the SR behavior as a result of a 20 A to 0 A current load step. The VOUT deviation is less than 50 mV and PROUT1 burst mode occurs beyond the 1 ms time scale shown.




CH1: PROUT1 (10 V/div), CH2: SROUT1 (10 V/div),
CH3: Output Voltage (100 mV(AC)/div), CH4: COMP Voltage (2 V/div), Time (500 µs/div)

**Figure 38. PWM Burst to PFM to SR Modes, $I_{OUT}$=0 A to 20 A Step, VIN=400 $V_{DC}$**

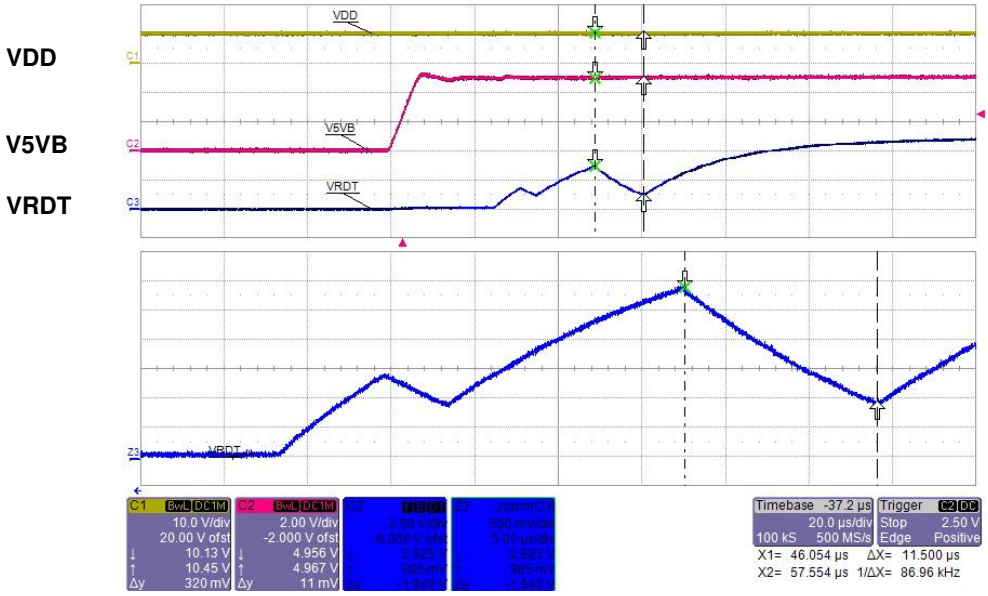



CH1: PROUT1 (10 V/div), CH2: SROUT1 (10 V/div), CH3: Output Voltage (100 mV(AC)/div),
CH4: COMP Voltage (2 V/div), Time (1 ms/div)

**Figure 39. SR to PFM to PWM Burst Modes, $I_{OUT}$=20 A to 0 A Step, VIN=400 $V_{DC}$**

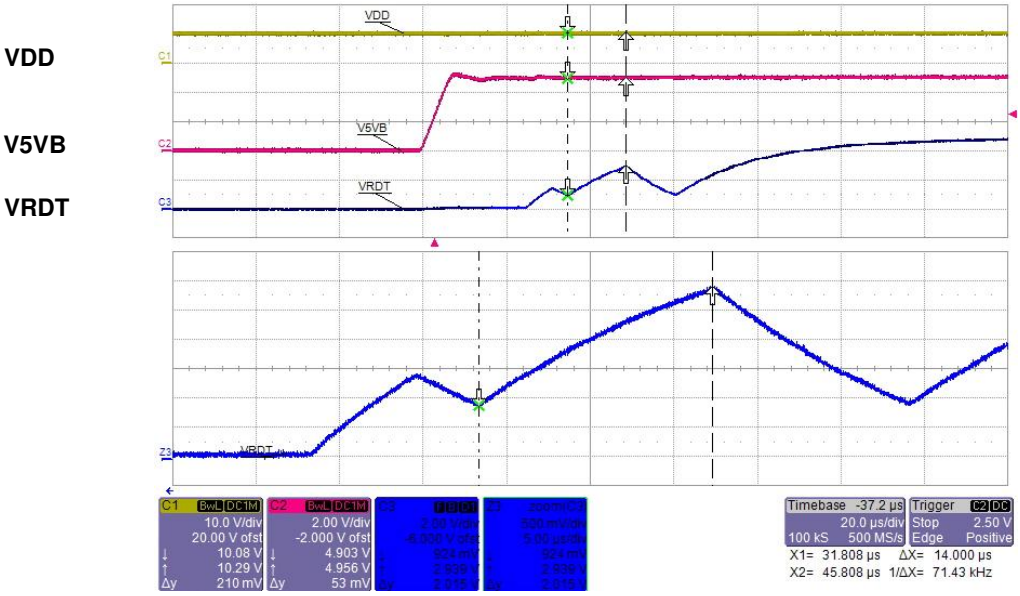
## 10.6. PRDT and SRDT Timing

R28 (43.2 kΩ) and C23 (470 pF) are selected according to the desired dead times shown in the table (SRDT=225 ns, PRDT=350 ns) in the FAN7688 data sheet. During startup, the RDT pin charging time (1 V to 3 V) shown in Figure 41, is used to determine the SR dead time. Similarly, the discharging time (3 V to 1 V) shown in Figure 40 is used to determine the PR dead time. As a result, a single pin (RDT, pin 9) is used to program the PR and SR dead times accordingly.




CH1: VDD Voltage (10V/div), CH2: 5VB Voltage (2 V/div), CH3: RDT Voltage (2 V/div), Time (20 µs/div), Zoom Time (5 µs/div)

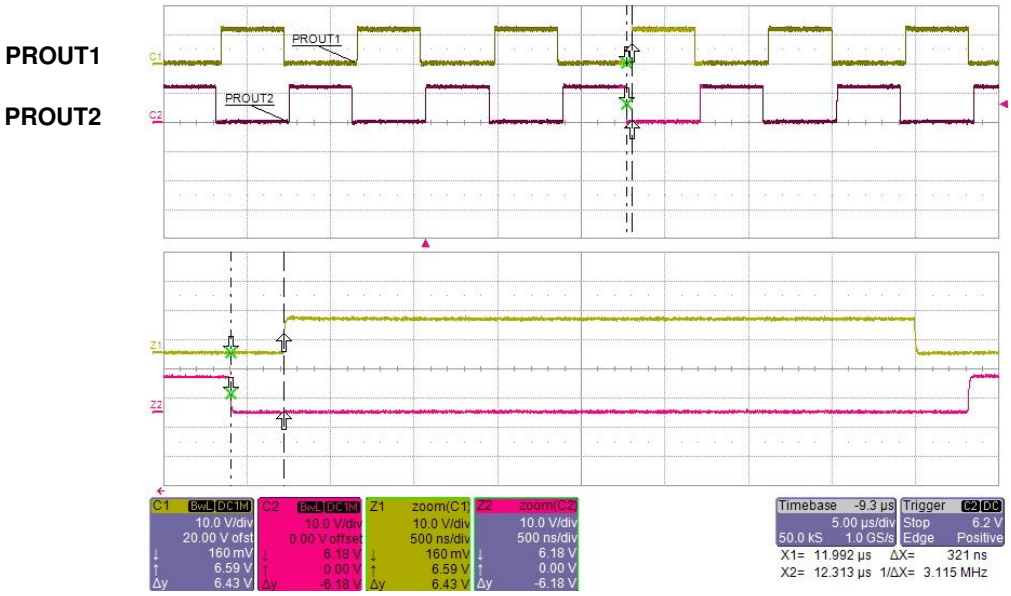
**Figure 40. VRDT Measurement for PRDT (PROUT Dead Time), PRDT=11.5 µs/32=359 ns**




CH1: VDD Voltage (10 V/div), CH2: 5VB Voltage (2 V/div), CH3: RDT Voltage (2 V/div), Time (20 µs/div), Zoom Time (5 µs/div)

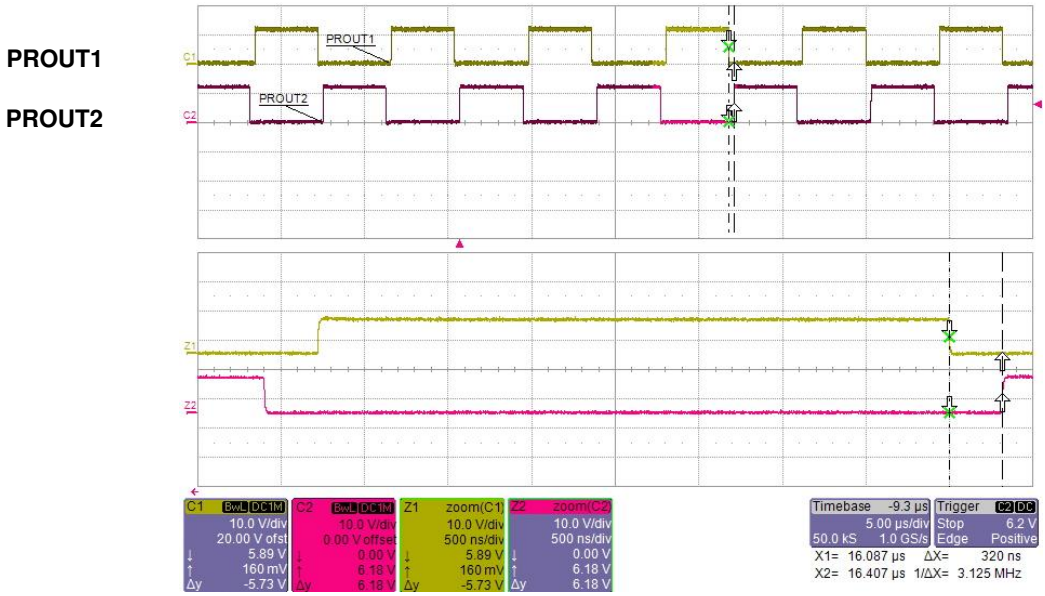
**Figure 41. VRDT Measurement for SRDT (SROUT Dead Time), SRDT=14 µs/64=219 ns**

During PFM operation, the actual measured dead times between PROUT1 and PROUT2 are shown in Figure 42 and Figure 43 respectively. The measured dead times of 320 ns are within the expected 50 ns of acceptable error compared to 359 ns determined from Figure 40.




CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), Time (5 µs/div), Zoom Time (500 ns/div)

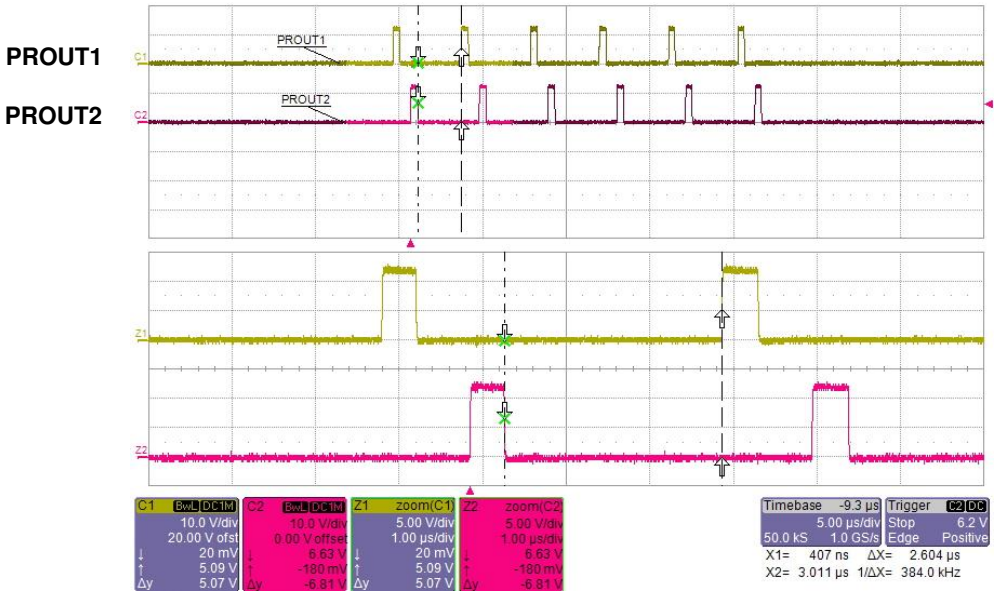
**Figure 42. PFM Mode, PROUT2-1 Measured Dead Time, $I_{OUT}$=10 A, VIN=400 $V_{DC}$, PRDT2-1=321 ns**




CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), Time (5 µs/div), Zoom Time (500 ns/div)

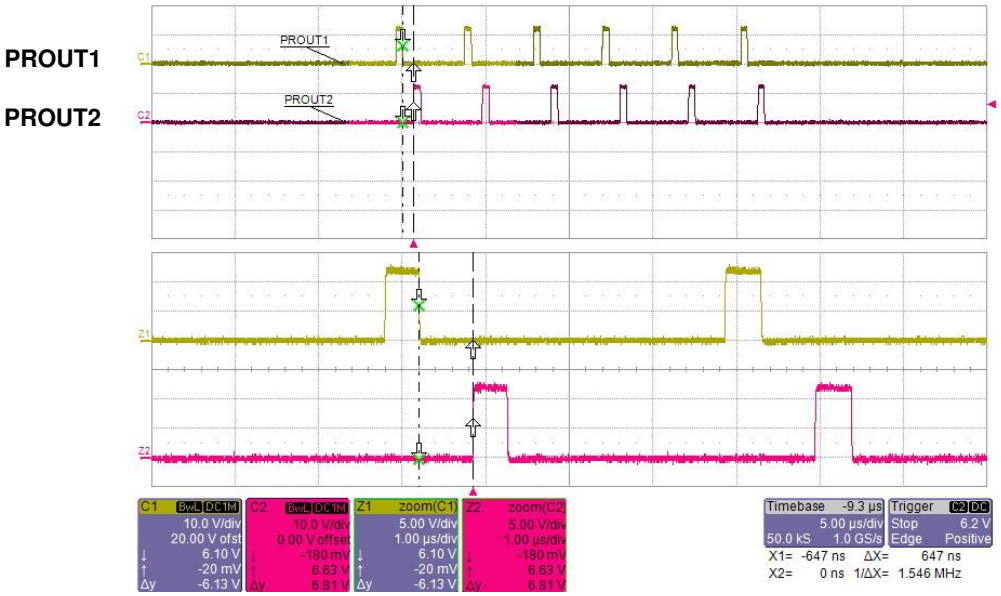
**Figure 43. PFM Mode, PROUT1-2 Measured Dead Time, $I_{OUT}$=10 A, VIN=400 $V_{DC}$, PRDT1-2=320 ns**

During PWM mode operation, the actual measured dead times between PROUT1 and PROUT2 are shown in Figure 44 and Figure 45 respectively. The measured dead time of 647 ns shown in Figure 45 is twice the measured value shown in Figure 42 and Figure 43. This “dead time doubling” function only occurs during PWM mode for the purpose of retaining “partial ZVS” (Figure 32) during light load PWM operation.




CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), Time (5 µs/div), Zoom Time (1 µs/div)

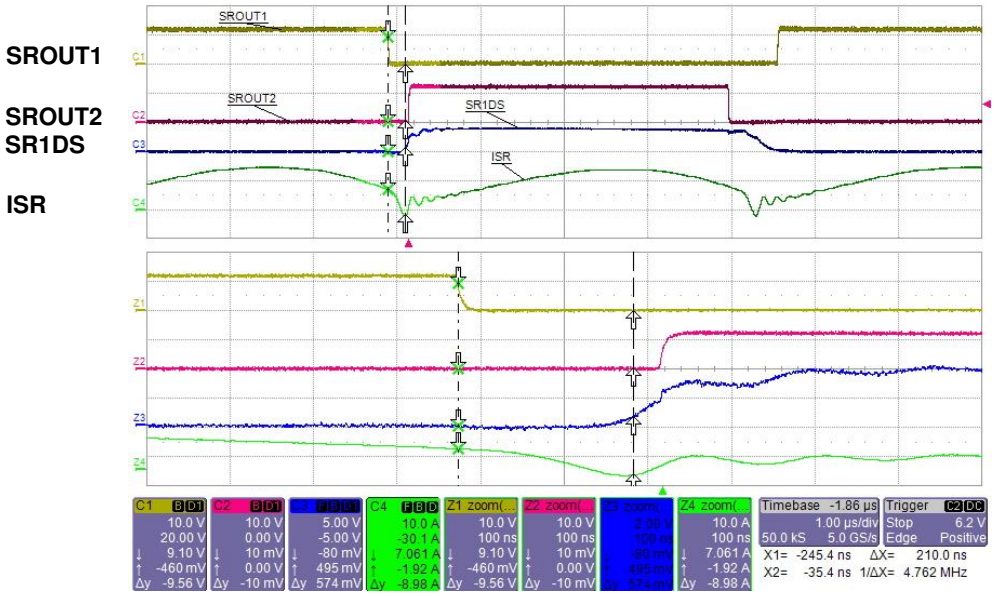
**Figure 44. PWM Burst Mode, PROUT2-1 Measured Dead Time, $I_{OUT}$=250 mA, VIN=400 $V_{DC}$, PRDT2-1=2.6 µs**




CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), Time (5 µs/div), Zoom Time (1 µs/div)

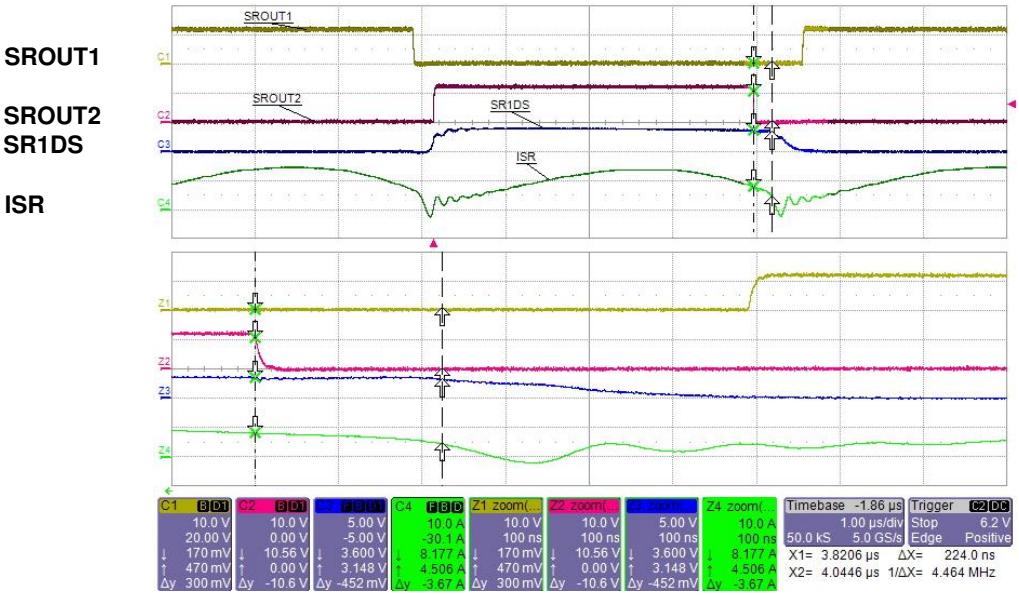
**Figure 45. PWM Burst Mode, PROUT1-2 Measured Dead Time, $I_{OUT}$=250 mA, VIN=400 $V_{DC}$, PRDT1-2=647 ns**

During PFM, SR ENABLE operation, the actual measured dead times for SROUT1 and SROUT2 are shown in Figure 46 and Figure 47 respectively. The measured dead times of 210 ns and 224 ns are within the expected 50n s of acceptable error compared to 219 ns determined from Figure 41.




CH1: SROUT1 (10 V/div), CH2: SROUT2 (10 V/div), CH3: SR1DS (5 V/div), CH4: SR Current (10 A/div), Time (1 µs/div), Zoom Time (100 ns/div)

**Figure 46. PFM Mode, SROUT1 Measured Dead Time, $I_{OUT}$=10 A, VIN=400 $V_{DC}$, SRDT1=210 ns**

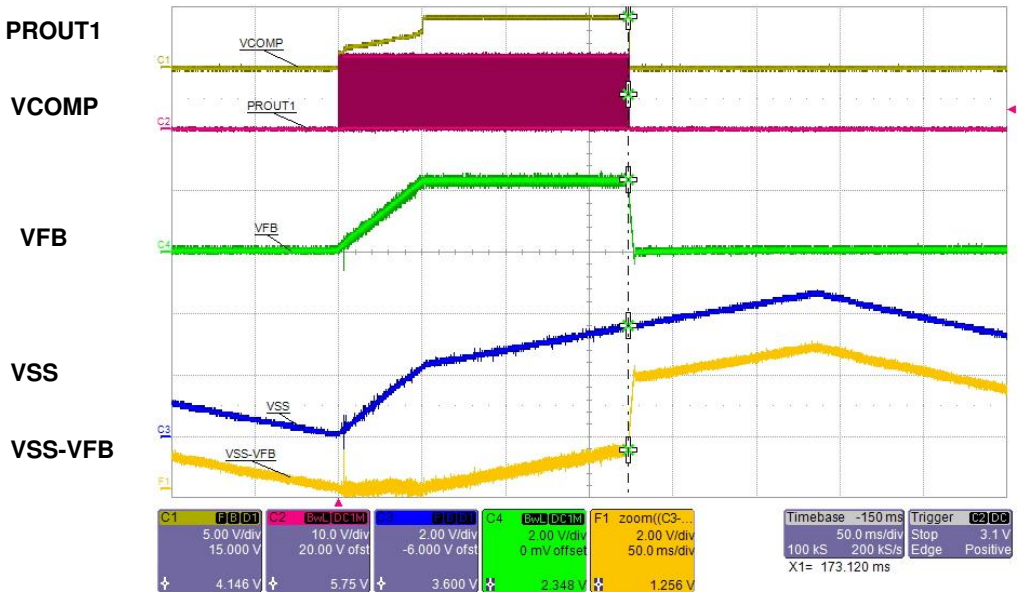



CH1: SROUT1 (10 V/div), CH2: SROUT2 (10 V/div), CH3: SR1DS (5 V/div), CH4: SR Current (10 A/div), Time (1 µs/div), Zoom Time (100 ns/div)

**Figure 47. PFM Mode, SROUT2 Measured Dead Time, $I_{OUT}$=10 A, VIN=400 $V_{DC}$, SRDT2=224 ns**

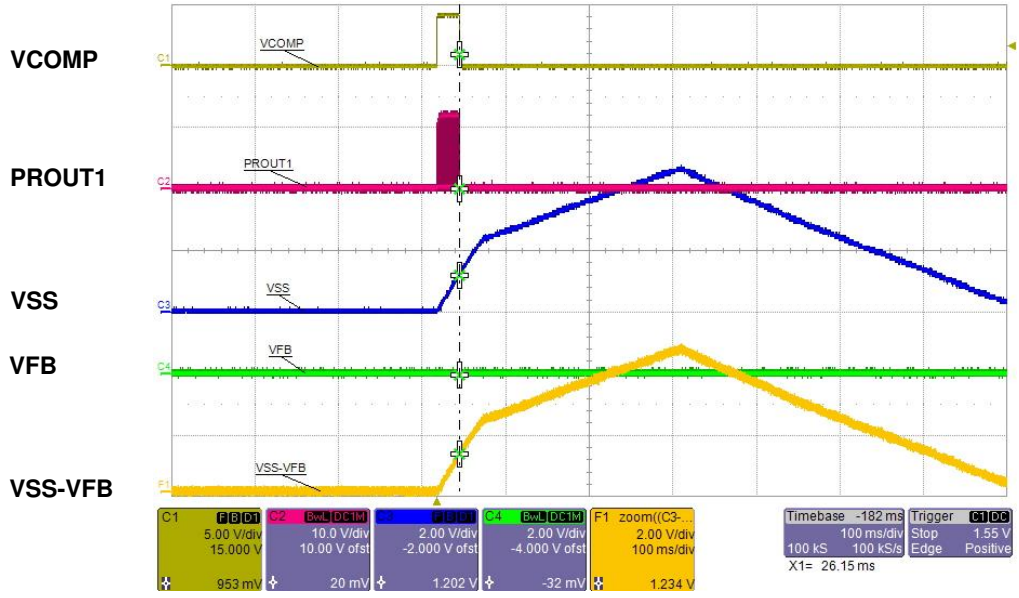
## 10.7. Protection Functions

During startup, if the COMP voltage is saturated high (4.2 V) and the difference between the soft-start voltage and feedback voltage (VSS-VFB) is greater than 0 V but less than 1.2 V, when the soft-start voltage reaches 3.6 V, Overload Protection (OLP) is enabled, as shown in Figure 48. If VSS-VFB is greater than 1.2 V, regardless of the soft-start voltage, then Output Short Protection (OSP) is enabled, as shown in Figure 49.




CH1: COMP Voltage (5 V/div), CH2: PROUT1 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: Soft-Start Voltage (2 V/div), VSS-VFB (2 V/div), Time (50 ms/div)

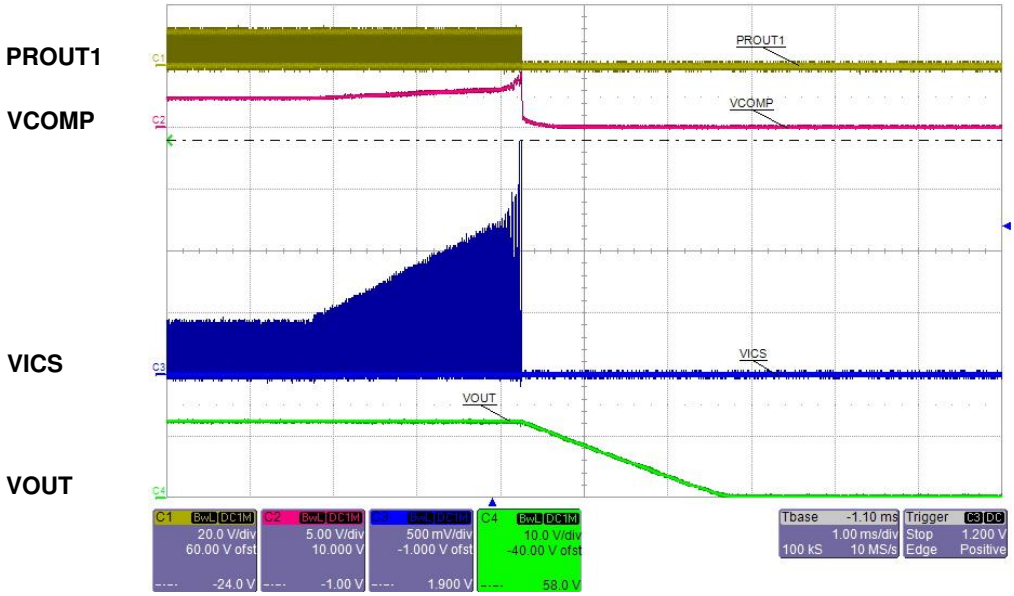
**Figure 48. OLP, $I_{OUT}$=23 A, VIN=350 $V_{DC}$**




CH1: COMP Voltage (5 V/div), CH2: PROUT1 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: Soft-Start Voltage (2 V/div), VSS-VFB (2 V/div), Time (100 ms/div)

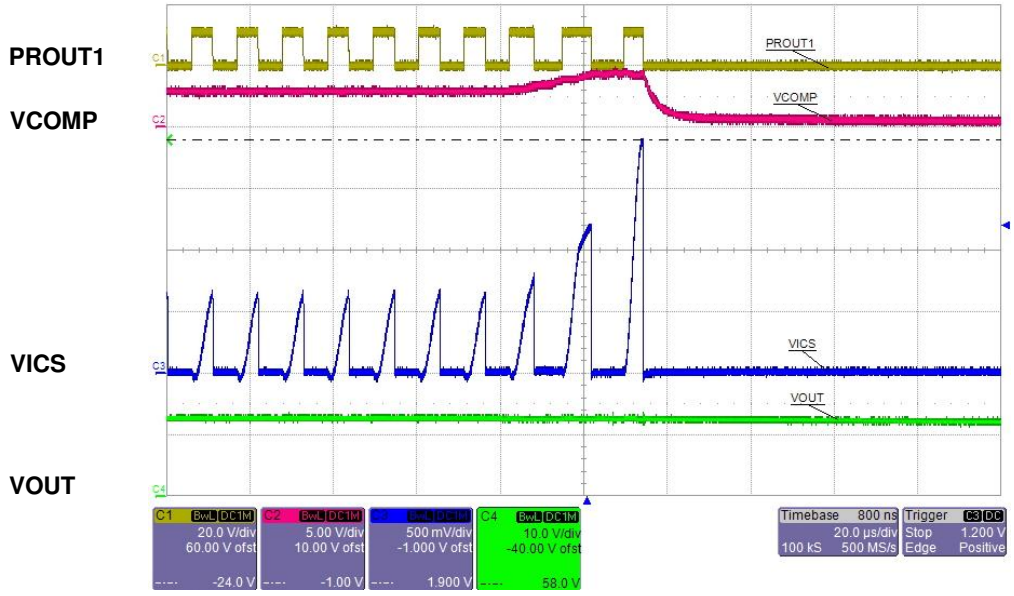
**Figure 49. OSP, Start with VDD only, $I_{OUT}$=0 A, VIN=0 $V_{DC}$**

If the ICS voltage reaches the 1.9 V threshold, Over-Current Protection (OCP) is triggered as shown in Figure 50 and Figure 51.




CH1: PROUT1 (20 V/div), CH2: COMP Voltage (5 V/div), CH3: ICS Voltage (500 mV/div), CH4: Output Voltage (10 V/div), Time (1 ms/div)

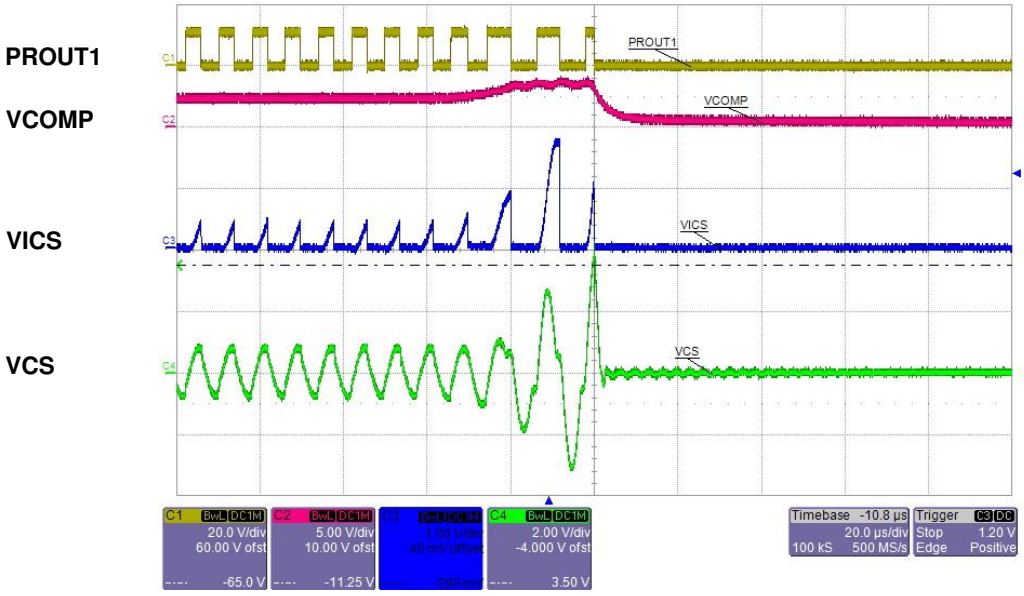
**Figure 50. Above Resonance, OCP, $I_{OUT}$=10 A to 35 A, VIN=400 $V_{DC}$**




CH1: PROUT1 (20 V/div), CH2: COMP Voltage (5 V/div), CH3: ICS Voltage (500 mV/div), CH4: Output Voltage (10 V/div), Time (1 ms/div)

**Figure 51. Below Resonance, OCP, $I_{OUT}$=10 A to 35 A, VIN=330 $V_{DC}$**

If the CS voltage reaches the 3.5 V threshold, a second level Over-Current Protection (OCP) ($V_{OCP2P/N}$) is triggered. The second level OCP is designed to protect the converter from catastrophic failures such as transformer saturation, MOSFET and/or gate drive failures or any type of short circuit failure. The waveform captured in Figure 52 was taken during a hard short applied to the converter output and shows the CS voltage crossing 3.5 V, while the ICS voltage remains below its corresponding 1.9 V threshold. As can be seen, the FAN7688 controller instantly responds by terminating the PROUT1 (and PROUT2, not shown), even in the middle of a single pulse.




CH1: PROUT1 (20 V/div), CH2: COMP Voltage (5 V/div), CH3: ICS Voltage (500 mV/div), CH4: Output Voltage (10 V/div), VSS-VFB (2 V/div), Time (1 ms/div)

**Figure 52. Above Resonance, Second Level OCP, $I_{OUT}$=10 A to Short Circuit, VIN=400 $V_{DC}$**

## 10.1. Efficiency

Figure 53 shows the measured efficiency verses load for VIN=400 V. The peak efficiency is 97% at 50% maximum rated load and >95% for 50 W<POUT<250 W. The EVB has been optimized for maximum efficiency around the 20% maximum load power point. As a result, the SRs are enabled in shrink mode at 10% load and are fully enabled at the 30% load condition. The red line shows the measured efficiency as the load is increased from 0 W to 250 W while the blue line shows measured efficiency when decreasing the load from 58 W (point where SR shrink begins when decreasing load) down to 10 W. The light load efficiency difference between the red and blue lines highlights the SR enable/disable hysteresis effect on efficiency. Measured efficiency test data is detailed in Table 6.

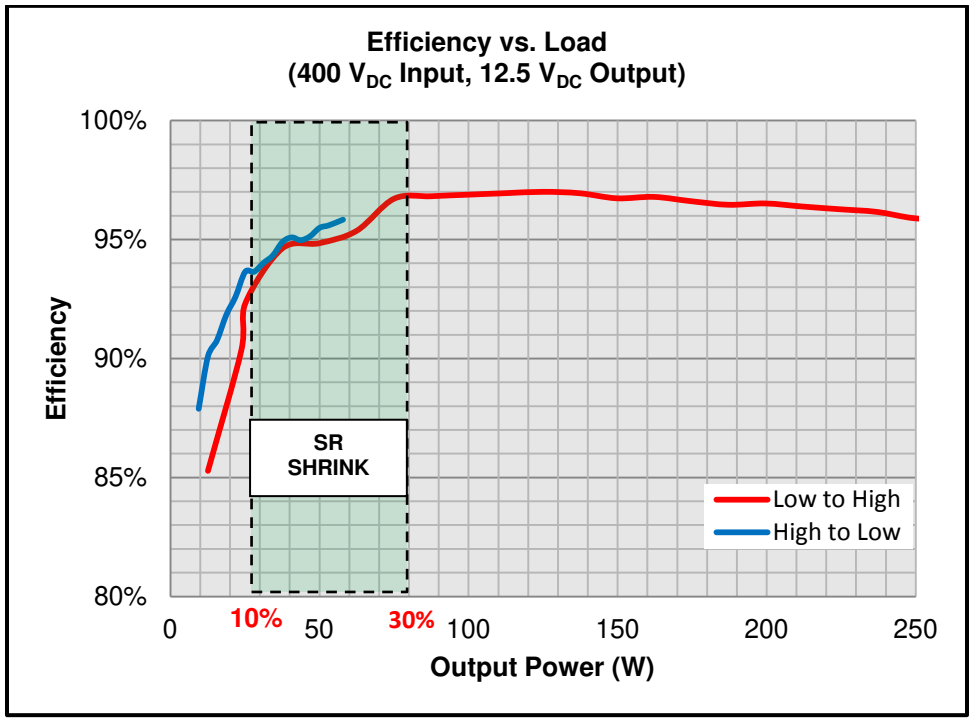



**Figure 53. Efficiency vs. Load**

**Table 6. Measured Efficiency Data**

| $V_{OUT}$ ($V_{DC}$) | $I_{OUT}$ ($A_{DC}$) | $P_{OUT}$ (W) | $V_{IN}$ ($V_{DC}$) | $I_{IN}$ ($A_{DC}$) | $P_{IN}$ (W) | η | %Max. Load | Mode | SR |
|---|---|---|---|---|---|---|---|---|---|
| **LOW TO HIGH MEASUREMENTS (RED LINE IN Figure 53)** | | | | | | | | | |
| 12.497 | 1.01 | 12.62 | 400.00 | 0.04 | 14.80 | 85.3% | 5.1% | PWM | NO SR |
| 12.491 | 1.91 | 23.86 | 400.00 | 0.07 | 26.40 | 90.4% | 9.6% | PFM | NO SR |
| 12.491 | 2.01 | 25.11 | 400.00 | 0.07 | 27.20 | 92.3% | 10.1% | PFM | SR SHRINK |
| 12.49 | 3.00 | 37.47 | 400.00 | 0.10 | 39.60 | 94.6% | 15.0% | PFM | SR SHRINK |
| 12.489 | 4.01 | 50.08 | 400.00 | 0.13 | 52.80 | 94.9% | 20.1% | PFM | SR SHRINK |
| 12.488 | 5.01 | 62.56 | 400.00 | 0.16 | 65.60 | 95.4% | 25.1% | PFM | SR SHRINK |
| 12.488 | 6.01 | 75.05 | 400.00 | 0.19 | 77.60 | 96.7% | 30.1% | PFM | SR EN |
| 12.486 | 7.01 | 87.53 | 400.00 | 0.23 | 90.40 | 96.8% | 35.1% | PFM | SR EN |
| 12.483 | 8.01 | 99.99 | 400.00 | 0.26 | 103.20 | 96.9% | 40.1% | PFM | SR EN |
| 12.482 | 9.01 | 112.34 | 400.00 | 0.29 | 116.00 | 97.0% | 45.1% | PFM | SR EN |
| 12.482 | 10.01 | 124.82 | 400.00 | 0.32 | 128.80 | 97.0% | 50.1% | PFM | SR EN |
| 12.48 | 11.00 | 137.28 | 400.00 | 0.35 | 141.60 | 96.9% | 55.1% | PFM | SR EN |
| 12.479 | 12.00 | 149.75 | 400.00 | 0.39 | 154.80 | 96.7% | 60.1% | PFM | SR EN |
| 12.479 | 13.00 | 162.23 | 400.00 | 0.42 | 167.60 | 96.8% | 65.1% | PFM | SR EN |
| 12.477 | 14.00 | 174.68 | 400.00 | 0.45 | 180.80 | 96.6% | 70.1% | PFM | SR EN |
| 12.476 | 15.00 | 187.14 | 400.00 | 0.49 | 194.00 | 96.5% | 75.1% | PFM | SR EN |
| 12.475 | 16.00 | 199.60 | 400.00 | 0.52 | 206.80 | 96.5% | 80.1% | PFM | SR EN |
| 12.474 | 17.00 | 212.06 | 400.00 | 0.55 | 220.00 | 96.4% | 85.0% | PFM | SR EN |
| 12.473 | 18.00 | 224.51 | 400.00 | 0.58 | 233.20 | 96.3% | 90.0% | PFM | SR EN |
| 12.471 | 19.00 | 236.95 | 400.00 | 0.62 | 246.40 | 96.2% | 95.0% | PFM | SR EN |
| 12.467 | 20.00 | 249.34 | 400.00 | 0.65 | 260.00 | 95.9% | 100.0% | PFM | SR EN |
| 12.467 | 21.00 | 261.81 | 400.00 | 0.68 | 273.20 | 95.8% | 105.0% | PFM | SR EN |
| 12.465 | 22.00 | 274.23 | 400.00 | 0.72 | 286.40 | 95.8% | 110.0% | PFM | SR EN |
| 12.462 | 23.01 | 286.75 | 400.00 | 0.75 | 300.40 | 95.5% | 115.0% | PFM | SR EN |
| 12.461 | 24.01 | 299.19 | 400.00 | 0.79 | 314.00 | 95.3% | 120.0% | PFM | SR EN |
| 12.458 | 25.01 | 311.57 | 400.00 | 0.82 | 327.60 | 95.1% | 125.0% | PFM | SR EN |
| **HIGH TO LOW MEASUREMENTS (BLUE LINE IN Figure 53)** | | | | | | | | | |
| 12.476 | 4.64 | 57.89 | 400.00 | 0.15 | 60.40 | 95.8% | 25.8% | PFM | SR SHRINK |
| 12.478 | 4.26 | 53.16 | 400.00 | 0.14 | 55.60 | 95.6% | 23.7% | PFM | SR SHRINK |
| 12.479 | 4.01 | 50.04 | 400.00 | 0.13 | 52.40 | 95.5% | 22.3% | PFM | SR SHRINK |
| 12.479 | 3.75 | 46.80 | 399.90 | 0.12 | 49.19 | 95.1% | 20.8% | PFM | SR SHRINK |
| 12.48 | 3.50 | 43.68 | 399.90 | 0.12 | 45.99 | 95.0% | 19.5% | PFM | SR SHRINK |
| 12.482 | 3.26 | 40.69 | 399.90 | 0.11 | 42.79 | 95.1% | 18.1% | PFM | SR SHRINK |
| 12.482 | 3.01 | 37.57 | 399.90 | 0.10 | 39.59 | 94.9% | 16.7% | PFM | SR SHRINK |
| 12.483 | 2.75 | 34.33 | 399.90 | 0.09 | 36.39 | 94.3% | 15.3% | PFM | SR SHRINK |
| 12.483 | 2.5 | 31.21 | 399.90 | 0.08 | 33.19 | 94.0% | 13.9% | PFM | SR SHRINK |
| 12.484 | 2.25 | 28.09 | 399.90 | 0.08 | 29.99 | 93.7% | 12.5% | PFM | SR SHRINK |
| 12.484 | 2.01 | 25.09 | 399.90 | 0.07 | 26.79 | 93.7% | 11.2% | PFM | SR SHRINK |
| 12.485 | 1.75 | 21.85 | 399.90 | 0.06 | 23.59 | 92.6% | 9.7% | PFM | SR SHRINK |
| 12.486 | 1.50 | 18.73 | 399.90 | 0.05 | 20.39 | 91.8% | 8.3% | PFM | SR SHRINK |
| 12.486 | 1.25 | 15.61 | 399.90 | 0.04 | 17.20 | 90.8% | 7.0% | PFM | SR SHRINK |
| 12.486 | 1.01 | 12.61 | 399.90 | 0.04 | 14.00 | 90.1% | 5.6% | PFM | SR SHRINK |
| 12.487 | 0.76 | 9.49 | 399.90 | 0.03 | 10.80 | 87.9% | 4.2% | PFM | SR SHRINK |

**Note:**

**3.** Operating the converter at or above 20 A max. rated load (shaded region shown in Table 6) requires a fan blowing on the transformer and SR section of the EVB.

## 10.2. Output Voltage Load Regulation

Figure 54 shows the output voltage regulation as a function of varying load for 400 $V_{DC}$ input.

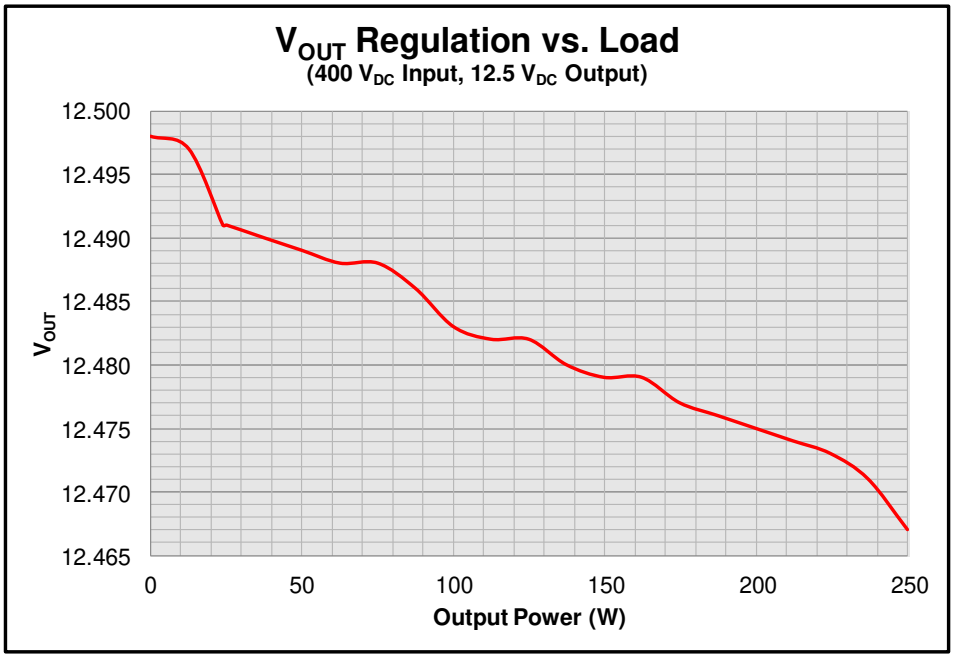



**Figure 54. Output Voltage Regulation vs. Load**

**Table 7. Output Voltage Load Regulation**

| $V_{OUT(MIN)}$ $P_{OUT}$=250 W | $V_{OUT(MAX)}$ $P_{OUT}$=0 W | %Load Reg. |
|---|---|---|
| 12.467 V | 12.498 V | 0.25% |

$$\%Load\ Reg = \frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{V_{OUT(MIN)}}$$

## 10.3. Control to Output Measurements

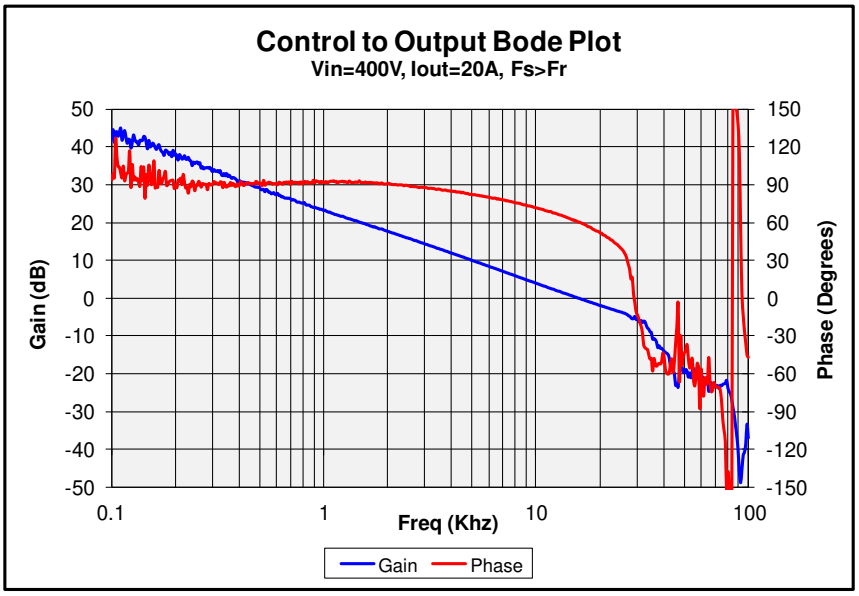



**Figure 55. Above Resonance, Max Load, Measured Gain & Phase**

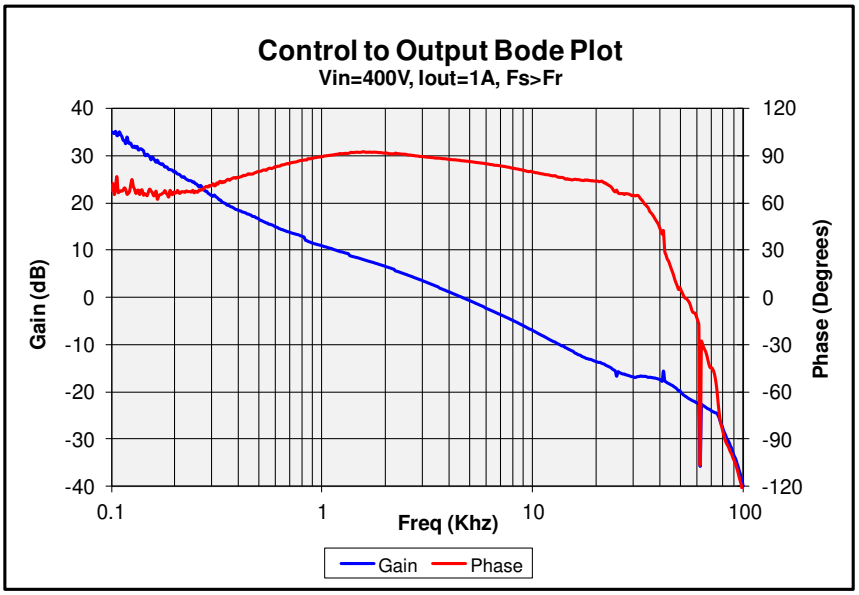



**Figure 56. Above Resonance, Min. Load, Measured Gain & Phase**

**Table 8. Above Resonance, Control to Output Phase Margin, Gain Margin and Bandwidth**

| Above Resonance, $F_S$>$F_R$ (115 kHz>105 kHz), 400 V | | | |
|---|---|---|---|
| | $\Phi_M$ | $G_M$ | BW |
| Max. Load (20 A) | 60º | -5 dB | 15.9 kHz |
| Min. Load (1 A) | 86º | -20 dB | 4.6 kHz |

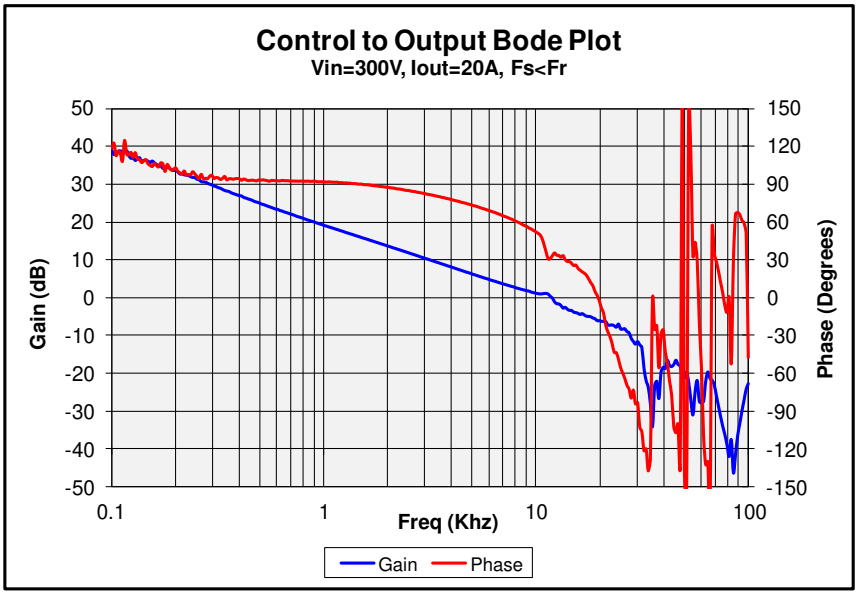



**Figure 57. Below Resonance, Max. Load, Measured Gain & Phase**

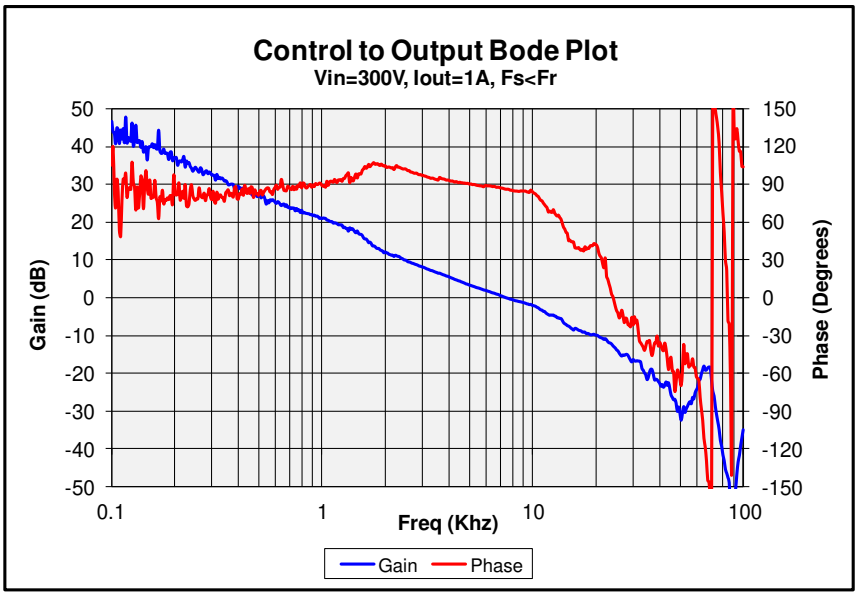



**Figure 58. Below Resonance, Min. Load, Measured Gain & Phase**

**Table 9. Below Resonance, Control to Output Phase Margin, Gain Margin and Bandwidth**

| Below Resonance, $f_S<f_R$ (80 kHz<105 kHz), 300 V | | | |
|---|---|---|---|
| | $\Phi_M$ | $G_M$ | BW |
| Max. Load (20 A) | 32º | -6 dB | 11.8 kHz |
| Min. Load (1 A) | 86º | -13 dB | 7.5 kHz |

## 10.4. Thermal Images

Thermal images of the top side of the EVB are shown while operating from 400 $V_{DC}$ (above resonance) at no load (PWM mode) in Figure 59 and maximum load in Figure 60. As mentioned in section 4.1 and illustrated in Figure 5, a fan is required for prolonged use when loading the converter near or above 20 A. R5 (111°C) is the 0 Ω jumper used to allow the insertion of a current loop for measuring AC output current but the culprit of the highest temperature is really the secondary winding of the LLC transformer, T1.

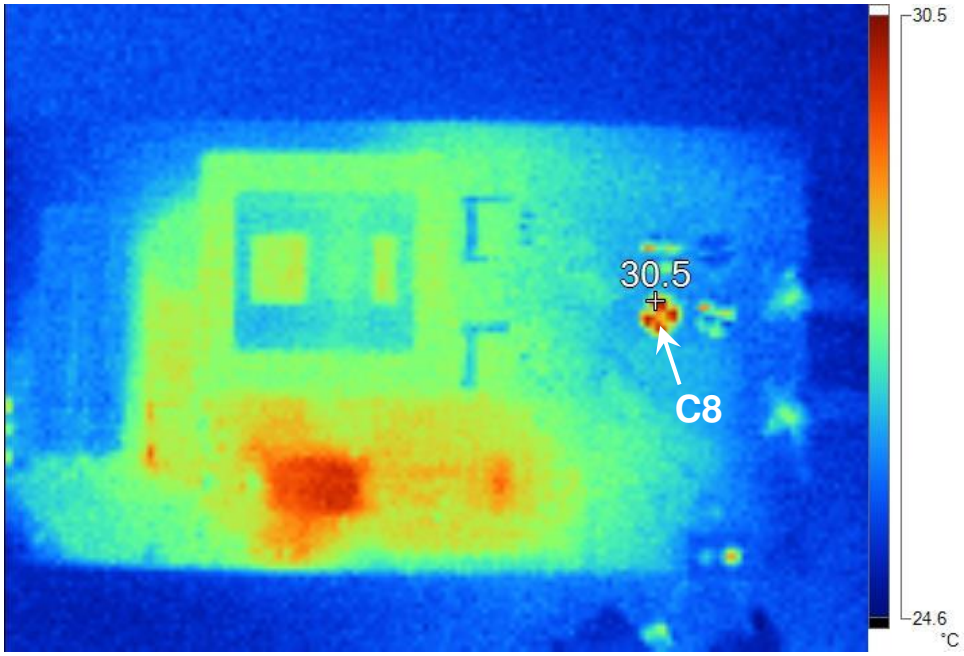



**Figure 59. No Load, Above Resonance, 400 V, 0 A**

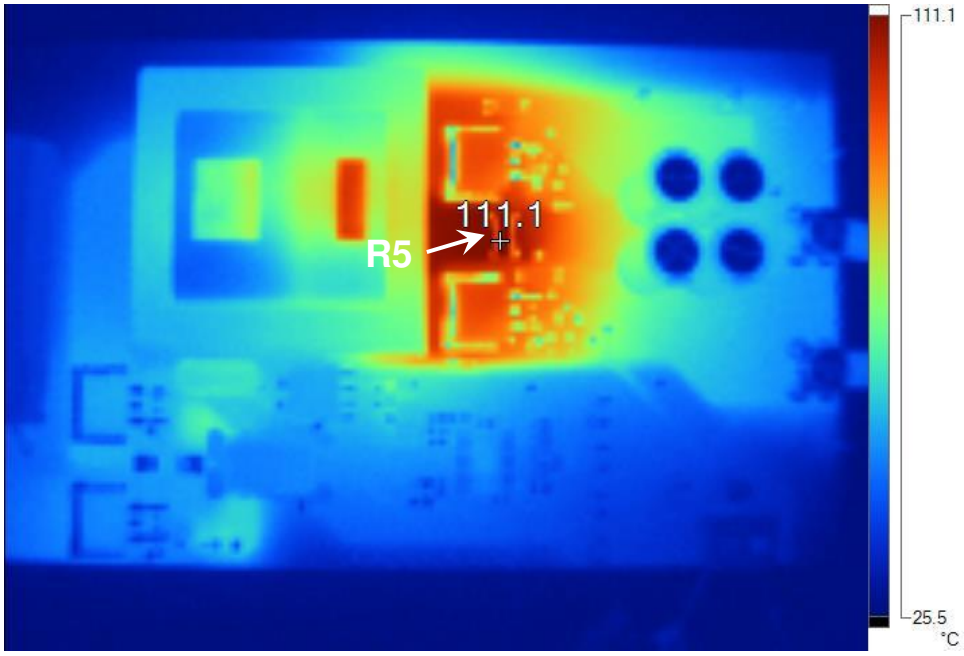



**Figure 60. Max. Load, Above Resonance, 400 V, 20 A**

Thermal images of the top side of the EVB are shown operating from 300 $V_{DC}$ (below resonance) at no load (PWM mode) in Figure 61 and maximum load in Figure 62. As mentioned in section 4.1 and illustrated in Figure 5, a fan is required for prolonged use when loading the converter near or above 20 A. Recommendation for improvement would be to increase PCB copper at D1, R1 junction.

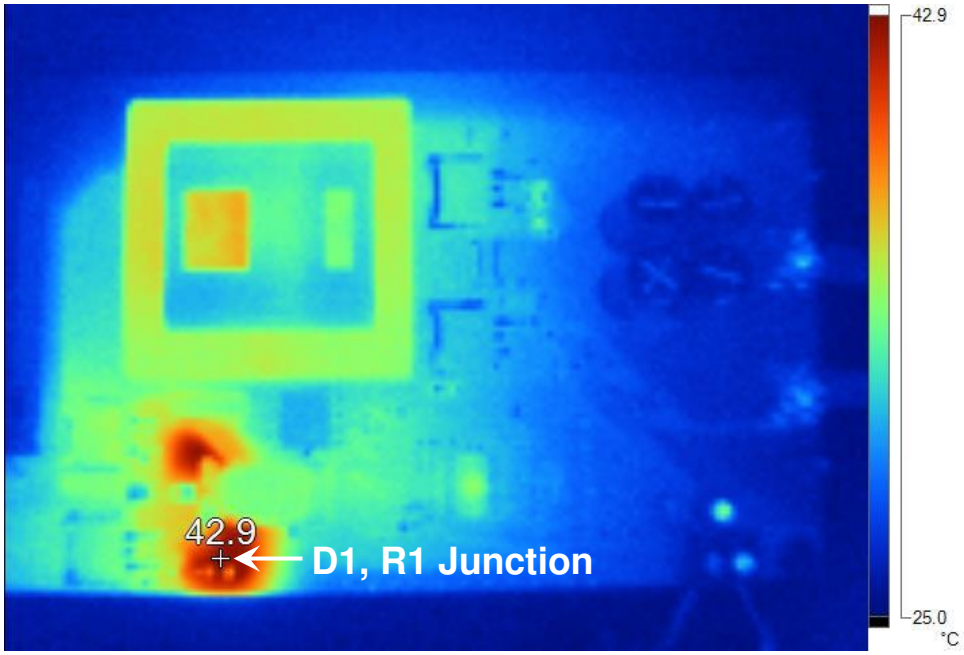



**Figure 61. No Load, Below Resonance, 300 V, 0 A**

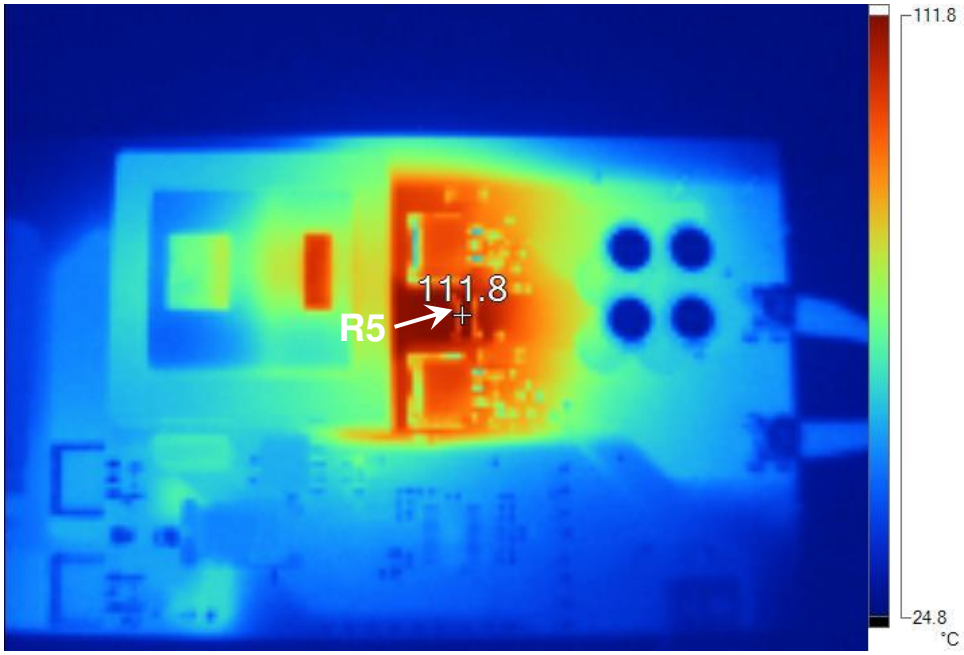



**Figure 62. Max. Load, Below Resonance, 300 V, 20 A**

# 11. Ordering Information

| Orderable Part Number | Description |
|---|---|
| FEBFAN7688_I00250A | FAN7688, 400V to 12.5V, 250W Evaluation Board |

# 12. Revision History

| Date | Revision | Description |
|---|---|---|
| August 2015 | 0.0.1 | Initial release |