

**50V N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET IN SOT23**

**Features and Benefits**

- $BV_{DSS} > 50V$
- $R_{DS(on)} \leq 3.5\Omega @ V_{GS} = 5V$
- Maximum continuous drain current  $I_D = 200mA$
- "Lead Free", RoHS Compliant (Note 1)
- Halogen and Antimony Free. "Green" Device (Note 2)
- Qualified to AEC-Q101 Standards for High Reliability

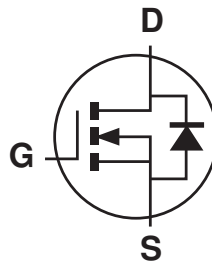
**Mechanical Data**

- Case: SOT-23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matt Tin Finish; Solderable per MIL-STD-202, Method 208
- Weight: 0.008 grams (approximate)

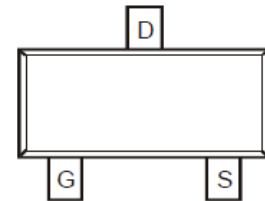
SOT-23



Top View



Device symbol



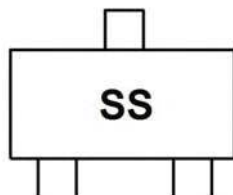
Pin-Out  
Top View

**Ordering Information** (Note 3)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
BSS138TA	SS	7	8	3000

- Notes:
1. No purposefully added lead
  2. Diodes Inc's "Green" policy can be found on our website at <http://www.diodes.com>.
  3. For packaging details, go to our website at <http://www.diodes.com>.

**Marking Information**



SS = Product Type Marking Code

**Maximum Ratings** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

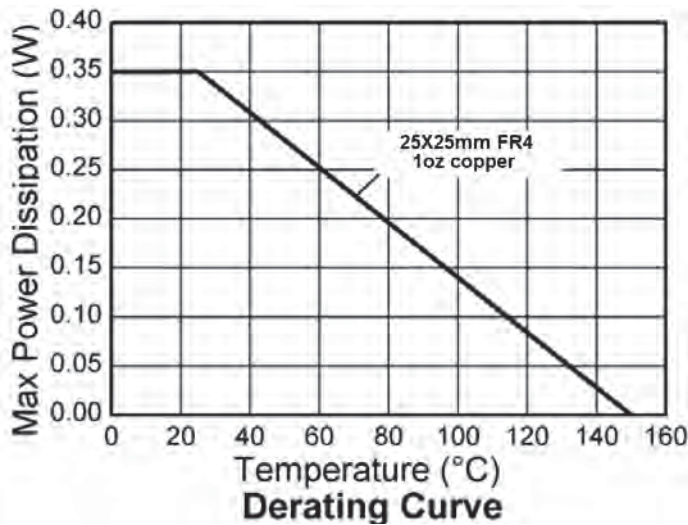
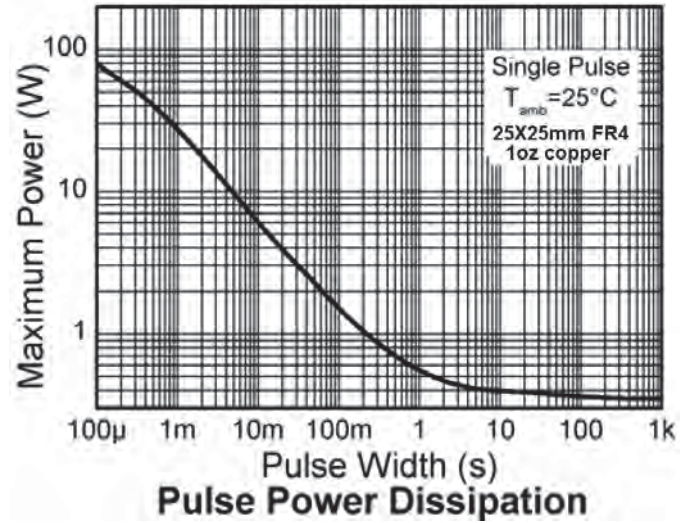
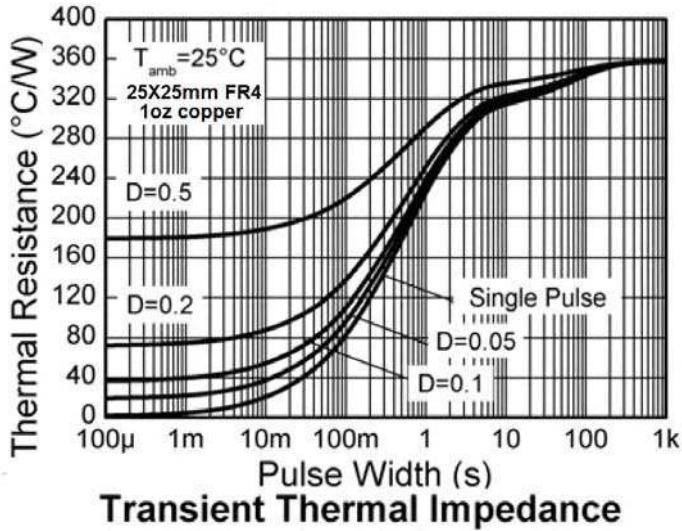
Characteristic	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	50	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	200	mA
Pulsed Drain Current (Note 5)	$I_{DM}$	800	mA

**Thermal Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	$P_D$	350	mW
Thermal Resistance, Junction to Ambient (Note 4)	$R_{\theta JA}$	357	$^\circ\text{C/W}$
Thermal Resistance, Junction to Leads (Note 6)	$R_{\theta JL}$	195	$^\circ\text{C/W}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

- Notes:
4. For a device mounted on 25mm X 25mm X 1.6mm FR-4 PCV with high coverage of single sided 1oz copper, in still air condition.
  5. Device mounted on minimum recommended pad layout test board, 10 $\mu\text{s}$  pulse duty cycle = 1%.
  6. Thermal resistance from junction to solder-point (at the end of the collector lead).

**Thermal Characteristics**

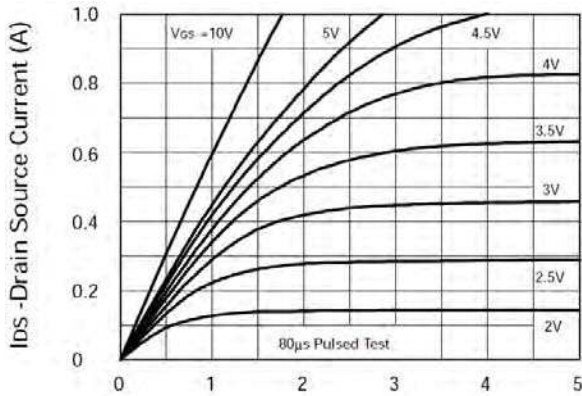


**Electrical Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	50	-	-	V	$V_{GS} = 0V, I_D = 0.25mA$
Zero Gate Voltage Drain Current	$I_{DSS}$	-	-	0.5 5 100	$\mu A$ $\mu A$ nA	$V_{DS} = 50V, V_{GS} = 0V$ $V_{DS} = 50V, V_{GS} = 0V, T_A = 125^\circ\text{C}$ $V_{DS} = 20V, V_{GS} = 0V$
Gate-Source Leakage	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	0.5	-	1.5	V	$V_{DS} = V_{GS}, I_D = 1mA$
Static Drain-Source On-Resistance (Note 7)	$R_{DS(on)}$	-	-	3.5	$\Omega$	$V_{GS} = 5V, I_D = 200mA$
Forward Transconductance (Note 7 & 8)	$g_{fs}$	120	-	-	mS	$V_{DS} = 25V, I_D = 200mA$
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	$C_{iss}$	-	-	50	pF	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$
Output Capacitance	$C_{oss}$	-	-	25	pF	
Reverse Transfer Capacitance	$C_{rss}$	-	-	8	pF	
Turn-On Delay Time (Note 9)	$t_{D(on)}$	-	10	-	ns	$V_{DD} = 30V, I_D = 280mA$
Turn-On Rise Time (Note 9)	$t_r$	-	10	-	ns	
Turn-Off Delay Time (Note 9)	$t_{D(off)}$	-	15	-	ns	
Turn-Off Fall Time (Note 9)	$t_f$	-	25	-	ns	

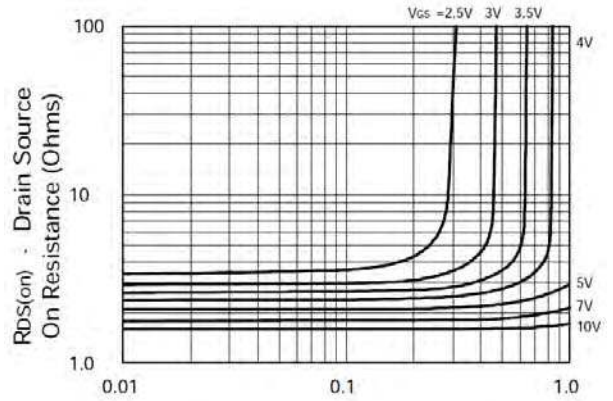
- Notes:**
7. Measured under pulsed conditions. Width = 300 $\mu s$ . Duty cycle  $\leq 2\%$ .
  8. Sample test.
  9. Switching times measured with 50 $\Omega$  source impedance and <5ns rise time on a pulse generator.

**Electrical Characteristics**



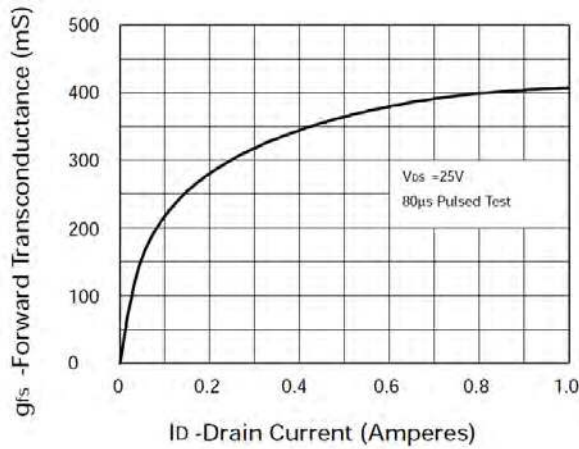
V<sub>DS</sub> - Drain Source Voltage (Volts)

**Saturation Characteristics**

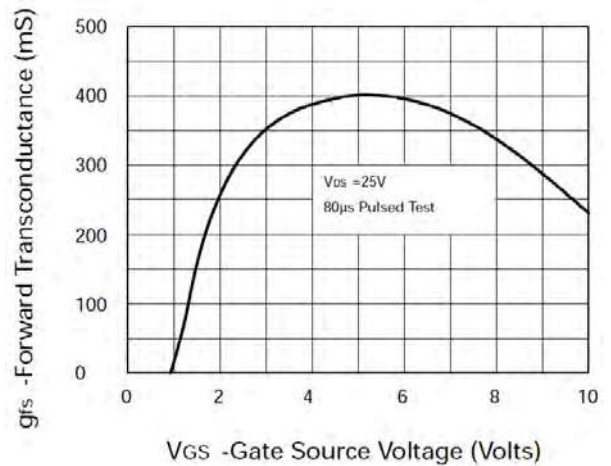


I<sub>D</sub> - Drain Current (Amperes)

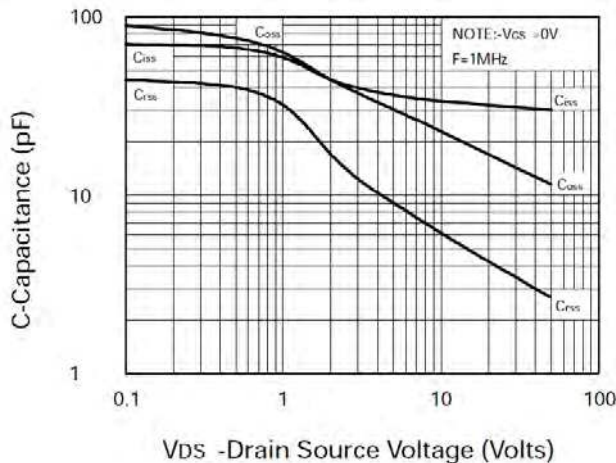
**Typical On Resistance vs. Drain Current**



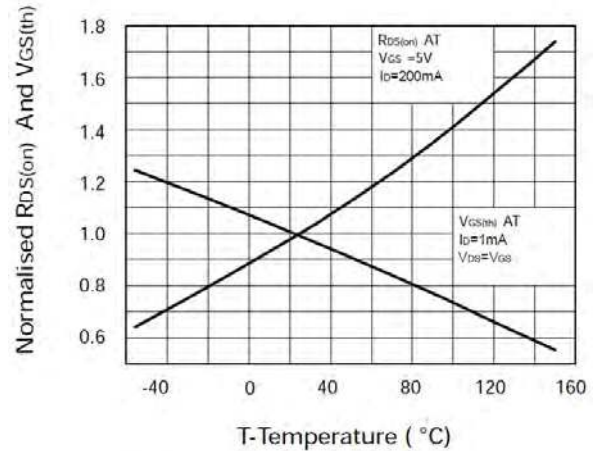
**Typical Transconductance vs. Drain Current**



**Typical Transconductance vs. Gate - Source Voltage**

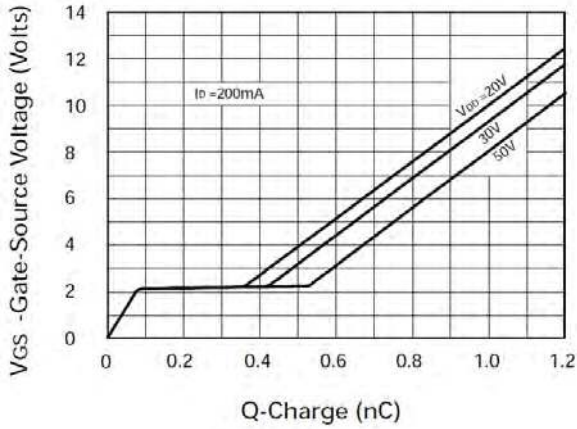


**Typical Capacitance vs. Drain - Source Voltage**

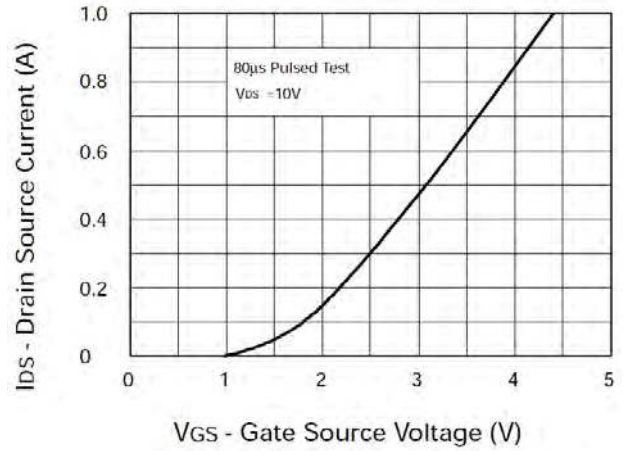


**Normalised R<sub>DS(on)</sub> And V<sub>GS(th)</sub> vs. Temperature**

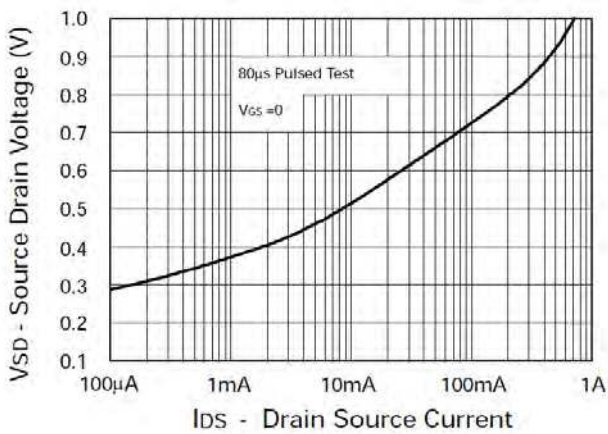
**Electrical Characteristics – (Continuous)**



**Typical Gate Charge vs. Gate-Source Voltage**

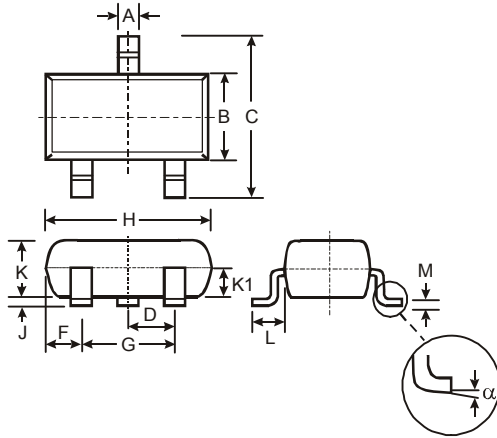


**Typical Transfer Characteristics**



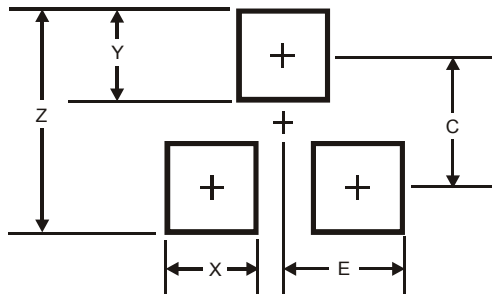
**Typical Diode Forward Voltage**

**Package Outline Dimensions**



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

**Suggested Pad Layout**



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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