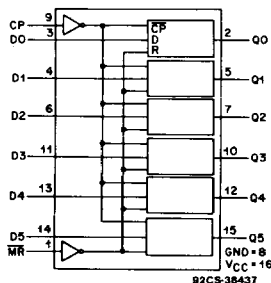


CD54/74AC174 CD54/74ACT174



FUNCTIONAL DIAGRAM

Hex D Flip-Flop with Reset

Type Features:

- Buffered inputs
- Typical propagation delay:
6.4 ns @ $V_{CC} = 5V, T_A = 25^\circ C, C_L = 50 pF$

The RCA CD54/74AC174 and CD54/74ACT174 are hex D flip-flops with reset that use the RCA ADVANCED CMOS technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All six flip-flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a low voltage level independent of the clock.

The CD74AC174 and CD74ACT174 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC174 and CD54ACT174, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- Exceeds 2-kV ESD Protection — MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced Propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- ± 24 mA output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET (MR)	CLOCK CP	DATA D _n	Q _n
L	X	X	L
H		H	H
H		L	L
H	L	X	Q ₀

H = High Level (Steady State)
 L = Low Level (Steady State)
 X = Irrelevant
 = Transition from Low to High level
 Q₀ = Level before the Indicated Steady-State input conditions were established

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	± 50 mA*
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND})	± 100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

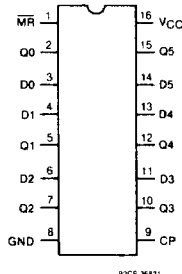
*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}^* : (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A :	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

*Unless otherwise specified, all voltages are referenced to ground.



TOP VIEW
TERMINAL ASSIGNMENT

CD54/74AC174

CD54/74ACT174

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V _{IH}			1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V _{IL}			1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage V _{OH}	V _{IH} or V _{IL}	#, * {	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage V _{OL}	V _{IH} or V _{IL}	#, * {	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
Input Leakage Current I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC174 CD54/74ACT174

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A)- °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V _{IL}		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V _{OZH}	V _{IH} or V _{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OZL}	V _{IH} or V _{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{CC} or GND	5.5	—	±0.1	—	±1	—	±1	µA	
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
Dn, MR	0.5
CP	0.83

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC174

CD54/74ACT174

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t _{SU}	1.5 3.3* 5†	2 2 2	— — —	2 2 2	— — —	ns
Hold Time	t _H	1.5 3.3 5	33 3.7 2.6	— — —	38 4.2 3	— — —	ns
Removal Time MR to CP	t _{REM}	1.5 3.3 5	1.5 1.5 1.5	— — —	1.5 1.5 1.5	— — —	ns
MR Pulse Width	t _W	1.5 3.3 5	44 4.9 3.5	— — —	50 5.6 4	— — —	ns
CP Pulse Width	t _W	1.5 3.3 5	57 6.4 4.6	— — —	65 7.3 5.2	— — —	ns
CP Frequency	f _{MAX}	1.5 3.3 5	9 77 108	— — —	8 68 95	— — —	MHz

*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t _{PLH}	1.5	—	154	—	169	ns
	t _{PHL}	3.3*	4.9	17.2	4.7	18.9	
MR to Qn	t _{PHL}	5†	3.5	12.3	3.4	13.5	
	t _{PLH}	1.5	—	165	—	181	ns
	t _{PHL}	3.3	5.2	18.5	5.1	20.3	
	t _{PHL}	5	3.7	13.2	3.6	14.5	
Power Dissipation Capacitance	C _{PD} §	—	37 Typ.		37 Typ.		pF
Input Capacitance	C _I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$$

where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t _{SU}	5†	2	—	2	—	ns
Hold Time	t _H	5	2.2	—	2.5	—	ns
Removal Time MR to CP	t _{REM}	5	1.5	—	1.5	—	ns
MR Pulse Width	t _w	5	3.5	—	4	—	ns
CP Pulse Width	t _w	5	5.4	—	6.2	—	ns
CP Frequency	f _{MAX}	5	91	—	80	—	MHz

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q _n	t _{PLH} t _{PHL}	5†	3.6	12.6	3.5	14	ns
MR to Q _n	t _{PLH} t _{PHL}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C _{PD} §	—	37 Typ.		37 Typ.		pF
Input Capacitance	C _I	—	—	10	—	10	pF

†min. is @ 5.5 V
 max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
 $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where
 f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

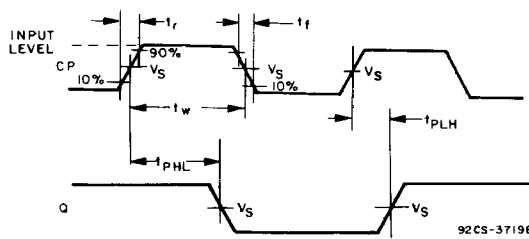


Fig. 1 - Propagation delay times and clock pulse width.

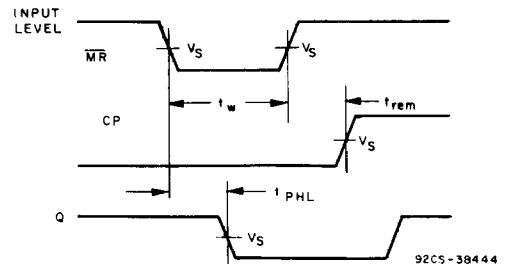


Fig. 2 - Prerequisite and propagation delay times for master reset.

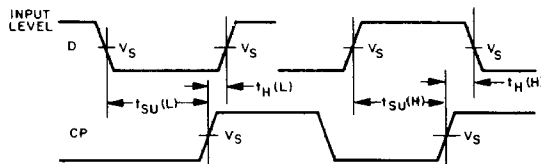
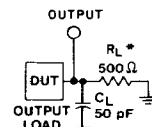


Fig. 3 - Prerequisite for clock.



*FOR AC SERIES ONLY: WHEN
 V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V _{CC}	3 V
Input Switching Voltage, V _S	0.5 V _{CC}	1.5 V
Output Switching Voltage, V _S	0.5 V _{CC}	0.5 V _{CC}