

PHM25NQ10T

TrenchMOS™ standard level FET

Rev. 03 — 11 September 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- SOT96 (SO-8) footprint compatible
- Surface mounted package
- Low thermal resistance
- Low profile.

1.3 Applications

- DC-to-DC primary side
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} \leq 100 \text{ V}$
- $I_D \leq 30.7 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DSon} \leq 30 \text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT685-1 (QLPAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	[1]	
4	gate (g)		
5,6,7,8	drain (d)		
mb	mounting base, connected to drain (d)		

Bottom view MBL585

SOT685-1 (QLPAK)

[1] Shaded area indicates terminal 1 index area.



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHM25NQ10T	QLPAK	Plastic surface mounted package; no leads; 8 terminals.	SOT685

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	30.7	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	19.4	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	60	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

Source-drain diode

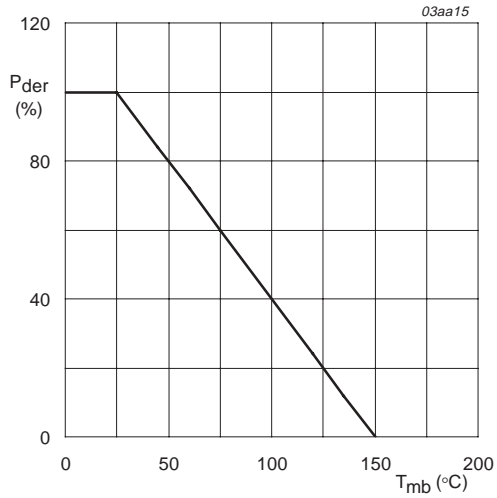
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	30.7	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	60	A

Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 9.9\text{ A}$; $t_p = 0.21\text{ ms}$; $V_{DD} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	170	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 1\text{ A}$; $t_p = 0.021\text{ ms}$; $V_{DD} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$	[1] - [2]	1.70	mJ

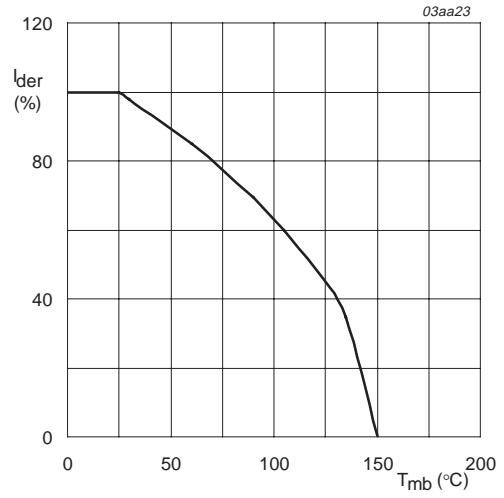
[1] Duty cycle limited by maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



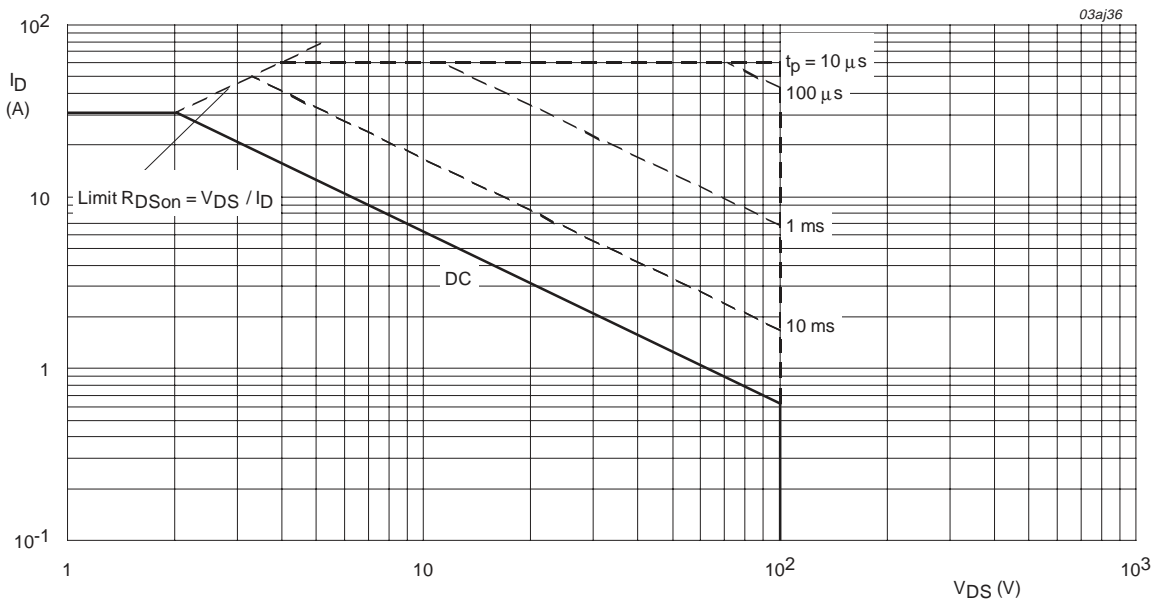
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

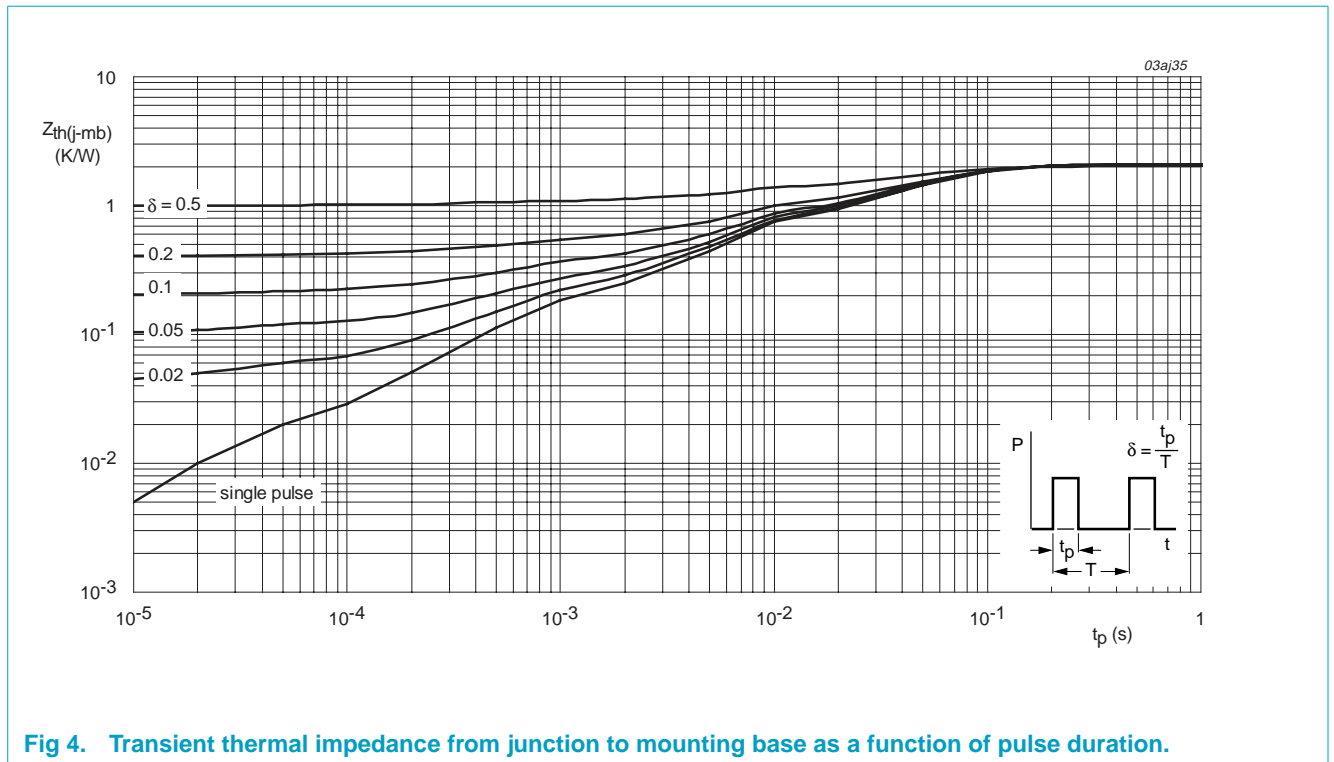


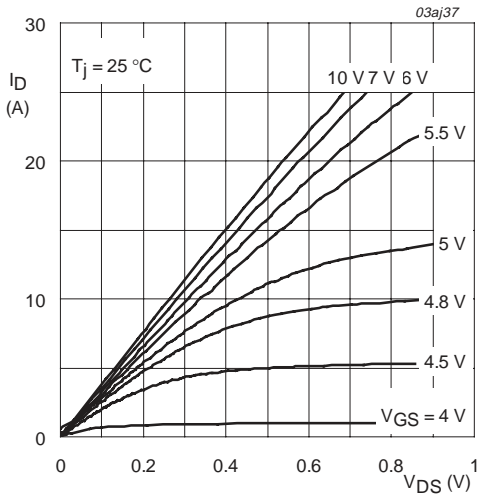
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

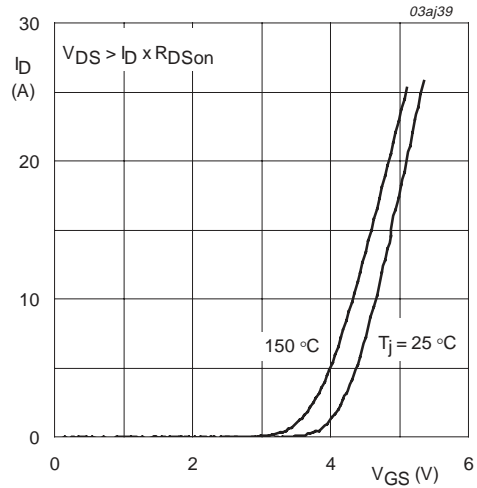
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	100	-	-	V
		$T_j = -55\text{ °C}$	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 80\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 150\text{ °C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ °C}$	-	26.5	30	$\text{m}\Omega$
		$T_j = 150\text{ °C}$	-	58.3	66	$\text{m}\Omega$
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 25\ \text{A}$; $V_{DD} = 50\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 13	-	26.6	-	nC
Q_{gs}	gate-source charge		-	8.4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	6.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 20\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	1800	-	pF
C_{oss}	output capacitance		-	275	-	pF
C_{rss}	reverse transfer capacitance		-	80	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 50\ \text{V}$; $R_L = 56\ \Omega$; $V_{GS} = 10\ \text{V}$; $R_G = 5.6\ \Omega$	-	18	-	ns
t_r	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	42	-	ns
t_f	fall time		-	29	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 10\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 4\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	-	70	-	ns
Q_r	recovered charge		-	95	-	nC



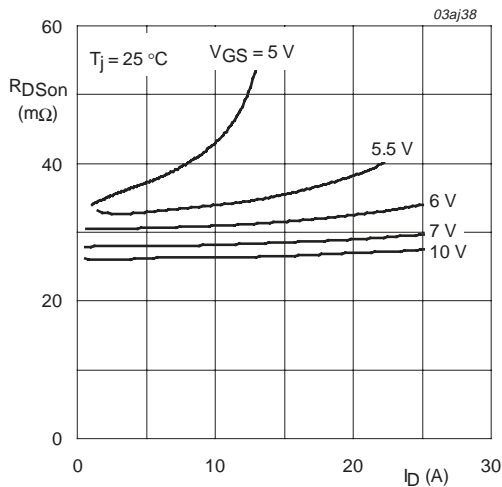
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



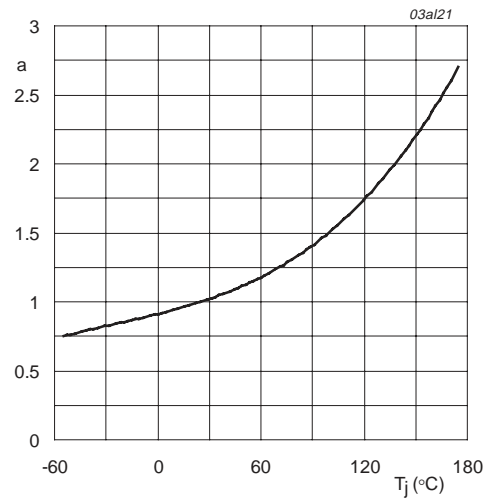
$T_j = 25\text{ °C}$ and 150 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



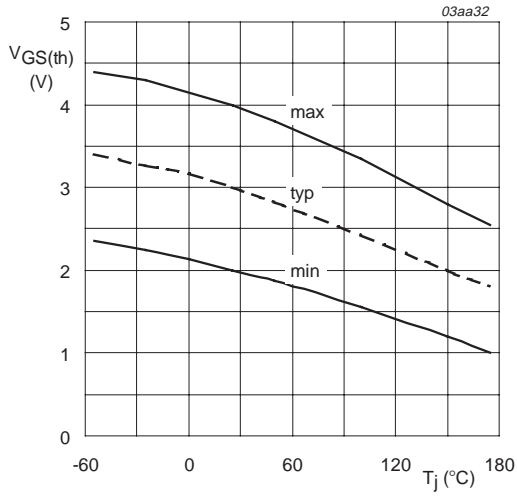
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



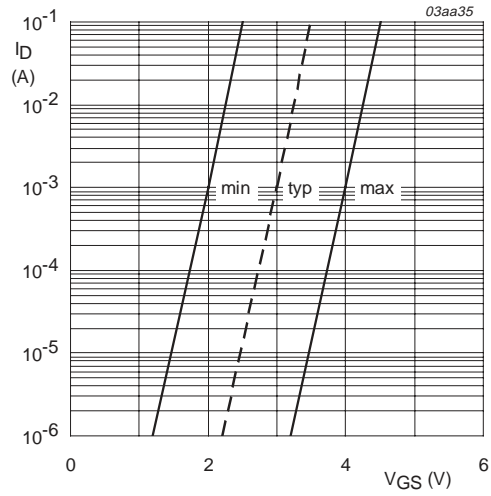
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



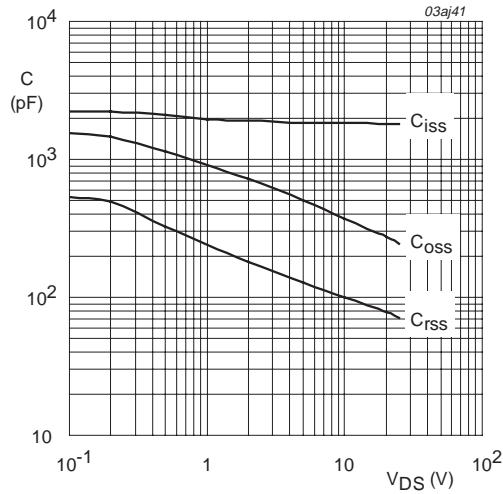
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



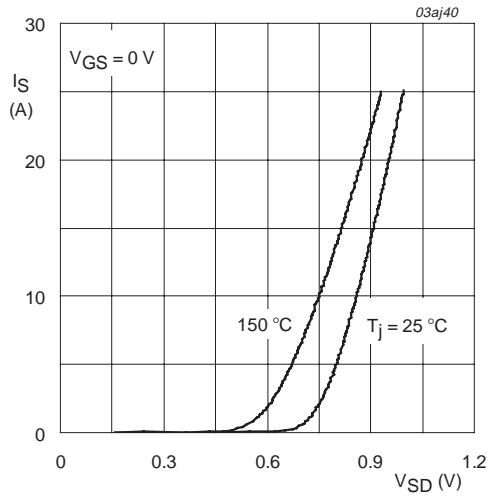
$T_j = 25 \text{ °C}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



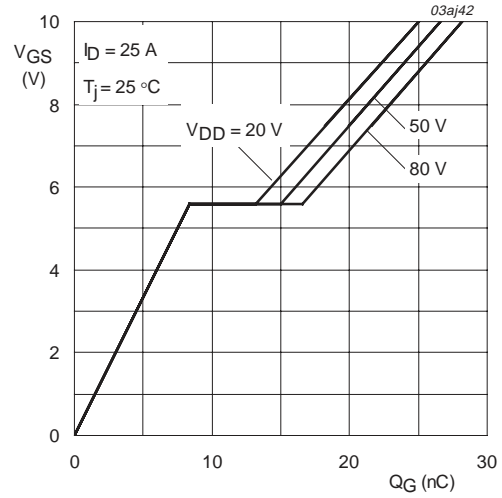
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 25\text{ A}$; $V_{DD} = 20\text{ V}, 50\text{ V}, 80\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 6 x 5 x 0.85 mm

SOT685-1

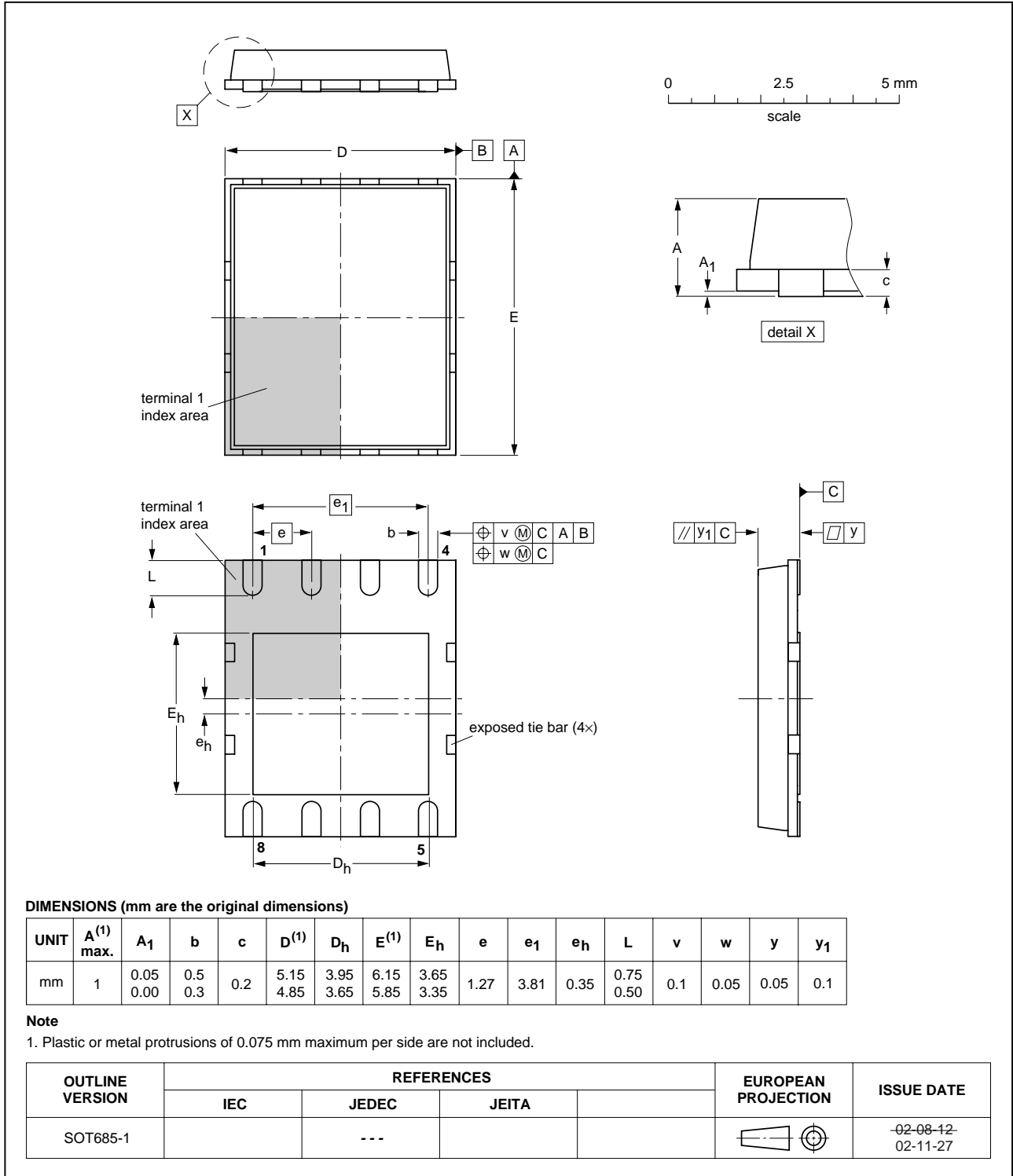
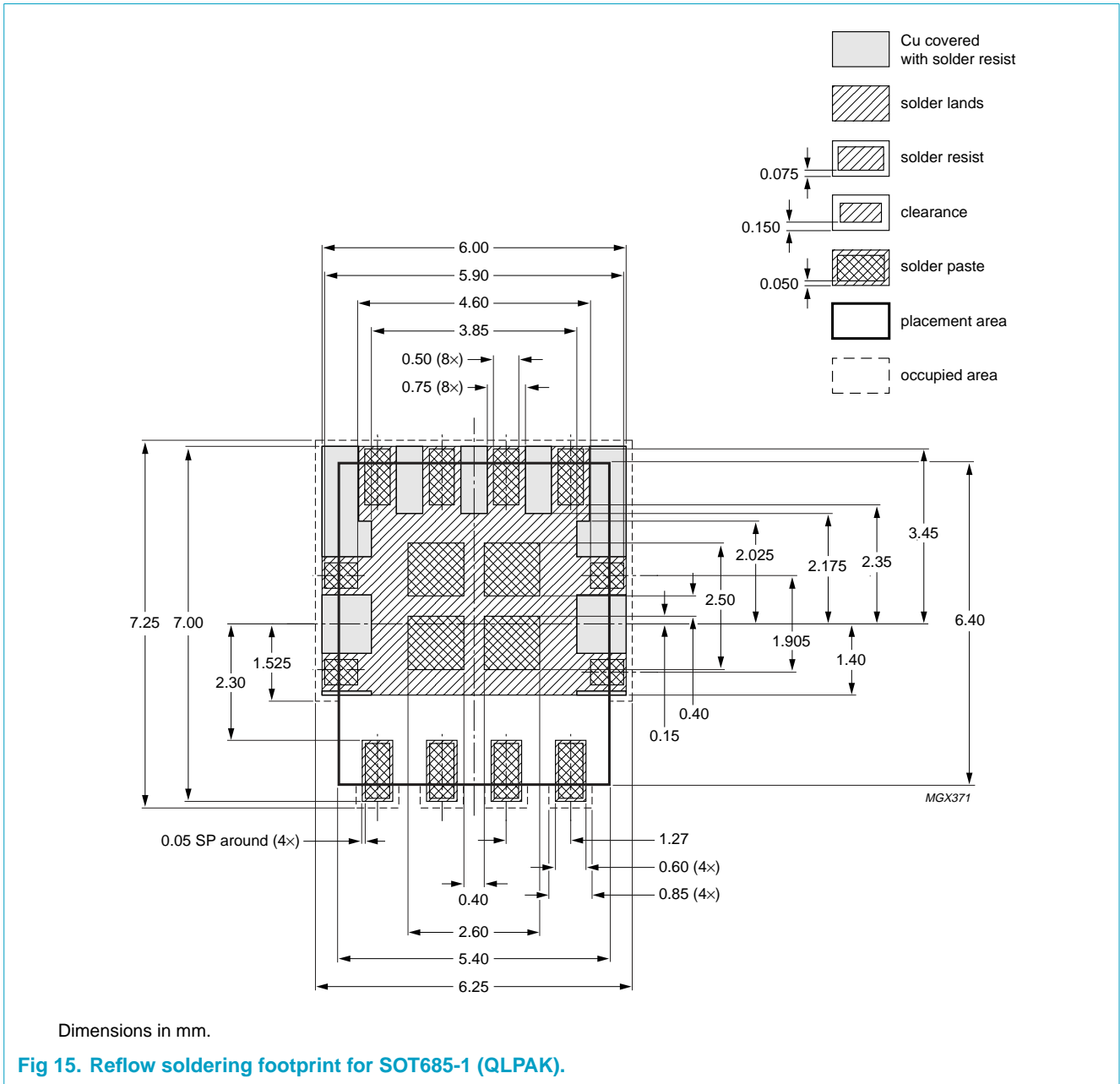


Fig 14. SOT685-1 (QLPAK).

8. Soldering



9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20030911	-	Product data (9397 750 11843) Modifications: <ul style="list-style-type: none"> • Section 3 “Ordering information” Addition of ordering information. • Section 4 “Limiting values” Addition of $E_{DS(AL)S}$. • Section 4 “Limiting values” Addition of $E_{DS(AL)R}$. • Section 8 “Soldering” Addition of soldering footprint.
02	20030129	-	Preliminary data (9397 750 10884) Modifications: <ul style="list-style-type: none"> • Section 5 “Thermal characteristics” Thermal resistance modified. • Section 5 “Thermal characteristics” Figure 4 modified. • Section 4 “Limiting values” Drain current (DC) modified. • Section 4 “Limiting values” Figure 3 modified. • Section 6 “Characteristics” $R_{DSon} T_j = 150\text{ °C}$ modified. • Section 6 “Characteristics” Figure 6 replaced. • Section 6 “Characteristics” Figure 8 modified. • Section 6 “Characteristics” Gate charge test condition and typical values modified. • Section 7 “Package outline” Mounting base repositioned.
01	20020530		Preliminary data (9397 750 09866)

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

Contents

1	Product profile	1
1.1	Description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
5.1	Transient thermal impedance	4
6	Characteristics	5
7	Package outline	9
8	Soldering	10
9	Revision history	11
10	Data sheet status	12
11	Definitions	12
12	Disclaimers	12
13	Trademarks	12

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