



# BUK9215-55A

N-channel TrenchMOS logic level FET

7 April 2014

Product data sheet

## 1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

## 2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

## 3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

## 4. Quick reference data

Table 1. Quick reference data

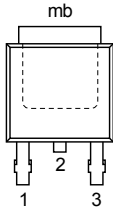
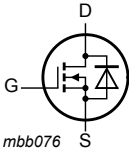
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	55	V
$I_D$	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	[1]	-	62	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	115	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	11	13.6	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	-	16.6	mΩ
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	13	15	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; V_{DS} = 44\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 9</a>	-	20	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 62\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped	-	-	211	mJ

[1] Current is limited by power dissipation chip rating.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;"><b>DPAK (SOT428)</b></p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9215-55A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 7. Limiting values

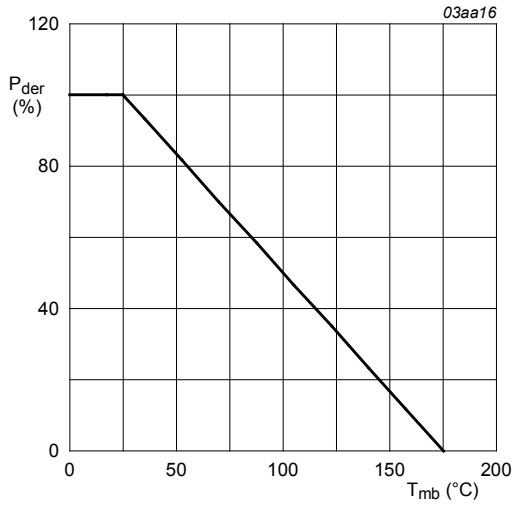
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	55	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	55	V
$V_{GS}$	gate-source voltage			-15	15	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	115	W
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	[1]	-	62	A
			[2]	-	55	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 2</a>	[1]	-	44	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Fig. 3</a>		-	248	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[2]	-	55	A
			[1]	-	62	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	248	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 62\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped		-	211	mJ

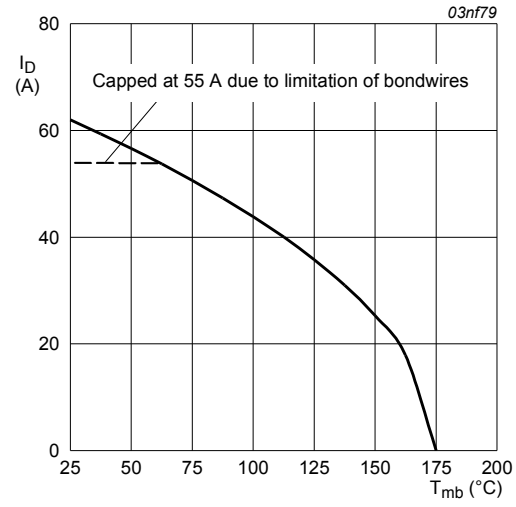
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by bond wires.



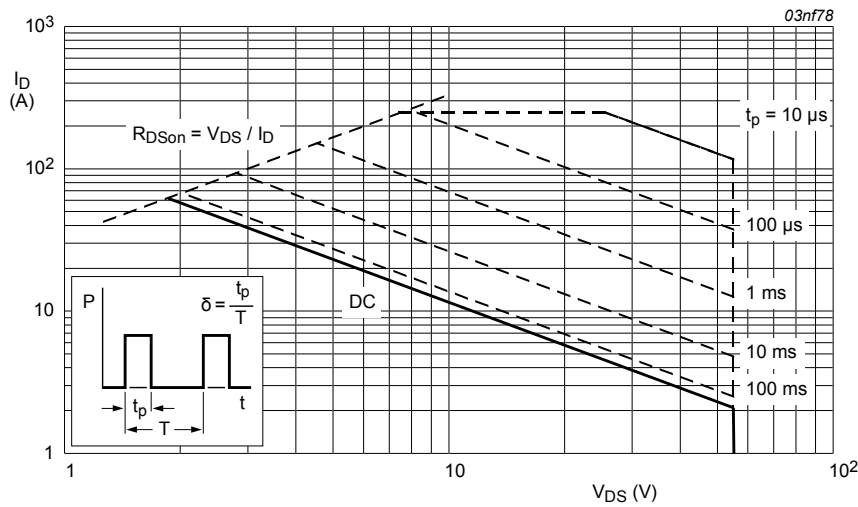
**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$



**Fig. 2. Continuous drain current as a function of mounting base temperature**

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$



**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25^\circ\text{C}; I_{DM}$  is single pulse

### 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	71.4	-	K/W

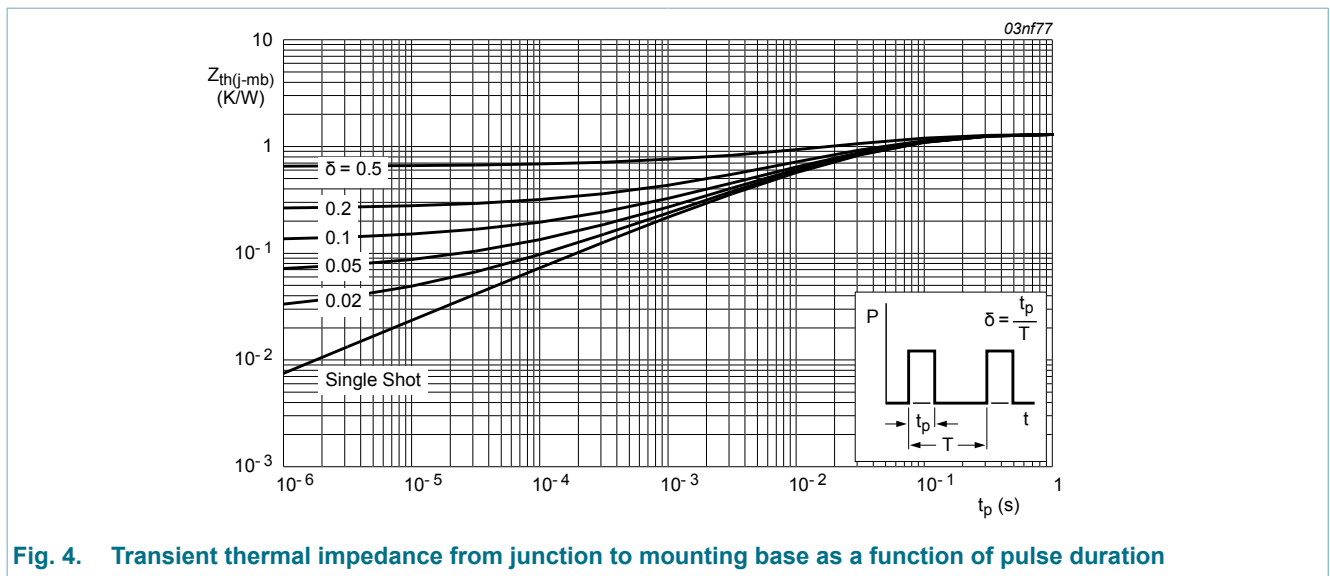


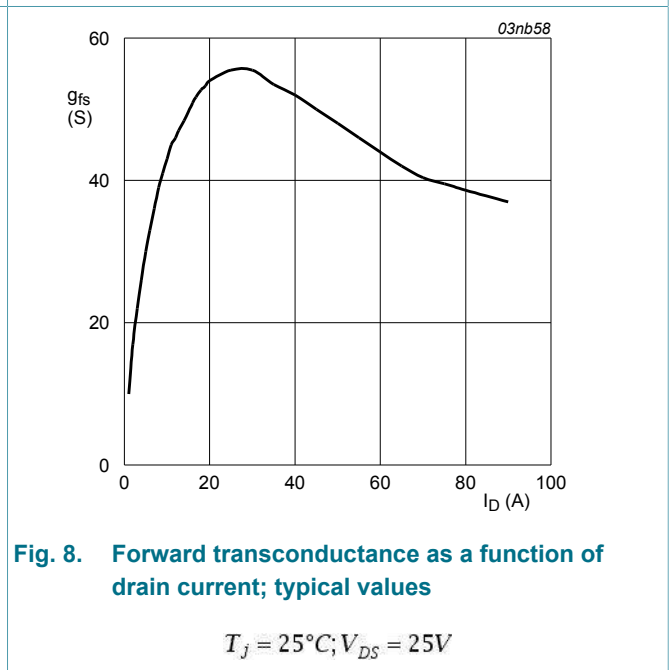
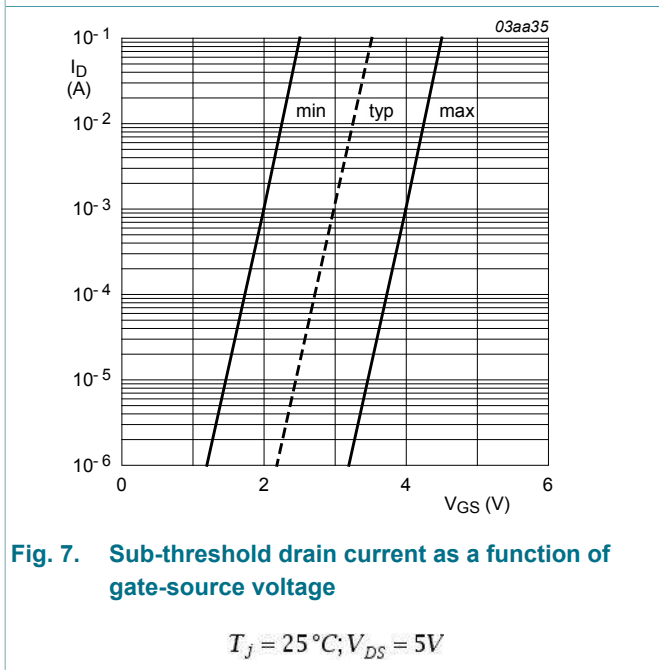
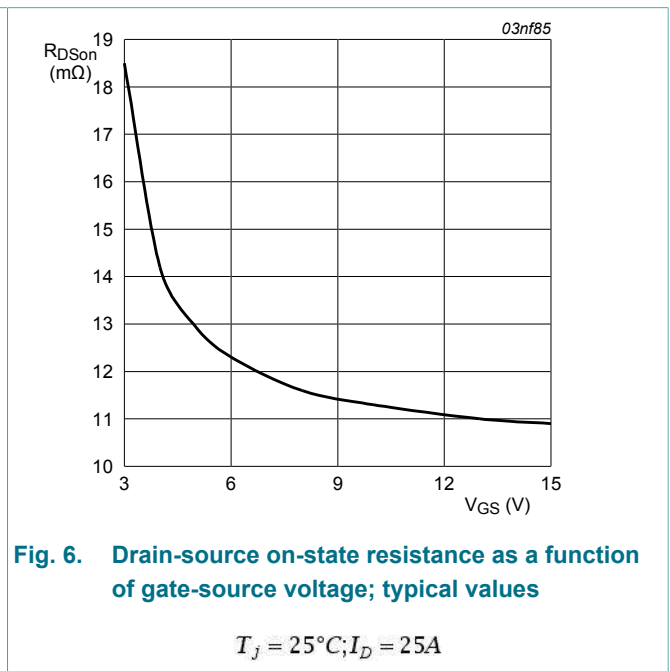
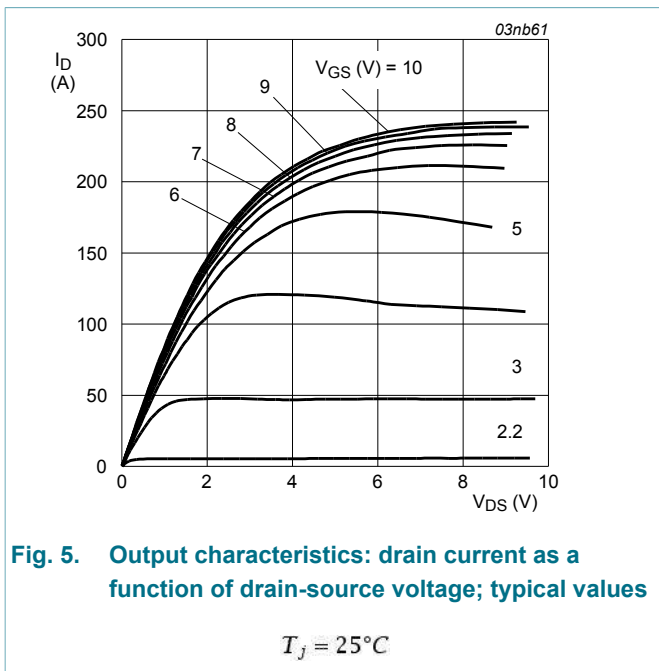
Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

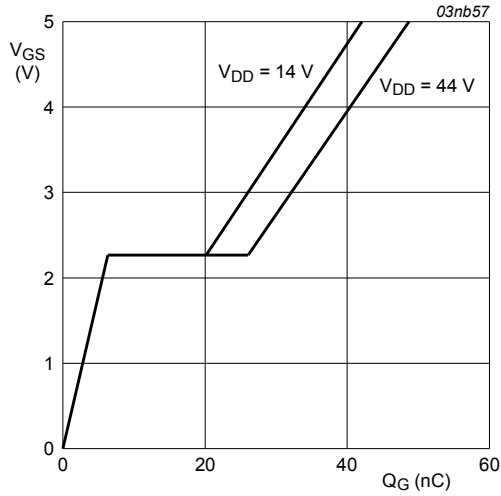
## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	11	13.6	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	16.6	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 11; Fig. 12</a>	-	-	30	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11; Fig. 12</a>	-	13	15	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	48	-	nC
$Q_{GS}$	gate-source charge		-	6	-	nC
$Q_{GD}$	gate-drain charge		-	20	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13</a>	-	2190	2916	pF
$C_{oss}$	output capacitance		-	380	450	pF
$C_{rss}$	reverse transfer capacitance		-	250	344	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	19	-	ns
$t_r$	rise time		-	161	-	ns
$t_{d(off)}$	turn-off delay time		-	138	-	ns
$t_f$	fall time		-	165	-	ns
$L_D$	internal drain inductance	measured from drain to centre of die	-	2.5	-	nH

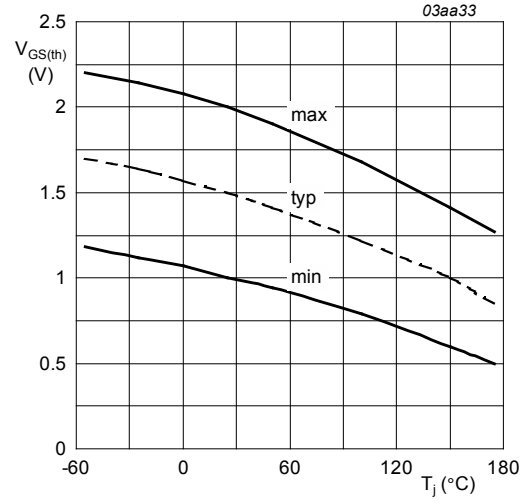
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$L_S$	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 20\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 14	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	51	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	102	-	nC





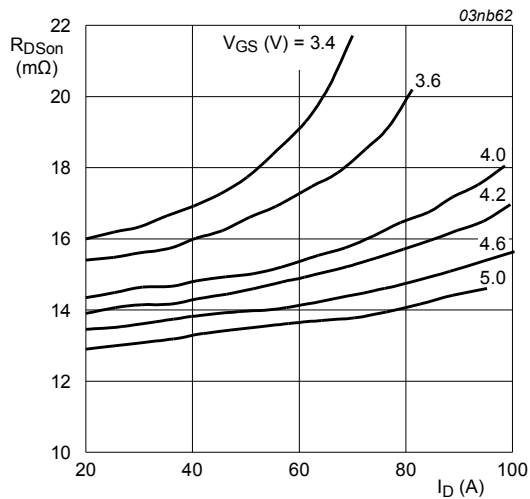
**Fig. 9. Gate-source voltage as a function of turn-on gate charge; typical values**

$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$



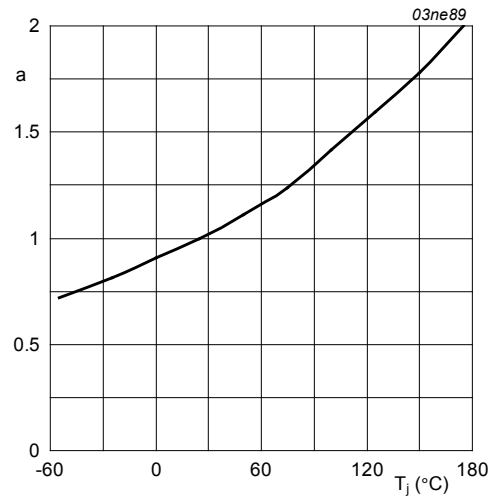
**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$



**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

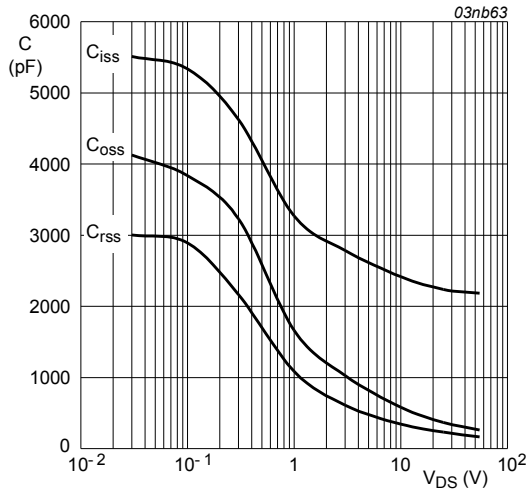
$$T_j = 25^\circ\text{C}$$



**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

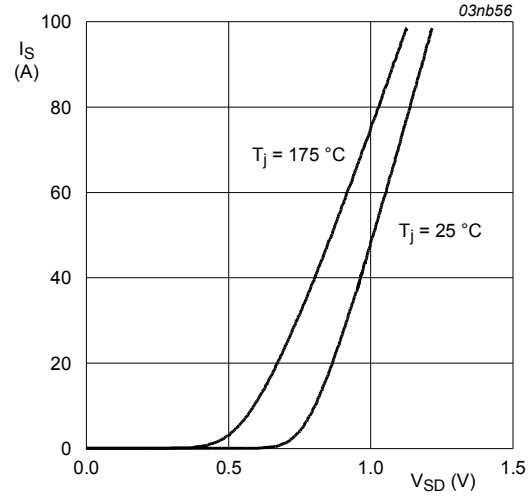
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$





**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0V; f = 1MHz$$

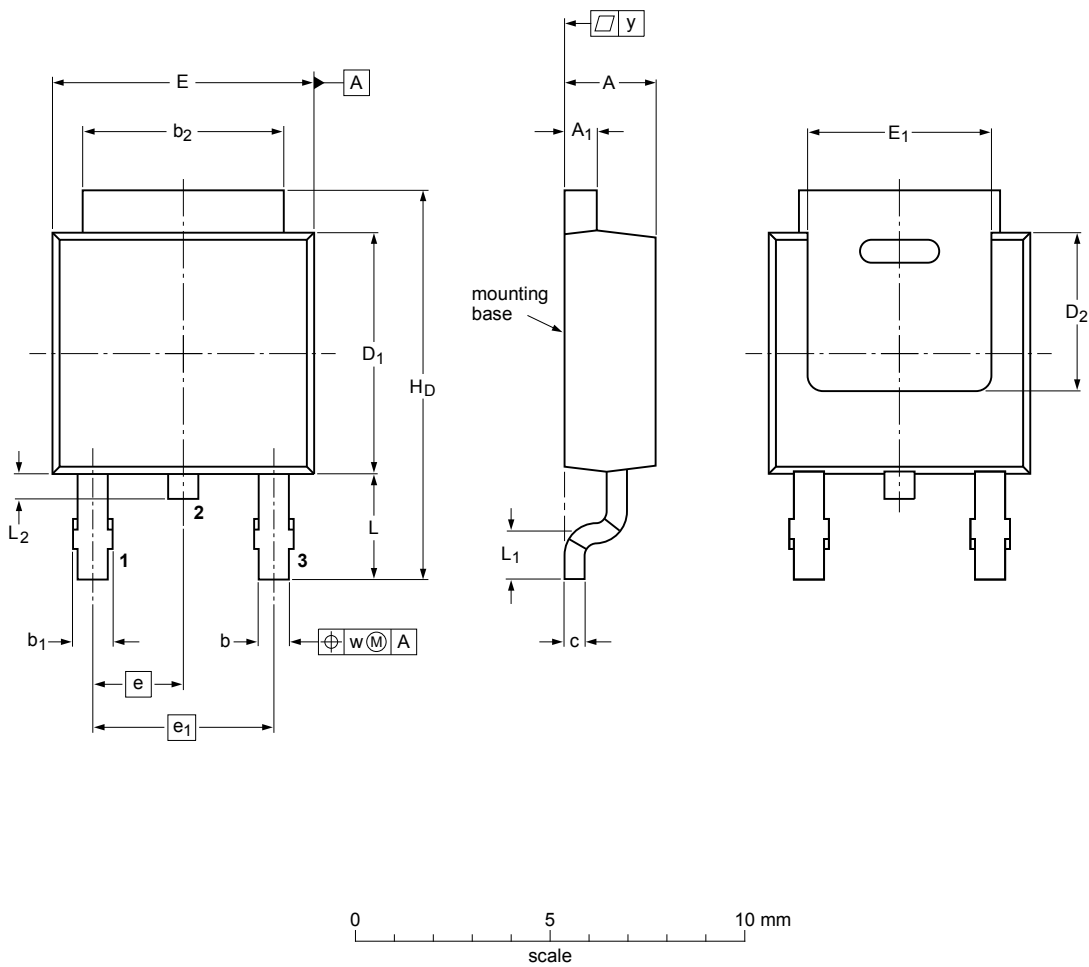


**Fig. 14. Reverse diode current; typical value**

$$V_{GS} = 0V$$

### 10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sub>1</sub>	D <sub>2</sub> min	E	E <sub>1</sub> min	e	e <sub>1</sub>	H <sub>D</sub>	L	L <sub>1</sub> min	L <sub>2</sub>	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT428		TO-252	SC-63		06-02-14 06-03-16

Fig. 15. Package outline DPAK (SOT428)

## 11. Legal information

### 11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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