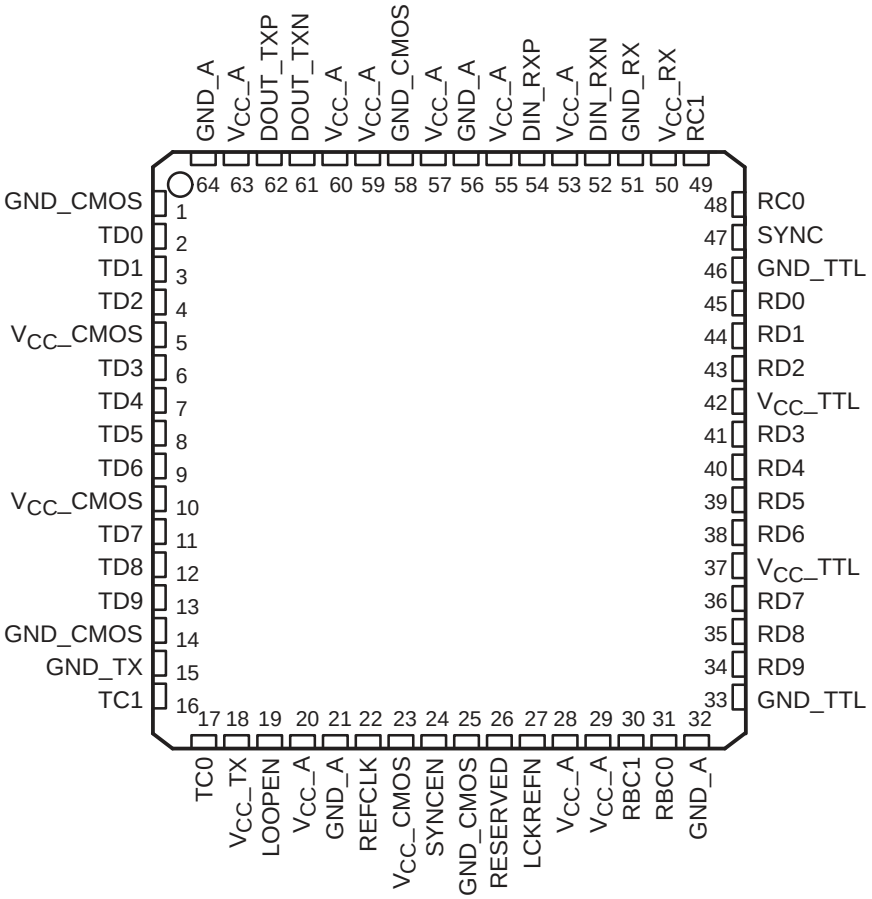
- **1.0625 Gigabits Per Second (Gbps) Fibre Channel Transceiver Compatible With ANSI X3T11 (FC-PH-0)**
- **Designed to Support X3T11 10-Bit I/F Specification**
- **Transmits Serial Data up to 1.0625 Gbps (100 Megabytes Per Second [MBps] of Data Bandwidth)**
- **Operates With 3.3-V Supply Voltage**
- **Interfaces to Electrical Cables/Backplane or with Optical Modules**
- **PECL Voltage Differential Signaling Load, 1 V Typ with 50 Ω – 75 Ω**
- **Receiver Differential Input Voltage 200 mV Minimum**
- **64-Pin Quad Flat Pack With Thermally Enhanced Package**
- **5-V Tolerant I/O Terminals**

description

The SN75FC1000B fibre channel transceiver provides for ultra high-speed bidirectional point-to-point data transmission. This device supports the ANSI X3T11 Fibre Channel standard and the functional and timing requirements of the proposed 10-bit interface specification generated by ANSI X3T11.

PHD OR PJD PACKAGE
(TOP VIEW)



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description (continued)

The intended application of this device is to provide building blocks for developing point-to-point baseband data transmission over controlled-impedance media of approximately 50 Ω to 75 Ω. The transmission media can be printed-circuit board traces, back planes, cables, or fiber optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

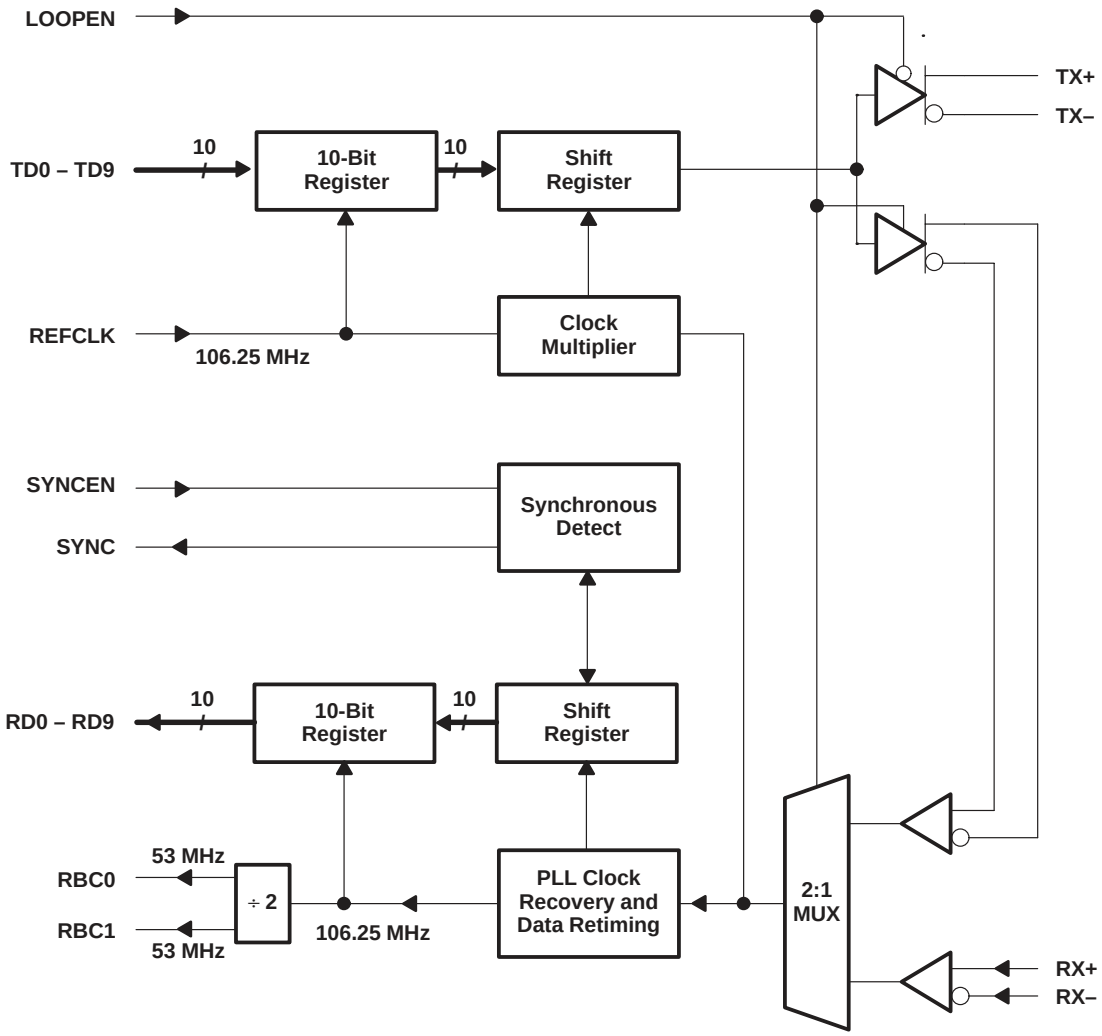
The SN75FC1000B performs the data serialization and deserialization (SERDES) functions for the fibre channel physical layer interface. The transceiver operates at 1.0625 Gbps (typical), providing up to 100 MBps of bandwidth over a copper or optical media interface. The serializer/transmitter accepts 8b/10b parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially nonreturn-to-zero (NRZ) at pseudo-ECL (PECL) voltage levels. The deserializer/receiver extracts clock information from the input serial stream and deserializes the data, outputting a parallel 10-bit data byte. The 10-bit data bytes are output with respect to two receive byte clocks (RBC0, RBC1) allowing a protocol device to clock the parallel bytes in RBC clock rising edges.

The transceiver automatically locks onto incoming data without the need to prelock. However, the transceiver can be commanded to lock to the externally supplied reference clock (REFCLK) as a reset function, if needed.

The SN75FC1000B provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer allowing the protocol device a functional self-check of the physical interface.

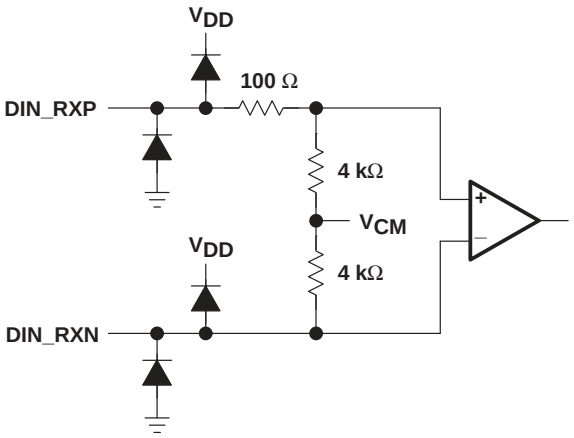
The SN75FC1000B is characterized for operation from 0°C to 70°C.

functional block diagram

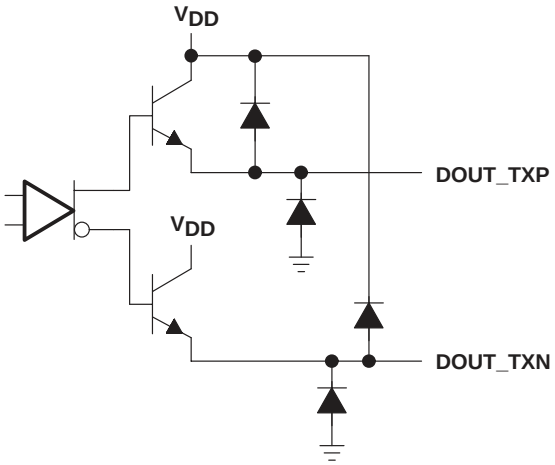


I/O structures

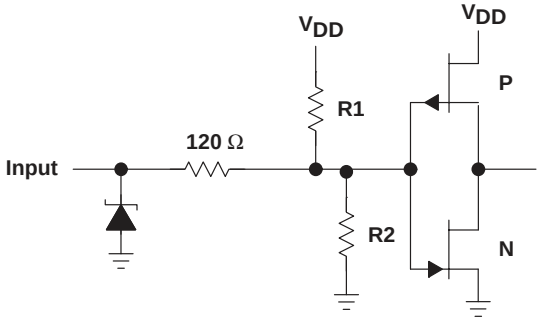
PECL inputs (DIN_RXP, DIN_RXN)



PECL outputs (DIN_TXP, DIN_TXN)

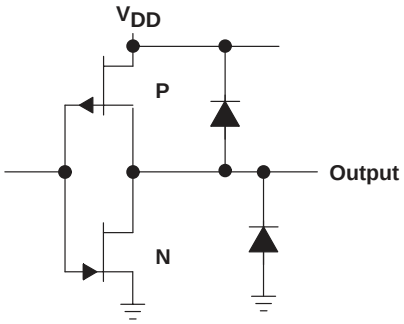


CMOS inputs (TD0 – TD9, LOOPEN, REFCLK, SYNCEN, LCKREFN)



TERMINALS	R1	R2
REFCLK, TD0 – TD9	Open Circuit	Open Circuit
LOOPEN	Open Circuit	400 kΩ
SYNCEN, LCKREFN	400 kΩ	Open Circuit

CMOS outputs (RD0 – RD9, RBC0, RBC1, SYNC)



Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.	TYPE	
I/O and DATA			
DOUT_TXP DOUT_TXN	62 61	Output	Differential output transmit. DOUT_TXP and DOUT_TXN are differential serial outputs that interface to a copper or an optical I/F module. These terminals transmit NRZ data at a rate of 1.0625 Gbps. DOUT_TXP and DOUT_TXN are held static when LOOPEN is high and are active when LOOPEN is low .
DIN_RXP DIN_RXN	54 52	Input	Differential input receive. DIN_RXP and DIN_RXN together are the differential serial input interface from a copper or an optical I/F module. These terminals receive NRZ data at a rate of 1.0625 Gbps and are active when LOOPEN is held low.
LCKREFN	27	Input	Lock to reference. When LCKREFN is asserted low, the receive PLL phase locks to the supplied REFCLK signal. LCKREFN prelocks or resets the receive PLL.
LOOPEN	19	Input	Loop enable. When LOOPEN is high (active), the internal loop-back path is activated. The transmitted serial data is directly routed to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUT_TXP and DOUT_TXN outputs are held static during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
RBC0 RBC1	31 30	Output	Receive byte clock. RBC0 and RBC1 are 53.125-MHz recovered clocks used for synchronizing the 10-bit output data on RD0 – RD9. The 10-bit output data words are valid on the rising edges of RBC0 and RBC1. These clocks are adjusted to half-word boundaries in conjunction with synchronous detect. The clocks are always expanded during data realignment and never slivered or truncated. RBC0 registers bytes 1 and 3 of received data. RBC1 registers bytes 0 and 2 of received data.
RC1, RC0	49 48	Analog	Receive capacitor. RC0 and RC1 are external capacitor connections used for the receiver internal PLL filter. The recommend value for this external capacitor is 2 nF.
RD0 – RD9	45,44,43,41, 40,39,38,36, 35,34	Output	Receive data. These outputs carry 10-bit parallel data output from the transceiver to the protocol layer. The data is referenced to terminals RBC0 and RBC1. Received data byte 0, which contains the K28.5 character, is byte aligned to the rising edge of RBC1. RD0 is the first bit received.
REFCLK	22	Input	Reference clock. REFCLK is an external 106.25 MHz input clock that synchronizes the receiver and transmitter interfaces. The transmitter uses this clock to register the 10-bit input data (TD0..TD9) for serialization. REFCLK is also used as a RX PLL preset or reference when LCKREFN is enabled.
SYNC	47	Output	Synchronous detect. SYNC is asserted high upon detection of the K28.5 character in the serial data path. SYNC is a high level for 1/2 REFCLK period. SYNC pulses are output only when SYNCEN is activated (asserted high).
SYNCEN	24	Input	Synchronous function enable. When SYNCEN is asserted high, the internal synchronization function is activated. When this function is enabled, the transceiver detects the K28.5 character (0011111010 negative beginning disparity) in the serial data stream and realigns data on byte boundaries if required. When SYNCEN is low, serial input data is unframed in RD0 – RD9.
TC1 TC0	16 17	Analog	Transmit capacitor. TC0 and TC1 are external capacitor connections used for the transmitter internal PLL filter. The recommended value of this external capacitor is 2 nF.
TD0 – TD9	2,3,4,6 7,8,9,11 12,13	Input	Transmit data. These inputs carry 10-bit parallel data output from a protocol device to the transceiver for serialization and transmission. This 10-bit parallel data is clocked into the transceiver on the rising edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit.

Terminal Functions (Continued)

TERMINAL			DESCRIPTION
NAME	NO.	TYPE	
POWER			
V_{CC}_A	20,28,29,53 55,57,59,60 63	Supply	Analog power. V_{CC}_A provides a supply reference voltage for the high-speed analog circuits.
V_{CC}_CMOS	5,10,23,	Supply	Digital PECL logic power. V_{CC}_CMOS provides an isolated low-noise power supply for the logic circuits.
V_{CC}_RX	50	Supply	Receiver power. V_{CC}_RX provides a low-noise supply reference voltage for the receiver high-speed analog circuits.
V_{CC}_TTL	42,37	Supply	TTL power. V_{CC}_TTL provides a supply reference voltage for the receiver TTL circuits.
V_{CC}_TX	18	Supply	Transmitter power. V_{CC}_TX provides a low-noise supply reference voltage for the transmitter high-speed analog circuits.
GROUND			
GND_A	21,32,56,64	Ground	Analog ground. GND_A provides a ground reference for the high-speed analog circuits.
GND_CMOS	1,14, 25,58	Ground	Digital PECL logic ground. GND_CMOS provides an isolated low-noise ground for the logic circuits.
GND_RX	51	Ground	Receiver ground. GND_RX provides a ground reference for the receiver circuits.
GND_TTL	33,46	Ground	TTL circuit ground. GND_TTL provides a ground for TTL interface circuits.
GND_TX	15	Ground	Transmitter ground. GND_TX provides a ground reference for the transmitter circuits.
MISCELLANEOUS			
RESERVED	26		Reserved. Internally pulled to GND, leave open or assert low.

detailed description

data transmission

The transmitter registers incoming 10-bit-wide data words (8b/10b encoded data, TD0 – TD9) on the rising edge of REFCLK (106.25 MHz). The reference clock is also used by the serializer, which multiplies the clock by a factor of 10 providing a 1.0625 Gbaud signal that is fed to the shift register. The data is then transmitted differentially at PECL voltage levels. The 8b/10b encoded data is transmitted sequentially bit 0 through 9.

transmission latency

The data transmission latency of the SN75FC1000B is defined as the delay from the initial 10-bit word load to the serial transmission of bit 9. The typical transmission latency is 13 ns.

data reception

The receiver of the SN75FC1000B deserializes 1.0625 Gbps differential serial data. The 8b/10b data (or equivalent) is retimed based on an extracted clock from the serial data. The serial data is then aligned to the 10-bit word boundaries and presented to the protocol controller along with two receive byte clocks (RBC0, RBC1). RBC0 and RBC1 are 180 degrees out of phase and are generated by dividing down the recovered 1.0625 Gbps (531 MHz) clock by 10 providing for two 53-MHz signals. The receiver presents the protocol device byte 0 of the received data valid on the rising edge of RBC1.

NOTE:
This allows the option of byte alignment without the use of the synchronous detection (SYNC) function by the protocol device.

The receiver PLL can lock to the incoming 1.0625 GHz data without the need for a lock-to-reference preset. The received serial data rate (RX+ and RX–) should be 1.0625 Gbps ±0.01% (100 ppm) for proper operation.

data reception (continued)

During a bus error condition or word alignment, the receive byte clocks RBC0 and RBC1 are stretched (never truncated), ensuring that their frequency never exceeds 60 MHz. When the incoming serial data does not meet its frequency requirements, then the receive byte clock frequency is maintained and never exceeds 60 MHz.

receive PLL operation

The receive PLL provides automatic locking to the incoming data. At power up, the maximum initial lock time is 500 μs. The PLL can also be initiated or set to phase lock to the externally supplied reference clock by enabling lock-to-reference (LCKREFN). The lock-to-reference causes the receive PLL to lock to 10× the reference clock (REFCLK) input providing a PLL preset and reset capability.

If during normal operation a transient occurs, which is defined as any arbitrary phase shift in the incoming data and/or a frequency wander of up to 200 ppm, then the PLL recovers lock within 2.4 μs (2500 serial bit times). Any condition exceeding these values is considered a power-up scenario and the PLL recovers lock within 500 μs.

receiver word alignment

The SN75FC1000B uses a 10-bit K28.5 character (comma character) word alignment scheme. The following sections explain how this scheme works and how it realigns itself.

comma character on expected boundary

The SN75FC1000B provides 10-bit K28.5 character recognition and word alignment. The 10-bit word alignment is enabled by forcing SYCNEN high. This enables the function that examines and compares ten bits of serial input data to the K28.5 synchronization character. The K28.5 character is defined in the fibre channel standard as a pattern consisting of 0011111010 (a negative number beginning disparity) with the 7 MSBs (0011111) referred to as the comma character. The K28.5 character was implemented specifically for aligning fibre channel data words. As long as the K28.5 character falls within the expected 10-bit word boundary, the received 10-bit data is properly aligned and data realignment is not required. Figure 1 shows the timing characteristics of RBC0, RBC1, SYNC and RD0 – RD9 while synchronized.

NOTE:
The K28.5 character is valid on the rising edge of RBC1.

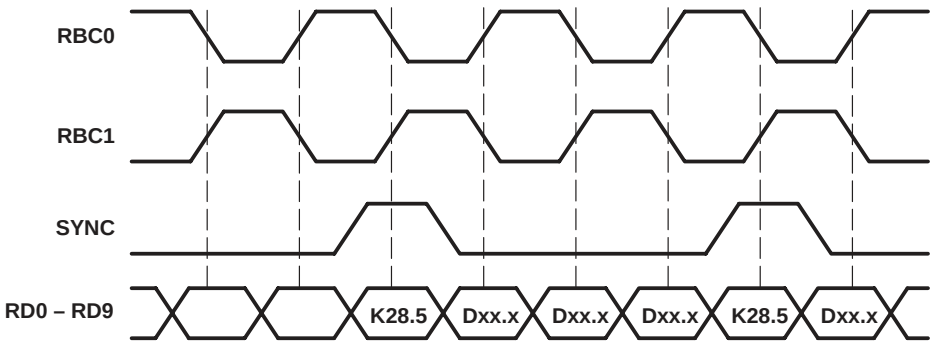


Figure 1. Synchronous Timing Characteristics Waveforms

comma character not on expected boundary

When synchronization is enabled and a K28.5 character straddles the expected 10-bit word boundary, then word realignment is necessary. Realignment or shifting the 10-bit word boundary truncates the character following the misaligned K28.5, but the following K28.5 and all subsequent data is aligned properly as shown in Figure 2. The 10b specification requires that RCLK cycles can not be truncated and can only be stretched or stalled in their current state during realignment. With this design the maximum stretch that occurs is an extra 10 bit times. This occurs during a worst case scenario when the K28.5 is aligned to the falling edge of RBC1 instead of the rising edge. Fibre channel compliant systems transmit a minimum of three consecutively ordered K28.5 data sets between frames and ensure that the receiver sees at least two of K28.5 sets (the fabric is allowed to drop one). Figure 2 shows the timing characteristics of the data realignment.

Systems that do not require framed data can disable byte alignment by tying SYNCEN low.

When a synchronization character is detected the SYNC signal is asserted high and is aligned with the K28.5 character. The duration of the SYNC-signal pulse is equal to the duration of the data which is half an RCLK period.

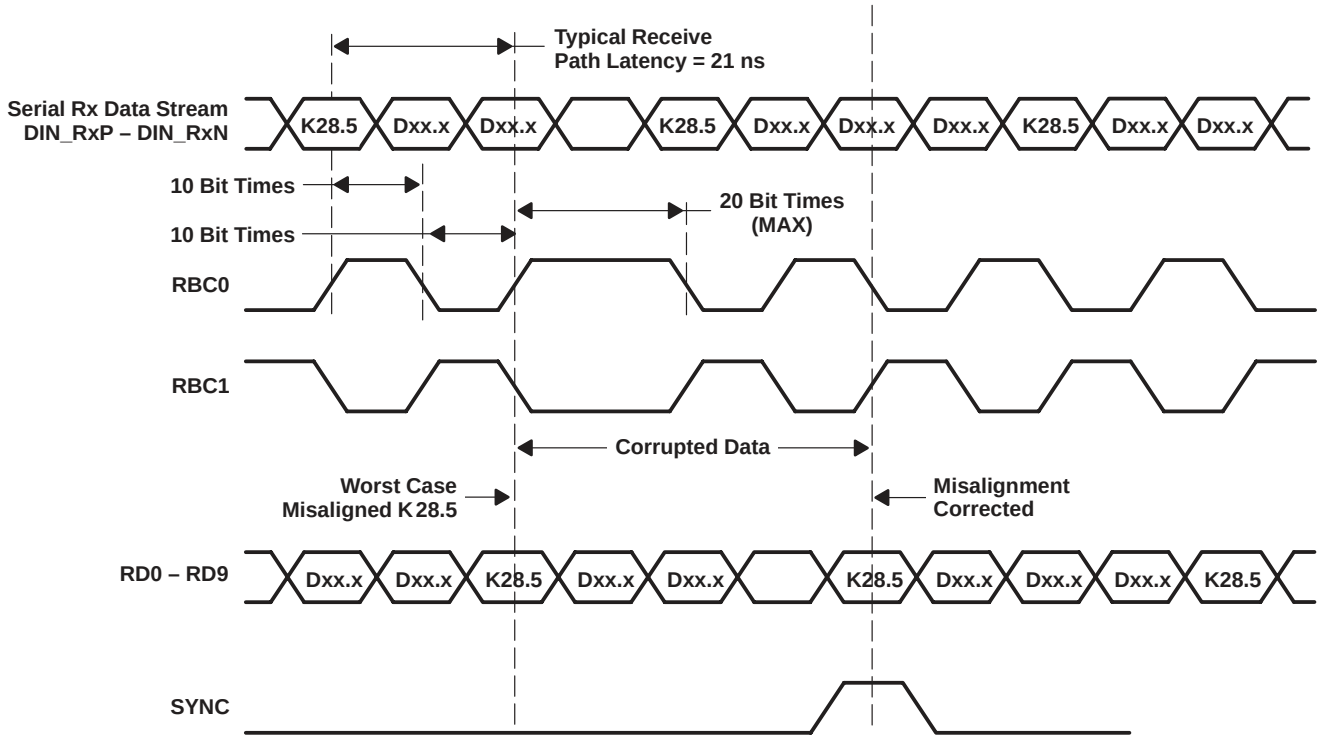


Figure 2. Word Realignment Timing Characteristics Waveforms

data reception latency

The serial-to-parallel data latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RD0 received as first bit. The receive latency is typically 21 ns.

loop-back testing

The transceiver can provide a self-test function by enabling (LOOPEN to high level) the internal loop-back path. Enabling LOOPEN causes serially transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. The external differential output is held in a static state during loop-back testing.

absolute maximum ratings†

Supply voltage, V_{CC} (see Note 1) . . . . . –0.5 to 4 V
Input voltage, V_I (TTL, PECL) . . . . . –0.5 to 4 V
Input voltage, V_I (I/O Terminals) . . . . . –0.5 to 5.5 V
Output current I_O (TTL) . . . . . 50 mA
Output current I_O (PECL) . . . . . –50 mA
Voltage range at any terminal . . . . . –0.5 to V_{CC} + 0.5 V
Electrostatic discharge, 5-V tolerant terminals (see Note 2) . . . . . Class 1, A:1 kV, B:150 V
Electrostatic discharge, all other terminals (see Note 2) . . . . . Class 1, A:2 kV, B:200 V
Characterized free-air operating temperature range . . . . . 0°C to 70°C
Storage temperature . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground.
2. This parameter is tested in accordance with MIL-PRF-38535.

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3.14	3.3	3.47	V
Supply current, I_{CC} (static)	Static pattern†		160	250	mA
Power dissipation, P_D (static)	Outputs open, (static pattern)†		530	875	mW
Supply current, I_{CC} (dynamic)	K28.5		230	310	mA
Power dissipation, P_D (dynamic)	Outputs open, (K28.5)		760	1085	mW
Operating free-air temperature, T_A		0		70	°C

† Power (static pattern) = 106.25 MHz to receiver and 5 ones and 5 zeros to transmitter.

reference clock (REFCLK) timing requirements over recommended operating conditions (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Frequency			106.25		MHz
Accuracy		–100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Random and deterministic			40	ps

† This clock should be crystal referenced to meet the requirements of the this table. The maximum rate of frequency change specified is valid after 10 seconds from power on.

electrical characteristics over recommended operating conditions (unless otherwise noted)

TTL Signals: TD0 – TD9, REFCLK, LOOPEN, SYNCEN, SYNC, RD0 – RD9, RBC0, RBC1, LCKREFN

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = –400 µA	2.4	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 1 mA		0.25	0.4	V
V_{IH}	High-level input voltage			2		5.5	V
V_{IL}	Low-level input voltage					0.8	V
I_{IH}	Input high current		V_{CC} = MAX, V_I = 2.4 V			40	µA
		REFCLK	V_{CC} = MAX, V_I = 2.4 V			900	µA
I_{IL}	Input low current		V_{CC} = MAX, V_I = 0.4 V	–40			µA
		REFCLK	V_{CC} = MAX, V_I = 0.4 V	–900			µA
c_i	Input capacitance					4	pF

TRANSMITTER SECTION

differential electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential driver output voltage (peak-to-peak)	R_L = 75 Ω, See Figure 3	1200		2200	mV
		R_L = 50 Ω, See Figure 3	1200		2200	
V_{OC}	Driver common-mode output voltage	R_L = 75 Ω		2100		mV

differential switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Serial data deterministic jitter (peak-to-peak)	Differential output jitter			75	ps
	Serial data total jitter (peak-to-peak)	Differential output jitter			197	ps
t_{r3}	Differential signal rise time (20% to 80%)	R_L = 75 Ω, C_L = 5 pF, See Figure 3			300	ps
t_{f3}	Differential signal fall time (20% to 80%)				300	ps

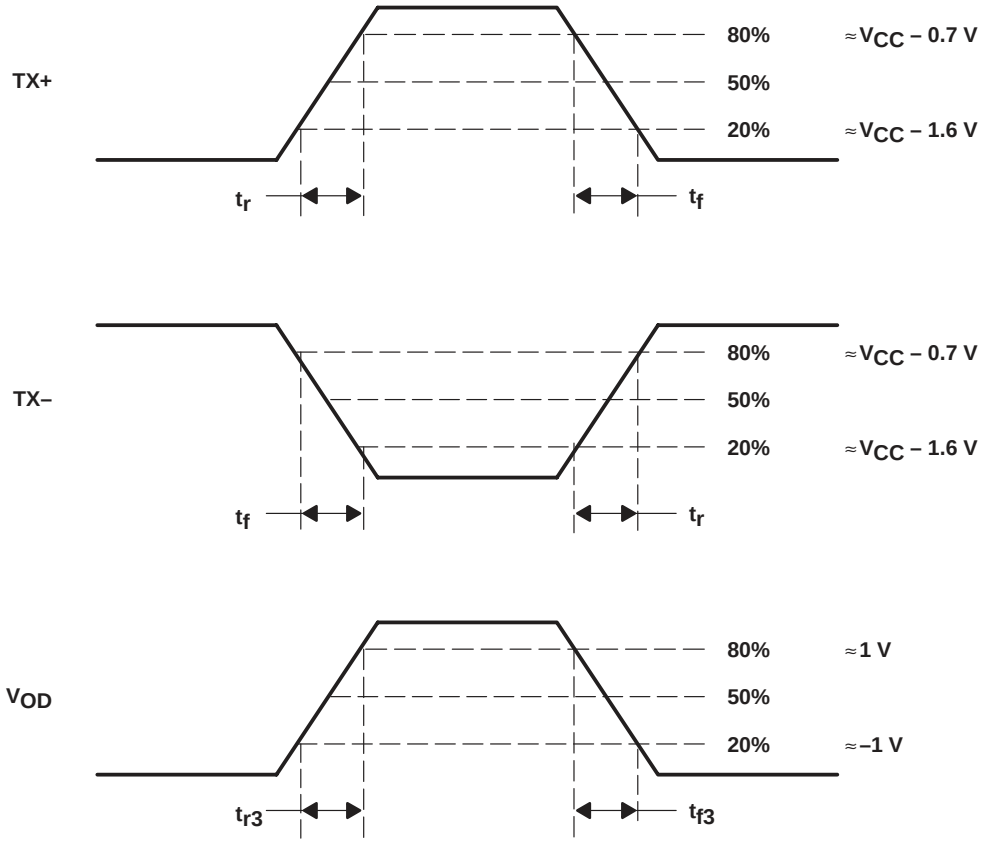


Figure 3. Differential and Common-mode Output Voltage Definitions

TRANSMITTER SECTION

transmitter timing requirements over recommended operating conditions (unless otherwise noted)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{su1}	Setup time, TD0 – TD9 valid to REFCLK ↑	See Figure 4	2			ns
t_{h1}	Hold time, REFCLK ↑ to TD0 – TD9 invalid	See Figure 4	1.5			ns
	Parallel-to-serial data latency			13		ns

transmit interface timing

The transmit interface is defined in the 10 b specification as the 10-bit parallel data input to the physical layer for serial transmission. The timing values are specified from REFCLK midpoint to valid input signal levels or from valid input signal levels to REFCLK midpoint.

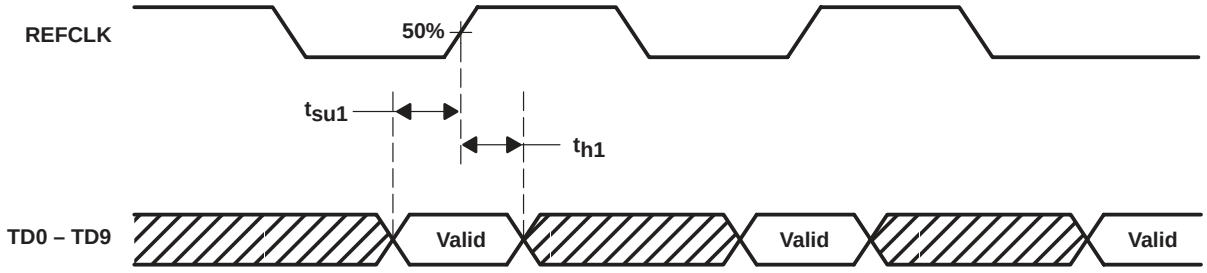


Figure 4. Transmit 10-Bit Interface Timing Waveforms

RECEIVER SECTION

differential electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{ID}\|$	Differential input voltage		200		1300	mV

receiver and phase-locked loop performance characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT†
Jitter tolerance (input data eye closure)	See FC-PH-0 specification			70%	UI
Data acquisition lock time	From power up			500	us
Data relock time	From synchronization loss			2500	ns

† UI is the unit interval of a single bit (941 ps).

receive clock timing requirements over recommended operating condtions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Clock frequency, RCLK (0)			53.125		MHz
f_{clk}	Clock frequency, RCLK (1) (180 deg out of phase with RCLK (0))			53.125		MHz
t_{r4}	Data rise time	See Figure 5	0.7		4	ns
t_{f4}	Data fall time	See Figure 5	0.7		4	ns
t_{r5}	Rise time, single-ended output signal on RCLK	See Figure 5	0.7		2	ns
t_{f5}	Fall time, single-ended output signal on RCLK	See Figure 5	0.7		2	ns
	Duty cycle, RCLK		40%		60%	
$t_{(skew)}$	Skew time, RCLK(1) ↑ to RCLK(0) ↑	See Figure 6	8.9	9.4	9.9	ns
t_{su2}	Setup time, RD0 – RD9 valid to RCLK(0) ↑	See Figure 6	3			ns
t_{su3}	Setup time, RD0 – RD9 valid to RCLK(1) ↑	See Figure 6	3			ns
t_{su4}	Setup time, RCLK(1) ↑ to RD0 – RD9 invalid	See Figure 6	1.5			ns
t_{su5}	Setup time, RCLK(0) ↑ to RD0 – RD9 invalid	See Figure 6	1.5			ns
	Serial-to-parallel data latency			21		ns

RECEIVER SECTION

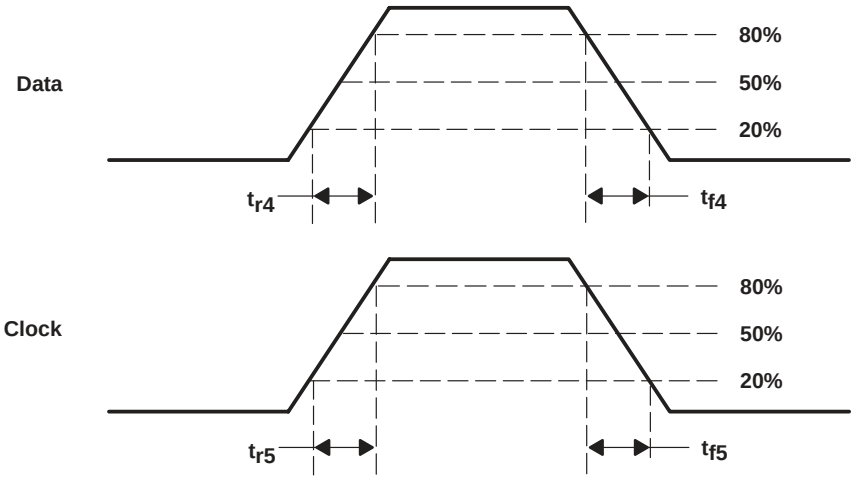


Figure 5. Receiver Data Measurement Levels

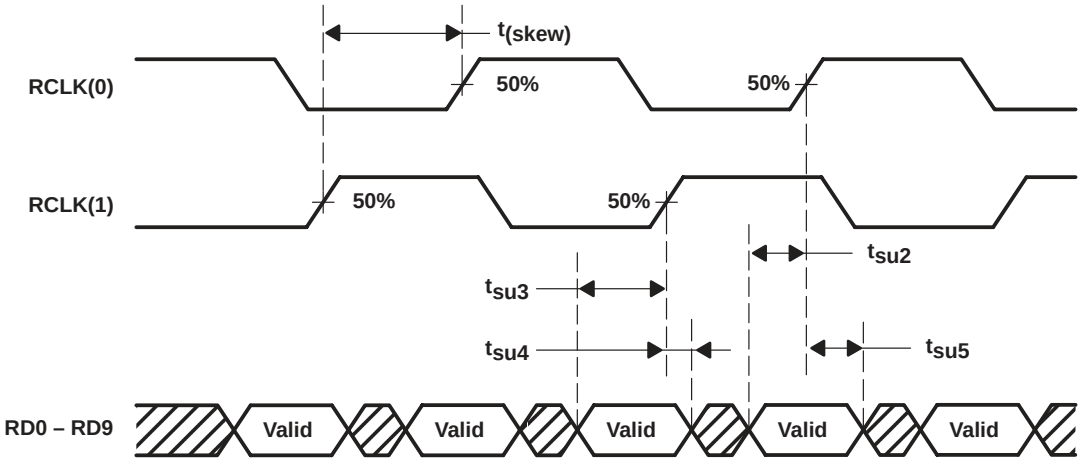
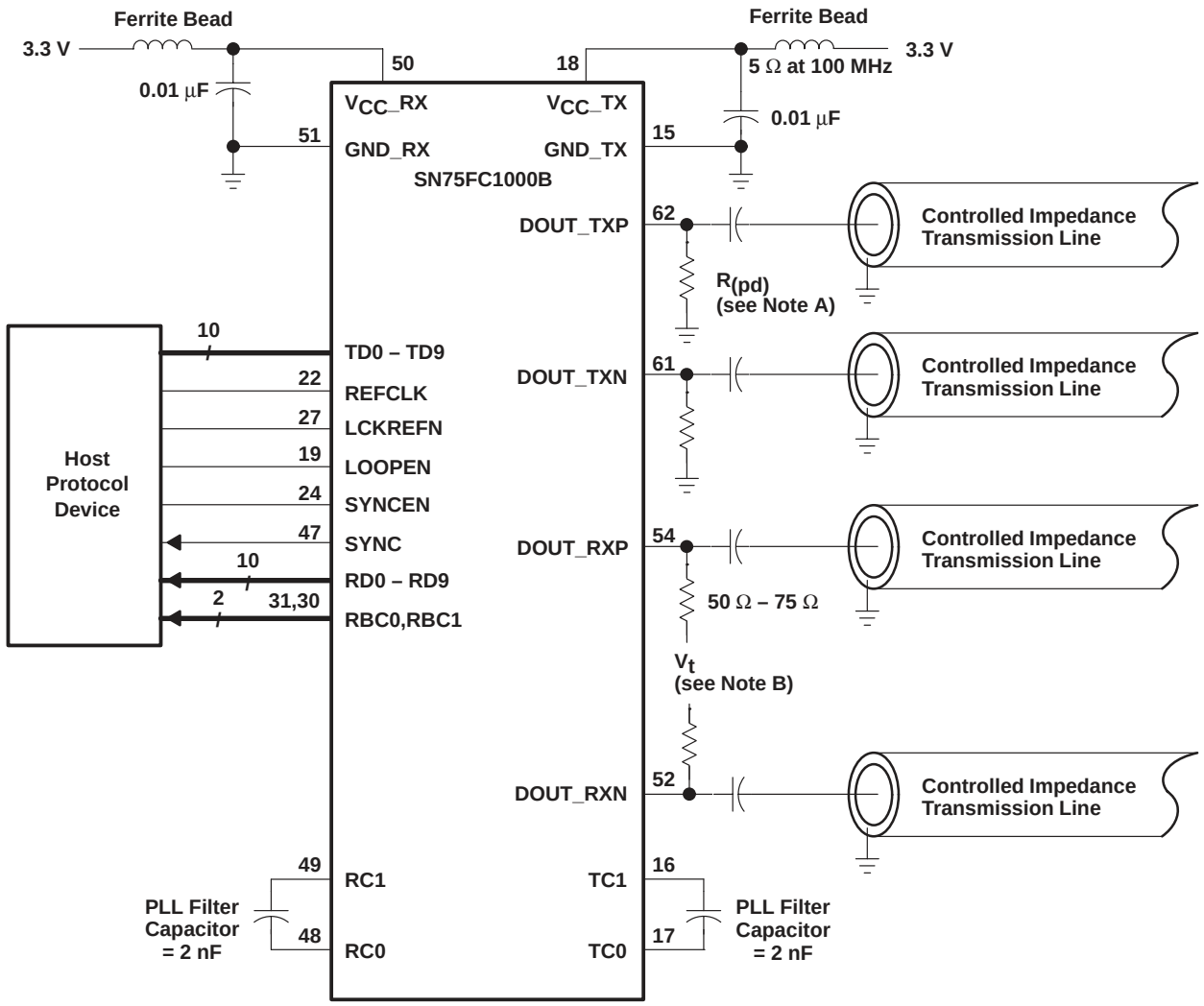


Figure 6. Receiver Interface Timing Waveforms

APPLICATION INFORMATION



NOTES: A. R(pd) – This value is set to match the falling edge to rising edge transistion times, typically 150 Ω.
B. V_t (termination voltage): for termination R = 50 Ω, $V_t = V_{CC} – 1.3$ V; R = 75 Ω, V_t = GND

Figure 7. Typical Application Circuit

MECHANICAL INFORMATION

The SN75FC1000B incorporates the latest development in TI's package line. The new patent-pending design, designated the PWP delivers thermal performance comparative to a heat-spreader design in a true low-profile package. The PWP, for the SN75FC1000B is designed to maximize heat transfer away from the die through the top of the chip. As seen in Figures 9 and 10 the bottom of the leadframe is deep downset towards the top of the chip, providing a thermal path away from the die and board. All this has been accomplished without exceeding the 1.15 mm height of the TQFP. This package in the 10mm × 10mm TQFP (PJD) provides a thermal resistance $R_{\theta JA}$ of 40°C/W and the package in the 14mm × 14mm TQFP (PHD) provides a $R_{\theta JA}$ of 40°C/W.

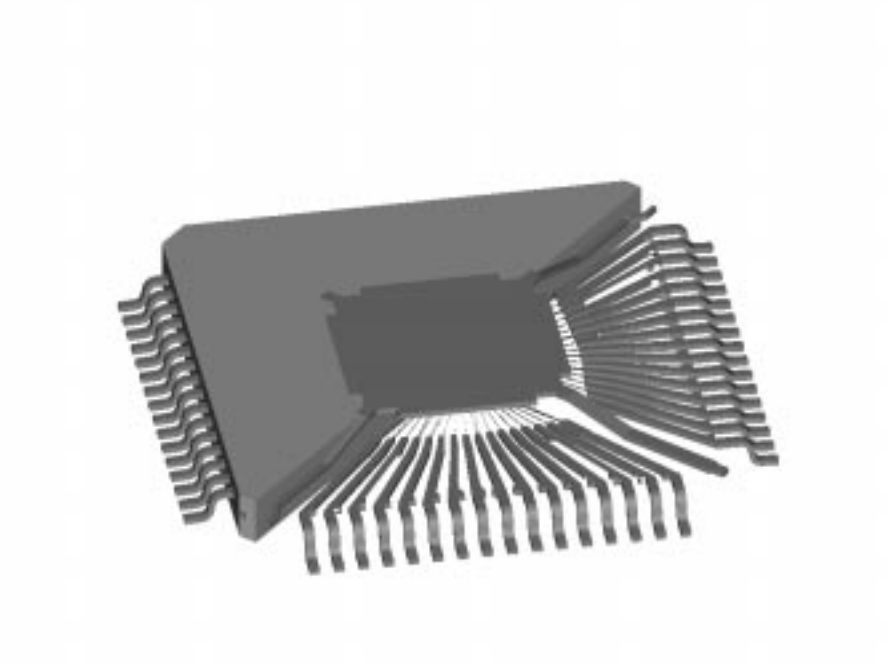


Figure 8. Heat-Spreader Design

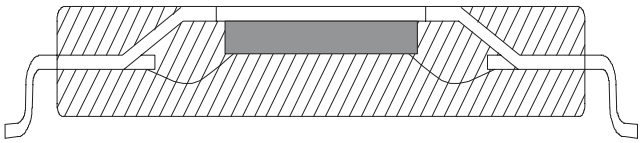
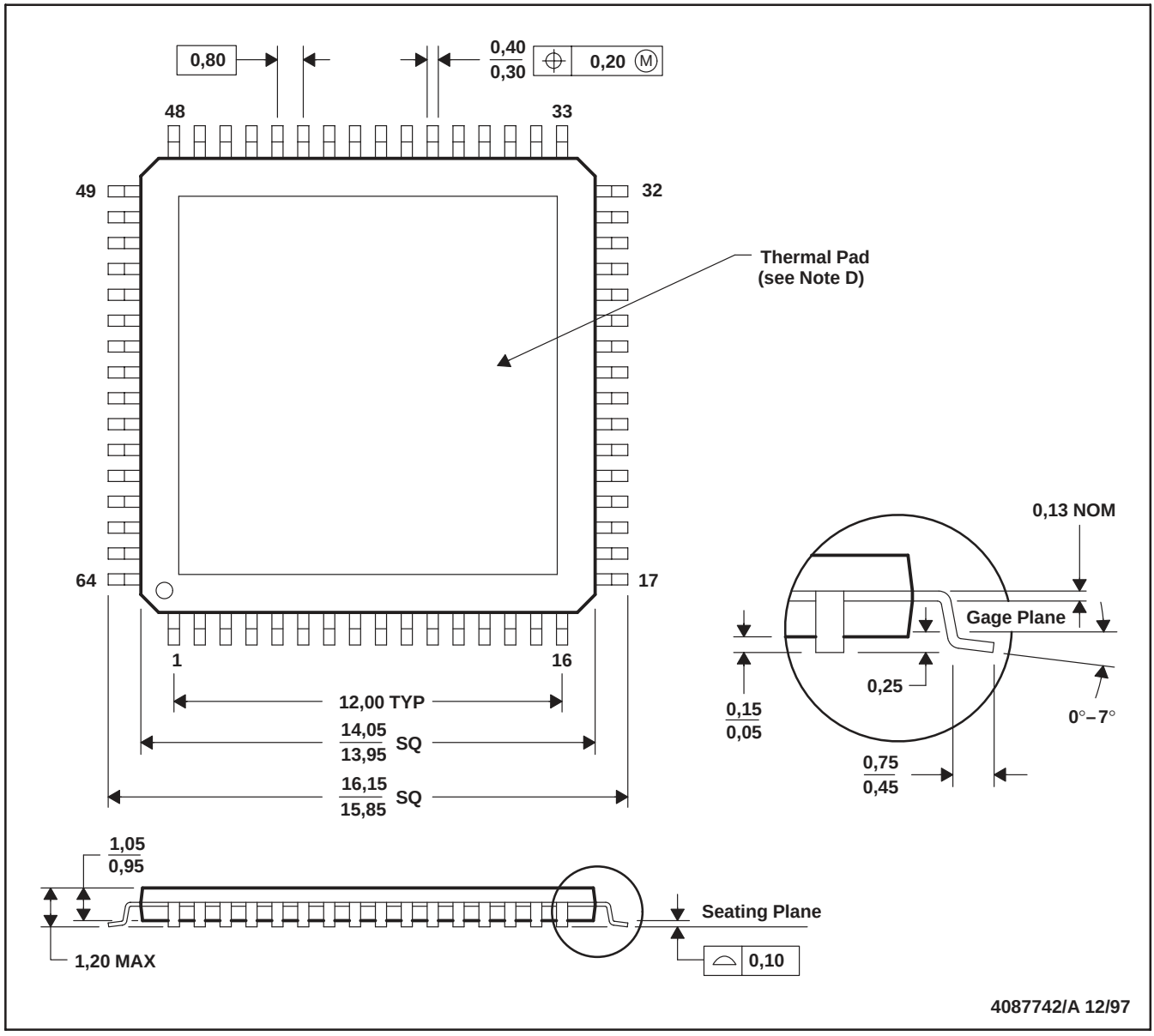


Figure 9. Leadframe Downset

MECHANICAL INFORMATION

PHD (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments Incorporated.

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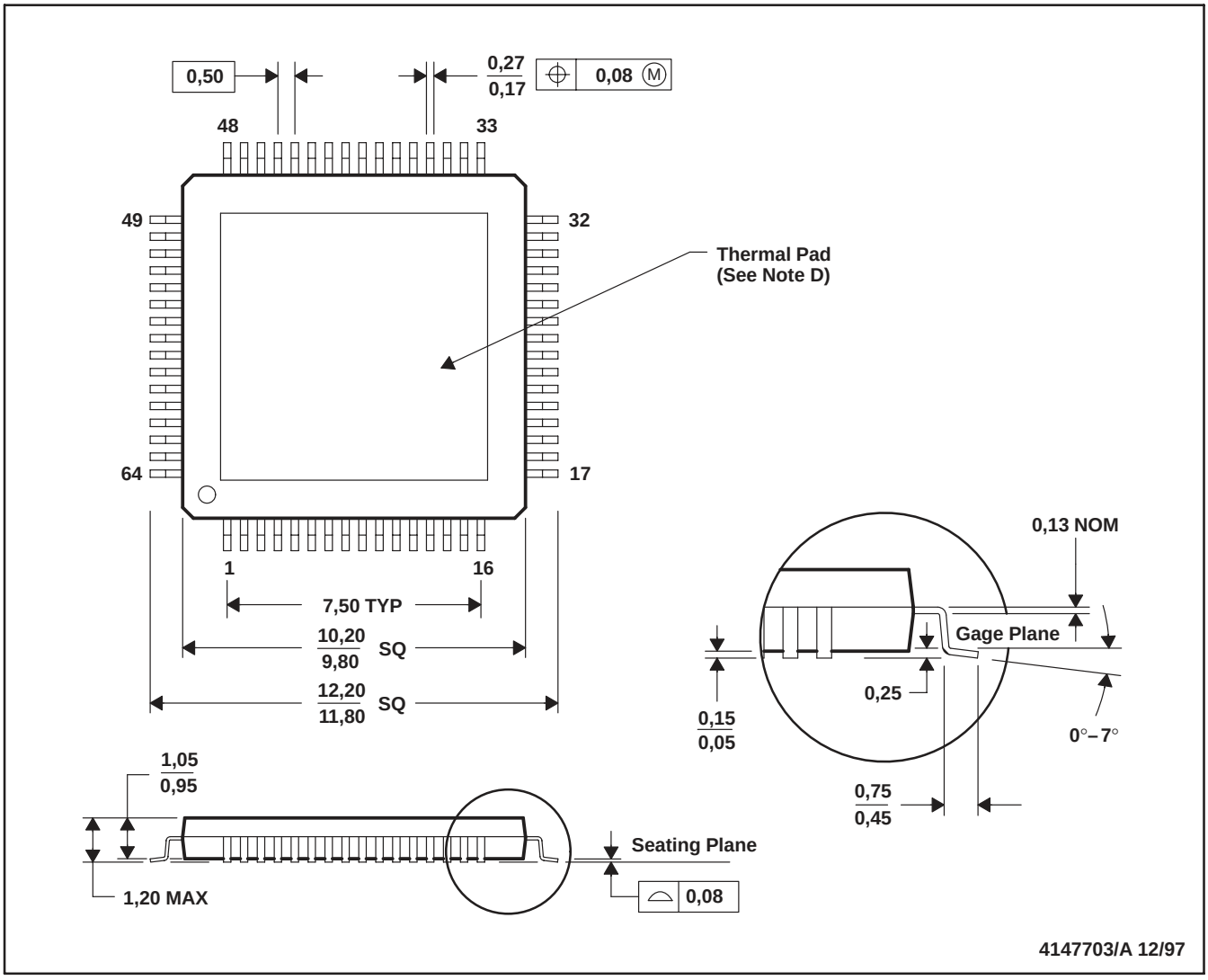
PJD (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)**



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