EVAL-ADGS5412SDZ User Guide

UG-1141

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Evaluation Board for the ADGS5412 Serially Controlled, High Voltage, Latch-Up Proof, Quad SPST Switch

FEATURES

- SPI interface with error detection
- Includes CRC, invalid read/write address, and SCLK count error detection
- Analog supply voltages
- Dual-supply: ±9 V to ±22 V
- Single-supply: 9 V to 40 V
- PC control in conjunction with the evaluation software
- EVAL-SDP-CB1Z SDP

EVALUATION KIT CONTENTS

- EVAL-ADGS5412SDZ

DOCUMENTS NEEDED

- ADGS5412 data sheet

EQUIPMENT NEEDED

- EVAL-SDP-CB1Z controller board
- ACE software with EVAL-ADGS5412SDZ plug-in
- DC voltage source
  - ±22 V for dual-supply
  - 40 V for single-supply
- Optional digital logic supply: 3.3 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADGS5412SDZ is the evaluation board for the ADGS5412. The ADGS5412 is a latch-up proof, quad single-pole, single-throw (SPST) switch controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read/write address detection, and serial clock (SCLK) count error detection. It is possible to daisy-chain multiple ADGS5412 devices together. This enables the configuration of multiple devices with a minimal amount of digital lines. The ADGS5412 also supports burst mode that decreases the time between SPI commands.

Figure 1 shows the EVAL-ADGS5412SDZ in a typical evaluation setup. The EVAL-ADGS5412SDZ is controlled by the EVAL-SDP-CB1Z system demonstration platform (SDP), which connects to a PC via a USB port. The ADGS5412 is on the center of the evaluation board and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, and a fourth terminal provides users with a defined digital logic supply voltage, if required. Alternatively, the digital logic supply voltage can be supplied from the SDP.

Full specifications on the ADGS5412 are available in the ADGS5412 data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the SDP board. The EVAL-SDP-CB1Z board (SDP-B controller board) is available to order on the Analog Devices website at www.analog.com.

TABLE OF CONTENTS

REVISION HISTORY

5/2017—Revision 0: Initial Version

ADGS5412 EVALUATION BOARD LAYOUT

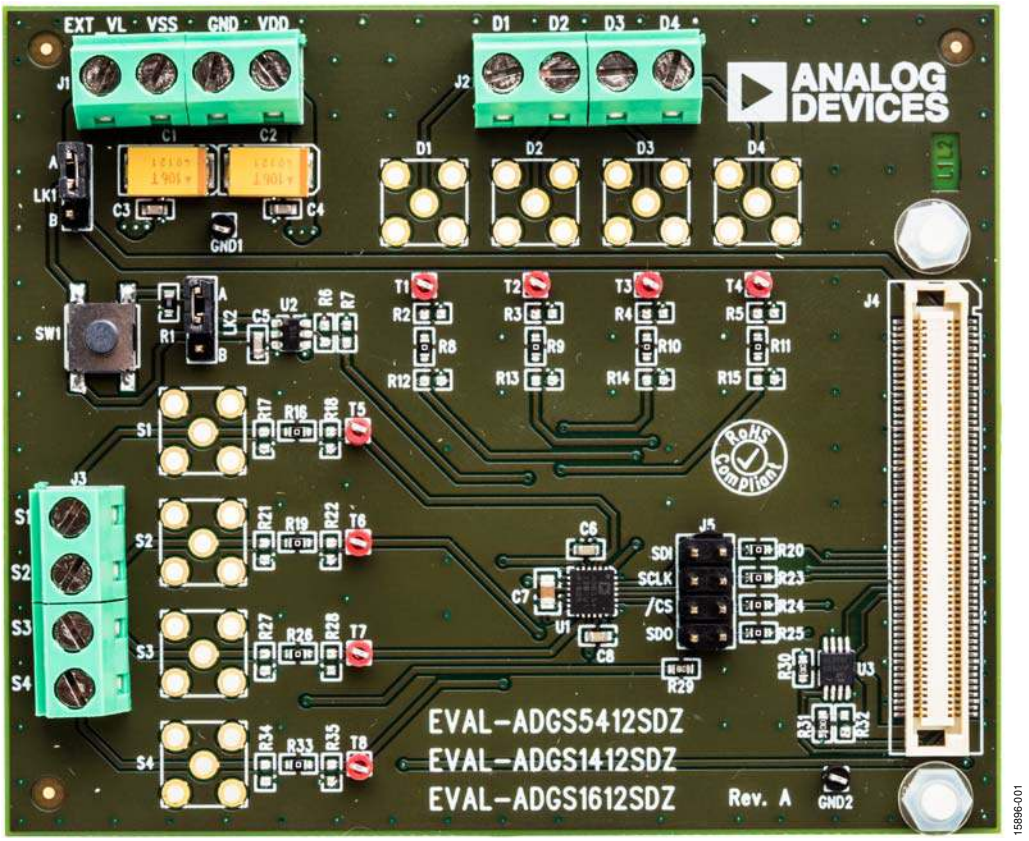

Figure 1.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Connector J1 provides access to the supply pins of the ADGS5412. V_{DD}, GND, and V_{SS} on J1 terminal block link to the appropriate pins on the ADGS5412. For dual-supply voltages, the evaluation board can be powered from ±9 V to ±22 V. For single-supply voltages, the GND and V_{SS} terminals must connect together and power the evaluation board with 9 V to 40 V. Additionally, 3.3 V is supplied to the V_L pin of the ADGS5412 by the SDP when Link LK1 is in Position B. When controlling the ADGS5412 by another method other than the SDP, supply between 2.7 V and 5.5 V to the V_L pin of the ADGS5412 via the EXT_VL screw terminal input on J1. LK1 must be in Position A.

INPUT SIGNALS

Two screw connectors, J2 and J3, are provided to connect to both the source and drain pins of the ADGS5412. Additional subminiature version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain side includes two sets of 0603 pads, which can place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can create a simple resistor-capacitor (RC) filter.

LINK OPTIONS

A number of link options are provided on the EVAL-ADGS5412SDZ evaluation board that must be set for the required operating conditions before using. Table 1 describes the positions of the links to control the evaluation board via the SDP board using a PC and external power supplies. The functions of these link options are described in detail in Table 2.

When using the SDP in conjunction with the EVAL-ADGS5412SDZ, LK1 must be in Position B to avoid damage to the SDP.

Table 1. Link Options for SDP Control (Default)

Link Number	Option
LK1	B
LK2	B

Table 2. Link Functions

Link Number	Function
LK1	This link selects the source of the V_L voltage supplied to the ADGS5412. Position A selects EXT_VL from J1. Position B selects the 3.3 V from the SDP.
LK2	This link selects how a hardware reset is performed. Position A indicates the SW1 push button performs a hardware reset. Position B indicates the SDP can perform a hardware reset.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-ADGS5412SDZ evaluation board uses the Analog Devices Analysis Control Evaluation (ACE) software. ACE is a desktop software application that allows the evaluation and control of multiple evaluation systems.

ACE installs the necessary SDP drivers and .NET Framework 4 by default. Install ACE before connecting the SDP. The ACE software and access to full instructions on how to install and use ACE can be found on the Analog Devices website.

After the installation is finished, the EVAL-ADGS5412SDZ evaluation board plug-ins appear when opening ACE.

INITIAL SET UP

To set up the evaluation board, complete the following steps:

1. Connect the evaluation board to the SDP board and connect the SDP board to the computer via a USB cable.
2. Power the evaluation board as described in the Power Supplies section.
3. Run the ACE application. The EVAL-ADGS5412SDZ board plug-ins appear in the attached hardware section of the **Start** tab.
4. Double-click on the evaluation board plug-in to open the evaluation board view seen in Figure 2.
5. The chip block diagram can be accessed by double-clicking on the ADGS5412 icon (see Figure 2). This view provides a basic representation of functionality of the evaluation board. The main functions are labeled in Figure 3.

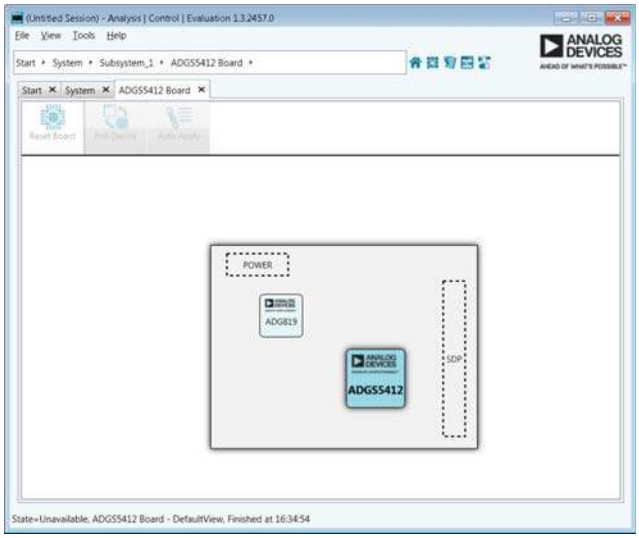

Figure 2. Evaluation Board View of the EVAL-ADGS5412SDZ

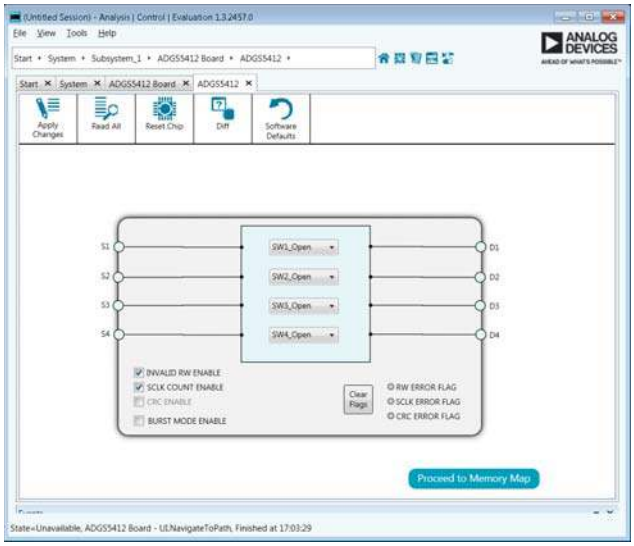

Figure 3. Chip Block Diagram View for the ADGS5412

BLOCK DIAGRAM AND DESCRIPTION

The EVAL-ADGS5412SDZ software is organized so that it appears similar to the functional block diagram shown in the ADGS5412 data sheet. In this way, it is easy to correlate the functions on the EVAL-ADGS5412SDZ board with the description in the data sheets. A full description of each block, register, and setting is given in the ADGS5412 data sheet.

Some of the blocks and their functions are described here as they pertain to the evaluation board. The full screen block diagram, shown in Figure 4, describes the functionality of each

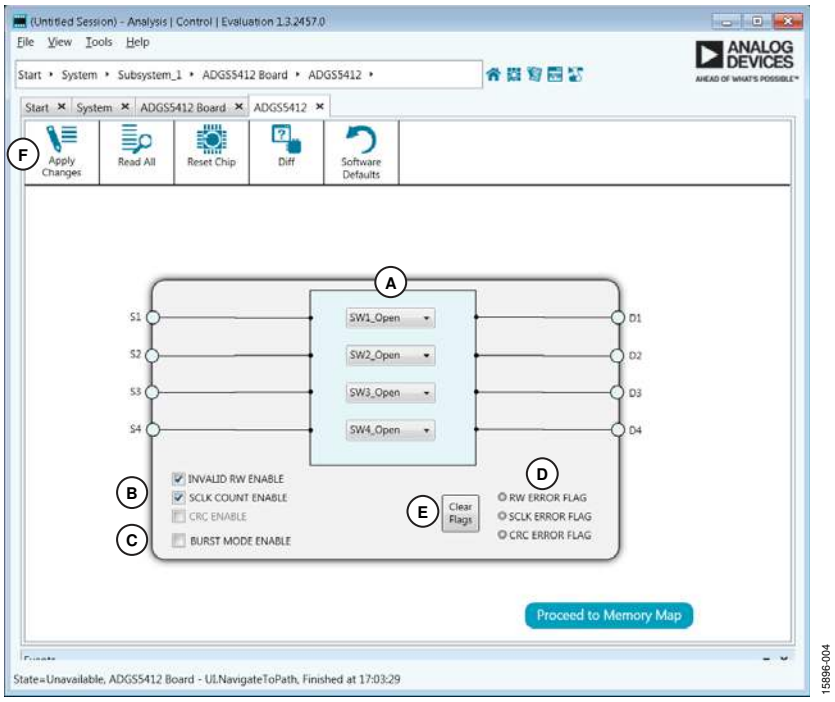

Figure 4. EVAL-ADGS5412SDZ Block Diagram with Labels

Table 3. Block Diagram Functions

Label	Function
A	The dropdown menus configure SW1 to SW4 as open or closed.
B	The **INVALID RW ENABLE**, **SCLK COUNT ENABLE**, and **CRC ENABLE** checkboxes enable or disable the error detection features on the SPI interface.
C	The **BURST MODE ENABLE** checkbox enables or disables burst mode.
D	The **RW ERROR FLAG**, **SCLK ERROR**, and **CRC ERROR FLAG** indicators illuminate red if the relevant error flags assert in the error flags register.
E	The **Clear Flags** button clears the error flags register.
F	The **Apply Changes** button applies all modified values to the devices.

MEMORY MAP

All registers are fully accessible from the **Memory Map** tab; this allows registers to be edited at a bit level (see Figure 5 and Figure 6). The bits shaded in dark gray are read-only bits and cannot be accessed from ACE. All other bits are toggled. The **Apply Changes** button transfers data to the device.

All changes here correspond to the block diagram; for example, if the internal register bit is enabled, it displays as enabled on the block diagram. Any bits or registers that are bold are modified values that have not been transferred to the evaluation board. After clicking **Apply Changes**, the data is transferred to the evaluation board.

Registers

+ / -	Address (Hex)	Name	Data (Hex)	Data (Binary)
+	0001	* SW_DATA	01	0 0 0 0 0 0 0 1
+	0002	ERR_CONFIG	06	0 0 0 0 0 1 1 0
+	0003	* ERR_FLAGS	00	0 0 0 0 0 0 0 0
+	0005	BURST_EN	00	0 0 0 0 0 0 0 0
+	000B	SOFT_RESETB	00	0 0 0 0 0 0 0 0
+	0025	DAISY_CHAIN_EN	00	0 0 0 0 0 0 0 0
+	006C	ERR_FLAGS_RESET	A9	1 0 1 0 1 0 0 1

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Figure 5. ADGS5412 Memory Map

Registers

+ / -	Address (Hex)	Name	Data (Hex)	Data (Binary)
+	**0001**	*** SW_DATA**	09	**0 0 0 0 1 0 0 1**
+	0002	ERR_CONFIG	06	0 0 0 0 0 1 1 0
+	0003	* ERR_FLAGS	00	0 0 0 0 0 0 0 0
+	0005	BURST_EN	00	0 0 0 0 0 0 0 0
+	000B	SOFT_RESETB	00	0 0 0 0 0 0 0 0
+	0025	DAISY_CHAIN_EN	00	0 0 0 0 0 0 0 0
+	006C	ERR_FLAGS_RESET	A9	1 0 1 0 1 0 0 1

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Figure 6. ADGS5412 Memory Map with Unapplied Changes in the SW_DATA Register

EVALUATION BOARD SCHEMATICS AND ARTWORK

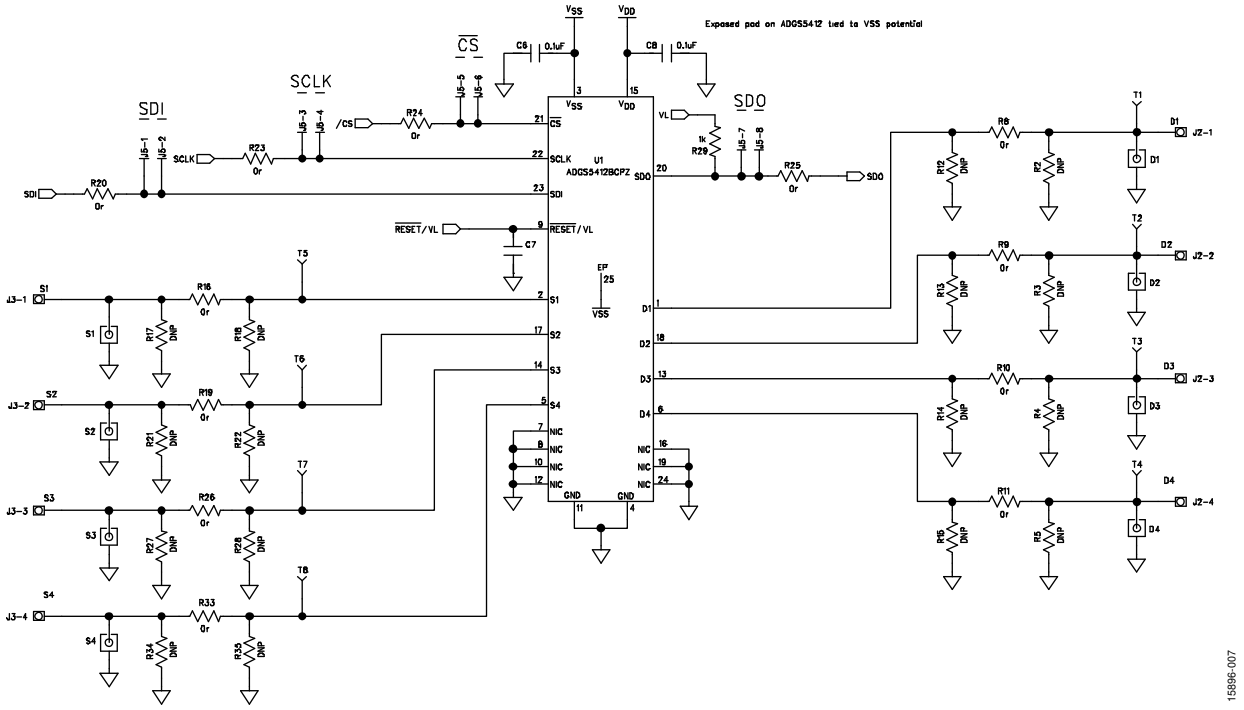

Figure 7. EVAL-ADGS5412SDZ Schematic 1

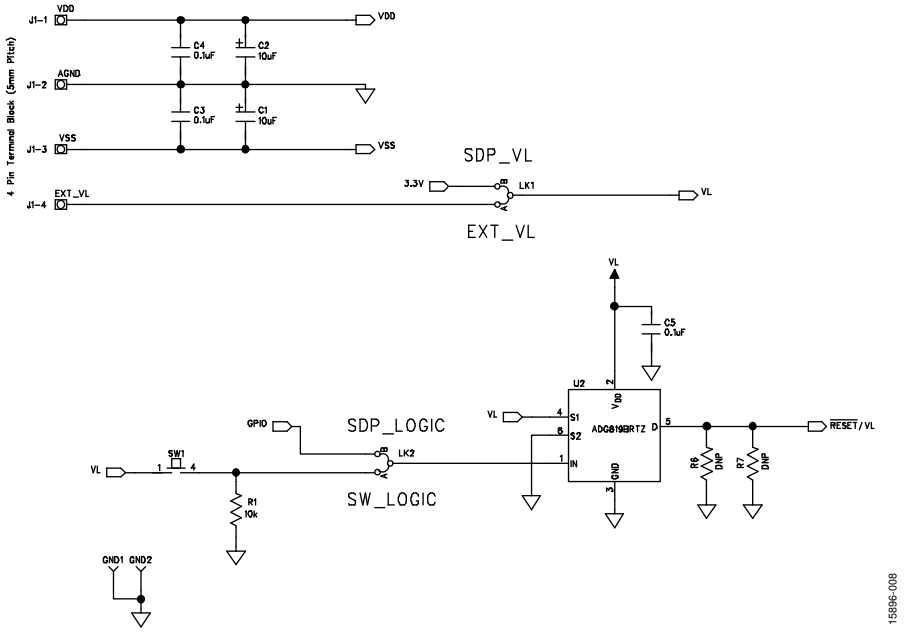

Figure 8. EVAL-ADGS5412SDZ Schematic 2

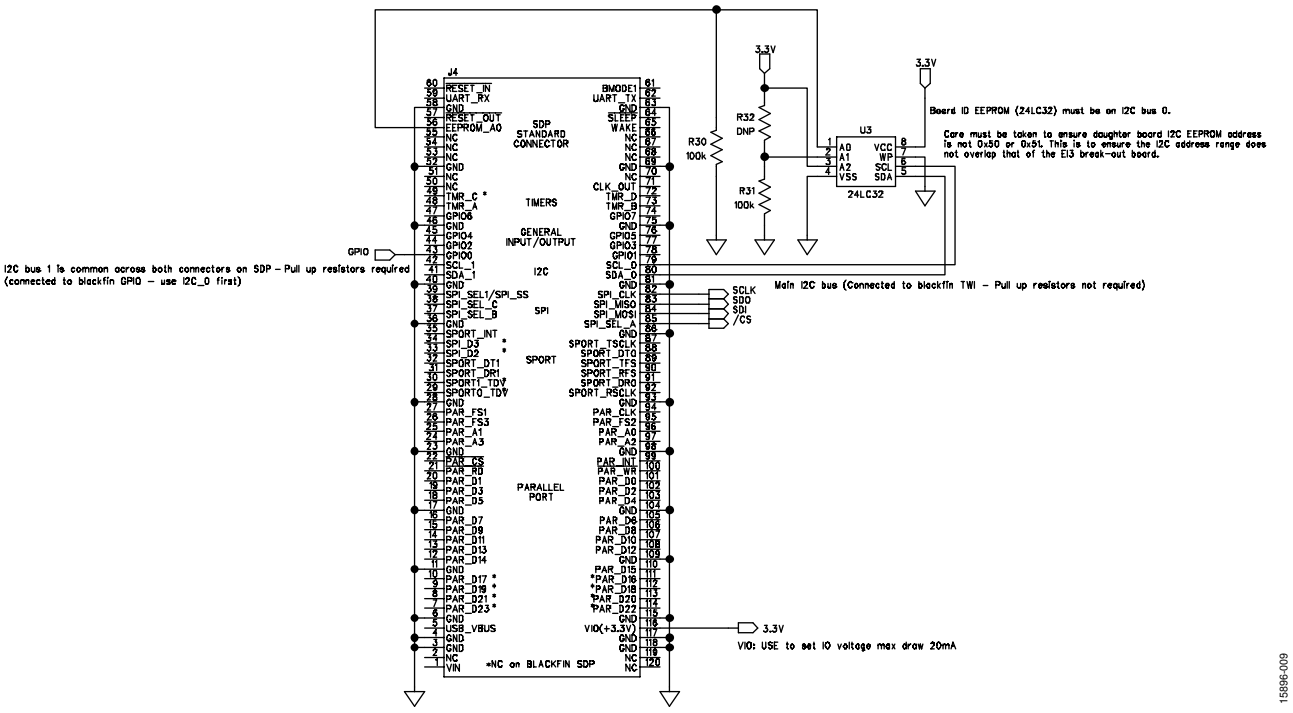

Figure 9. EVAL-ADGS5412SDZ Schematic 3

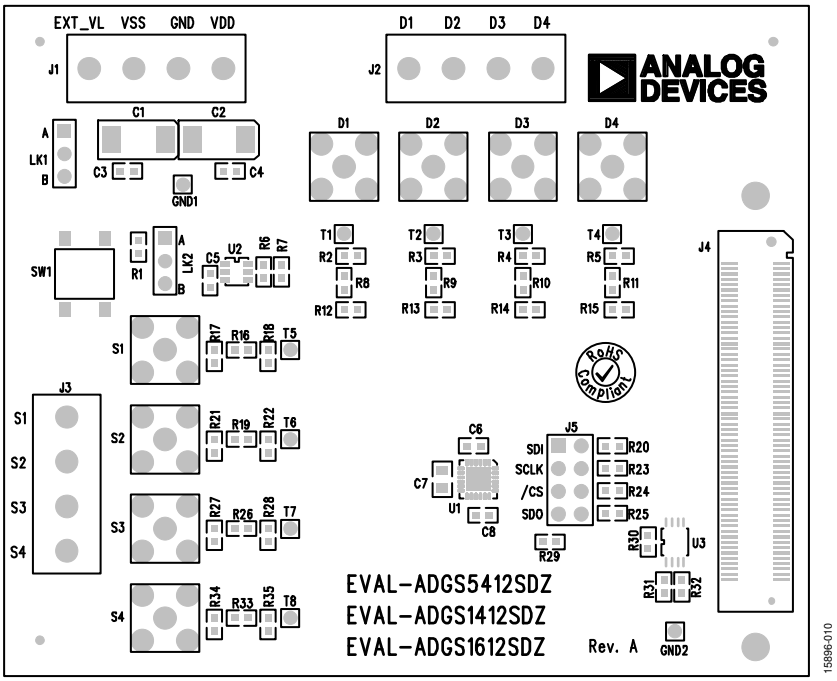

Figure 10. EVAL-ADGS5412SDZ Silk Screen

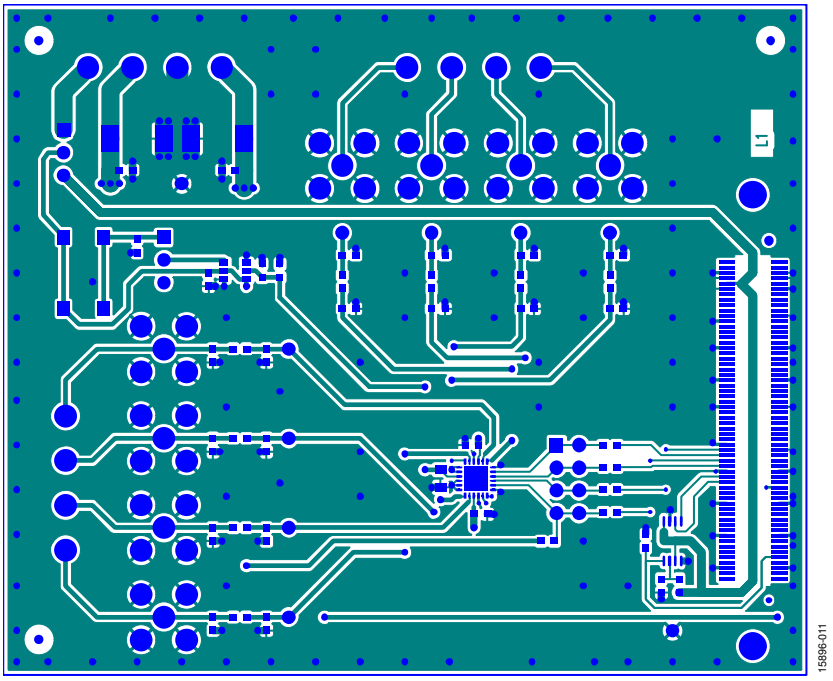

Figure 11. EVAL-ADGS5412SDZ Top Layer

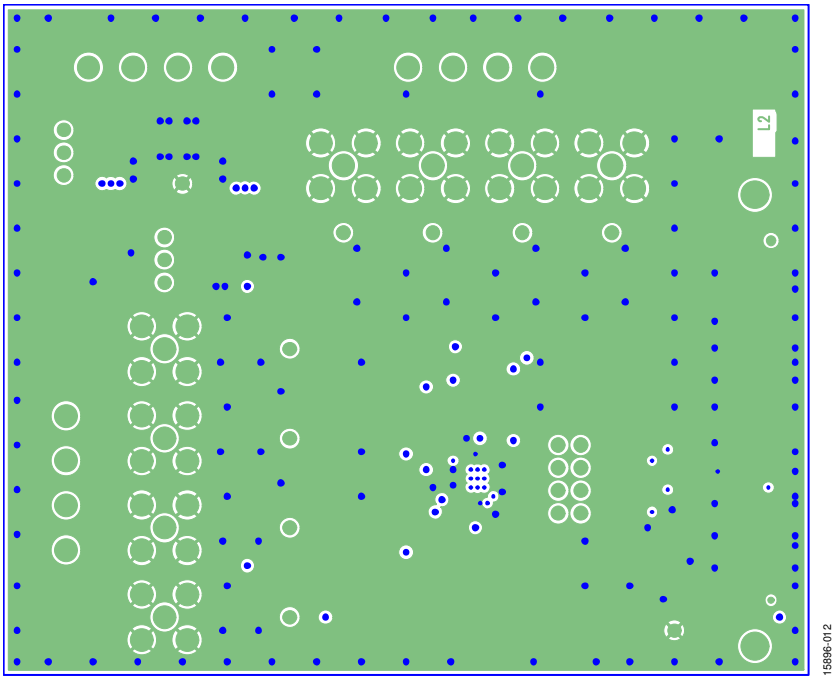

Figure 12. EVAL-ADGS5412SDZ Layer 2

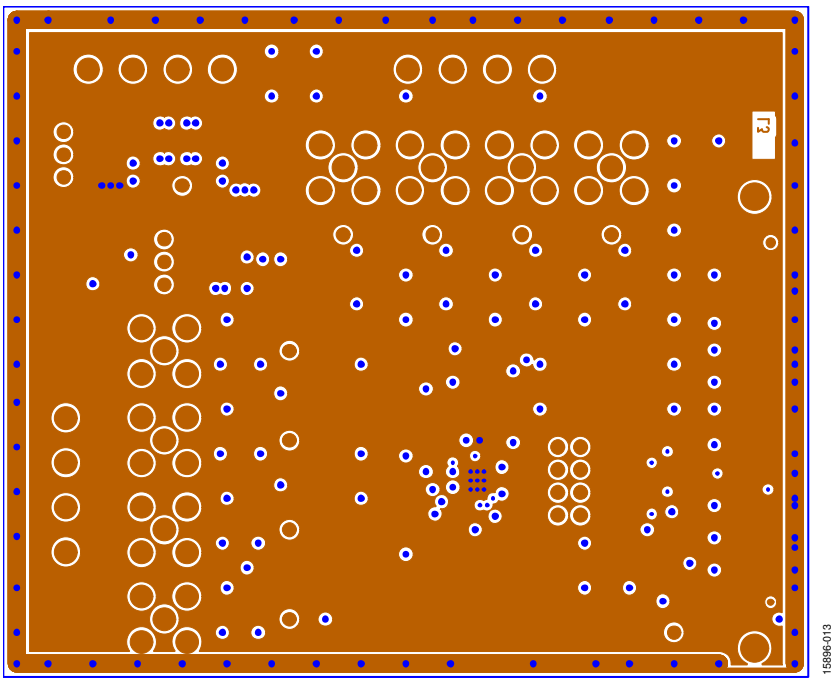

Figure 13. EVAL-ADGS5412SDZ Layer 3

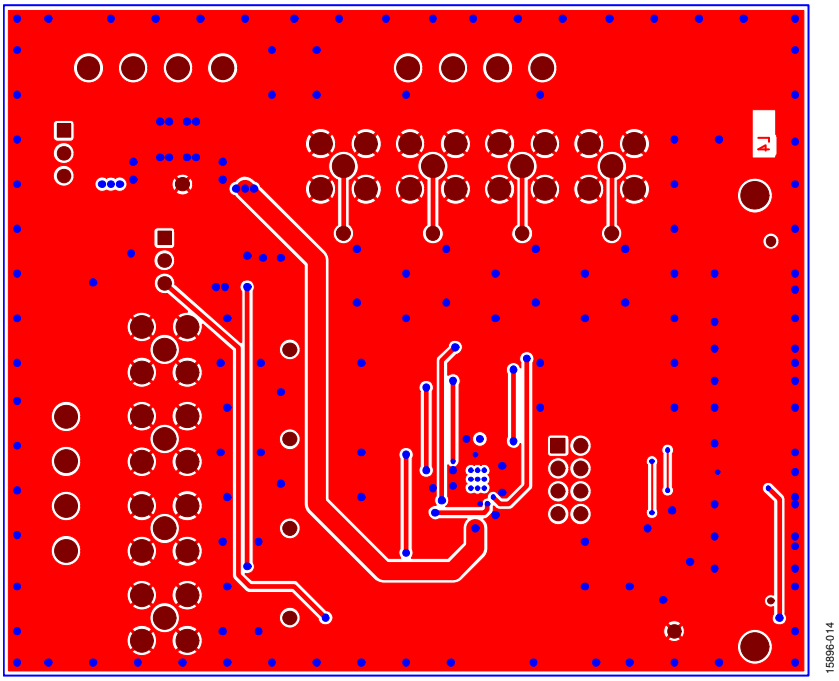

Figure 14. EVAL-ADGS5412SDZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description
C1 to C2	50 V tantalum capacitor, 10 µF, D size
C3 to C6, C8	50 V, X7R multilayer ceramic capacitor, 0.1 µF, 0603
C7	Capacitor, 10 µF, 0805, 16 V
D1 to D4	Not placed
S1 to S4	Not placed
T1 to T8	Red test point
GND1, GND2	Black test point
J1 to J3	4-pin terminal block, 5 mm pitch
J4	120-way connector, 0.6 mm pitch
J5	Through hole, header, 4 × 2, 2.54 mm
LK1, LK2	3-pin single inline (SIL) header and shorting link
R2 to R7, R12 to R15, R17, R18, R21, R22, R27, R28, R32, R34, R35	Not placed
R8 to R11, R16, R19, R20, R23 to R26, R33	Resistor, 0 Ω, 0603, 1%
R1	Resistor, 10 kΩ, 0.063 W, 1%, 0603
R29	Resistor, 1 kΩ, 0.063 W, 1%, 0603
R30, R31	Resistor, 100 kΩ, 0.063 W, 1%, 0603
SW1	Surface mount device (SMD) push button switch
U1	ADGS5412, SPI controlled, quad SPST switch
U2	ADG819, 1.8 V to 5.5 V, 2:1 multiplexer/SPDT switch
U3	24LC32A-I/MS, 32 kΩ, I2 C serial EEPROM

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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