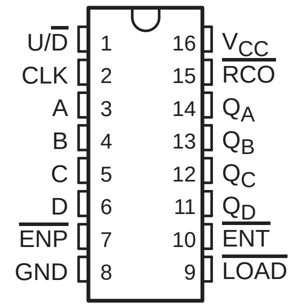
SN74F168
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTER

SDFS057A − D2932, MARCH 1987 − REVISED OCTOBER 1993

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This synchronous, presettable, 4-bit up/down decade counter features an internal carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

This counter is fully programmable; that is, it may be preset to any number between 0 and its maximum count. The load-input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load ($\overline{LOAD}$) input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and a ripple-carry ($\overline{RCO}$) output. Both $\overline{ENP}$ and $\overline{ENT}$ must be low to count. The direction of the count is determined by the level of the up/down (U/$\overline{D}$) input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the $\overline{RCO}$. $\overline{RCO}$ thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

The SN74F168 features a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$ or U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

The SN74F168 is characterized for operation from 0°C to 70°C.

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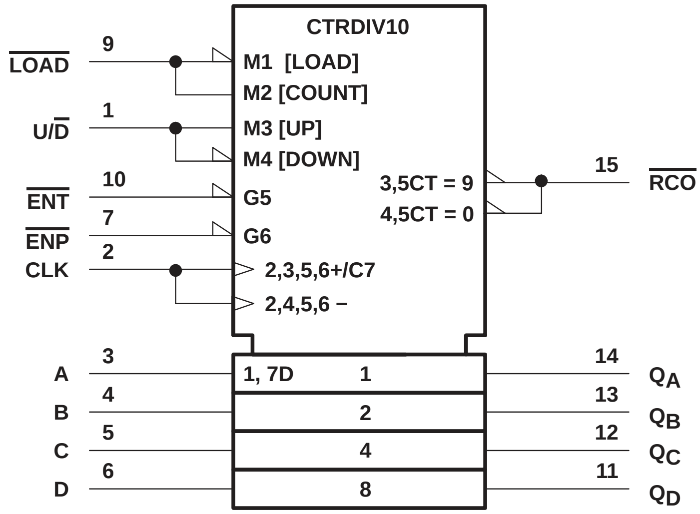
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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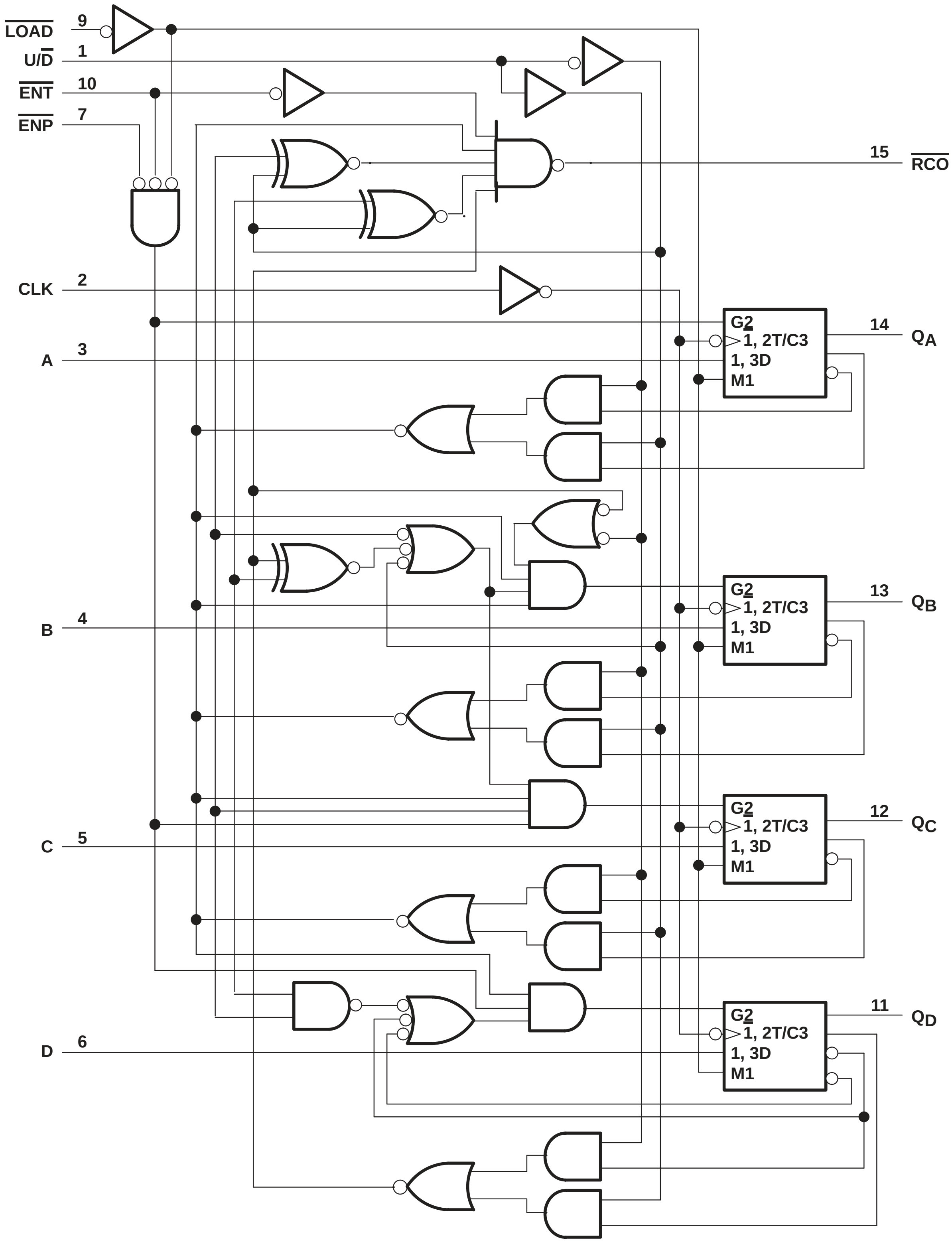
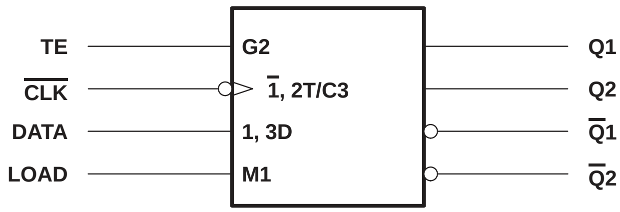
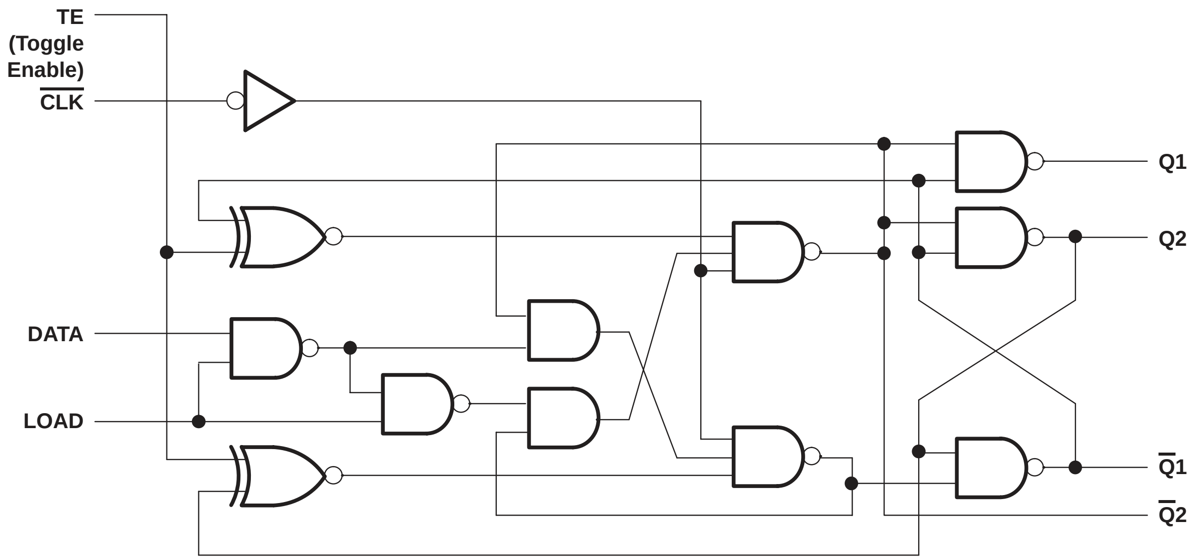
logic diagram (positive logic)



logic symbol, each flip-flop



logic diagram, each flip-flop (positive logic)



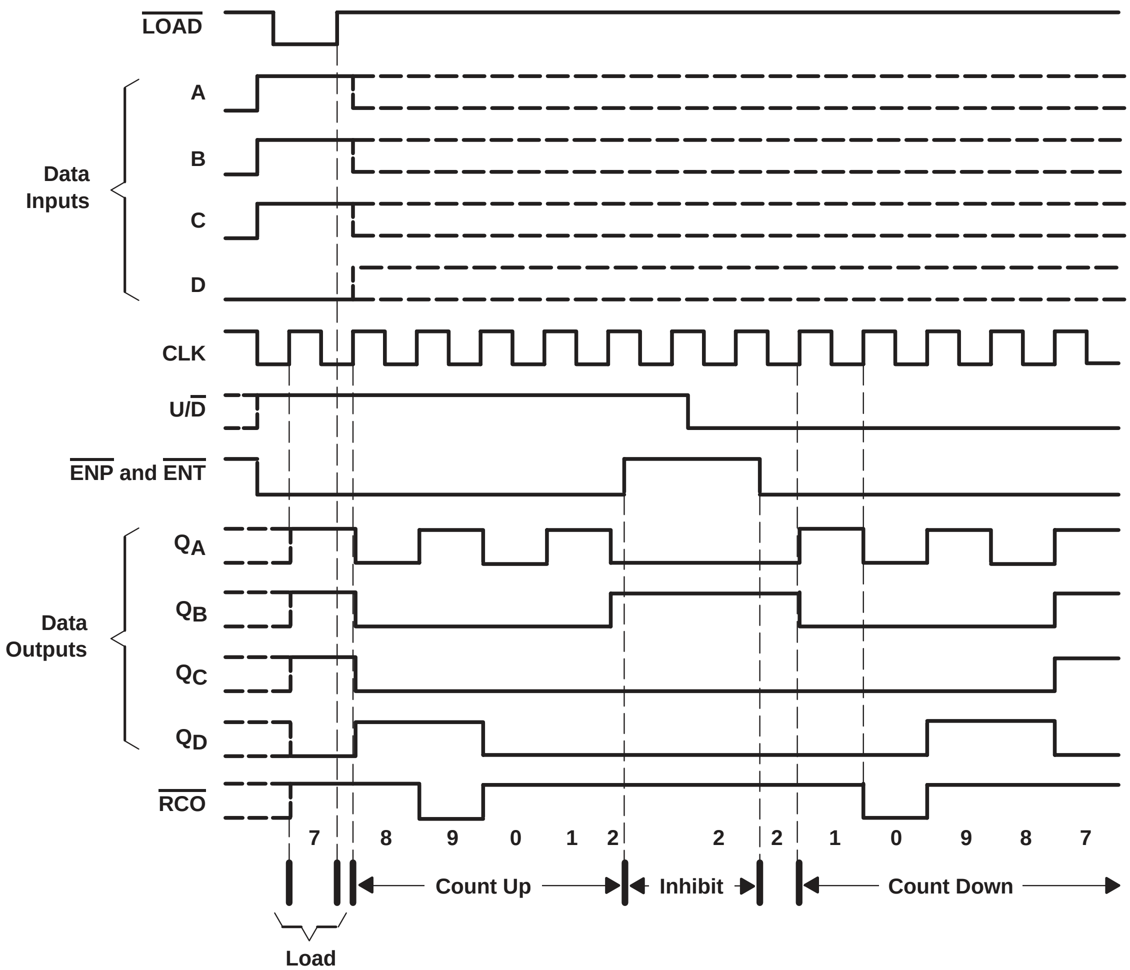
FUNCTION TABLE
(each flip-flop)

COUNTER INPUTS		FLIP-FLOP INPUTS				OUTPUTS	
$\overline{LOAD}$	CLK	LOAD	TE	$\overline{CLK}$	DATA	Q	$\overline{Q}$
L	↑	H	L	↓	H	H	L
L	↑	H	L	↓	L	L	H
H	↑	L	H	↓	X	$\overline{Q}_0$	Q_0
H	↑	L	L	↓	X	Q_0	$\overline{Q}_0$

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −1.2 V to 7 V
Input current range . . . . . −30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			− 1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 1 mA	2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = − 1 mA	2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.5 V			− 1.2	mA
	All others					− 0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 2		38	52	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with B and $\overline{ENT}$ inputs high and all other inputs low.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f_{clock}	Clock frequency			0	100	0	90	MHz
t_w	Pulse duration	CLK high or low		5		5.5		ns
t_{su}	Setup time	Data before CLK↑	High or low	4		4.5		ns
		$\overline{LOAD}$ before CLK↑	High or low	8		9		
		$\overline{ENP}$ and $\overline{ENT}$ before CLK↑	High or low	5		6		
		U/$\overline{D}$ before CLK↑	High	11		12.5		
			Low	16.5		18		
t_h	Hold time	Data after CLK↑	High or low	3		3.5		ns
		$\overline{LOAD}$ after CLK↑	High or low	0		0		
		$\overline{ENP}$ and $\overline{ENT}$ after CLK↑	High or low	0		0		
		U/$\overline{D}$ after CLK↑	High or low	0		0		

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	115		90		MHz
t_{PLH}	CLK	Q	2.2	6.1	8.5	2.2	9.5	ns
t_{PHL}			3.2	8.6	11.5	3.2	13	
t_{PLH}	CLK	$\overline{RCO}$	4.7	11.6	15.5	4.7	17	ns
t_{PHL}			3.2	8.1	11	3.2	12.5	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.7	4.1	6	1.7	7	ns
t_{PHL}			1.7	5.6	8	1.7	9	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	2.7	8.1	11	2.7	12.5	ns
t_{PHL}			3.2	12.1	16	3.2	17.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74F168D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74F168N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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