TCC-303

Three-Output PTIC Control IC

Introduction

TCC−303 is a three−output high−voltage digital to analog control IC specifically designed to control and bias ON Semiconductor's Passive Tunable Integrated Circuits (PTICs).

These tunable capacitor control circuits are intended for use in mobile phones and dedicated RF tuning applications. The implementation of ON Semiconductor's tunable circuits in mobile phones enables significant improvement in terms of antenna radiated performance.

The tunable capacitors are controlled through a bias voltage ranging from 1 V to 24 V. The TCC−303 high−voltage PTIC control IC has been specifically designed to cover this need, providing three independent high−voltage outputs that control up to three different tunable PTICs in parallel. The device is fully controlled through a MIPI RFFE digital interface.

Key Features

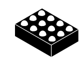
- Controls ON Semiconductor's PTIC Tunable Capacitors
- Compliant with Timing Needs of Cellular and Other Wireless System Requirements
- 28 V Integrated Boost Converter with Three 24 V Programmable DAC Outputs
- Low Power Consumption
- MIPI RFFE Interfaces (1.8 V)
- Available in WLCSP (RDL ball arrays)
- Compliant with MIPI 26 MHz Read−Back
- This is a Pb−Free Device

Typical Applications

- Multi−band, Multi−standard, Advanced and Simple Mobile Phones
- Tunable Antenna Matching Networks
- Compatible with Closed−loop and Open−loop Antenna Tuner Applications

ON Semiconductor®

www.onsemi.com



WLCSP12
CASE 567MW

MARKING DIAGRAM

T33x= Specific Device Code
x = A or B
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.

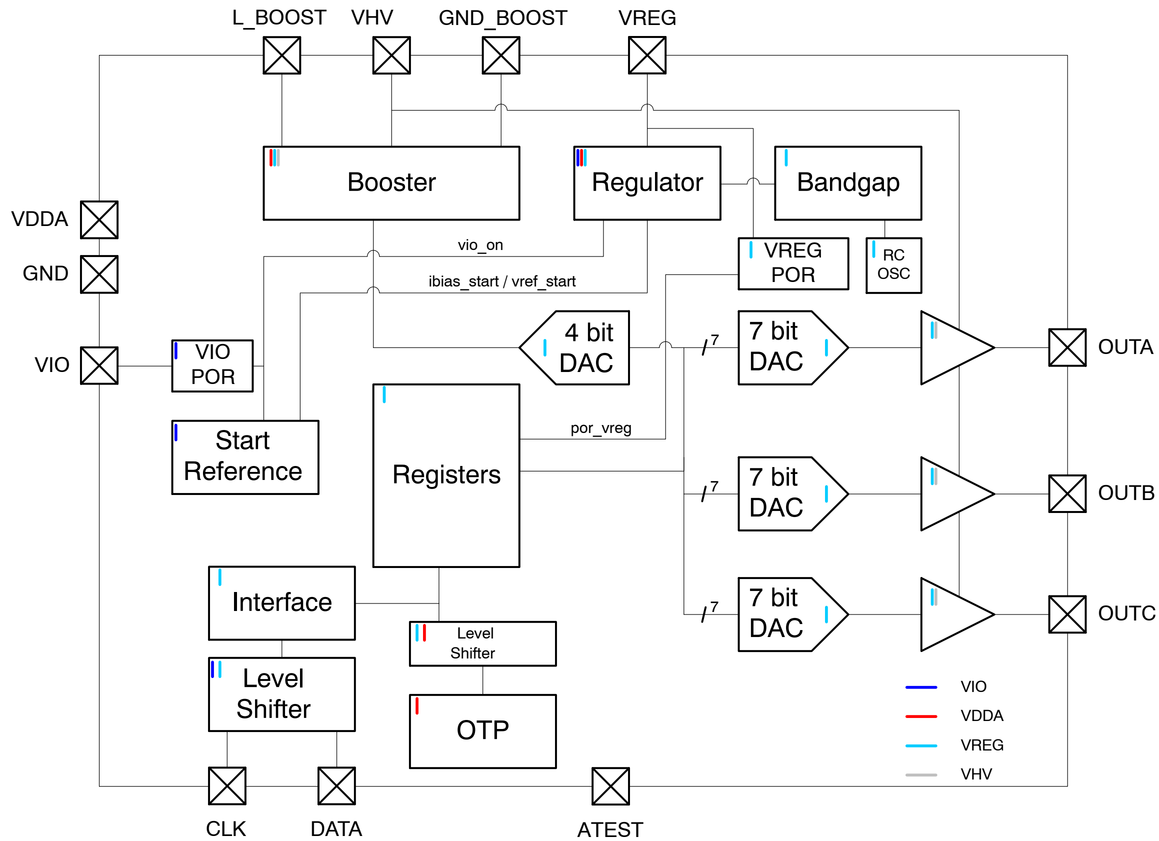


Figure 1. Control IC Functional Block Diagram

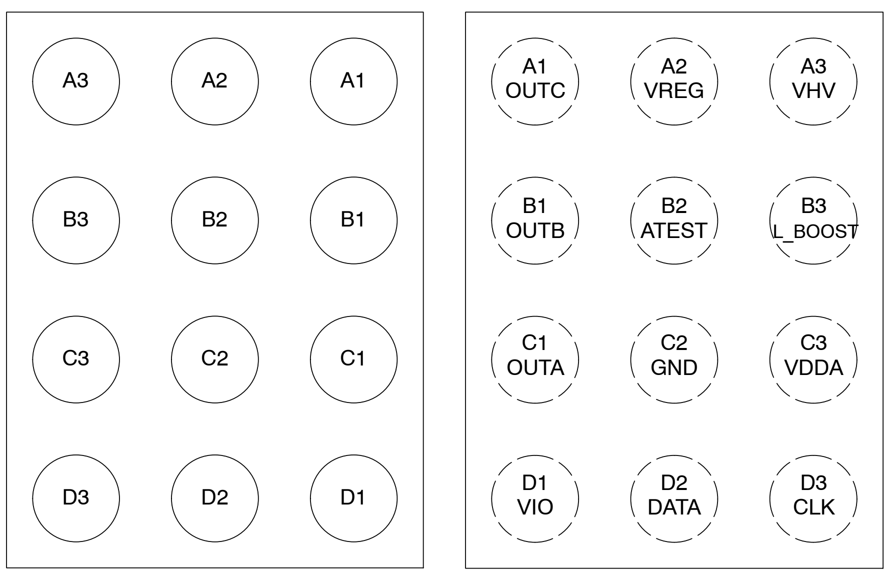


Figure 2. RDL Padout, Bump Side View (left), PCB footprint (right), with RDL Bump Assignment

RDL Pin Out

Table 1. PAD DESCRIPTIONS

RDL	Name	Type	Description
A1	OUTC	AOH	High Voltage Output C
A2	VREG	AO	Regulator Output
A3	VHV	AOH / AIH	Boost High Voltage can be Forced Externally
B1	OUTB	AOH	High Voltage Output B
B2	ATEST	AO	Analog Test Out (Note 1)
B3	L_BOOST	AOH	Boost Inductor
C1	OUTA	AOH	High Voltage Output A
C2	GND	P	Ground
C3	VDDA	P	Analog Supply
D1	VIO	P	Digital IO Supply
D2	DATA	DIO	MIPI RFFE Digital IO
D3	CLK	DI	MIPI RFFE Clock

Legend: Pad Types
AIH= High Voltage Analog Input
AO= Analog Output
AOH= High Voltage Analog Output
DI= Digital Input
DIO= Digital Input/Output (IO)
P= Power

1. To be grounded in normal operation.

ELECTRICAL PERFORMANCE SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDDA	Analog Supply Voltage	−0.3 to +5.5	V
VIO	IO Reference Supply Voltage	−0.3 to +2.5	V
$V_{I/O}$	Input Voltage Logic Lines (DATA, CLK)	−0.3 to VIO + 0.3	V
V_{HVH}	VHV Maximum Voltage	−0.3 to 30	V
$V_{ESD\ (HBM)}$	Human Body Model, JESD22−A114, All I/O	2,000	V
$V_{ESD\ (MM)}$	Machine Model, JESD22−A115	200	V
T_{STG}	Storage Temperature	−55 to +150	°C
$T_{AMB\_OP\_MAX}$	Max Operating Ambient Temperature without Damage	+110	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating			Unit
		Min	Typ	Max	
T_{AMB_OP}	Operating Ambient Temperature	−30	–	+85	°C
T_{J_OP}	Operating Junction Temperature	−30	–	+125	°C
VDDA	Analog Supply Voltage	2.3	–	5.5	V
VIO	IO Reference Supply Voltage	1.62	–	1.98	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC CHARACTERISTICS (T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V<VDDA< 5.5 V; V_{IO} = 1.8 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
SHUTDOWN MODE						
I_{VDDA}	VDDA Supply Current	–	–	1.5	μA	VIO Supply is Low
I_{L_BOOST}	L_BOOST Leakage	–	–	1.5		
I_{BATT}	Battery Current	–	–	2.5		
I_{VIO}	VIO Supply Current	−1	–	1		
I_{CLK}	CLK Leakage	−1	–	1		
I_{DATA}	DATA Leakage	−1	–	1		
ACTIVE MODE						
I_{BATT}	Average battery current, 3 outputs actively switching 16 V for 1205 μs to 2 V for 1705 μs to 8 V for 1705 μs	–	980	1290	μA	At VHV = 20 V VDDA = 3.3 V
I_{BATT_SS0}	Average battery current, 3 outputs @ 0 V steady state	–	590	830		At VHV = 20 V VDDA = 3.3 V
I_{BAT_SS2}	Average battery current, 3 outputs @ 2 V steady state	–	610	860	μA	At VHV = 20 V VDDA = 3.3 V
I_{BATT_SS16}	Average battery current, 3 outputs @ 16 V steady state	–	780	1020		At VHV = 20 V VDDA = 3.3 V
I_{L_BOOST}	Average inductor current, 3 outputs actively switching 16 V for 1205 μs to 2 V for 1705 μs to 8 V for 1705 μs and 3 outputs are @ 16 V steady state	–	730	1000		At VHV = 20 V VDDA = 3.3 V
$I_{L\_BOOST\_SS0}$	Average inductor current, 3 outputs @ 0 V steady state	–	350	550		At VHV = 20 V VDDA = 3.3 V
$I_{L\_BOOST\_SS2}$	Average inductor current, 3 outputs @ 2 V steady state	–	380	570		At VHV = 20 V VDDA = 3.3 V
$I_{L\_BOOST\_SS16}$	Average inductor current, 3 outputs @ 16 V steady state	–	550	750		At VHV = 20 V VDDA = 3.3 V
I_{VIO_INACT}	VIO average inactive current	–	–	3		VIO is high, no bus activity
I_{VIO_ACTIVE}	VIO average active current	–	–	250		VIO = 1.8 V, master sending data at 26 MHz
V_{VREG}		1.7	–	1.9	V	No external load allowed

Table 4. DC CHARACTERISTICS (T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V<VDDA< 5.5 V; V_{IO} = 1.8 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
LOW POWER MODE						
I_{VDDA}	VDDA Supply Current	–	–	8	μA	
I_{L_BOOST}	L_BOOST Leakage	–	–	6		
I_{BATT}	Battery Current	–	–	14		$I_{VDDA} + I_{L\_BOOST}$
I_{VIO}	VIO Supply Current	–	–	3		No bus activity
V_{VREG}		1.6	–	1.9	V	No external load allowed

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. BOOST CONVERTER CHARACTERISTICS
(VDDA from 2.3 V to 5.5 V; V_{IO} = 1.8 V; T_A = –30 to +85°C; C_{HV} = 22 nF; L_{BOOST} = 15 μH; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VHV_min	Minimum programmable output voltage (average), DAC Boost = 0h	Active mode	–	13	–	V
VHV_max	Maximum programmable output voltage (average), DAC Boost = Fh	Active mode	–	28	–	
Resolution	Boost voltage resolution	4−bit DAC	–	1	–	
$I_{L\_BOOST\_LIMIT}$	Inductor current limit		–	200	–	mA

Table 6. ANALOG OUTPUTS (OUT A, OUT B, OUT C)
(VDDA from 2.3 V to 5.5 V; V_{IO} = 1.8 V; V_{HV} = 26 V; T_A = –30 to +85°C; R_{load} = ∞ unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
SHUTDOWN MODE						
Z_{OUT}	OUT A, OUT B, OUT C output impedance	7	–	–	MΩ	DAC disabled
ACTIVE MODE						
V_{OH}	Maximum output voltage	–	24	–	V	DAC A, B, C = 7Fh, DAC Boost = Fh, I_{OH} < 10 μA
V_{OL}	Minimum output voltage	–	–	1	V	DAC A, B C = 01h, DAC Boost = 0h to Fh, I_{OH} < 10 μA
Slew Rate		–	3	10	μs	2 V to 20 V step, measured at V_{OUT} = 15.2 V, R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF, Turbo enabled
R_{PD}	OUT A, OUT B, OUT C set in pull−down mode	–	–	1000	Ω	DAC A, B C = 00h, DAC Boost = 0h to Fh, selected output(s) is disabled
Resolution	Voltage resolution (1−bit)	–	189	–	mV	(1 LSB = 1−bit)
V_{OFFSET}	Zero scale, least squared best fit	−1	–	+1	LSB	
Gain Error		−3.0	–	+3.0	$\%V_{OUT}$	1 V to 24 V with 26 V VHV
DNL	Differential non−linearity least squared best fit	−0.9	–	+0.9	LSB	1 V to 24 V with 26 V VHV
INL	Integral non−linearity least squared best fit	−1	–	+1	LSB	1 V to 24 V with 26 V VHV
I_{SC}	Over current protection	–	5	65	mA	Any DAC output shorted to ground
V_{RIPPLE}	Output ripple with all outputs at steady state	–	–	40	mV RMS	1 V to 24 V with 26 V VHV

THEORY OF OPERATION

Overview

The control IC outputs are directly controlled by programming the three DACs (DAC A, DAC B, DAC C) through the digital interface.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high−voltage amplifier supplied from the boost converter (see Figure 1 − Control IC Functional Block Diagram).

The control IC output voltages are scaled from 0 V to 24 V, with 128 steps of 189 mV. The nominal control IC output can be approximated to 189 mV x (DAC value).

For performance optimization the boost output voltage (VHV) can be programmed to levels between 13 V and 28 V via the DAC_boost register (4 bits with 1 V steps). The startup default level for the boosted voltage is VHV = 24 V.

For proper operation and to avoid saturation of the output devices and noise issues, it is recommended to operate the boosted VHV voltage at least 2 V (4 V if using Turbo−Charge Mode) above the highest programmed V_{OUT} voltage of any of the three outputs.

Operating Modes

The following operating modes are available:

1. **Shutdown Mode:** All circuit blocks are off, the DAC outputs are disabled and placed in high Z state and current consumption is limited to minimal leakage current. The shutdown mode is entered upon initial application of VDDA or upon VIO being placed in the low state. The contents of the registers are not maintained in shutdown mode.
2. **Startup Mode:** Startup is only a transitory mode. Startup mode is entered upon a VIO high state. In startup mode all registers are reset to their default states, the digital interface is functional, the boost converter is activated, outputs OUT A, OUT B, OUT C are disabled and the DAC outputs are placed in a high Z state. Control software can request a full hardware and register reset of the TCC−303 by sending an appropriate PWR_MODE command to direct the chip from either the active mode or the low power mode to the startup mode. From the startup mode the device automatically proceeds to the active mode.
3. **Active Mode:** All blocks of the TCC−303 are activated and the DAC outputs are fully controlled through the digital interface, DACs remain off until enabled. The DAC settings can be dynamically modified and the HV outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or switched off according to application requirements. Active mode is automatically entered from the startup mode. Active mode can also be entered from the low power mode under control software command.
4. **Low Power Mode:** In low power mode the serial interface stays enabled, the DAC outputs are disabled and are placed in a high Z state and the boost voltage circuit is disabled. Control software can request to enter the low power mode from the active mode by sending an appropriate PWR_MODE command. The contents of all registers are maintained in the low power mode.

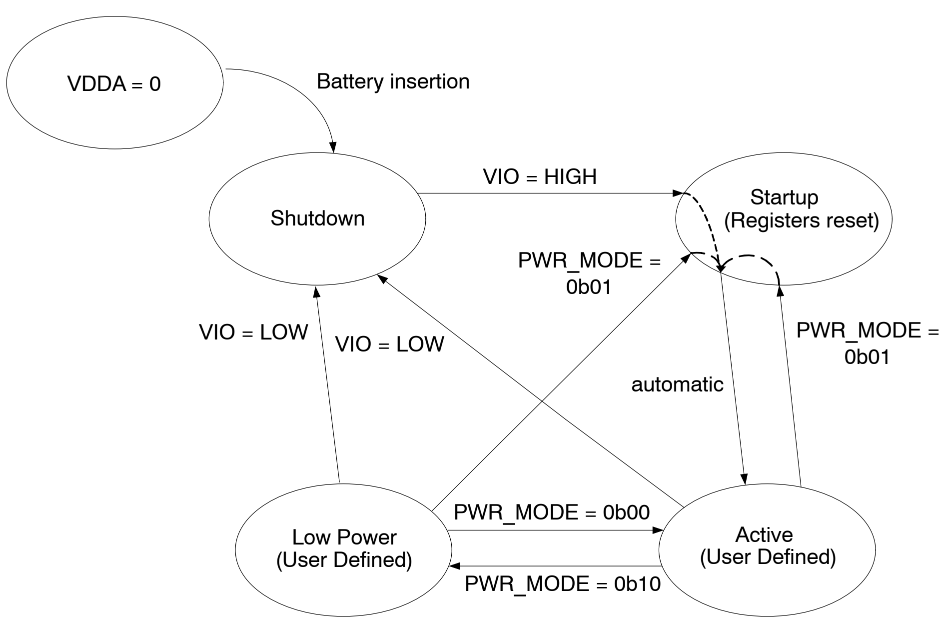


Figure 3. Modes of Operation

VDDA Power−On Reset (POR)

Upon application of VDDA, TCC−303 will be in shutdown mode. All circuit blocks are off and the chip draws only minimal leakage current.

VIO Power−On Reset and Startup Conditions

A high level on VIO places the chip in startup mode which provides a POR to TCC−303. POR resets all registers to their default settings as described in Register Content Details. VIO POR also resets the serial interface circuitry. POR is not a brown−out detector and VIO needs to be brought back to a low level to enable the POR to trigger again.

Table 7. VIO POWER−ON RESET AND STARTUP

Register	Default State for VIO POR	Comment
DAC Boost	[1011]	VHV = 24 V
Power Mode	[01]>[00]	Transitions from shutdown to startup and then automatically to active mode
DAC Enable	[000]	V_{OUT} A, B, C Disabled
DAC A		Output in High−Z Mode
DAC B		Output in High−Z Mode
DAC C		Output in High−Z Mode

VIO Shutdown

A low level at any time on VIO places the chip in shutdown mode in which all circuit blocks are off. The contents of the registers are not maintained in shutdown mode.

Table 8. VIO THRESHOLDS (VDDA from 2.3 V to 5.5 V; T_A = –30 to +85°C unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comments
VIORST	VIO Low Threshold	–	–	0.2	V	When VIO is lowered below this threshold level the chip is reset and placed into the shutdown mode

Power Supply Sequencing

The VDDA input is typically directly supplied from the battery and thus is the first on. After VDDA is applied and before VIO is applied to the chip, all circuits are in the shutdown mode and draw minimum leakage currents. Upon application of VIO, the chip automatically starts up using default settings and is placed in the active state waiting for a command via the serial interface.

Table 9. TIMING (VDDA from 2.3 V to 5.5 V; V_{IO} = 1.8 V; T_A = –30 to +85°C; OUT A, OUT B, OUT C; CHV = 47 nF; L_{BOOST} = 15 μH; VHV = 20 V; Turbo−Charge mode off unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comments
T_{POR_VREG}	Internal bias settling time from shutdown to active mode	–	50	120	μs	For info only
T_{BOOST_START}	Time to charge CHV @ 95% of set VHV	–	130	–	μs	For info only
$T_{SD\_TO\_ACT}$	Startup time from shutdown to active mode	–	180	300	μs	
T_{SET+}	Timing for a 2 V to 16 V transition, measured when voltage reaches within 5% of target voltage, measured between the R (5.6 kΩ) and C (2.7 nF) of an equivalent PTIC series load.	–	50	60	μs	Voltage settling time connected on V_{OUT} A, B, C
T_{SET-}	Timing for a 16 V to 2 V transition, measured when voltage reaches within 5% of target voltage, measured between the R (5. 6 kΩ) and C (2.7 nF) of an equivalent PTIC series load.	–	50	60	μs	Effective PTIC tuning voltage settling time, measured between an equivalent R and C PTIC load
T_{SET+}	Output A, B, C positive settling time with Turbo	–	35	–	μs	Voltage settling time connected on V_{OUT} A, B, C
T_{SET-}	Output A, B, C negative settling time with Turbo	–	35	–	μs	Voltage settling time connected on V_{OUT} A, B, C

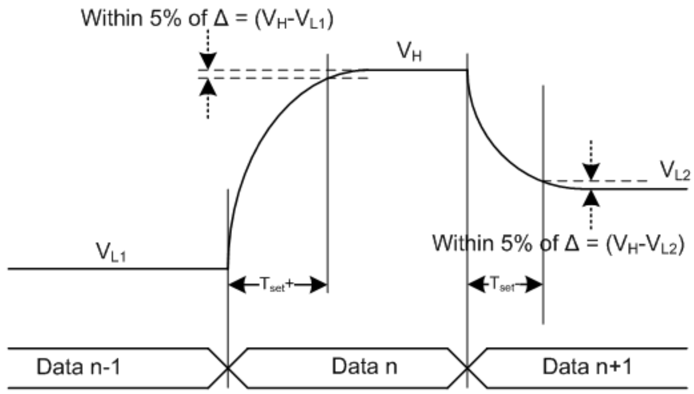


Figure 4. Output Settling Diagram

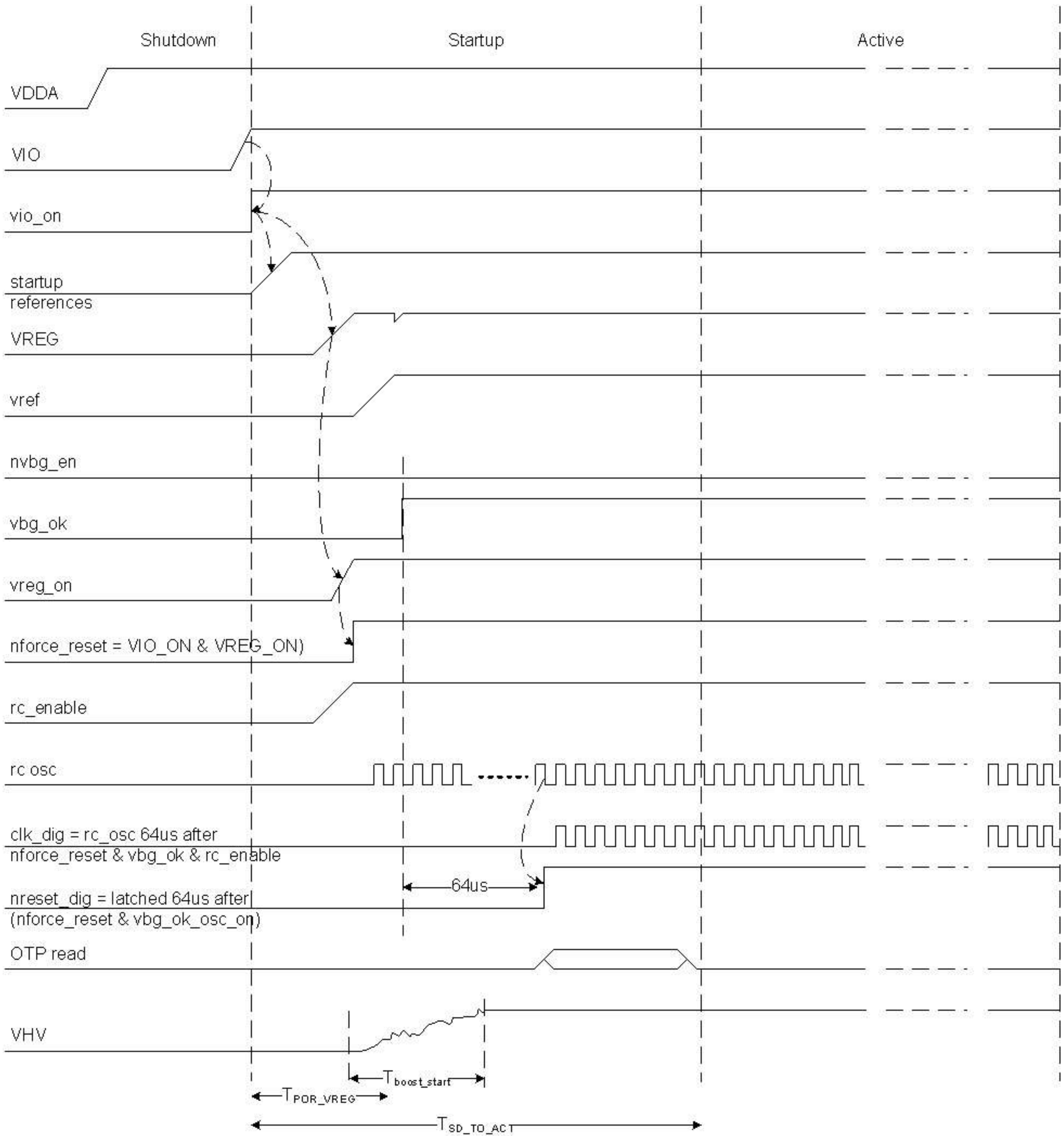


Figure 5. Startup Timing Diagram

Boost Control

TCC−303 integrates an asynchronous current control boost converter. It operates in a discontinuous mode and features spread−spectrum circuitry for Electro−Magnetic Interference (EMI) reduction. The average boost clock is 2 MHz and the clock is spread between 0.8 MHz and 4 MHz.

Boost Output Voltage (VHV) Control Principle

The asynchronous control starts the boost converter as soon as the VHV voltage drops below the reference set by the 4−bit DAC and stops the boost converter when the VHV voltage rises above the reference again.

Due to the slow response time of the control loop, the VHV voltage may drop below the set voltage before the control loop compensates for it. In the same manner, VHV can rise higher than the set value. This effect may reduce the maximum output voltage available. Please refer to Figure 6 below.

The asynchronous control reduces switching losses and improves the output (VHV) regulation of the DC/DC converter under light load, particularly in the situation where TCC−303 only maintains the output voltages to fixed values.

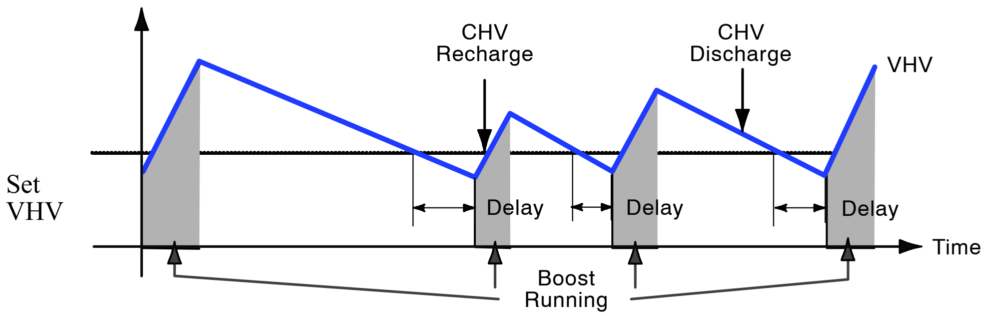


Figure 6. VHV Voltage Waveform

High Impedance (High Z) Feature

In shutdown mode the OUT pins are set to a high impedance mode (high Z). Following is the principle of operation for the control IC:

1. The DAC output voltage V_{OUT} is defined by:

$$V_{OUT} = \frac{\text{DAC code}}{127} \times 24\ \text{V} \qquad \text{(eq. 1)}$$

2. The voltage VHV defines the maximum supply voltage of the DAC supply output regulator and is set by a 4−bit control.
3. The maximum DAC DC output voltage V_{OUT} is limited to (VHV – 2 V). DAC can achieve higher output voltages, but timing is not maintained for swings above VHV – 2 V.
4. The minimum output DAC voltage V_{OUT} is 1.0 V max.

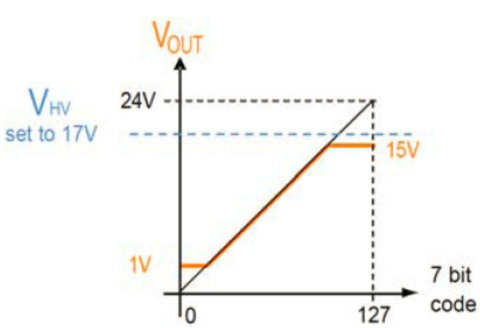


Figure 7. DAC Output Range Example A

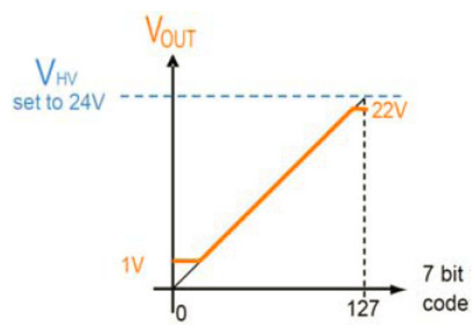


Figure 8. DAC Output Range Example B

Digital Interface

The control IC is fully controlled through a digital interface (DATA, CLK). The digital interface is described in the following sections of this document.

Turbo−Charge Mode

The TCC−303 control IC has a Turbo−Charge Mode that significantly shortens the system settling time when changing programming voltages.

In Turbo−Charge Mode the DAC output target voltage is temporarily set to either a delta voltage above or a delta voltage below the actual desired target. The delta voltage is 4 volts.

After the DAC value message is received, the delta voltage is calculated by hardware, and is applied in digital format to the input of the DAC, right after trigger is received. The period for which the delta voltage is maintained to the input of the DAC, the Turbo time, is calculated based on following considerations:

- DAC_TIMER_A[4:0] / DAC_TIMER_B[4:0] / DAC_TIMER_C[4:0]: These are the DAC timer configuration fields. For the turbo mode, they define the turbo latency value, when the target+delta voltage is active. If each DAC is updated over and over with the same turbo delay value, these fields do NOT need to be updated at each DAC update. The register has to hold a non−zero value for a Turbo update.
- DAC_TC2X_A / DAC_TC2X_B / DAC_TC2X_C: If these bits are set, the timer loads DAC_TIMER_X * 2 value as opposed to DAC_TIMER_X value. This allows a turbo operation delay up to 124 μs.
- DAC_TCM_A [1:0] / DAC_TCM_B [1:0] / DAC_TCM_C [1:0] : If the Turbo direction is down and the Turbo target is below 4 V, these multiplication factors are utilized to extend the turbo delay. Further formula provided below.
- GL_A / GL_B / GL_C: These are the DAC update mode configuration fields, which need to be set to turbo mode at the new DAC value update and prior to the SW trigger (optional). These bits are part of the DAC value register. If they are set to 0, the DAC is in Turbo Mode, as long as the corresponding DAC_TIMER register is non−zero. A DAC_TIMER =0 means an immediate update independent of the GL_A/B/C value.
- The Turbo UP or DOWN voltage is decided based on the comparison of the new DAC value and the old DAC value. If the new value is greater, the turbo direction will be UP. Otherwise it will be down. In case of both DAC values being equal, there is no DAC update applied.After a turbo request is received, any trigger will start the turbo output transition. The trigger could be:
  - A MIPI−RFFE software trigger controlled by RFFE_PM_TRIG register
  - An internal generated trigger after the corresponding DAC value is updated, as described in section **DAC Update Triggering.**

The DAC values send by digital turbo−charge logic to DACs are:

- During turbo−charge delay duration the value applied is “DAC_new ±4 V” (the polarity of the 4 V turbo will depend on if turbo charge is up or down)
- If DAC_new > DAC old, and DAC_new+4 V is exceeding the word length of the DAC, it is saturated to max value possible.
- If DAC_new < DAC_old, and DAC_new−4 V is a negative number, a DAC value of 0 is applied.
  - After turbo−charge delay duration the value applied is the actual DAC_new.

Table 10. DAC_TIMER_A/B/C UNIT DELAYS

DAC_TIMER_A/B/C [4:0]					Turbo delay time in Turbo Mode or glide step duration in Glide Mode [μs]
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	Immediate Update
0	0	0	0	1	2
0	0	0	1	0	4
0	0	0	1	1	6
0	0	1	0	0	8
0	0	1	0	1	10
0	0	1	1	0	12
0	0	1	1	1	14
0	1	0	0	0	16
0	1	0	0	1	18
0	1	0	1	0	20
0	1	0	1	1	22
0	1	1	0	0	24
0	1	1	0	1	26
0	1	1	1	0	28
0	1	1	1	1	30
1	0	0	0	0	32
1	0	0	0	1	34
1	0	0	1	0	36
1	0	0	1	1	38
1	0	1	0	0	40
1	0	1	0	1	42
1	0	1	1	0	44
1	0	1	1	1	46
1	1	0	0	0	48
1	1	0	0	1	50
1	1	0	1	0	52
1	1	0	1	1	54
1	1	1	0	0	56
1	1	1	0	1	58
1	1	1	1	0	60
1	1	1	1	1	62

The value of turbo delay time is deducted based on the hardware comparison of new DAC value in respect to old DAC value, as follows. In this calculation the decimal “21” value corresponds to 4 V DAC drive. As the DAC new value is closer to 0 V in a down Turbo, the delay time increases more.

If DAC new > DAC old, then T_{UP} = DAC_TIMER_A/B/C << DAC_TC2X_A/B/C

If DAC new < DAC old, and DAC new < 21, then T_{DOWN} = DAC_TIMER_A/B/C << DAC_TC2X_A/B/C + DAC_TCM_A/B/C * (21 – DAC new)

If DAC new < DAC old, and DAC new > 21, then T_{DOWN} = DAC_TIMER_A/B/C << DAC_TC2X_A/B/C

If DAC new < DAC old, and DAC new = 21, then T_{DOWN} = DAC_TIMER_A/B/C << DAC_TC2X_A/B/C

Table 11. TURBO−CHARGE MULTIPLICATION FACTOR

TCM [1:0]	Multiplication Factor
00 (default)	4
01	3
10	2
11	1

Transition from Turbo to Turbo or Immediate Update

In the event a new trigger is received during a turbo transition, the ongoing turbo operation is halted and the new DAC value is applied immediately. There won't be any Turbo and the hi_slew is kept low.

Transition from Turbo to Glide

In the event that a new glide transition is triggered during a turbo event, then the turbo process is stopped and the current target value is set at the DAC output immediately without hi_slew. The new glide is started from this value.

DAC disable during Turbo (including active to low power mode transition)

If the DAC, which is in Turbo is disabled, the target DAC value is immediately applied without hi_slew. The DAC does not continue with the Turbo when it is re−enabled.

Glide Mode

The TCC−303 control IC has a Glide Mode that significantly extends the system transition time when changing programming voltages.

Glide Mode is controlled by the following registers:

- DAC_TIMER_A[4:0] / DAC_TIMER_B[4:0] / DAC_TIMER_C[4:0]: These are the DAC timer configuration fields. For the glide mode they define the step duration. If each DAC is updated over and over with the same glide step, these fields do NOT need to be updated at each DAC update. The register has to hold a non−zero value for a Glide update.
- GL_A / GL_B / GL_C: These are the DAC update mode configuration fields, which need to be set to glide mode at the new DAC value update and prior to the SW trigger (optional). These bits are part of the DAC value register. If they are set to 1, the DAC is in glide mode, as long as the corresponding DAC_TIMER register is non−zero. A DAC_TIMER =0 means an immediate update independent of the GL_A/B/C value.

After a Glide request is received, any trigger will start the Glide output transition.

The trigger could be:

- a MIPI−RFFE software trigger controlled by RFFE_PM_TRIG register
- an internal generated trigger after the corresponding DAC value is updated, as described in a later section.

Immediately after the trigger, the DAC_old value is loaded in the MSB's of the upper byte of a 15 bit accumulator, while the lower byte of accumulator is being reset to 0x00.

At the same time a count step is calculated:

GLIDE_STEP[6:0] = DAC_new − DAC_old; if DAC_new > DAC_old

GLIDE_STEP[6:0] = DAC_old − DAC_new; if DAC_new < DAC_old

ACCUMULATOR[14:0] = DAC_old, 0x00;

NOTE: Glide is disabled if DAC_new = DAC_old.

From the moment the trigger is received, a tick is generated internally, with a frequency controlled by the DAC_TIMER_A/B/C registers. Each DAC has its own tick generator running independently of the other DAC. Each time a trigger is received for a DAC, the setting of the DAC_TIMER_A/B/C register is sampled in a counter dedicated to that DAC. Any update of the DAC_TIMER_A/B/C register after trigger is received will be ignored until the next trigger is received

Each time a tick is generated, the content of the accumulator is either incremented or decremented, depending whether DAC_new is either bigger or smaller than DAC_old.

ACCUMULATOR[14:0] = ACCUMULATOR[14:0] + GLIDE_STEP; if DAC_new > DAC_old

ACCUMULATOR[14:0] = ACCUMULATOR[14:0] − GLIDE_STEP; if DAC_new < DAC_old

Each time a tick is generated, the output of the DAC[6:0] is updated with the value of ACCUMULATOR[14:8];

The Gliding process continues until, upper 7 bits of the accumulator matches the value of the DAC_new.

ACCUMULATOR[14:8] ≥ DAC_new, when DAC_new > DAC_old

ACCUMULATOR[14:8] ≤ DAC_new, when DAC_new < DAC_old

The Glide timer will reference the 2 MHz clock divided to provide between 2 μs and 62 μs per glide step.

Each DAC is independent in terms of its switching operation, thus each DAC may be independently programmed for Normal, Turbo or Glide regardless of the switching operation of the other DACs.

Use−case hint:

In a scenario where the Turbo delay needs to be set to 54 us and the glide should be taking ~7 ms, the DAC_TIMER can be configured as 7000/256 = 27 μs and the DAC_TC2X configuration can be set. This way the timer value would not need to be updated during the glide – turbo switches, and only the GL_X bit in DAC value update needs to be toggled.

Transition from Glide to Glide

In the event a new glide request is received during a glide transition, the ongoing glide operation is halted and the new glide operation is started from the DAC value, where the previous glide has left off. The DAC timers can be updated to a new value at the trigger.

Transition from Glide to Turbo or Normal Switching

In the event that a new Normal switching or Turbo DAC value is received during a Glide transition, then the Glide process is stopped and the DAC immediately switches to the newly received target value without Turbo or Glide. The hi_slew is not applied.

DAC Disable during Glide (including active to low power mode transition)

If the DAC, which is gliding is disabled, the DAC value holds on to the value where the glide stops. The DAC does not continue with the glide when it is re−enabled. It drives the last calculated DAC value without a hi_slew.

DAC Update Triggering

The entire digital logic responsible for DAC updates is using the clock provided by the internal RC oscillator. In order to minimize the power consumption, the RC clock is set at a low frequency around 2 MHz.

DAC Writes

Figure 9 shows the diagram of the DAC data path, from the moment data is written into DACx_value register, until it is sent out to DAC.

After the DACx_value register is written using MIPI−RFFE clock, the data is copied on RC clock domain, into the first data stage represented in Figure 9 as ‘Completed’. The data is moved into ‘New’ and ‘DAC−Out’ stages by the DAC driver state machine, once the trigger is detected. The Turbo path also highlights the glide calculation.

If SW trigger is not enabled, then data will flow through the stages right after the corresponding DAC is updated, without waiting for a trigger (MIPI write is considered as the trigger).

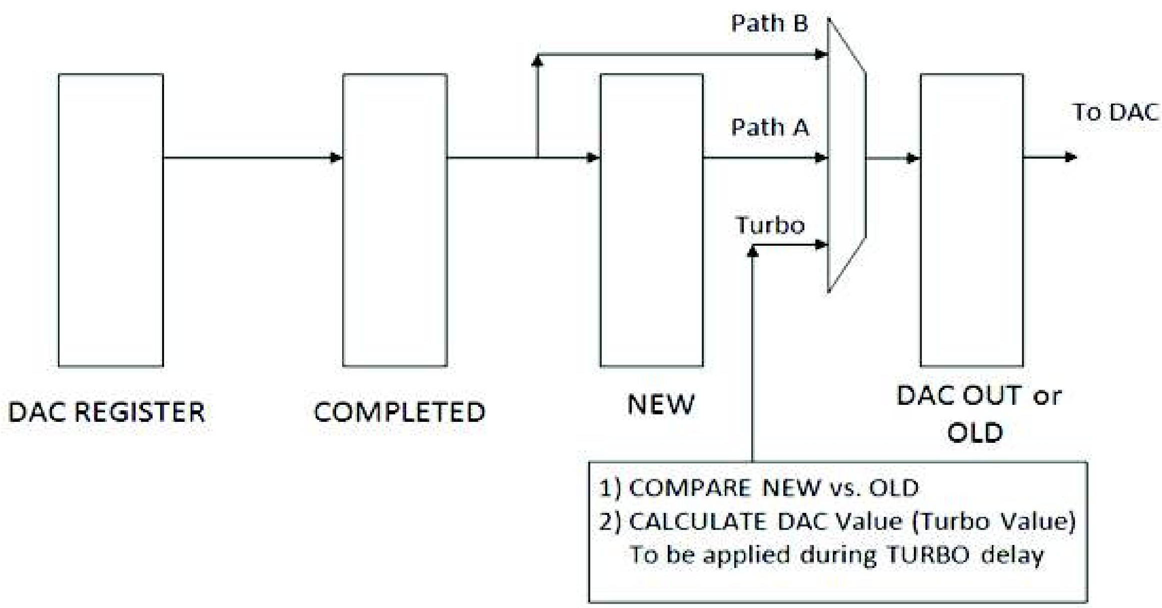


Figure 9. DACx Data Path

To bypass the SW trigger and enable an immediate trigger the Mask bits under the RFFE_PM_TRIG register should be set according to the USID control of the DAC. Trigger Mask 2 is controller with USID_2, Trigger Mask 1 is controlled with USID_1 and Trigger Mask 0 is controlled with USID_0. In MIPI−RFFE configuration, if RFFE_PM_TRIG / Trigger_Mask_2 = ‘1’, and RFFE_PM_TRIG / Trigger_Mask_1 = ‘1’ and RFFE_PM_TRIG / Trigger_Mask_0 = ‘1’ (all software triggers are masked), then each DAC value is copied into ‘Completed’ stages of each DAC, after the messages RFFE_REG_0x06, RFFE_REG_0x07 or RFFE_REG_0x08 respectively are received, as shown in following sequence.

MIPI_RFFE_WRITE #1: send DAC_A_value and glide/turbo mode to RFFE_REG_0x06

MIPI_RFFE_WRITE #2: send DAC_B_value and glide/turbo mode to RFFE_REG_0x07

MIPI_RFFE_WRITE #3: send DAC_C_value and glide/turbo mode to RFFE_REG_0x08

The individual writes above could be combined into a single extended write with all DACs controlled with the same USID or the DURs of the DACs are sitting at “11” configuration. Right after MIPI_RFEE_WRITE #1 to RFFE_REG_0x06, above, is received the DAC_A value register is copied in ‘Completed’ stage of DAC_A. The timers DO NOT need to be updated for each DAC update. But if they need to be, they can be updated as part of a full extended write or single write prior to the DAC value updates without any timing limitation. Since the SW trigger is masked, next RC clock cycle after DAC values are copied in ‘Completed’ stage, the data will move in next stages ‘New’ and ‘DAC−Out’ without waiting for any trigger.

The similar events occur for DAC_B and DAC_C after the MIPI_RFEE_WRITE #2 and MIPI_RFEE_WRITE #3.

Due to the fact that the MIPI−RFFE master can send DAC updates messages at a higher frequency, than RC clock, the data buffer ‘Completed’, can be overwritten if new DAC updates occur in the same time when the buffer is loaded.

While data and configuration are copied from DACx_value register into ‘Completed’ stage, the MIPI−RFFE master must not send any new DAC updates to DACx_value registers or configurations. The time required for the data to be copied from DACx_value register into ‘Completed’ stage is Max 1500 ns, which is defined by the three RC clock cycles required to synchronize data from MIPI−RFFE clock domain to RC clock domain.

In Figure 10, DAC_UPDATE_LAT represents the period when MIPI−RFFE master is not allowed to send any new DAC updates to DACx_value registers and DAC configuration registers.

The DAC enables (RFFE_REG_0x00) and Booster configurations (RFFE_REG_0x02) are applied immediately without waiting any trigger. These registers should be configured prior, so that the DAC updates are effective as fast as possible. In test mode the hi_slew settings are sampled at the trigger similar to the dac_timers.

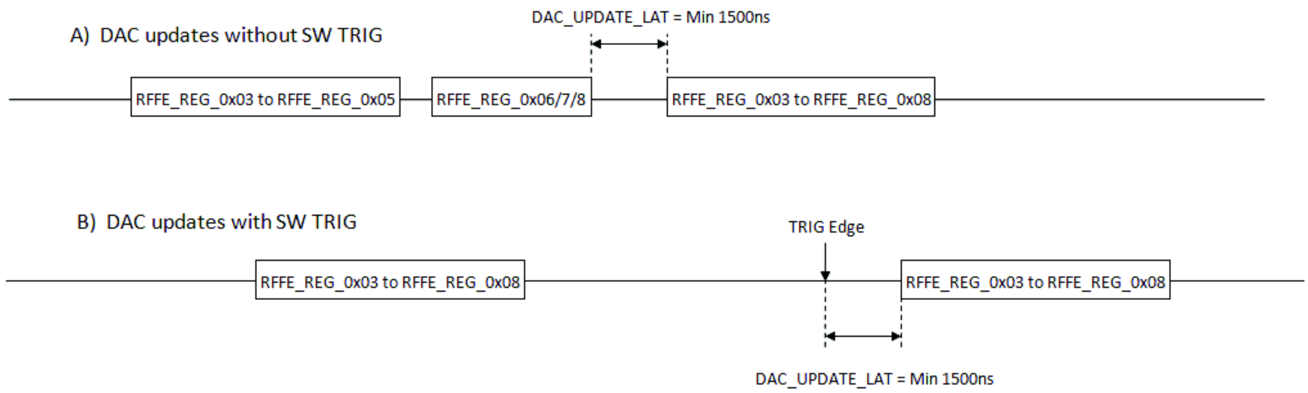


Figure 10. DAC_UPDATE_LAT Requirement

The SW trigger as well as immediate trigger can be configured in many combinations using the DUR settings of the DACs and the USID values. The SW trigger masks can only be changed with the write access using the slave address of their corresponding USID. But the corresponding triggers can be set by accesses over broadcast, with broadcast ID (0x0) or GSID.

The triggering and DAC register access is governed by these rules:

- The DUR configuration assigns a DAC to a USID. The corresponding DAC registers can only be accessed with USID defined by its DUR.
- The immediate update of this DAC is enabled if the SW trigger mask of the corresponding USID is set (disabled).
- The PM_TRIG register bit0 (SW trigger0) is masked by bit4 and assigned to DACs triggering, which are mapped to USID0 or all USIDs (the DAC DUR=0 or 3).
- The PM_TRIG register bit1 (SW trigger1) is masked by bit5 and assigned to DACs triggering, which are mapped to USID1 or all USIDs (the DAC DUR=1 or 3).
- The PM_TRIG register bit2 (SW trigger2) is masked by bit6 and assigned to DACs triggering, which are mapped to USID2 or all USIDs (the DAC DUR=2 or 3).
- For a DAC with DUR=3, all SW masks need to be set for that DAC to be triggered with direct access to its target register.

If all DACs are kept at DUR values of 3 and the USIDs are kept the same (reset condition), the part behaves according to the MIPI spec with single USID. If some of the USIDs are different while DUR=3, the part responds to the accesses with these different USIDs the same fashion.

If all USIDs are kept equal, the part functions with a single USID. But the DUR settings still control the SW trigger mapping for the DACs independent of the USID values. The DACs which are not holding a DUR value of 3 will be under the control of the SW trigger−mask duo mapped by their DUR setting.

In Table 12 some example register settings for listed functionality are provided. For the given functionality the response of the part to DAC updates and SW triggers are tabulated. In this table the “DAC trigger” corresponds to a trigger happening at the time of the DAC value update. The “SW trigger” corresponds to a trigger happening with the PM_TRIG register write. At this point, it is assumed that the DACs are enabled and the new DAC value is not matching to the existing pre−triggered DAC value in the active register. Some of the abbreviations utilized in the table are:

TRG = successful trigger of the new targets

HLD = no trigger, hold on to existing DAC drives

WR = The new DAC values are captured into RFFE shadow registers

NW = The RFFE write to shadow registers are blocked, no register update.

Table 12. IMMEDIATE vs SOFTWARE TRIGGERING USING USIDs and DURs

FUNCTIONALITY & EXAMPLE REGISTER VALUES	DACA WR ID0	DACA WR ID1	DACA WR ID2	DACA WR Broad	Trigger 3b111 ID0	Trigger 3b111 ID1	Trigger 3b111 ID2	Trigger 3b111 Broad	Trigger 3b001 Broad	Trigger 3b010 Broad	Trigger 3b100 Broad	Comments
(DEFAULT) DAC TRIGGER – SINGLE USID – DUR=3 DUR_A = 3 (USIDx, TRGx) SW–TRG Mask = 3'b111 USID0,1,2 = 4b0111	TRG (WR)	TRG (WR)	TRG (WR)	HLD (NW)	HLD	HLD	HLD	HLD	HLD	HLD	HLD	All USIDs are the same. All SW triggers are masked. The USID DAC writes trigger immediately.
SW TRIGGER –SINGLE USID – DUR =3 DUR_A = 3 (USIDx, TRGx) SW–TRG Mask = 3'b101 USID0,1,2 = 4b0111	HLD (WR)	HLD (WR)	HLD (WR)	HLD (NW)	TRG	TRG	TRG	TRG	HLD	TRG	HLD	All USIDs are the same. Only trigger 1 is enabled. This enables the SW trigger since DUR=3, mapping the DAC to all triggers
DAC TRIGGER –SINGLE USID – DUR=0 DUR_A = 0 (USID0, TRG0) SW–TRG Mask = 3'b101 USID0,1,2 = 4b0111	TRG (WR)	TRG (WR)	TRG (WR)	HLD (NW)	HLD	HLD	HLD	HLD	HLD	HLD	HLD	All USIDs are the same. Only trigger 1 is enabled. The DUR of the DAC is mapping it to trigger 0 (masked). Therefore SW trigger is disabled.
SW TRIGGER –SINGLE USID – DUR =1 DUR_A = 1 (USID1, TRG1) SW–TRG Mask = 3'b101 USID0,1,2 = 4b0111	HLD (WR)	HLD (WR)	HLD (WR)	HLD (NW)	TRG	TRG	TRG	TRG	HLD	TRG	HLD	All USID's are the same. Only trigger 1 is enabled. The DUR of the DAC is mapping it to trigger 1 (enabled). Therefore SW trigger is enabled.
DAC TRIGGER – (1,2) USIDs – DUR=2 DUR_A = 2 (USID2, TRG2) SW–TRG Mask = 3'b100 USID0,1 = 4b0111, USID2 = 4b1000	HLD (NW)	HLD (NW)	TRG (WR)	HLD (NW)	HLD	HLD	HLD	HLD	HLD	HLD	HLD	USID2 is different, only USID2 dac access is allowed and the DAC triggers immediately, since the SW trigger mask is set.
SW TRIGGER – (1,2) USIDs – DUR =2 DUR_A = 2 (USID2, TRG2) SW–TRG Mask = 3'b000 USID0,1 = 4b0111, USID2 = 4b1000	HLD (NW)	HLD (NW)	HLD (WR)	HLD (NW)	HLD	HLD	TRG	TRG	HLD	HLD	TRG	USID2 is different, only USID2 dac access is allowed. Trigger 2 is unmasked, SW trigger is enabled. Only trigger 2 is active for USID2.
DAC TRIGGER – (2,1) USIDs – DUR = 1 DUR_A = 1 (USID1, TRG1) SW–TRG Mask = 3'b110 USID0,1 = 4b0111, USID2 = 4b1000	TRG (WR)	TRG (WR)	HLD (NW)	HLD (NW)	HLD	HLD	HLD	HLD	HLD	HLD	HLD	Since USID0 = USID1 both USID0, USID1 DAC target writes are allowed. SW trigger1 masked; SW triggering disabled
SW TRIGGER – (2,1) USIDs –DUR = 1 DUR_A = 1 (USID1, TRG1) SW–TRG Mask = 3'b100 USID0,1 = 4b0111, USID2 = 4b1000	HLD (WR)	HLD (WR)	HLD (NW)	HLD (NW)	TRG	TRG	HLD	TRG	HLD	TRG	HLD	Same as above but SW trigger 1 is enabled; SW triggering enabled. USID0, USID1 are the same but the DAC is mapped to Trg1 only. Trg0 alone does not trigger.
DAC TRIGGER – (1,1,1) USIDs – DUR = 0 DUR_A = 0 (USID0, TRG0) SW–TRG Mask = 3'b001 USID0 = 4b0111, USID1 = 4b1000, USID2 = 4b1001	TRG (WR)	HLD (NW)	HLD (NW)	HLD (NW)	HLD	HLD	HLD	HLD	HLD	HLD	HLD	The DAC is mapped to USID0 and the corresponding trigger is masked. It triggers immediately at DAC update with USID0
SW TRIGGER – (1,1,1) USIDs – DUR = 0 DUR_A = 0 (USID0, TRG0) SW–TRG Mask = 3'b000 USID0 = 4b0111, USID1 = 4b1000, USID2 = 4b1001	HLD (WR)	HLD (NW)	HLD (NW)	HLD (NW)	TRG	HLD	HLD	TRG	TRG	HLD	HLD	The DAC is mapped to USID0 and the TRG0 is enabled. It triggers only at TRG0 with USID0 or Broadcast access

MIPI RFFE Interface

TCC−303 is a slave device and is fully compliant to the MIPI Alliance Specification for RF Front−End Control Interface (RFFE) Version 1.10.00.

Following MIPI RFFE commands are supported:

1. Register 0 WRITE
2. Register WRITE
3. Register READ
4. Extended Register WRITE
5. Extended Register READ

Registers 0x00 to 0x1F are available to be read/written. At full−speed read with heavy load, the RFFE read mode bit RFFE_RDM can be configured to ‘1’, to shift the data capture to falling edge. Otherwise it is recommended to keep this bit in its default state, since the falling edge read data capture is a violation for RFFE interface standard. The violation is due to the toggling during the 2nd half of the bus park cycle, which could create bus contention with the master.

The extended register write long and read long commands are not supported. If an extended register write long command is received, no register is written and the RFFE_STATUS.WURE flag is set. If an extended register read long command is received, the part responds with bus idle and the RFFE_STATUS.RURE flag is set.

The read access to registers RFFE_REG_0x03 to RFFE_REG_0x08 returns the active register content, which is the register updated after a trigger. The pre−trigger shadow register does not have read access.

Table 13. MIPI RFFE INTERFACE SPECIFICATION
(T_A = −30 to +85°C; 2.3 V < VDDA < 5.5 V; 1.1 V < V_{IO} < 1.8 V; unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comments
F_{SCLK}	Clock Full−Speed Frequency	0.032	–	26	MHz	Full−Speed Operation: 1.65 V < V_{IO} < 1.95 V
T_{SCLK}	Clock Full−Speed Period	0.038	–	32	μs	Full−Speed Operation: 1.65 V < V_{IO} < 1.95 V
T_{SCLKIH}	CLK Input High Time	11.25	–	–	ns	Full−Speed
T_{SCLKIL}	CLK Input Low Time	11.25	–	–	ns	Full−Speed
V_{TP}	Positive Going Threshold Voltage	0.4 x VIO	–	0.7 x VIO	V	CLK, DATA, 1.2 or 1.8 V Bus
V_{TN}	Negative Going Threshold Voltage	0.3 x VIO	–	0.6 x VIO	V	CLK, DATA, 1.2 or 1.8 V Bus
V_H	Hysteresis Voltage ($V_{TP} - V_{TN}$)	0.1 x VIO	–	0.4 x VIO	V	CLK, DATA, 1.2 or 1.8 V Bus
I_{IH}	Input Current High	−2	–	+10	μA	SDATA = 0.8 x VIO
		−1	–	+10	μA	SCLK = 0.8 x VIO
I_{IL}	Input Current Low	−2	–	+1	μA	SDATA = 0.2 x VIO
		−1	–	+1	μA	SCLK = 0.2 x VIO
C_{CLK}	Input Capacitance	–	–	2.2	pF	CLK Pin
C_{DATA}	Input Capacitance	–	–	2.5	pF	DATA Pin
TD_{SETUP}	Write DATA Setup Time	–	–	1	ns	Full−Speed
TD_{HOLD}	Write DATA Hold Time	–	–	5	ns	Full−Speed
T_{READ_ACCESS}	Read DATA valid from CLK rising edge	–	–	7.11	ns	Full Speed at V_{IO} = 1.80 V, +25°C, and max 15 pF load on DATA pin
T_{READ_ACCESS}	Read DATA valid from CLK rising edge	–	–	9.11	ns	Full Speed at V_{IO} = 1.80 V, +25°C, and max 50 pF load on DATA pin

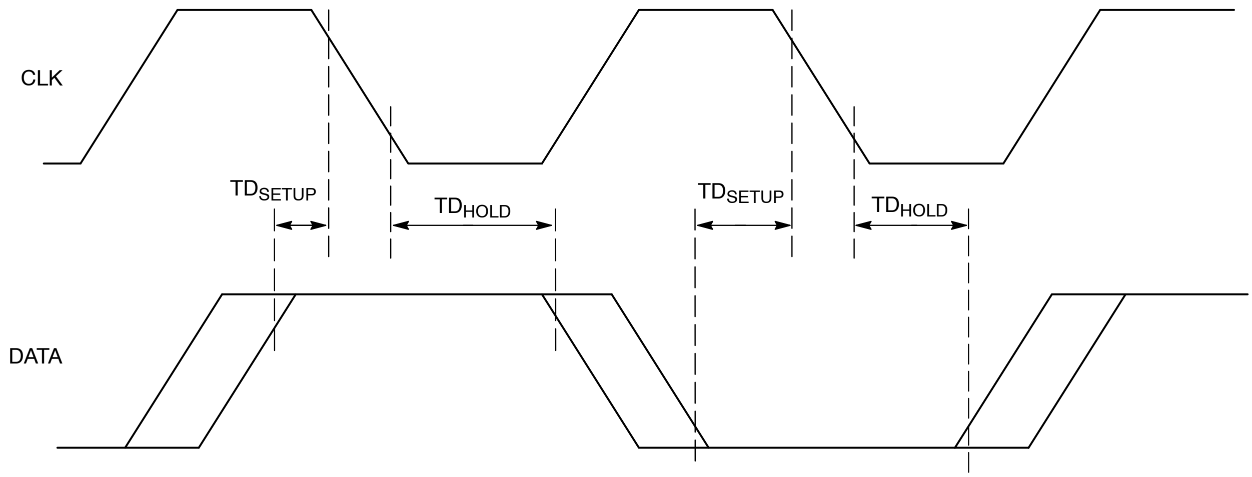


Figure 11. MIPI−RFFE Signal Timing during Master Writes to PTIC Control IC

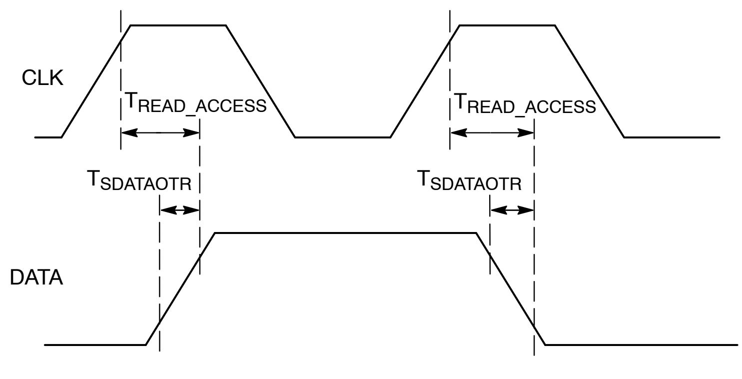


Figure 12. MIPI−RFFE Signal Timing during Master Reads from PTIC Control IC

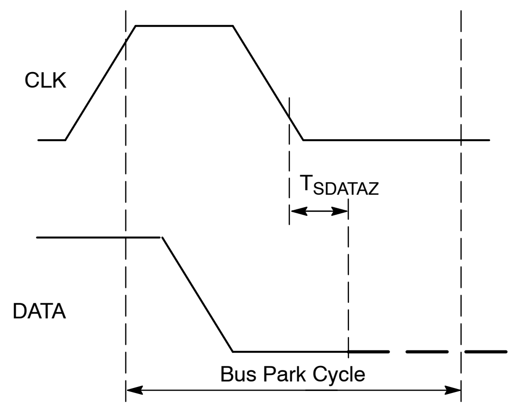


Figure 13. Bus Park Cycle Timing when MIPI−RFFE Master Reads from PTIC Control IC

The control IC contains eighteen 8−bit registers. Register content is described in Table 14. Some additional registers implemented as provision, are not described in this document.

Table 14. MIPI RFFE ADDRESS MAP

Address	Description	USID	Purpose	Access	Size [bits]
0x00	RFFE_REG_0x00	All	DAC enables	R/W RegWrite0	8
0x01	RFFE_REG_0x01	All	DUR for DAC_A/_B/_C	R/W	8
0x02	RFFE_REG_0x02	All	Booster settings	R/W	8
0x03	RFFE_REG_0x03	DUR_A	DAC_A timer setup	R/W	8
0x04	RFFE_REG_0x04	DUR_B	DAC_B timer setup	R/W	8
0x05	RFFE_REG_0x05	DUR_C	DAC_C timer setup	R/W	8
0x06	RFFE_REG_0x06	DUR_A	Used to set up / trigger OUT A	R/W	8
0x07	RFFE_REG_0x07	DUR_B	Used to set up / trigger OUT B	R/W	8
0x08	RFFE_REG_0x08	DUR_C	Used to set up / trigger OUT C	R/W	8
0x09	RFFE_REG_0x09	All	RFFE read mode control	R/W	8
0x09 to 0x17	SPARE	N/A	Spare for future product development	R/W	8
0x18	USID_1	USID_1 & Broadcast	Spare [7:6] [5,4] = Manufacturer ID [9:8] USID_1 [3:0]	R/W	8
0x19	USID_2	USID_2 & Broadcast	Spare [7:6] [5,4] = Manufacturer ID [9:8] USID_2 [3:0]	R/W	8
0x1A	RFFE_STATUS	All	RFFE status register	R/W	8
0x1B	RFFE_GROUP_SID	All	The Group Broadcast ID	R/W	8
0x1C	RFFE_PM_TRIG	All & Broadcast	Power Mode & Trigger Control PWR_MODE [7:6] TRIG_REG [5:0]	R/W	8
0x1D	PID_0, default	All	MIPI Product ID (Note 2)	R	8
0x1E	Manufacturer ID Register	All	MN (10bits long) Manufacturer ID[7:0] (Note 2)	R	8
0x1F	USID_0, default	USID_0 & Broadcast	Spare [7:6] [5,4] = Manufacturer ID [9:8] (Note 3) USID [3:0]	R/W	8

2. The least significant bits from the Product ID register are refined by OTP. The other seven bits of product ID are hardcoded in ASIC.
3. The manufacturer ID is hardcoded in ASIC, mapped in a READ−only register.

Register Content Details

Register RFFE:	RFFE_REG_0x00	Address RFFE A[4:0]:	[0x00]

<u>Reset Source:</u> nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	spare	spare	spare	spare	spare	DAC C en	DAC B en	DAC A en
Reset	U−0	U−0	U−0	U−0	U−0	W−0	W−0	W−0

Bit [2:0] Each DAC is enabled when the corresponding bit is set. The enable or disable occurs immediately without waiting for a trigger. 0: Off (default) 1: enabled

Bit [7]: Register 0 write command excludes this bit. The extended writes to this address ignores bit 7. The bit is not utilized.

Register RFFE:	RFFE_REG_0x01	Address RFFE A[4:0]:	0x01

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	spare		DUR_C [1:0]		DUR_B [1:0]		DUR_A [1:0]	
Reset	U−0	U−0	W−1	W−1	W−1	W−1	W−1	W−1

DUR_x [1:0] (DAC x USID response)
‘00’: Responds only to USID_0 in DAC register write. SW trigger0 mask defines the triggering source.
‘01’: Responds only to USID_1 in DAC register write. SW trigger1 mask defines the triggering source.
‘10’: Responds only to USID_2 in DAC register write. SW trigger2 mask defines the triggering source.
‘11’: Responds to any 3 USID in DAC register write. Any trigger mask cleared enables the SW triggering.

Register RFFE:	RFFE_REG_0x02	Address RFFE A[4:0]:	0x02

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	boost_clk_en	boost_pwm_en	spare	boost_en	Boost voltage value			
Reset	W−1	W−1	U−0	W−1	W−1	W−0	W−1	W−1

Bit [7]: Enables the booster clock. The clock should be disabled when the booster is turned off.

Bit [6]: Enables the boost oscillator pwm function. This signal should be turned off in case the booster generates low voltages to reduce the ripple.

Bit [4]: Enable/disable of the booster. Booster must be turned off when the high voltage is provided externally.

Bit [3:0]: **Boost voltage value**. Refer to Table 15 for values

Table 15. BOOST VOLTAGE SETTING

Boost Voltage Value[3:0]	VHV [V]	Note	Boost Voltage Value[3:0]	VHV [V]	Note
0000	13	Target values	1000	21	Target values
0001	14		1001	22	
0010	15		1010	23	
0011	16		1011	24 (default)	
0100	17		1100	25	
0101	18		1101	26	
0110	19		1110	27	
0111	20		1111	28	

Register RFFE:	RFFE_REG_0x03	Address RFFE A[4:0]:	[0x03]

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	DAC_TC2X_A	DAC_TCM_A		DAC_TIMER_A				
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Bit [7] If this bit is set, in Turbo mode dac_timer * 2 value is loaded into the DAC timer. The glide always sets the step delay to dac_timer value independent of this bit.
Bit [6:5] It defines the multiplication factor of timer extension when the turbo−down value is below 4 V.
Bit [4:0] For the definition of dac_timer field, see Table 10.

NOTE: The read access to this register will return the active content post−trigger, not the shadow register.

Register RFFE:	RFFE_REG_0x04	Address RFFE A[4:0]:	[0x04]

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	DAC_TC2X_B	DAC_TCM_B		DAC_TIMER_B				
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Bit [7] If this bit is set, in Turbo mode dac_timer * 2 value is loaded into the DAC timer. The glide always sets the step delay to dac_timer value independent of this bit.
Bit [6:5] Defines the multiplication factor of timer extension when the turbo−down value is below 4 V
Bit [4:0] For definition of dac_timer field, see Table 10.

NOTE: The read access to this register will return the active content post−trigger, not the shadow register.

Register RFFE:	RFFE_REG_0x05	Address RFFE A[4:0]:	[0x05]

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	DAC_TC2X_C	DAC_TCM_C		DAC_TIMER_C				
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Bit [7] If this bit is set, in Turbo mode dac_timer * 2 value is loaded into the DAC timer. The glide always sets the step delay to dac_timer value independent of this bit.
Bit [6:5] Defines the multiplication factor of timer extension when the turbo−down value is below 4 V
Bit [4:0] For definition of dac_timer field, see Table 10.

NOTE: The read access to this register will return the active content post−trigger, not the shadow register.

Register RFFE:	RFFE_REG_0x06	Address RFFE A[4:0]:	0x06

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	GL_A	DAC A value [6:0]						
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Bit [7] If the GL_A=1, a non−zero value in DAC timer in starts a glide. If GL_A =0 and the DAC_TIMER_A is not zero, Turbo is started with the new DAC A value.

NOTE: The read access to this register will return the active content post−trigger, not the shadow register. The DAC value read−back is not the actual analog drive, it is the target level.

Register RFFE:	RFFE_REG_0x07	Address RFFE A[4:0]:	0x07

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	GL_B	DAC B value [6:0]						
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Bit [7] If the GL_B=1, a non−zero value in DAC timer in starts a glide. If GL_B =0 and the DAC_TIMER_B is not zero, Turbo is started with the new DAC B value.

NOTE: The read access to this register will return the active content post−trigger, not the shadow register. The DAC value read−back is not the actual analog drive, it is the target level.

Register RFFE:	RFFE_REG_0x08	Address RFFE A[4:0]:	0x08

<u>Reset Source:</u> nreset_dig or SWR = '1' or PWR_MODE = '01' (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	GL_C	DAC C value [6:0]						
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Bit [7] If the GL_C=1, a non−zero value in DAC timer in starts a glide. If GL_C =0 and the DAC_TIMER_C is not zero, Turbo is started with the new DAC C value.

NOTE: The read access to this register will return the active content post−trigger, not the shadow register. The DAC value read−back is not the actual analog drive, it is the target level.

Register RFFE:	RFFE_REG_0x09	Address RFFE A[4:0]:	0x09

<u>Reset Source:</u> nreset_dig or SWR = '1' or PWR_MODE = '01' (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	spare	spare	spare	spare	spare	spare	spare	RFFE_RDM
Reset	U−0	U−0	U−0	U−0	U−0	U−0	U−0	W−0

Bit [0] this bit defines the read capture edge internal to the chip. If 1, the read data is released at the falling edge of the RFFE clock. In a system with very heavy load and 26 MHz speed, this bit can be set to gain some time .For speeds below full−speed and light load, it is recommended to keep this bit cleared to switch to rising edge read data release.

Register RFFE:	RFFE_USID_1	Address RFFE A[4:0]:	0x18

<u>Reset Source:</u> nreset_dig or SWR = '1' or PWR_MODE = '01' (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved (2)		MPN9 (2)	MPN8 (2)	USID3 (1)	USID2 (1)	USID1 (1)	USID0 (1)
Reset	0	0	0	1	W−0	W−1	W−1	W−1

USID = Unique Slave Identifier Register

1. USID field can be changed by:
   - MIPI−RFFE broadcast messages when USID field within the Register Write Command is 0b0000
   - MIPI−RFFE individual messages when USID field within the Register Write Command equal with content of RFFE_REG_0x18[3:0]
2. In the sequence of writing USID field, the upper [7:4] must match the value 0b0001 hardcoded in the RFFE register 0x18

NOTE: USID_1 value is NOT retained during SHUTDOWN power mode.

Register RFFE:	RFFE_USID_2	Address RFFE A[4:0]:	0x19

<u>Reset Source:</u> nreset_dig or SWR = '1' or PWR_MODE = '01' (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved (2)		MPN9 (2)	MPN8 (2)	USID3 (1)	USID2 (1)	USID1 (1)	USID0 (1)
Reset	0	0	0	1	W−0	W−1	W−1	W−1

USID = Unique Slave Identifier Register

1. USID field can be changed by:
   - MIPI−RFFE broadcast messages when USID field within the Register Write Command is 0b0000
   - MIPI−RFFE individual messages when USID field within the Register Write Command equal with content of RFFE_REG_0x19[3:0]
2. In the sequence of writing USID field, the upper [7:4] must match the value 0b0001 hardcoded in the RFFE register 0x19

NOTE: USID_2 value is NOT retained during SHUTDOWN power mode.

Register RFFE:	RFFE_STATUS	Address RFFE A[4:0]:	0x1A

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	SWR	CFPE	CLE	AFPE	DFPE	RURE	WURE	BGE
Reset	W−0	R−0	R−0	R−0	R−0	R−0	R−0	R−0

SWR Soft−Reset MIPI−RFFE registers

Write ‘1’ to this bit to reset all the MIPI−RFFE registers, except RFFE_PM_TRIG, RFFE_GROUP_SID, RFFE_USID_0, RFFE_USID_1 and RFFE_USID_2.

This bit will always Read−back ‘0’.

The soft reset occurs in the last clock cycle of the MIPI−RFFE frame which Writes ‘1’ to this bit.

Right immediately after this frame, all the MIPI−RFFE registers have the reset value and are ready to be reprogrammed as desired.

The OTP duplicated registers below the address 0x1F are reset to the values written in OTP.

RFFE_STATUS Bits [6:0] are set ‘1’ by hardware to flag when a certain condition is detected, as described below. RFFE_STATUS Bits [6:0] cannot be written, but it is cleared to ‘0’ under following conditions:

- Hardware Self−reset is applied after RFFE_STATUS is READ
- When SWR is written ‘1’
- When power mode transitions through STARTUP mode ‘01’
- After Power−up Reset

CFPE

1: Command frame with parity error received.

On the occurrence of this error, the slave will ignore the entire Command Sequence

CLE

1: Incompatible command length, due to unexpected SSC received before command length to be completed.

On the occurrence of this error, the slave will accept Write data up to the last correct and complete frame.

When MIPI−RFFE multi−byte Read command is detected, the slave will always replay with an extended Read command of length of one byte.

AFPE

1: Address frame with parity error received.

On the occurrence of this error, the slave will ignore the entire Command Sequence

DFPE

1: Data frame with parity error received.

On the occurrence of this error, the slave will ignore only the erroneous data byte (s)

RURE

1: Read of non−existent register was detected.

On the occurrence of this error, the slave will not respond to the Read command frame. It will keep the bus idle.

WURE

1: Write to non−existent register was detected.

On the occurrence of this error, the slave discards data being written, and on the next received frame, proceeds as normal

BGE

1: Read using the Broadcast ID was detected

On the occurrence of this error, the slave will ignore the entire Command Sequence

Register RFFE:	RFFE_GROUP_SID	Address RFFE A[4:0]:	0x1B

Reset Source: nreset_dig or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved	Reserved	Reserved	Reserved	GSID[3]	GSID[2]	GSID[1]	GSID[0]
Reset	0	0	0	0	W−0	W−0	W−0	W−0

GSID = Group Slave Identifier Register

NOTE: The GSID [3:0] field can be written directly by messages using USID_0, USID_1 or USID_2.

NOTE: GSID value is NOT retained during SHUTDOWN power mode.

NOTE: GSID value is not affected by SWR bit from RFFE_STATUS register

NOTE: Frames using slave address = GSID, can write only to RFFE_PM_TRIG [7:6] and [2:0].

NOTE: RFFE READ frames containing GSID will be ignored

Register RFFE:	RFFE_PM_TRIG	Address RFFE A[4:0]:	0x1C

Reset Source: nreset_dig or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Power Mode (Note 7)		Trigger Mask 2 (Notes 4, 5, 6)	Trigger Mask 1 (Notes 4, 5, 6)	Trigger Mask 0 (Notes 4, 5, 6)	Trigger 2 (Note 7)	Trigger 1 (Note 7)	Trigger 0 (Note 7)
Reset	W−0	W−0	W−1	W−1	W−1	W−0	W−0	W−0

4. The Trigger Mask 2 (bit [5]) can be changed, either set or cleared, only with an individual message using USID_2. The Trigger Mask 1 (bit [4]) can be changed, either set or cleared, only with an individual message using USID_1. The Trigger Mask 0 (bit [3]) can be changed, either set or cleared, only with an individual message using USID_0.
5. During broadcast MIPI−RFFE accesses using Broadcast ID or GSID, Trigger bits [2:0] are masked by the pre−existent setting of Trigger Mask bits [5:3].
6. During Individual MIPI−RFFE accesses, Trigger bits [2:0] are masked by the incoming Trigger Mask bits [5:3] within the same write message to RFFE_PM_TRIG register according to the DAC DUR configurations.
7. Power mode field bits [7:6] and Triggers bits [2:0] can be changed by either MIPI−RFFE broadcast messages (with GSID or Broadcast ID slave address). The power mode can be changed by all USID accesses. The trigger bits can be set by individual messages when slave address fields within the Register Write Command is are equal to their corresponding control USIDs.

NOTE: None of the 8 bits of RFFE_PM_TRIG register bits are affected by SWR bit from RFFE_STATUS register. The default reset values of the Trigger Masks are set to ‘1’ violating the RFFE spec, but the trigger at DAC write is requested to be the default

Bit [7:6]: **Power Mode**

00: **ACTIVE mode**, defined by following hardware behavior:
- Boost Control active, VHV set by Digital Interface
- Vout A, B, C enabled and controlled by Digital Interface

01: **STARTUP mode**, defined by following hardware behavior:
- Boost Control active, VHV set by Digital Interface
- Vout A, B, C disabled

10: **LOW POWER** mode is defined by following hardware behavior:
- Digital interface is active, while all other circuits are in low power mode

11: Reserved (State of hardware does not change)

Bit 5: **Mask trigger 2 (only USID_2 write access)**

0:Trigger 2 not masked. The DACs, which are configured in their DUR to be controlled by USID_2 have their active registers updated after the Trigger 2 is written a value of 1.

1:Trigger 2 is masked. The DACs, which are configured in their DUR to be controlled by USID_2 have their active registers updated as soon as their new DAC values are written in (default).

Bit 4: **Mask trigger 1 (only USID_1 write access)**

0:Trigger 1 not masked. The DACs, which are configured in their DUR to be controlled by USID_1 have their active registers updated after the Trigger 1 is written a value of 1.

1:Trigger 2 is masked. The DACs, which are configured in their DUR to be controlled by USID_1 have their active registers updated as soon as their new DAC values are written in (default).

Bit 3: **Mask trigger 0 (only USID_0 write access)**

0:Trigger 0 not masked. The DACs, which are configured in their DUR to be controlled by USID_0 have their active registers updated after the Trigger 0 is written a value of 1.

1:Trigger 2 is masked. The DACs, which are configured in their DUR to be controlled by USID_0 have their active registers updated as soon as their new DAC values are written in (default).

Bit 2: **Trigger 2 (USID_2 or broadcast write access)**
Write 1 to this bit, to move data in DACs, which are configured in their DUR under USID_2 control, from shadow registers into active registers. This trigger can be masked by bit 5. The read back of this field returns DACC pending trigger status (from immediate or SW trigger).

Bit 1: **Trigger 1 (USID_1 or broadcast write access)**
Write 1 to this bit, to move data in DACs, which are configured in their DUR under USID_1 control, from shadow registers into active registers. This trigger can be masked by bit 4. The read back of this field returns DACB pending trigger status (from immediate or SW trigger).

Bit 0: **Trigger 0 (USID_0 or broadcast write access)**
Write 1 to this bit, to move data in DACs, which are configured in their DUR under USID_0 control, from shadow registers into active registers. This trigger can be masked by bit 3. The read back of this field returns DACA pending trigger status (from immediate or SW trigger).

Register RFFE:	RFFE_PRODUCT_ID	Address RFFE A[4:0]:	0x1D

Reset Source: N/A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bits	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
Reset	0	0	0	1	0	0	0	0

Bits [7:1] are hardcoded in ASIC
Bit [0] depends on version – 0 for TCC−303A
PRODUCT Family ID History:

TCC−103A	0	0	0	0	0	1	0	0
TCC−106A	0	0	0	0	1	0	0	0
TCC−202A	0	0	1	0	0	0	0	0
TCC−206A	0	0	1	0	0	1	0	IDB0 pin
TCC−303A	0	0	0	1	0	0	0	0

Register RFFE:	RFFE_MANUFACTURER_ID	Address RFFE A[4:0]:	0x1E

Reset Source: N/A

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bits	MPN7	MPN6	MPN5	MPN4	MPN3	MPN2	MPN1	MPN0
Reset	0	0	1	0	1	1	1	0

The 10 MPN bits (MPN0 to MPN9 partially residing under USID registers) are manufacturing ID bits unique to ON Semiconductor.

Register RFFE:	RFFE_USID_0 (default)	Address RFFE A[4:0]:	0x1F

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved (2)		MPN9 (2)	MPN8 (2)	USID3 (1)	USID2 (1)	USID1 (1)	USID0 (1)
Reset	0	0	0	1	W−0	W−1	W−1	W−1

USID = Unique Slave Identifier Register

1. USID field can be changed by:
   - MIPI−RFFE broadcast messages when USID field within the Register Write Command is 0b0000
   - MIPI−RFFE individual messages when USID field within the Register Write Command equal with content of RFFE_REG_0x1F[3:0]
2. In the sequence of writing USID field, the upper [7:4] must match the value 0b0001 hardcoded in the RFFE register 0x1F

NOTE: USID value is NOT retained during SHUTDOWN power mode.

Register 0 Write Command Sequence

The Command Sequence starts with an SSC which is followed by the Register 0 Write Command Frame. This Frame contains the Slave address, a logic one, and the seven bit word that will be written to Register 0. The Command Sequence is depicted below.

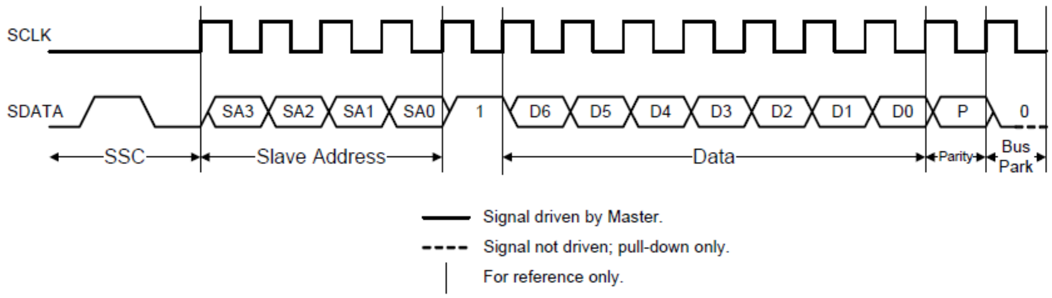


Figure 14. Register 0 Write Command Sequence

Table 16. RFFE COMMAND FRAME FOR REGISTER 0 WRITE COMMAND SEQUENCE

Description	SSC		Command Frame										BP
DAC Configuration	1	0	SA [3,0]	1	0	0	0	0	0	0	0	P	BP

Single Register Write Command Sequence

The Write Register command sequence may be used to access each register individually (addresses 0−31).

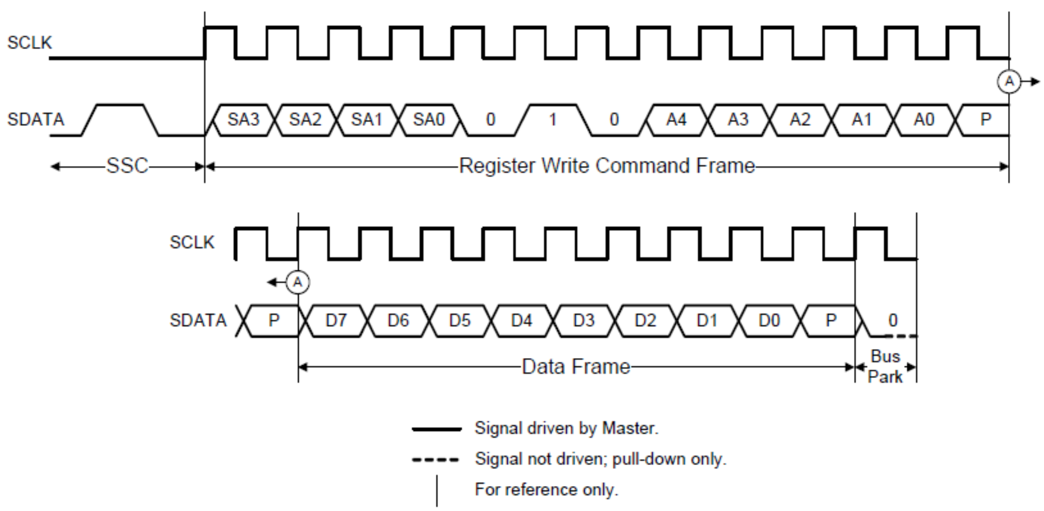


Figure 15. Single Register Write Command Sequence

Table 17. RFFE COMMAND FRAME for REGISTER WRITE COMMAND SEQUENCE for DACS LOADING PROCEDURE

Description	SSC		Command Frame										Data Frame		BP
Register Write DAC A	1	0	SA [3, 0]	0	1	0	0	0	1	1	0	P	GL_A & DAC_A [6:0]	P	BP
Register Write DAC B	1	0	SA [3, 0]	0	1	0	0	0	1	1	1	P	GL_B & DAC_B [6:0]	P	BP
Register Write DAC C	1	0	SA [3, 0]	0	1	0	0	1	0	0	0	P	GL_C & DAC_C [6:0]	P	BP

This sequence can be used for Read/Write procedure for some other purposes as shown on the following table:

Table 18. OTHER RFFE COMMAND SEQUENCES

Description	SSC		Command Frame										Data Frame									BP
Active Mode	1	0	SA [3, 0]	0	1	0	1	1	1	0	0	P	0	0	x	x	x	x	x	x	P	BP
Startup Mode	1	0	SA [3, 0]	0	1	0	1	1	1	0	0	P	0	1	x	x	x	x	x	x	P	BP
Low Power	1	0	SA [3, 0]	0	1	0	1	1	1	0	0	P	1	0	x	x	x	x	x	x	P	BP
Reserved	1	0	SA [3, 0]	0	1	0	1	1	1	0	0	P	1	1	x	x	x	x	x	x	P	BP
Product ID	1	0	SA [3, 0]	0	1	0	1	1	1	0	1	P	0	0	0	1	0	0	0	0/1	P	BP
Manufacturer ID	1	0	SA [3, 0]	0	1	0	1	1	1	1	0	P	0	0	1	0	1	1	1	0	P	BP
Manufacturer USID	1	0	SA [3, 0]	0	1	0	1	1	1	1	1	P	0	0	0	1	USID				P	BP

Extended Register Write Command Sequence

In order to access more than one register in one sequence this message could be used. Most commonly it will be used for loading three DAC registers at the same time. The four LSBs of the Extended Register Write Command Frame determine the number of bytes that will be written by the Command Sequence. A value of 0b0000 would write one byte and a value of 0b1111 would write sixteen bytes.

If more than one byte is to be written, the register address in the Command Sequence contains the address of the first extended register that will be written to and the Slave’s local extended register address shall be automatically incremented by one for each byte written up to address 0x1F, starting from the address indicated in the Address Frame.

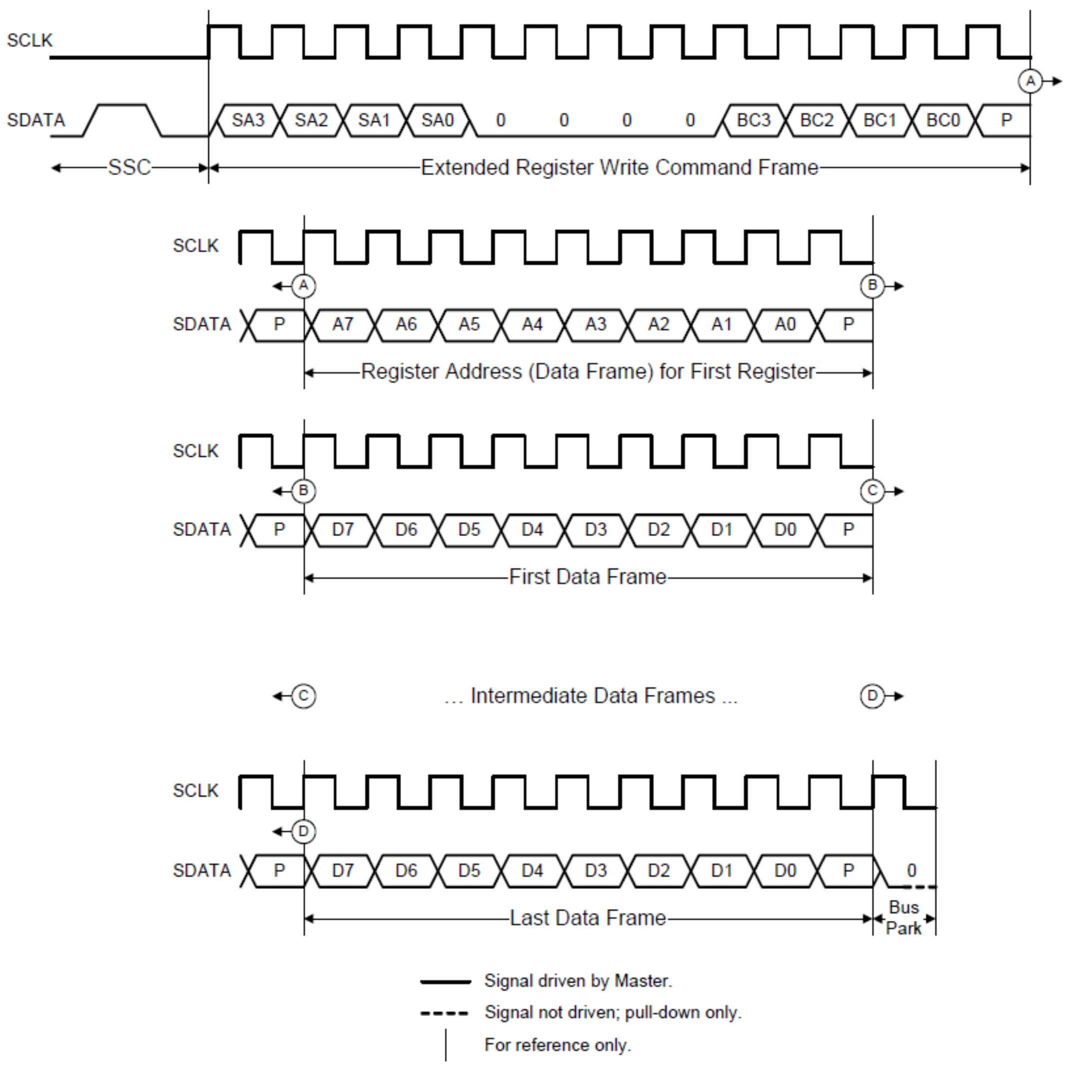


Figure 16. Extended Register Write Command Sequence

Table 19. RFFE Command Frame for Extended Register Write Command Sequence for DACs Loading Procedure

Description	SSC		Command Frame										Address Frame									Data Frame						Bus Park
								<byte count>					<starting address>															
Extended Register Write DAC A&B&C	1	0	SA [3, 0]	0	0	0	0	0	0	1	0	P	0	0	0	0	0	1	1	0	P	GL_A DAC_A [6:0]	P	GL_B & DAC_B [6:0]	P	GL_C & DAC_C	P	BP

Extended or Single Register Read Command Sequence

MIPI−RFFE Read operation can access any register from address 0x00 to 0x1F without the need to enter testkey. Both single Register Read and Extended Register Read commands are supported.

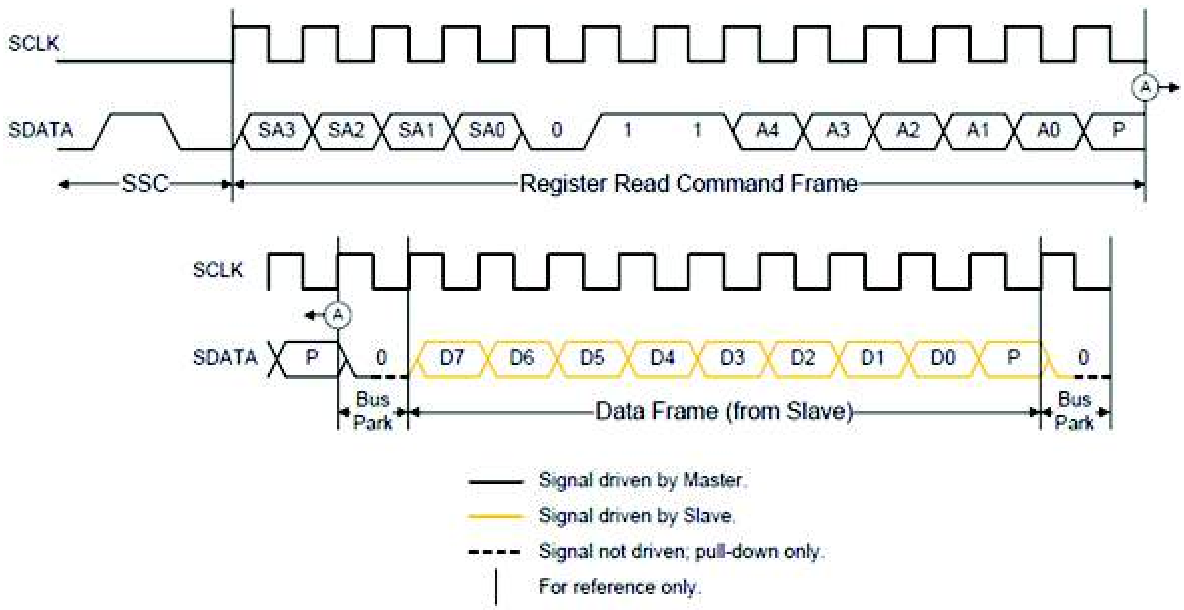


Figure 17. Single Register Read Command Sequence

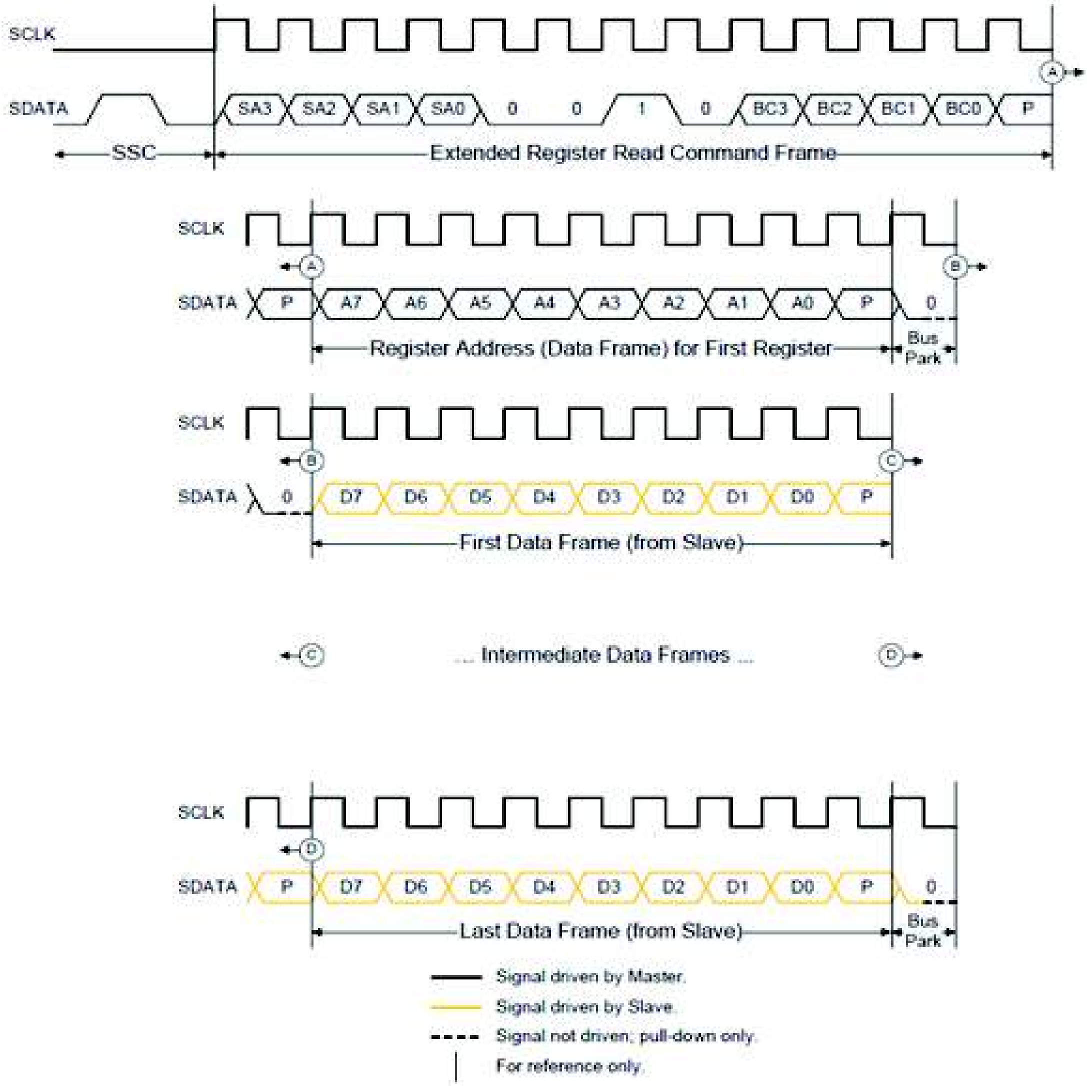


Figure 18. Extended Register Read Command Sequence

Changing USIDs

Changing USID is according to MIPI RFFE specifications. Same Manufacturer_ID and Product_ID apply for USID_0/_1/_2. Note that USID can be changed with broadcast commands, or commands targeting that particular USID. For example to change USID_0, broadcast commands or commands addressing USID_0 can be used.

Change USID_0

- RFFE_WRITE_REG 0x1D [0x10 + OTP[31]]
- RFFE_WRITE_REG 0x1E 0x2E
- RFFE_WRITE_REG 0x1F 0x1Z, where Z is the new USID_0 value

Change USID_1

- RFFE_WRITE_REG 0x1D [0x10 + OTP[31]]
- RFFE_WRITE_REG 0x1E 0x2E
- RFFE_WRITE_REG 0x18 0x1Z, where Z is the new USID_1 value

Change USID_2

- RFFE_WRITE_REG 0x1D [0x10 + OTP[31]]
- RFFE_WRITE_REG 0x1E 0x2E
- RFFE_WRITE_REG 0x19 0x1Z, where Z is the new USID_2 value

EXAMPLE DEVICE OPERATION

Device Setup

1. Enable all three DACs – Write 0x07 to Register 0x00
2. Change VHV voltage to 28 V (Default 24 V) – Write 0xDF to Register 0x02

Change DACs

- Change DACA voltage to 6.8 V; no Glide – Write 0x24 to Register 0x06
- Change DACB voltage to 12.0 V; no Glide – Write 0x40 to Register 0x07
- Change DACC voltage to 0.9 V; no Glide – Write 0x05 to Register 0x08

Setup Glide

- Set DACA Glide step duration to 28 μs – Write 0x0E to Register 0x03
- Set DACB Glide step duration to 20 μs – Write 0x0A to Register 0x04
- Set DACC Glide step duration to 42 μs – Write 0x15 to Register 0x05

Change DACs with Glide

- Keep DACA voltage at 6.8 V; Glide enabled – Write 0xA4 to Register 0x06 (Total Glide duration is 28 μs*256 μs = 7168 μs); No output change since DAC_OLD = DAC_NEW
- Change DACB voltage to 16.4 V; Glide enabled – Write 0xD7 to Register 0x07 (Total Glide duration is 20 μs*256 μs = 5120 μs); Transitions from 12 V to 16.4 V over 5.12 ms
- Change DACC Voltage to 20.5 V; Glide enabled – Write 0xED to Register 0x08 (Total Glide Duration is 42 μs*256 μs = 10752 us); Transitions from 0.9 V to 20.5 V over 10.75 ms

NOTE: Any sequential registers (Eg. 0x03−0x08, as mentioned in Setup Glide and Change DACs with Glide sections) can be written with a single extended MIPI write, rather than individual write commands.

Following picture shows TCC−303 and all the necessary external components

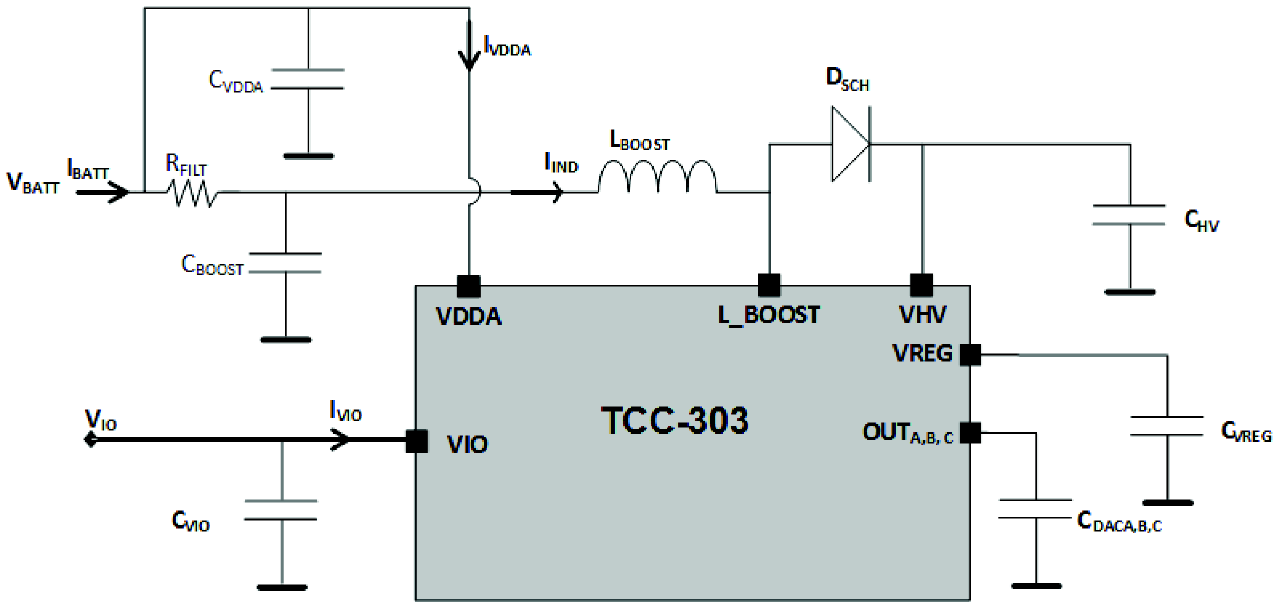


Figure 19. TCC−303 with External Components

Table 20. RECOMMENDED EXTERNAL BOM

Component	Description	Nominal Value	Package	Recommended P/N
C_{BOOST}	Boost Supply Capacitor, 10 V	1 μF	0402	TDK: C1005X5R1A105K
L_{BOOST}	Boost Inductor	15 μH	0603	TDK: VLS2010ET−150M, Sunlord SPH201610H150MT
R_{FILT}	Filtering resistor, 5%	3.3 Ωs	0402	Vishay : CRCW04023R30JNED
C_{VIO}	V_{IO} Supply Decoupling, 10 V	100 nF	0201	Murata: GRM033R61A104ME15D
C_{VDDA}	V_{VDDA} Supply Decoupling, 10 V	1 μF	0402	TDK: C1005X5R1A105K
C_{VREG}	V_{VREG} Supply Decoupling, 10 V	220 nF	0201	TDK: C0603X5R1A224M
C_{HV}	Boost Tank Capacitor, 50 V	47 nF	1005	Murata: GRM155C71H473KE19
$C_{dacA,B,C}$	Decoupling Capacitor, 50 V (Note 8)	100 pF	0201	Murata: GRM0335C1H101JD01D
D_{SCH}	Rectifying Schottky Diode		SOD−923	ON Semiconductor: NSR0240P2T5G, NSR0340HT1G (Note 9), RB521S030T1 (Note 9)

8. Recommended in noise reduction only− not essential but place next to PTIC if used
9. These devices have not been fully tested; performance cannot be guaranteed.

TAPE & REEL DIMENSIONS

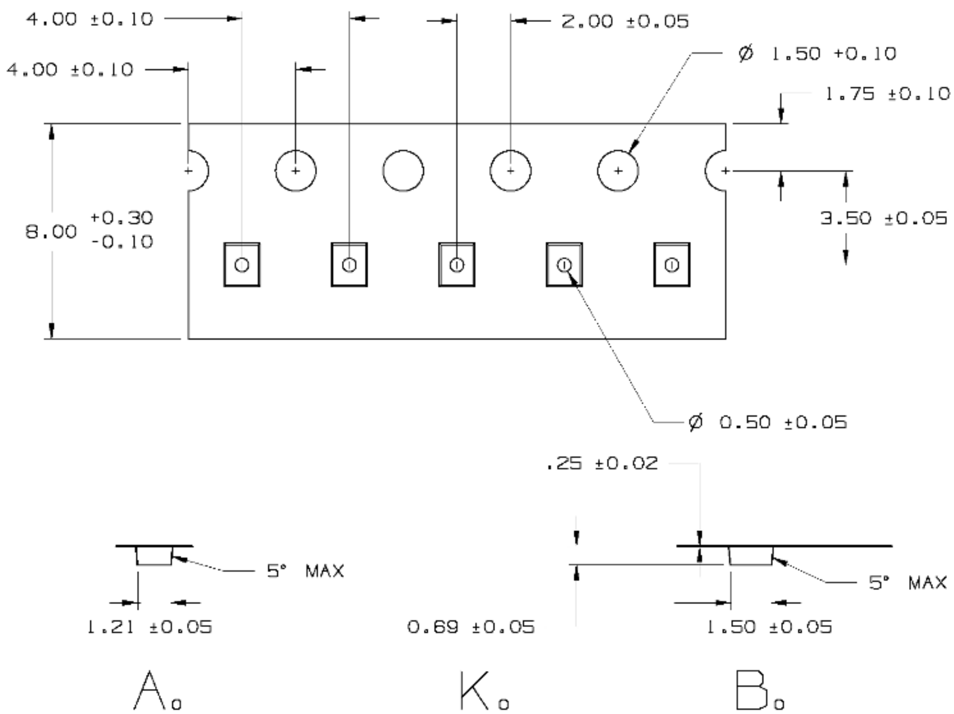


Figure 20. WLCSP Carrier Tape Drawings

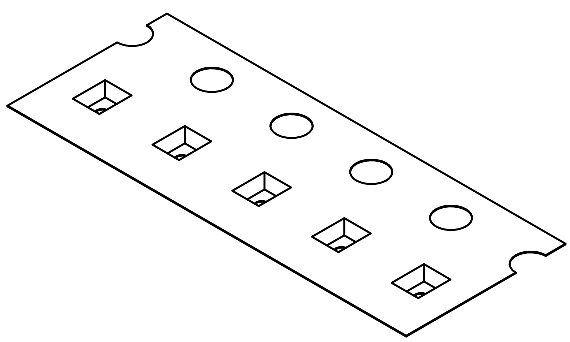


Figure 21. Orientation in Tape

Table 21. ORDERING INFORMATION

Device	Marking	Package	Shipping†
TCC−303A−RT	T33A	RDL (Pb−Free)	3000 / Tape & Reel
TCC−303B−RT	T33B		

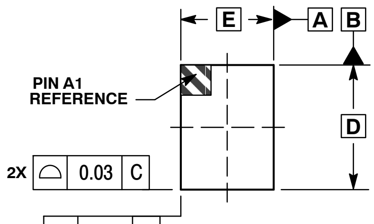
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ASSEMBLY INSTRUCTIONS

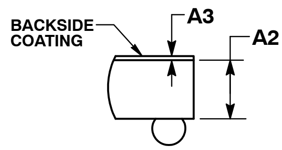
Note: It is recommended that under normal circumstances, this device and associated components should be located in a shielded enclosure.

PACKAGE DIMENSIONS

WLCSP12, 1.376x1.025x0.68
CASE 567MW
ISSUE A



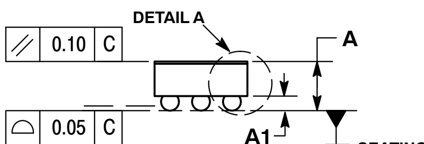
TOP VIEW



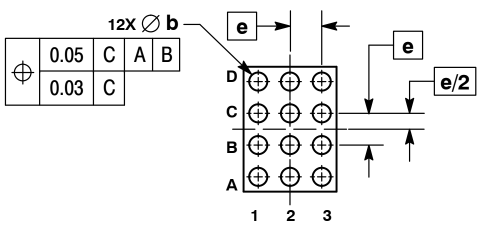
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS MIN	MAX
A	−−−	0.68
A1	0.13	0.19
A2	0.38 REF	
A3	0.025 REF	
b	0.17	0.23
D	1.376 BSC	
E	1.025 BSC	
e	0.35 BSC	

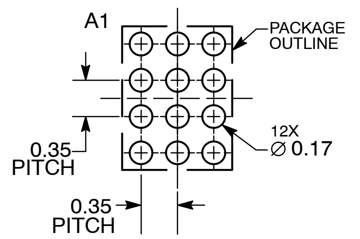


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative