

# MOSFET

## OptiMOS™ 5 Power-Transistor, 30 V

### Features

- Monolithically integrated Schottky-like diode
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- Optimized charges for fast switching
- Optimized  $Q_{gd}$  /  $Q_{gs}$  for induced turn on ruggedness
- 100% avalanche tested
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

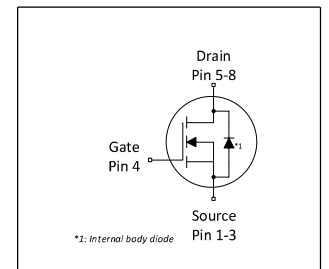
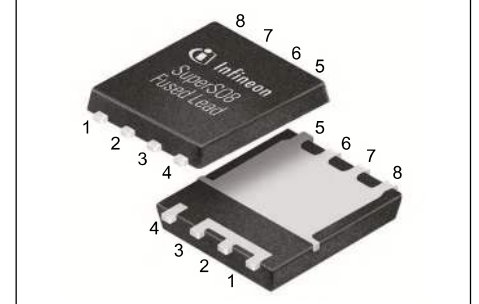
### Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	30	V
$R_{DS(on),max}$	0.55	m $\Omega$
$I_D$	433	A
$Q_{oss}$	78	nC
$Q_G(0V..4.5V)$	51	nC

TDSON-8 FL (enlarged source interconnection)



Type / Ordering Code	Package	Marking	Related Links
BSC005N03LS5I	PG-TDSON-8 FL	5N03LS5I	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	433 306 42	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	1731	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	430	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	188 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}^2)$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	0.8	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	°C/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area	$R_{thJA}$	-	-	50	°C/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/°C	$I_D=10\text{ mA}$ , referenced to $25\text{ °C}$
Gate threshold voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-	0.5	mA	$V_{DS}=24\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$
		-	10	-		$V_{DS}=24\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.51	0.55	mΩ	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$
		-	0.68	0.95		$V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	0.7	1.2	Ω	-
Transconductance	$g_{fs}$	-	290	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	7900	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	3000	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	240	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	24	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	39	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	16	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

<sup>1)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	19	-	nC	$V_{DD}=15\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	12	-	nC	$V_{DD}=15\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge <sup>2)</sup>	$Q_{gd}$	-	10	-	nC	$V_{DD}=15\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	17	-	nC	$V_{DD}=15\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>2)</sup>	$Q_g$	-	51	-	nC	$V_{DD}=15\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.3	-	V	$V_{DD}=15\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	$Q_g$	-	109	-	nC	$V_{DD}=15\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>2)</sup>	$Q_{oss}$	-	78	-	nC	$V_{DS}=15\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	235	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1731	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.56	0.7	V	$V_{GS}=0\text{ V}$ , $I_F=23\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$	-	30	-	nC	$V_R=15\text{ V}$ , $I_F=23\text{ A}$ , $di_F/dt=400\text{ A}/\mu\text{s}$

<sup>1)</sup> See "Gate charge waveforms" for parameter definition

<sup>2)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

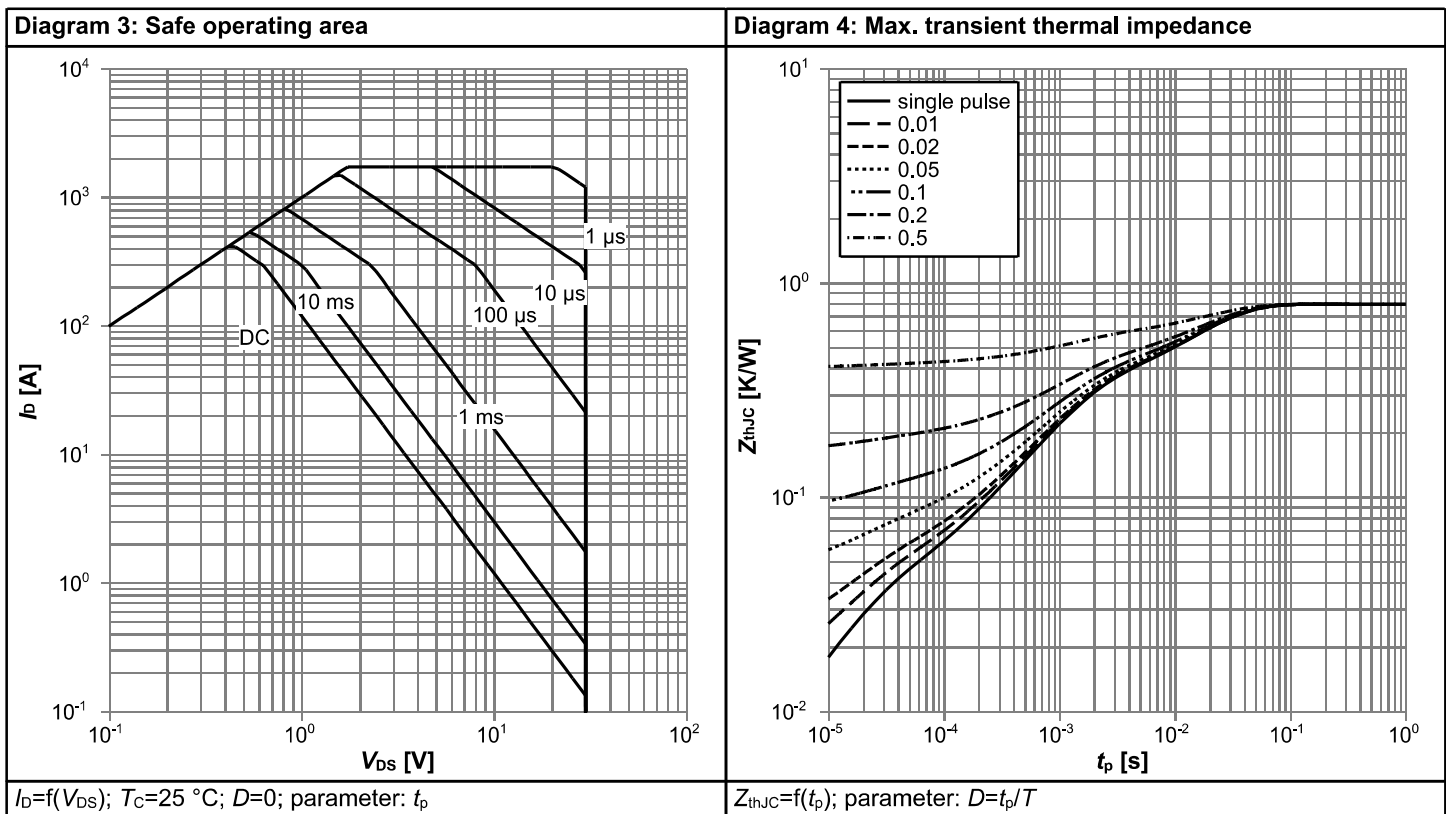
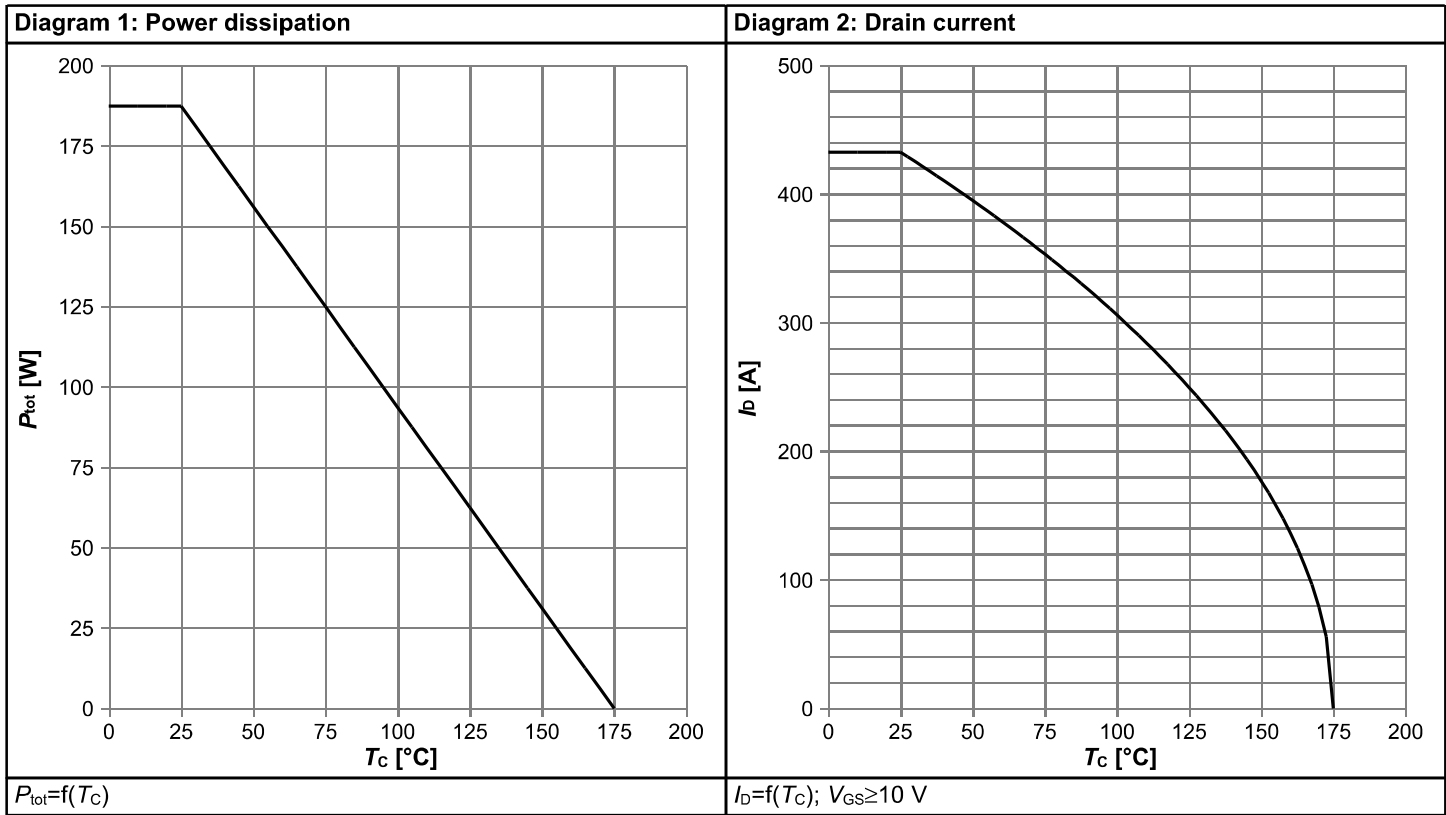
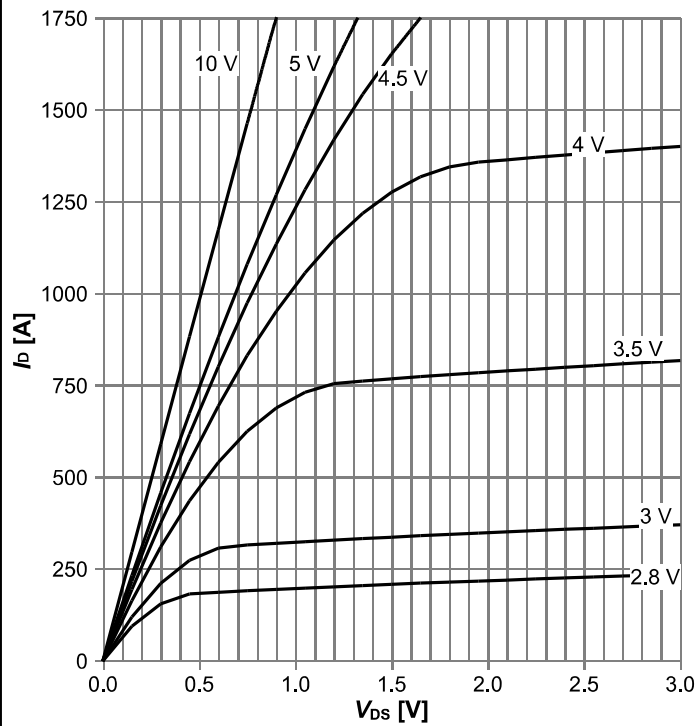
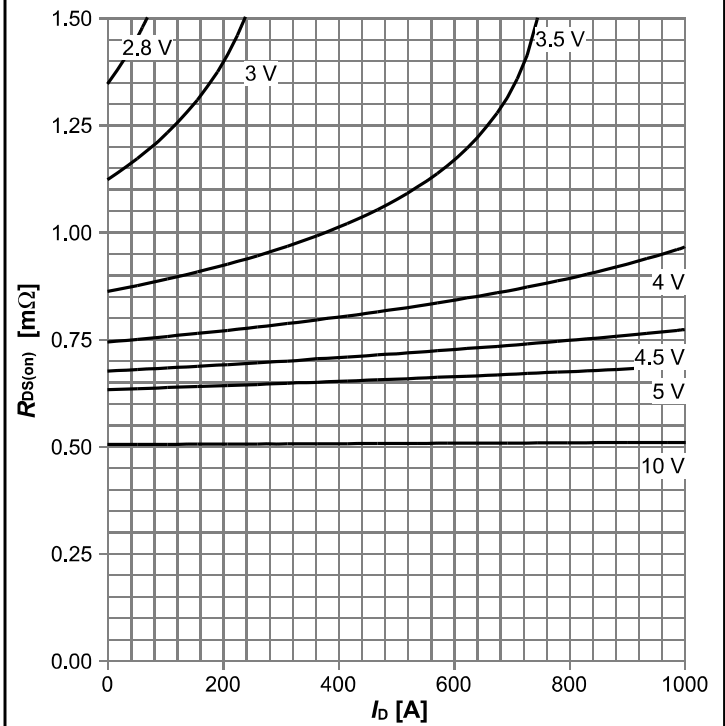


Diagram 5: Typ. output characteristics



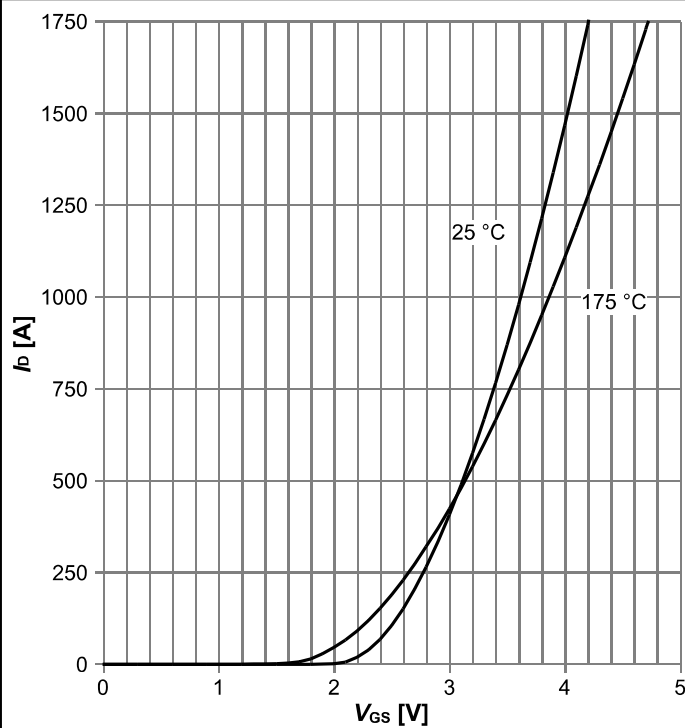
$I_D = f(V_{DS})$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



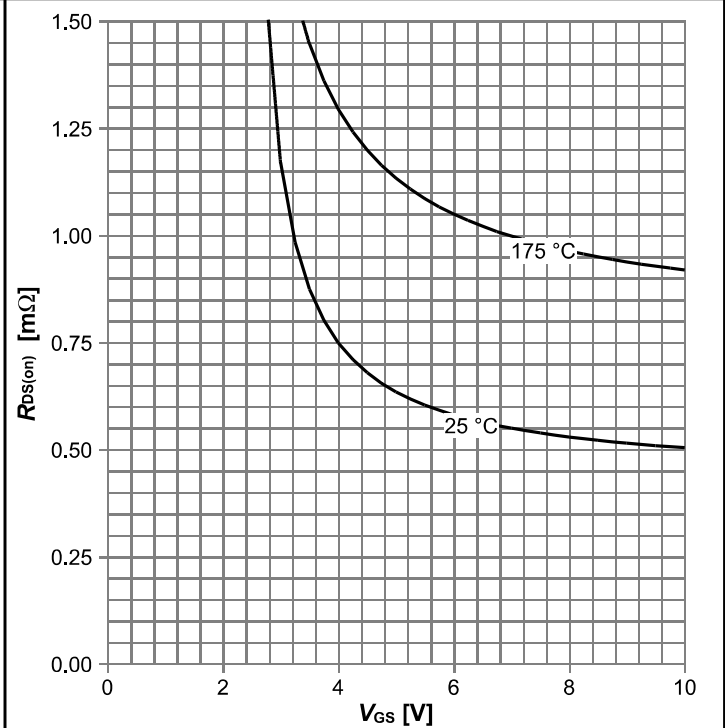
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



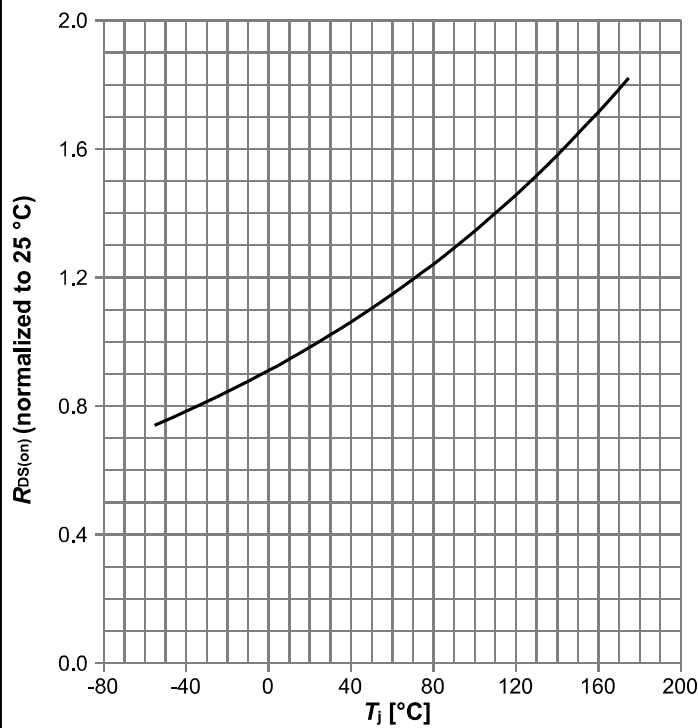
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. drain-source on resistance



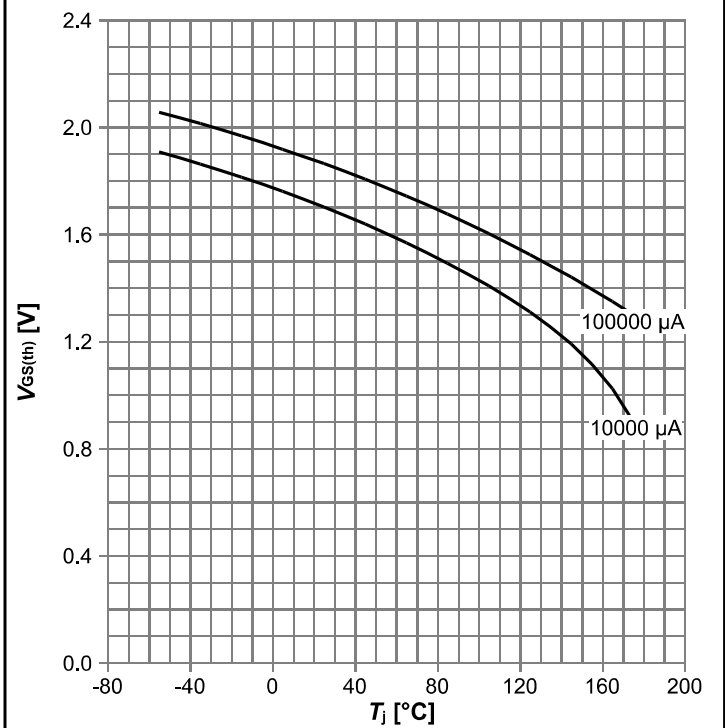
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 50\text{ A}$ ; parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



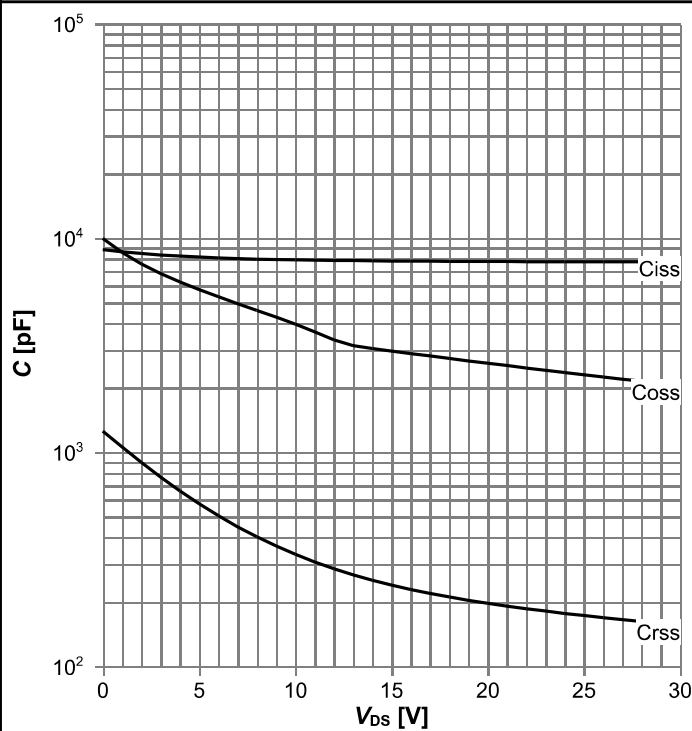
$R_{DS(on)}=f(T_j)$ ,  $I_D=50$  A,  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



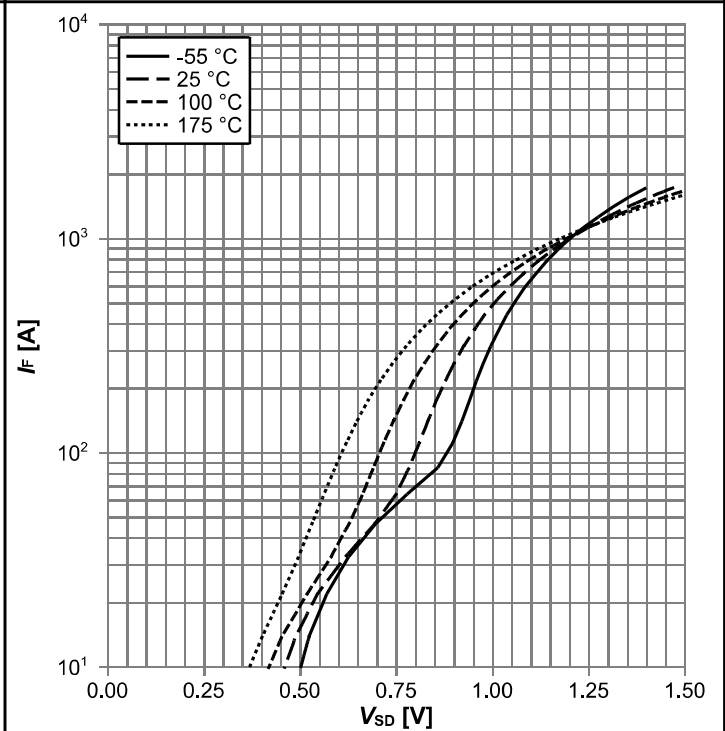
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

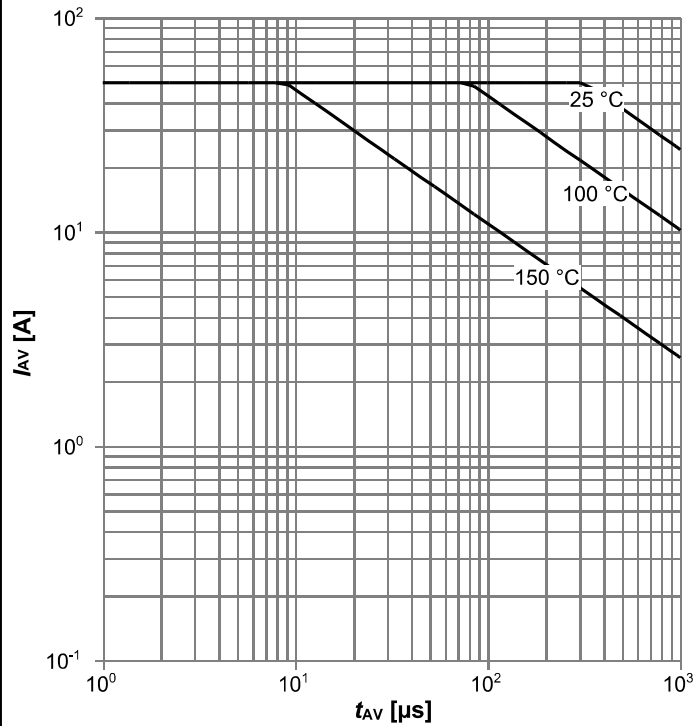
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

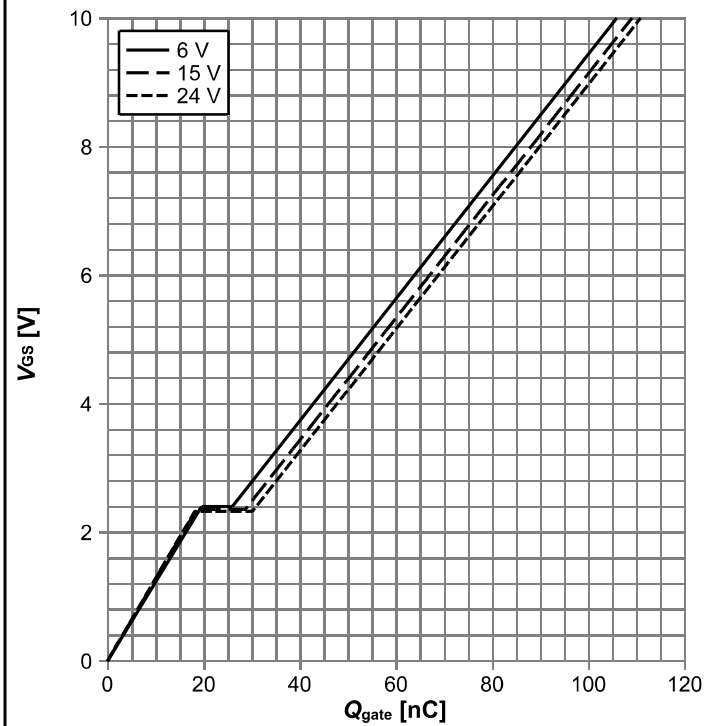


**Diagram 13: Avalanche characteristics**



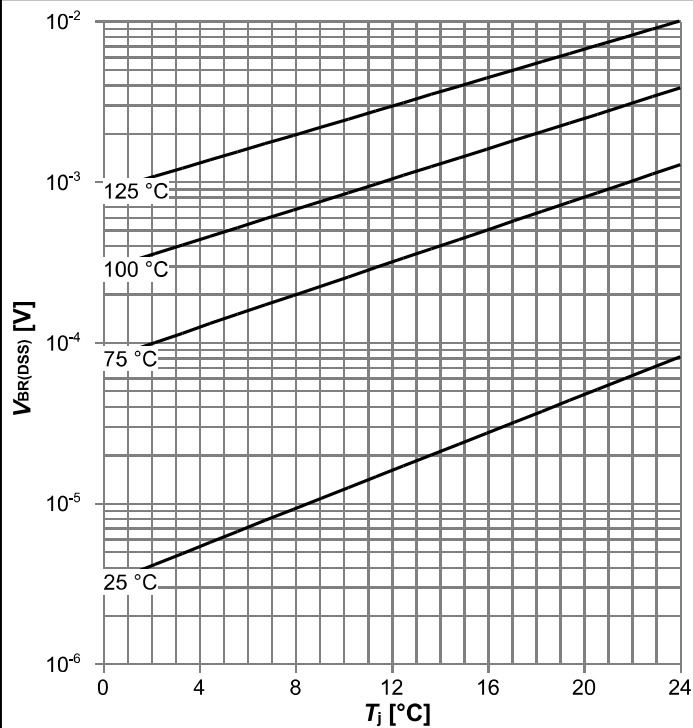
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



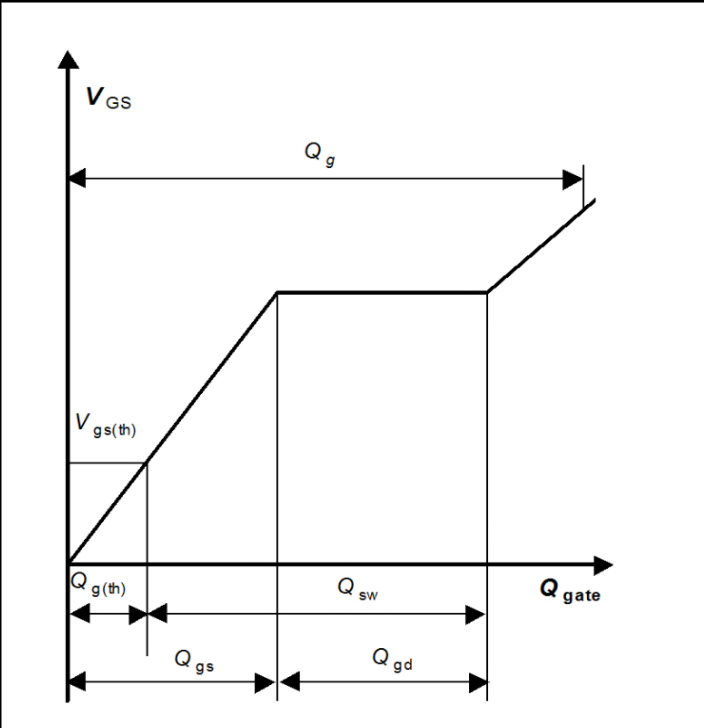
$V_{GS}=f(Q_{gate}), I_D=50 \text{ A pulsed}, T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source leakage current**

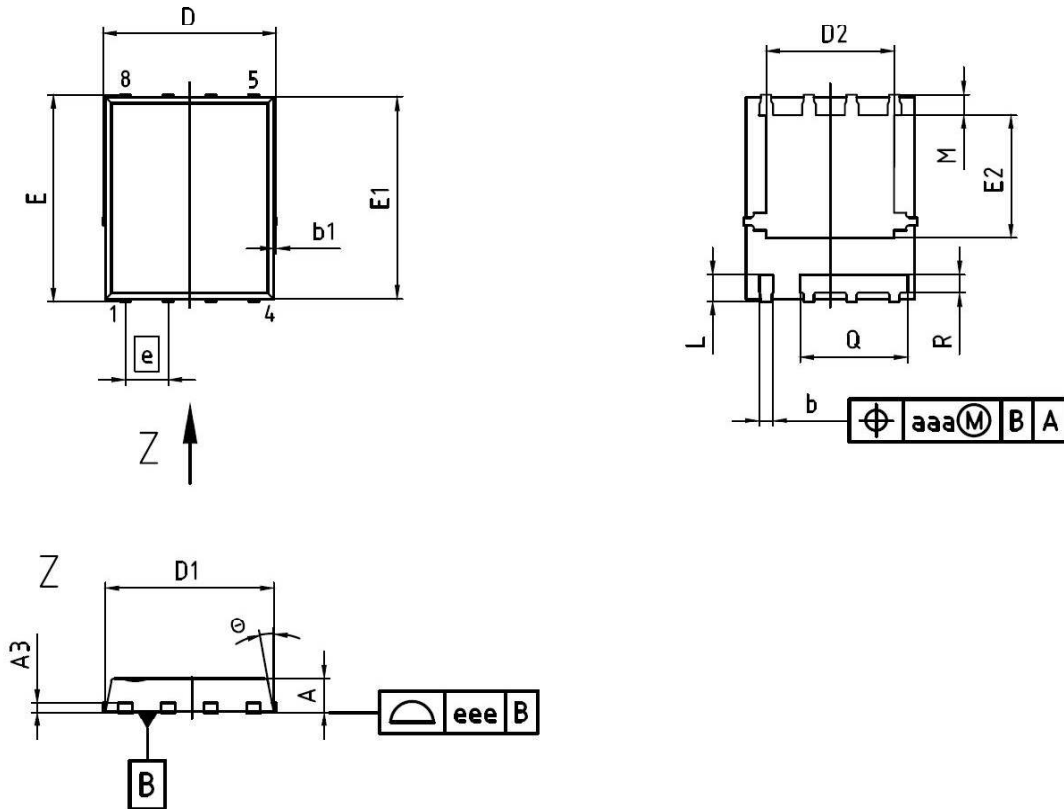


$I_{DSS}=f(V_{DS}), V_{GS}=0 \text{ V}$ ; parameter:  $T_j$

**Diagram Gate charge waveforms**



## 5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
A3	0.25 (REF)		0.011 (REF)	
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.009
D	5.15 (BSC)		0.203 (BSC)	
D1	5.00 (BSC)		0.197 (BSC)	
D2	3.70	4.40	0.146	0.173
E	6.15 (BSC)		0.242 (BSC)	
E1	6.00 (BSC)		0.236 (BSC)	
E2	3.40	3.80	0.134	0.150
e	1.27 (BSC)		0.050 (BSC)	
N	8		8	
L	0.74	0.84	0.029	0.033
M	0.45	0.66	0.018	0.026
o	8.5°	12°	8.5°	12°
Q	3.15	3.25	0.124	0.128
R	0.48	0.58	0.019	0.023
aaa	0.25		0.010	
eee	0.08		0.003	

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REVISION  
01

Figure 1 Outline PG-TDSON-8 FL, dimensions in mm/inches



## Revision History

BSC005N03LS5I

**Revision: 2021-07-22, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-04-16	Release of final version
2.1	2021-07-22	Update gate charges, capacitances, IS max and Id condition for VGS(th) and VSD

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