February 2005

RMPA1765
K-PCS, CDMA, CDMA2000-1X and WCDMA Power Edge™ Power Amplifier Module

Features

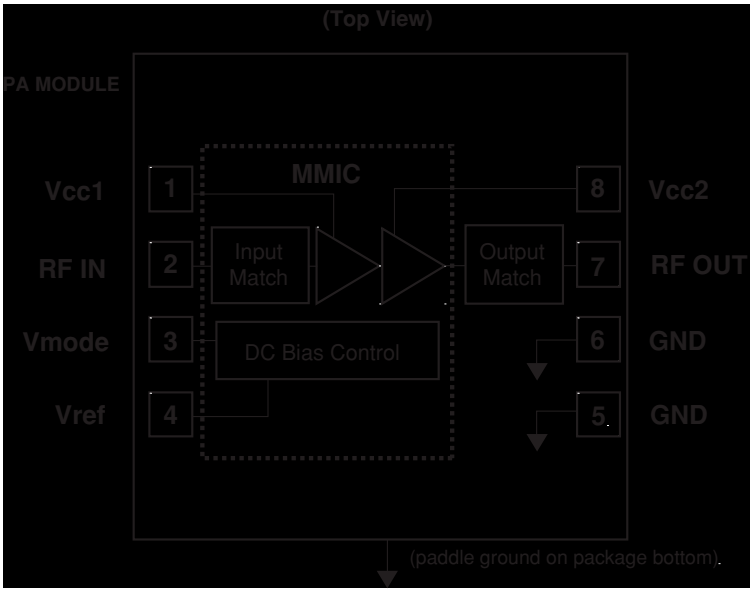
- Single positive-supply operation and low power and shutdown modes
- 38% CDMA/WCDMA efficiency at +28 dBm average output power
- Compact lead-free compliant LCC package- 3.0 x 3.0 x 1.0 mm with industry standard pinout
- Internally matched to 50 Ohms and DC blocked RF input/output.
- Meets CDMA2000-1XRTT/WCDMA performance requirements

General Description

The RMPA1765 power amplifier module (PAM) is designed for Korean CDMA, CDMA2000-1X and WCDMA personal communications system (PCS) applications. The 2 stage PAM is internally matched to 50 Ohms to minimize the use of external components and features a low-power mode to reduce standby current and DC power consumption during peak phone usage. High power-added efficiency and excellent linearity are achieved using Fairchild RF's InGaP Heterojunction Bipolar Transistor (HBT) process.

Device

Functional Block Diagram



Absolute Ratings[1]

Parameter	Symbol	Value	Units
Supply Voltages	Vcc1, Vcc2	5.0	V
Reference Voltage	Vref	2.6 to 3.5	V
Power Control Voltage	Vmode	3.5	V
RF Input Power	Pin	+10	dBm
Storage Temperature	Tstg	-55 to +150	°C

Note:

1. No permanent damage with one parameter set at extreme limit. Other parameters set to typical values.

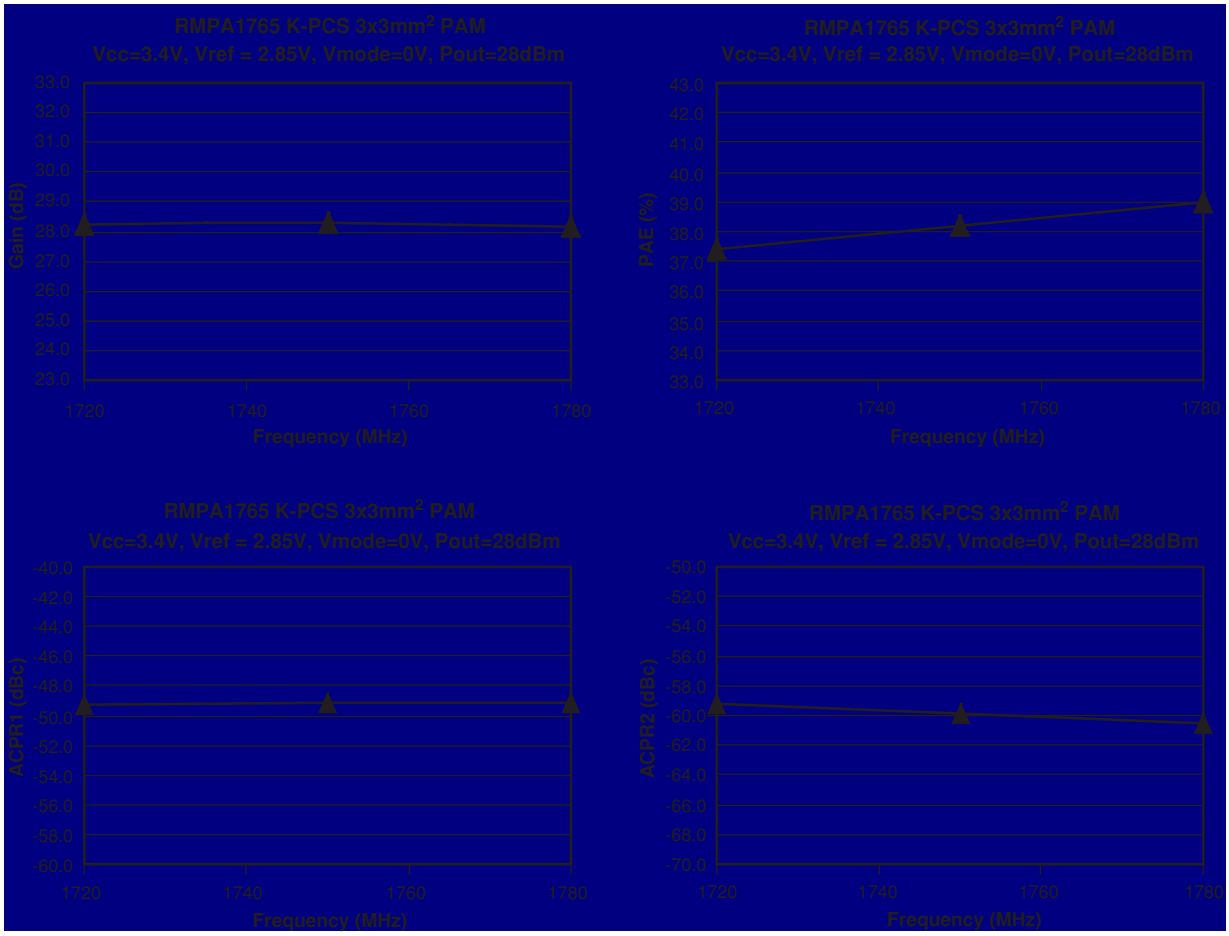
Electrical Characteristics[1]

Parameter	Symbol	Min	Typ	Max	Units	Comments
Operating Frequency	f	1720		1780	MHz	
CDMA Operation						
Small-Signal Gain	SSg		26		dB	Po = 0 dBm
Power Gain	Gp		28		dB	Po = +28 dBm; Vmode = 0V
			26		dB	Po = +16 dBm; Vmode = 2.0V
Linear Output Power	Po	28			dBm	Vmode = 0V
		16			dBm	Vmode ≥ 2.0V
PAEd (digital) @ +28 dBm	PAEd		38		%	Vmode = 0V
PAEd (digital) @ +16 dBm			9		%	Vmode ≥ 2.0V
PAEd (digital) @ +16 dBm			25		%	Vmode ≥ 2.0V, Vcc = 1.4 V
High Power Total Current	Itot		490		mA	Po = +28 dBm, Vmode = 0V
Low Power Total Current			130		mA	Po = +16 dBm, Vmode = 2.0V
Adjacent Channel Power Ratio						
±1.25 MHz Offset	ACPR1		-50		dBc	Po = +28 dBm; Vmode = 0V
			-52		dBc	Po = +16 dBm; Vmode = 2V
±2.25 MHz Offset	ACPR2		-60		dBc	Po = +28 dBm; Vmode = 0V, IS-95
			-68		dBc	Po = +16 dBm; Vmode = 2V
General Characteristics						
Input Impedance	VSWR		2.0:1			
Noise Figure	NF		4		dB	
Receive Band Noise Power	Rx No		-139		dBm/Hz	Po ≤ +28 dBm; 1840 to 1870 MHz
Harmonic Suppression	2fo-5fo			-30	dBc	Po ≤ +28 dBm
Spurious Outputs[2, 3]	S			-60	dBc	Load VSWR ≤ 5.0:1
Ruggedness w/ Load Mismatch[3]				10:1		No permanent damage.
Case Operating Temperature	Tc	-30		85	°C	
DC Characteristics						
Quiescent Current	Iccq		45		mA	Vmode ≥ 2.0V
Reference Current	Iref		5	8	mA	Po < +28 dBm
Shutdown Leakage Current	Icc(off)		1	5	µA	No applied RF signal.

Notes:

1. All parameters met at Tc = +25°C, Vcc = +3.4V, Vref = 2.85V, f = 1750 MHz and load VSWR ≤ 1.2:1, unless otherwise noted.
2. All phase angles.
3. Guaranteed by design.

Performance Data



Efficiency Improvement Applications

In addition to high-power/low-power bias modes, the efficiency of the PA module can be significantly increased at backed-off RF power levels by dynamically varying the supply voltage (Vcc) applied to the amplifier. Since mobile handsets and power amplifiers frequently operate at 10-20 dB back-off, or more, from maximum rated linear power, battery life is highly dependent on the DC power consumed at antenna power levels in the range of 0 to +16dBm. The reduced demand on transmitted RF power allows the PA supply voltage to be reduced for improved efficiency, while still meeting linearity requirements for CDMA modulation with excellent margin. High-efficiency DC-DC converters are now available to implement switched-voltage operation.

With the PA module in low-power mode (Vmode = +2.0V) at+16dBm output power and supply voltages reduced from 3.4V nominal down to 1.2V, power-added efficiency is more than doubled from 9.5 percent to nearly 25 percent (Vcc = 1.2V) while maintaining a typical ACPR1 of –52dBc and ACPR2 of less than –61dBc. Operation at even lower levels of Vcc supply voltage are possible with a further restriction on the maximum RF output power.

Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
Operating Frequency		f	1720		1780	MHz
Supply Voltage		Vcc1, Vcc2	3.0	3.4	4.2	V
Reference Voltage	(operating)	Vref	2.7	2.85	3.1	V
	(shutdown)		0		0.5	V
Bias Control Voltage	(low-power)	Vmode	1.8	2.0	3.0	V
	(high-power)		0		0.5	V
Linear Output Power	(high-power)	Pout			+28	dBm
	(low-power)				+16	dBm
Case Operating Temperature		Tc	-30		+85	°C

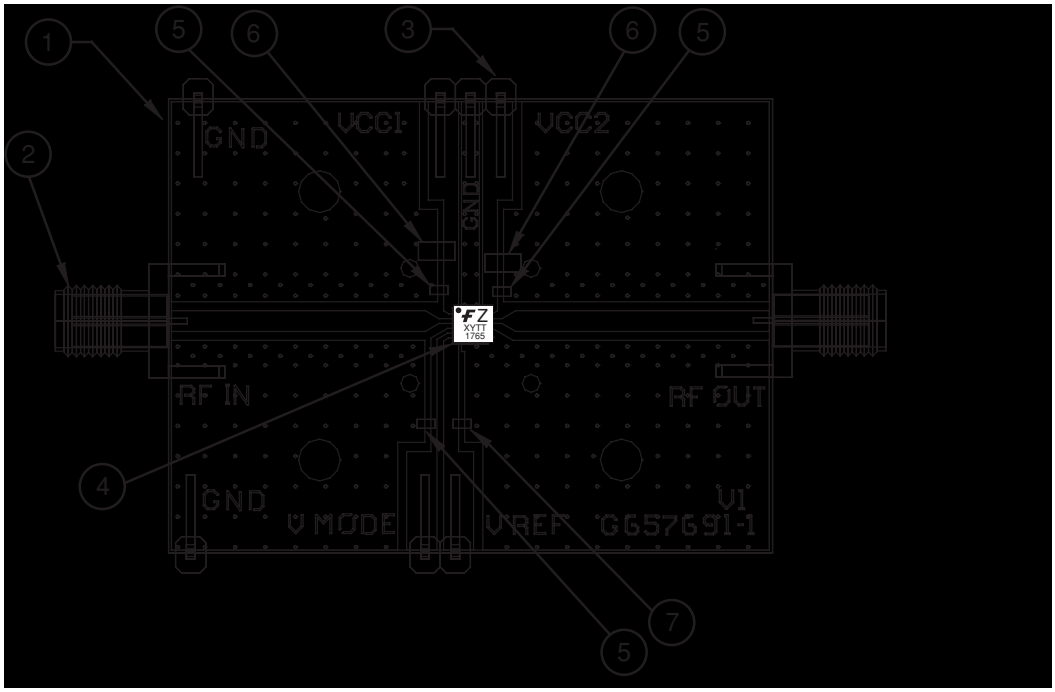
DC Turn-On Sequence

1) Vcc1 = Vcc2 = 3.4V (typical)

2) Vref = 2.85V (typical)

3) High-Power: Vmode = 0V (Pout > 16 dBm)
Low-Power: Vmode = 2V (Pout < 16 dBm)

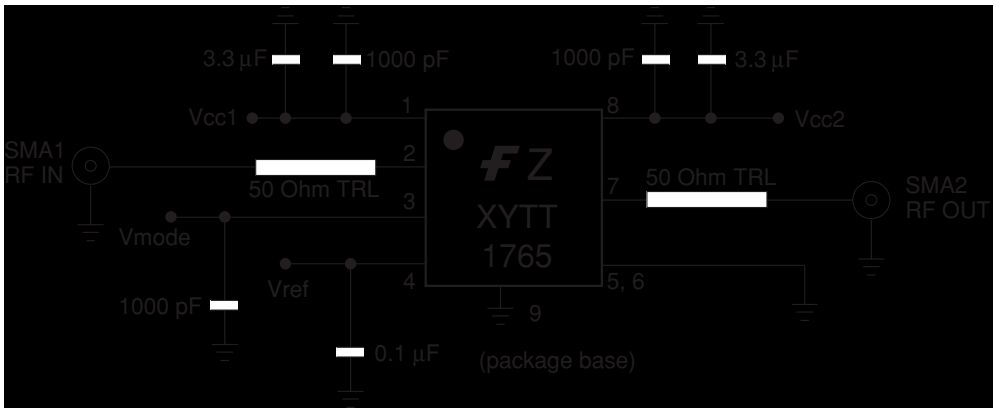
Evaluation Board Layout



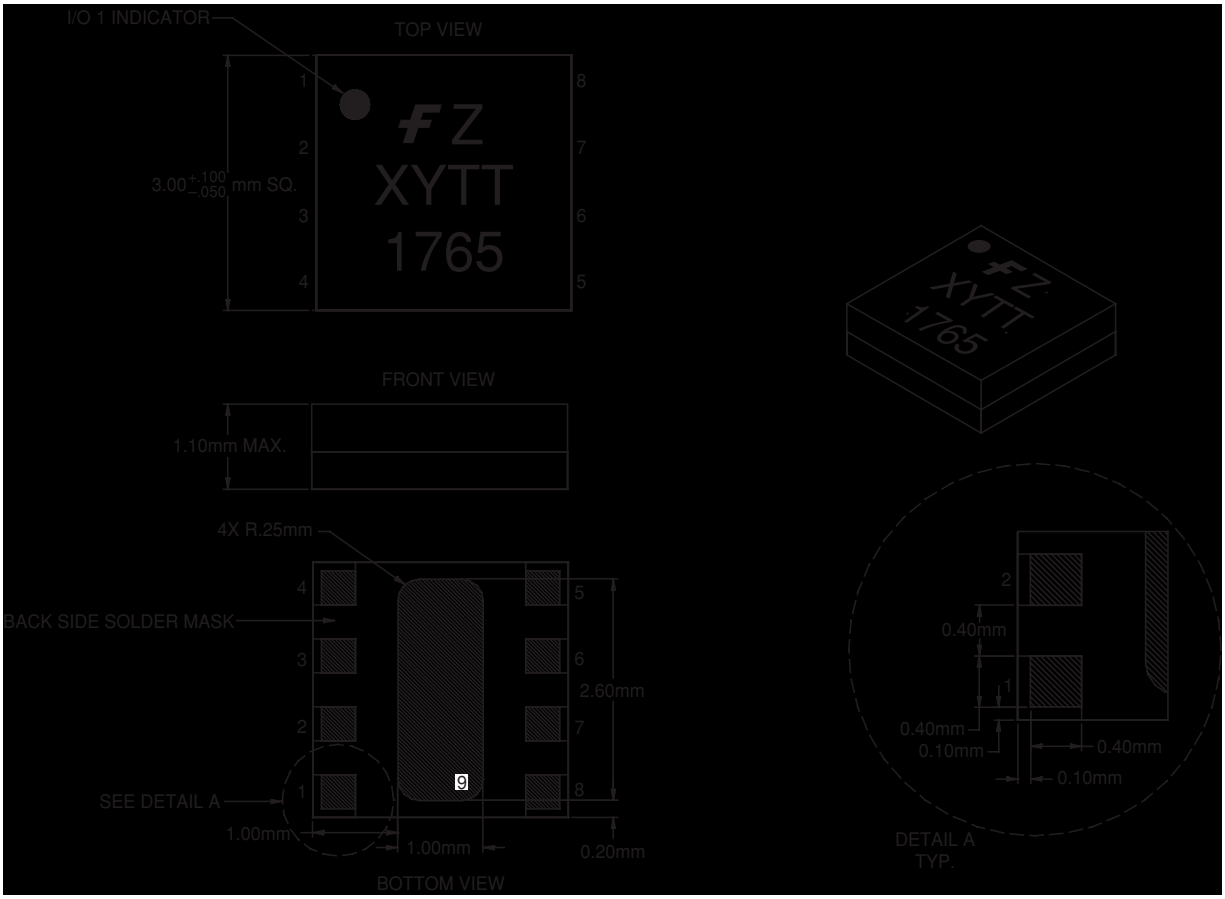
Materials List

Qty	Item No.	Part Number	Description	Vendor
1	1	G657691-1 V1	PC Board	Fairchild
2	2	#142-0701-841	SMA Connector	Johnson
7	3	#2340-5211TN	Terminals	3M
Ref	4		Assembly, RMPA1765	Fairchild
3	5	GRM39X7R102K50V	1000pF Capacitor (0603)	Murata
3	5 (Alt)	ECJ-1VB1H102K	1000pF Capacitor (0603)	Panasonic
2	6	C3216X5R1A335M	3.3µF Capacitor (1206)	TDK
1	7	GRM39Y5V104Z16V	0.1µF Capacitor (0603)	Murata
1	7 (Alt)	ECJ-1VB1C104K	0.1µF Capacitor (0603)	Panasonic
A/R	8	SN63	Solder Paste	Indium Corp.
A/R	9	SN96	Solder Paste	Indium Corp.

Evaluation Board Schematic



Package Outline



Signal Descriptions

Pin #	Signal Name	Description
1	Vcc1	Supply Voltage to Input Stage Reference Voltage
2	RF In	RF Input Signal
3	Vmode	High-Power/Low-Power Mode Control
4	Vref	Reference Voltage
5	GND	Ground
6	GND	Ground
7	RF Out	RF Output Signal
8	Vcc2	Supply Voltage to Output Stage

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.
- Device Usage: Fairchild recommends the following procedures prior to assembly.
  - Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
  - Assemble the dry-baked devices within 7 days of removal from the oven.
  - During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
  - If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

Solder Materials & Temperature Profile: Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

- **Reflow Profile**
  - Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1-2°C/sec.
  - Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
  - Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
  - Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

Recommended Solder Reflow Profile