HARRIS SEMICONDUCTOR

HI5735

12-Bit, 80 MSPS, High Speed Video D/A Converter

January 1998

Features

- Throughput Rate . . . . . 80 MSPS
- Low Power 650mW
- Integral Linearity Error . . . . . 0.75 LSB
- Low Glitch Energy 3.0pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.25ns
- Excellent Spurious Free Dynamic Range

Applications

- Professional Video
- Cable TV Headend Equipment

Description

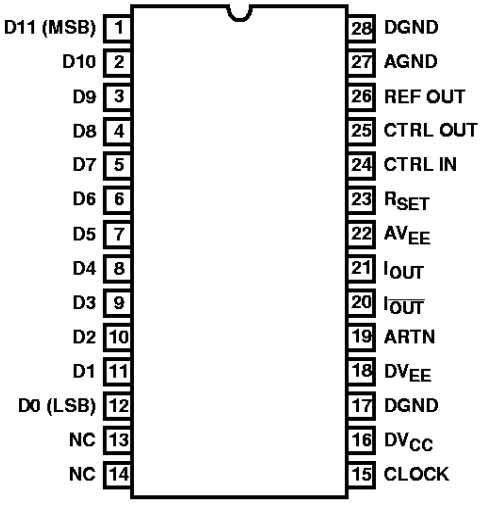
The HI5735 is a 12-bit, 80 MSPS, D/A converter which is implemented in the Harris BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides -20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 12-bit linearity is maintained along the entire transfer curve.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5735KCP	0 to 70	28 Lead PDIP	E28.6
HI5735KCB	0 to 70	28 Lead SOIC	M28.3

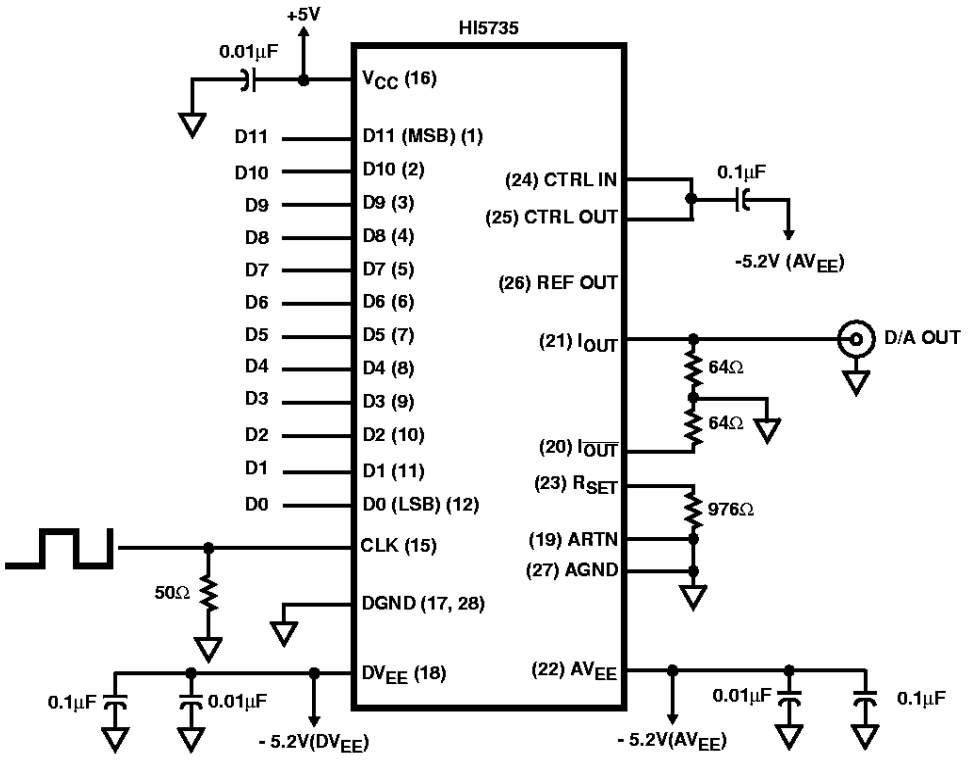
Pinout

HI5735
(PDIP, SOIC)
TOP VIEW

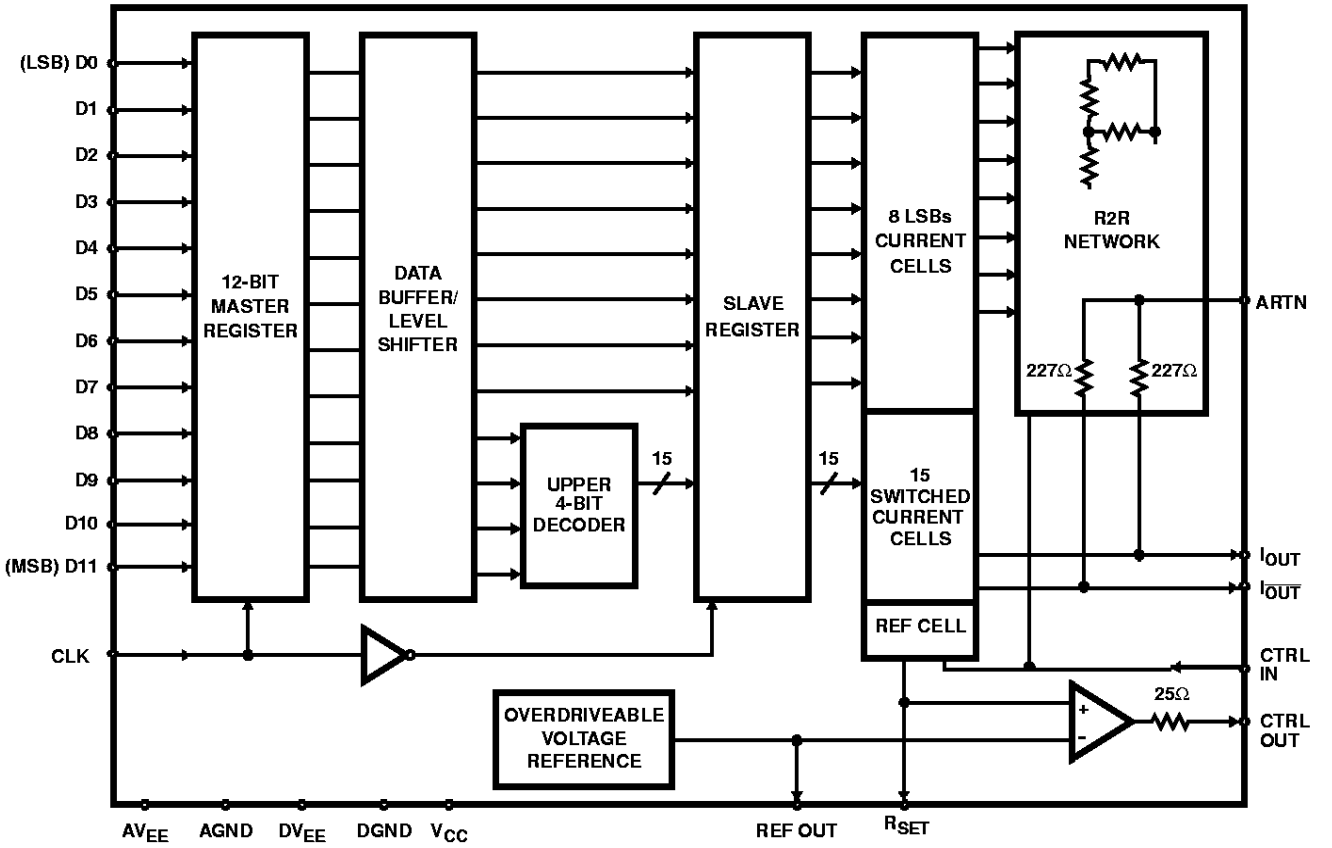


File Number 4133.3

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage V_{CC} to DGND . . . . . +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND . . . . . -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN . . . . . -5.5V
Digital Input Voltages (D11-D0, CLK) to DGND . . . . . DV_{CC} to -0.5V
Internal Reference Output Current . . . . . ±2.5mA
Voltage from CTRL IN to AV_{EE}. . . . . 2.5V to 0V
Control Amplifier Output Current . . . . . ±2.5mA
Reference Input Voltage Range . . . . . -3.7V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	55
SOIC Package	70

Maximum Junction Temperature
Plastic Packages . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range
HI5735BIx . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal
T_A = 25°C for All Typical Values

PARAMETER	TEST CONDITIONS	HI5735BI T_A = 0°C TO 70°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	(Note 4) ("Best Fit" Straight Line)	-	0.75	1.5	LSB
Differential Linearity Error, DNL	(Note 4)	-	0.5	1.0	LSB
Offset Error, I_{OS}	(Note 4)	-	20	75	µA
Full Scale Gain Error, FSE	(Notes 2, 4)	-	1	10	%
Offset Drift Coefficient	(Note 3)	-	-	0.05	µA/°C
Full Scale Output Current, I_{FS}		-	20.48	-	mA
Output Voltage Compliance Range	(Note 3)	-1.25	-	0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 5)	80	-	-	MSPS
Output Voltage Full Scale Step Settling Time, t_{SETT} Full Scale	To ±0.5 LSB Error Band R_L = 50Ω (Note 3)	-	20	-	ns
Single Glitch Area, GE (Peak)	R_L = 50Ω (Note 3)	-	5	-	pV-s
Doublet Glitch Area, (Net)		-	3	-	pV-s
Output Slew Rate	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	1,000	-	V/µs
Output Rise Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	675	-	ps
Output Fall Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	470	-	ps
Differential Gain	R_L = 50Ω (Note 3)	-	0.15	-	%
Differential Phase	R_L = 50Ω (Note 3)	-	0.07	-	Deg

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5735BI T_A = 0°C TO 70°C			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range to Nyquist (Note 3)	f_{CLK} = 40MHz, f_{OUT} = 2.02MHz, 20MHz Span	-	70	-	dBc
	f_{CLK} = 80MHz, f_{OUT} = 2.02MHz, 40MHz Span	-	70	-	dBc
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, V_{REF}	(Note 4)	-1.27	-1.23	-1.17	V
Internal Reference Voltage Drift	(Note 3)	-	50	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 3)	-125	-	+50	µA
Internal Reference Load Regulation	I_{REF} = 0 to I_{REF} = -125µA	-	50	-	µV
Input Impedance at REF OUT pin	(Note 3)	-	1.4	-	kΩ
Amplifier Large Signal Bandwidth ($0.6V_{P-P}$)	Sine Wave Input, to Slew Rate Limited (Note 3)	-	3	-	MHz
Amplifier Small Signal Bandwidth ($0.1V_{P-P}$)	Sine Wave Input, to -3dB Loss (Note 3)	-	10	-	MHz
Reference Input Impedance	(Note 3)	-	12	-	kΩ
Reference Input Multiplying Bandwidth (CTL IN)	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 3)	-	200	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 4)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 4)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 4)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 4)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1 (Note 3)	3.0	2.0	-	ns
Data Hold Time, t_{HLD}	See Figure 1 (Note 3)	0.5	0.25	-	ns
Propagation Delay Time, t_{PD}	See Figure 1 (Note 3)	-	4.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 1 (Note 3)	3.0	-	-	ns
POWER SUPPLY CHARACTERISITICS					
I_{EEA}	(Note 4)	-	42	50	mA
I_{EED}	(Note 4)	-	70	85	mA
I_{CCD}	(Note 4)	-	13	20	mA
Power Dissipation	(Note 4)	-	650	-	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5%	-	5	-	µA/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 1.28mA). Ideally the ratio should be 16.
3. Parameter guaranteed by design or characterization and not production tested.
4. All devices are 100% tested at 25°C. 100% production tested at temperature extremes for military temperature devices, sample tested for industrial temperature devices.
5. Dynamic Range must be limited to a 1V swing within the compliance range.