DAC60096 Evaluation Module

This user's guide describes the characteristics, operation, and use of the DAC60096 evaluation boards (EVMs). This user's guide also discusses the proper setup and configuration of both software and hardware, and reviews various aspects of program operation. A complete circuit description, schematic diagram, and bill of materials (BOM) are also included in this document.

Contents

List of Figures

List of Tables

1 Overview

This EVM features the DAC60096 device, a very low-power, 96 channel, 12-bit digital-to-analog converter (DAC). The device provides unbuffered bipolar voltage outputs up to ±10.5 V. The DAC60096 can be programmed for simultaneous update as well as simultaneous clear. In addition, a versatile external conversion trigger allows each DAC to operate as an amplitude-independent square-wave generator.

1.1 DAC60096EVM Kit Contents

Table 1 details the contents of the EVM kit. Contact the TI Product Information Center nearest you if any component is missing. TI highly recommends to verify that the user has the latest versions of the related software at the TI website, www.ti.com.

Table 1. Contents of DAC60096EVM Kit

Item	Quantity
DAC60096EVM PCB evaluation board	1
SDM-USB-DIG platform PCB	1
USB extender cable	1

1.2 Related Documentation from Texas Instruments

The following documents provide information regarding TI's integrated circuits used in the assembly of the DAC60096EVM. This user's guide is available from the TI web site under literature number SLAU644. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site at http://www.ti.com/, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 2. Related Documentation

Document	Literature Number
DAC60096 Product Data Sheet	SBAS721
SDM-USB-DIG Platform User's Guide	SBOU136

2 DAC60096EVM Hardware Setup

This section provides the overall system setup for the EVM. A personal computer (PC) runs software that communicates with the SDM-USB-DIG platform, which generates the optional DVDD power and digital signals used to communicate with the EVM board. Banana plug connectors are included on the EVM board for external power supplies. Figure 1 displays the system setup for the DAC60096EVM.

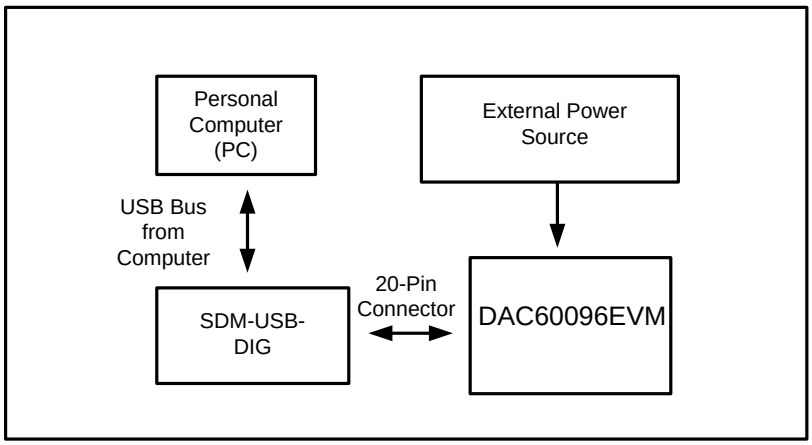

Figure 1. DAC60096EVM Hardware Setup

2.1 Theory of Operation for DAC60096 Hardware

A block diagram of the DAC60096EVM test board is displayed in Figure 2. The EVM board provides banana plugs for the supplies, 4 header pins connected to the DAC60096 DAC outputs, external trigger signal connection, optional external reference connection, and SPI input connections.

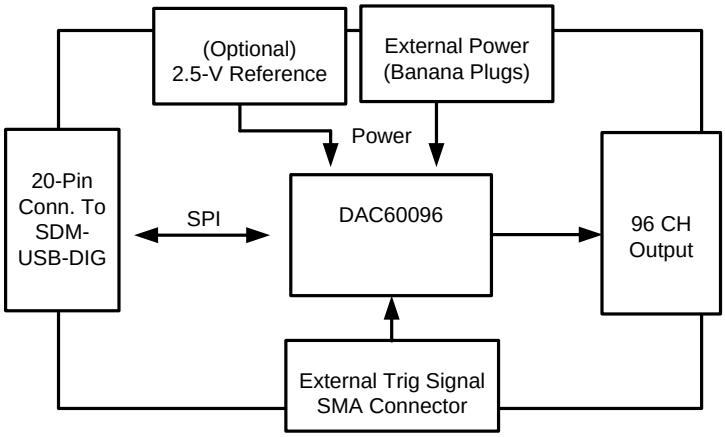

Figure 2. DAC60096 Test Board Block Diagram

2.2 Signal Definitions of J4 (20-Pin Connector)

The DAC60096 EVM includes a 20-pin connector used to communicate between the EVM and the SDM-USB-DIG platform. Table 3 shows the pin out of the J4 connector.

Table 3. J4 Signal Definition

Pin on J4	Signal	Description
1	SCL	I^2C Clock Signal (SCL)
2	DIG_GPIO2	GPIO – Control output or measure input
3	DIG_GPIO0	GPIO – Control output or measure input
4	DIG_GPIO3	GPIO – Control output or measure input
5	SDA	I^2C data signal (SDA)
6	DIG_GPIO4	GPIO – Control output or measure input
7	DIG_GPIO1	GPIO – Control output or measure input
8	DIG_GPIO5	GPIO – Control output or measure input
9	MOSI	SPI data output (MOSI)
10	DIG_GPIO6	GPIO – Control output or measure input
11	VDUT	Switchable DUT power supply: 3.3 V, 5 V, Hi-Z (Disconnected). **Note:** When VDUT is Hi-Z, all digital I/Os are Hi-Z as well.
12	DIG_GPIO7	GPIO – Control output or measure input
13	SCLK	SPI clock signal (SCLK)
14	DIG_GPIO8	GPIO – Control output or measure input
15	GND	Power return (GND)
16	DIG_GPIO9	GPIO – Control output or measure input
17	CS	SPI chip select signal (/CS)
18	DIG_GPIO10	GPIO – Control output or measure input
19	MISO	SPI data input (MISO)
20	DIG_GPIO11	GPIO – Control output or measure input

2.3 SDM-USB-DIG Platform Theory of Operation

The SDM-USB-DIG platform is a general-purpose data acquisition system that is used on several Texas Instruments evaluation modules.

The core component of the platform is the MSP430F5528, an ultra-low power 16-bit MCU. The microcontroller receives information from the host PC and translates it into I^2C, SPI, or other digital I/O patterns. The connected device, which in this case is the DAC60096 device, connects to the I/O interface of the platform. During digital I/O transactions, the platform obtains information from the DAC60096 device and sends to the host PC for interpretation. Figure 3 illustrates a block diagram of the platform..

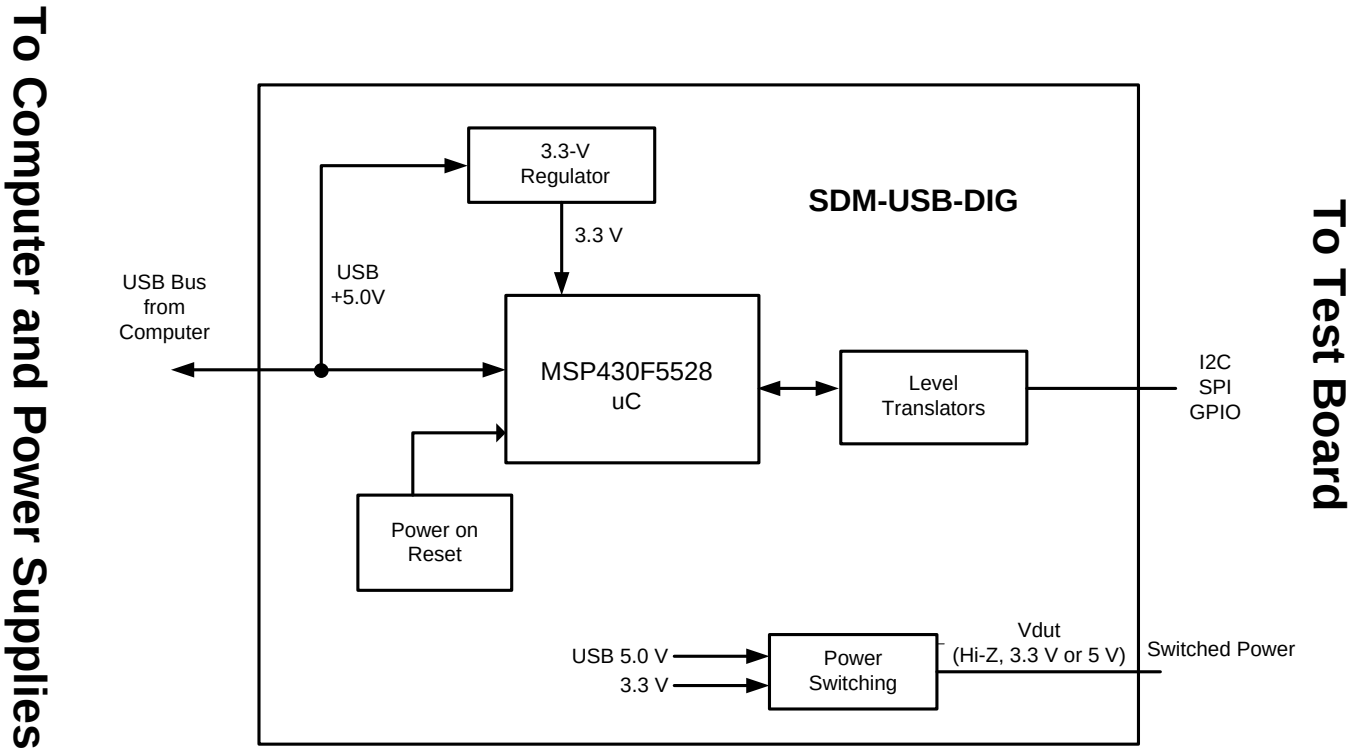

Figure 3. SDM-USB-DIG Platform Block Diagram

3 DAC60096EVM Software Setup

This section provides the procedure for EVM software installation.

3.1 Operating Systems for DAC60096EVM Software

The EVM software has been tested on the Microsoft® Windows® XP, and Windows 7 operating systems with the United States and European regional settings. The software should also be compatible with other Windows operating systems.

3.2 DAC60096EVM Software Installation

The software is available through the EVM product folder on the TI website. Once the software is downloaded onto the PC, navigate to the DAC60096EVM folder, and run the Setup_DAC60096_EVM.exe file, as shown in Figure 4. When the software is launched, an installation dialog opens, and prompts the user to select an installation directory. If left unchanged, the software location defaults to C:\Program Files (x86)\Texas Instruments\DAC60096 EVM as shown in Figure 5. The software installation automatically copies the required drivers for the SDM-USB-DIG and DAC60096EVM to the PC. After the software is installed, connecting the SDM-USB-DIG to a USB port may launch a driver installation dialog. Choose the 'Install this driver software anyway' option to continue with installation. (**Note:** On XP machines, choose to have the system automatically find the driver/software.)

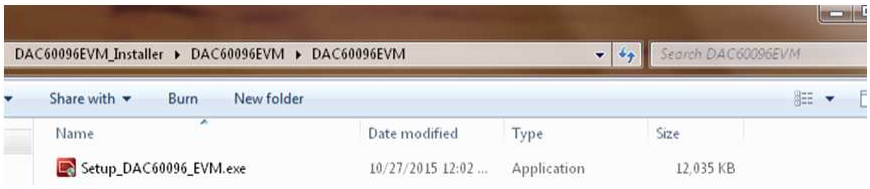

Figure 4. DAC60096EVM Installer Directory

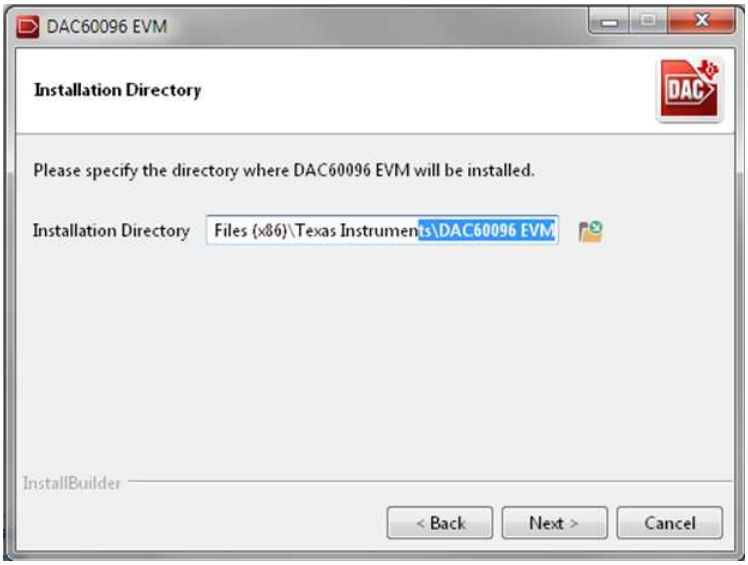

Figure 5. DAC60096EVM Install Path

4 DAC60096EVM Hardware Overview

The subsequent sections provide detailed information on the EVM hardware and jumper configuration settings. Table 4 displays the default configurations of all jumper connections on the DAC60096EVM. Connect the USB extender cable from the SDM-USB-DIG to the PC.

Table 4. Default Jumper Settings

Jumper	Default Position	Function
JP1	Shunt on 2-3	DVDD selection: • 1–2: J5 to DVDD pin • 2–3: SDM-USB-DIG 5V to DVDD pin
JP2	Shunt on 1-2	2.5-V reference selection: • 1–2: connects reference to onboard REF5025 • 2–3: connects reference to J9 Connection

4.1 Electrostatic Discharge Warning

Many of the components on the DAC60096EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

4.2 Connecting the Hardware

To connect the SDM-USB-DIG to the EVM board, align and firmly connect the female and male ends of the 20-pin connectors, Figure 6. Verify the connection is snug, as loose connections may cause intermittent operation.

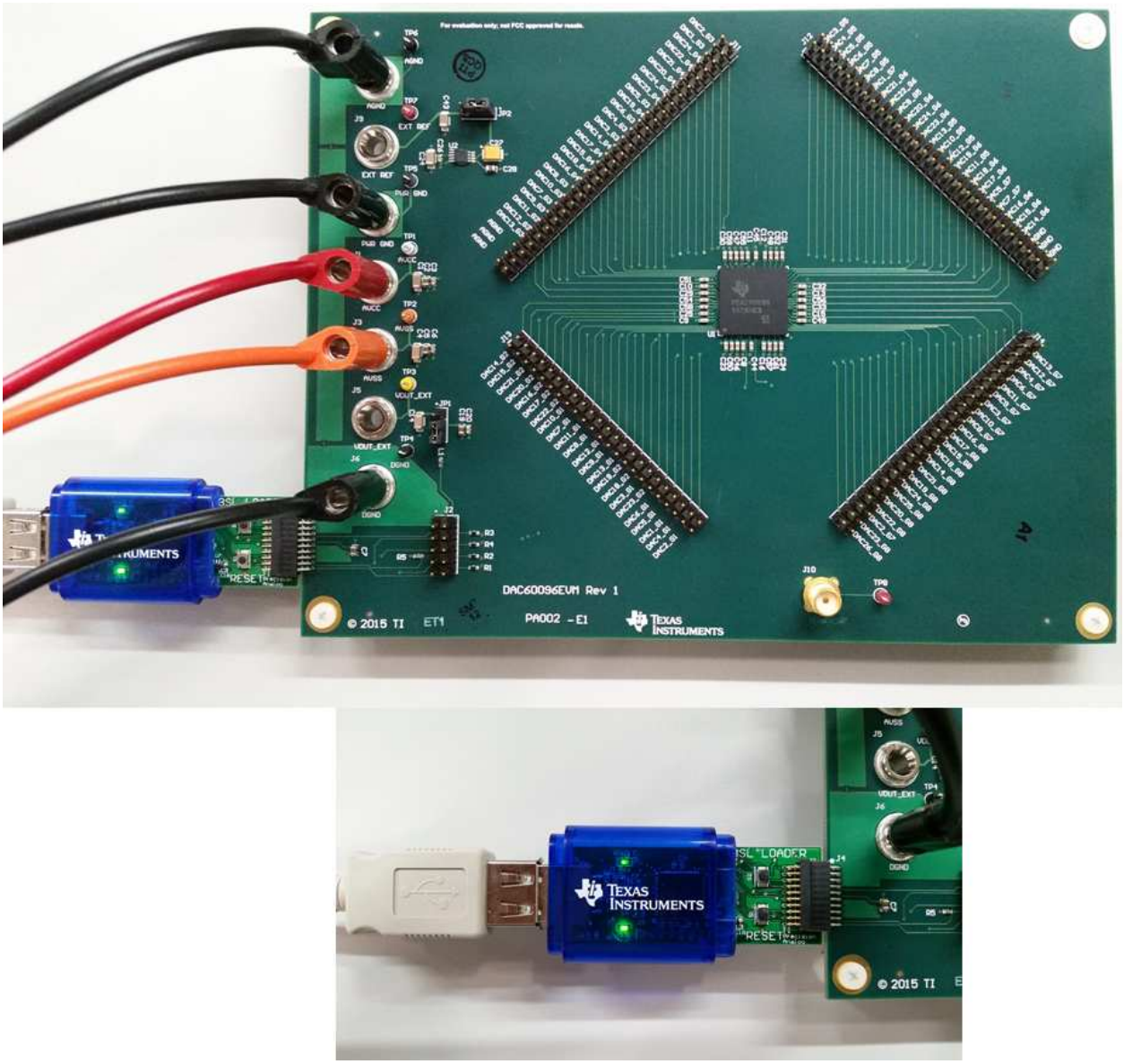

Figure 6. Typical Hardware Connections on the DAC60096EVM

4.3 Connecting the USB Cable to the SDM-DIG

Figure 7 shows the typical response when connecting the SDM-USB-DIG platform to a USB port of a PC for the first time. The PC usually responds with a *Found New Hardware, USB Device* pop-up dialog window. The pop-up window then changes to *Found New Hardware, Virtual COM Port (CDC)*. This pop-up indicates that the device is ready for use. The CDC driver is used for communication between the SDM-USB-DIG and PC.

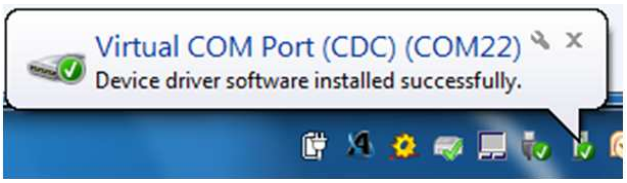

Figure 7. Confirmation of SDM-USB-DIG Platform Driver Installation

4.4 DAC60096EVM Power Configurations

The DAC60096EVM provides electrical connections to the device supply pins. The connectors and optional configurations are shown in Table 5.

Table 5. DAC60096EVM Power Supply Configuration

Connector	Connection Type	Description
J1	Banana plug	External AVCC connection (12 V)
J3	Banana plug	External AVSS connection (–12 V)
J5	Banana plug	External DVDD selection: • JP1 set to 1-2 connects J5 to DVDD pin • JP1 set to 2-3 connects SDM-USB-DIG 5V to DVDD pin
J6	Banana plug	Digital Ground connection
J7	Banana plug	Power Ground connection
J8	Banana plug	REF (reference) GND and analog GND connection
J9	Banana plug	External REF (reference) connection: • JP2 set to 1-2 connects reference to onboard REF5025 • JP2 set to 2-3 connects reference to J9 Connection

DVDD is supplied by the SDM-USB-DIG by default. If a different source is required, it is possible to separate the SDM-USB-DIG and DVDD by setting the jumper JP1 to 1-2. An external supply can then connect to J5 to power DVDD.

The DAC60096EVM provides access to all DAC outputs through connection headers J11, J12, J13, and J14 as shown in Figure 8, and listed in Table 6.

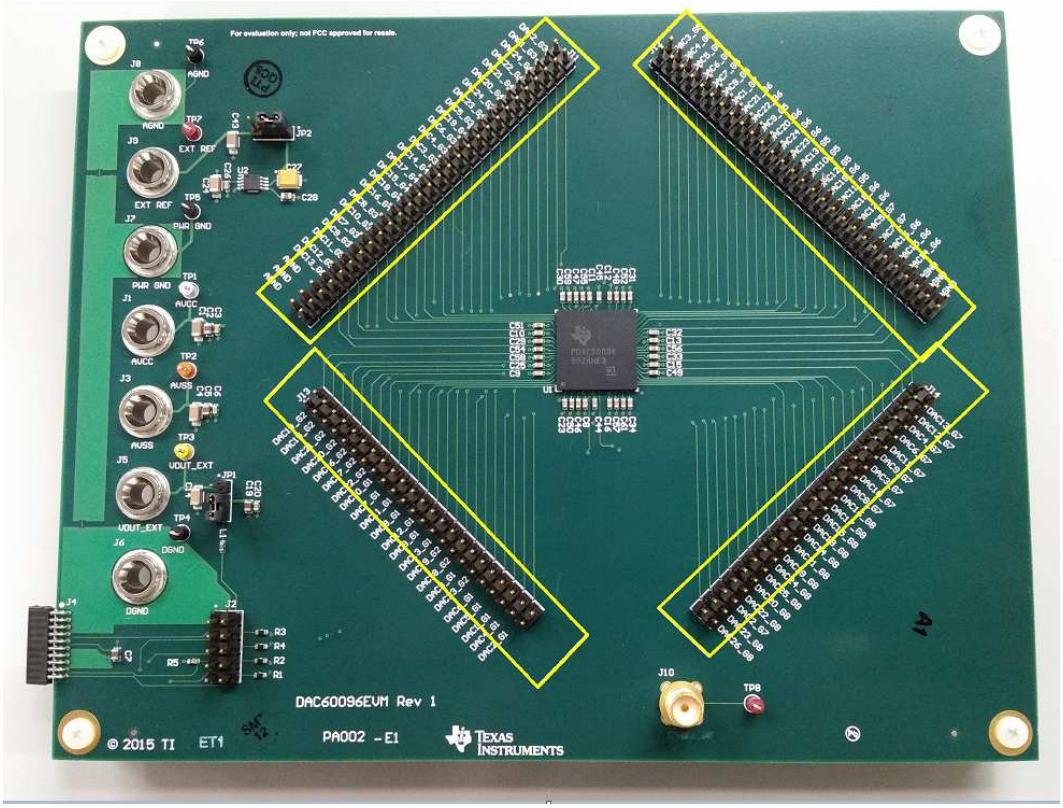

Figure 8. DAC Output Connection Headers

Table 6. DAC60096EVM DAC Signal Connections

Name	Connector	Description
DAC2_G3	J11-2	Un-buffered DAC output voltage
DAC1_G3	J11-4	Un-buffered DAC output voltage
DAC24_G4	J11-6	Un-buffered DAC output voltage
DAC22_G4	J11-8	Un-buffered DAC output voltage
DAC21_G4	J11-10	Un-buffered DAC output voltage
DAC20_G4	J11-12	Un-buffered DAC output voltage
DAC24_G2	J11-14	Un-buffered DAC output voltage
DAC23_G4	J11-16	Un-buffered DAC output voltage
DAC5_G3	J1-18	Un-buffered DAC output voltage
DAC19_G4	J11-20	Un-buffered DAC output voltage
DAC6_G3	J11-22	Un-buffered DAC output voltage
DAC4_G3	J11-24	Un-buffered DAC output voltage
DAC3_G3	J11-26	Un-buffered DAC output voltage
DAC14_G4	J11-28	Un-buffered DAC output voltage
DAC17_G4	J11-30	Un-buffered DAC output voltage
DAC15_G4	J11-32	Un-buffered DAC output voltage
DAC18_G4	J11-34	Un-buffered DAC output voltage
DAC16_G4	J11-36	Un-buffered DAC output voltage
DAC8_G3	J11-38	Un-buffered DAC output voltage

Table 6. DAC60096EVM DAC Signal Connections (continued)

Name	Connector	Description
DAC10_G3	J11-40	Un-buffered DAC output voltage
DAC7_G3	J11-42	Un-buffered DAC output voltage
DAC9_G3	J11-44	Un-buffered DAC output voltage
DAC11_G3	J11-46	Un-buffered DAC output voltage
DAC12_G3	J11-48	Un-buffered DAC output voltage
DAC13_G3	J11-50	Un-buffered DAC output voltage
DAC3_G5	J12-1	Un-buffered DAC output voltage
DAC4_G5	J12-3	Un-buffered DAC output voltage
DAC5_G5	J12-5	Un-buffered DAC output voltage
DAC6_G5	J12-7	Un-buffered DAC output voltage
DAC7_G5	J12-9	Un-buffered DAC output voltage
DAC8_G5	J12-11	Un-buffered DAC output voltage
DAC1_G7	J12-13	Un-buffered DAC output voltage
DAC21_G6	J12-15	Un-buffered DAC output voltage
DAC22_G6	J12-17	Un-buffered DAC output voltage
DAC9_G5	J12-19	Un-buffered DAC output voltage
DAC20_G6	J12-21	Un-buffered DAC output voltage
DAC24_G6	J12-23	Un-buffered DAC output voltage
DAC23_G6	J12-25	Un-buffered DAC output voltage
DAC13_G5	J12-27	Un-buffered DAC output voltage
DAC10_G5	J12-29	Un-buffered DAC output voltage
DAC12_G5	J12-31	Un-buffered DAC output voltage
DAC19_G6	J12-33	Un-buffered DAC output voltage
DAC11_G5	J12-35	Un-buffered DAC output voltage
DAC18_G6	J12-37	Un-buffered DAC output voltage
DAC17_G6	J12-39	Un-buffered DAC output voltage
DAC5_G7	J12-41	Un-buffered DAC output voltage
DAC7_G7	J12-43	Un-buffered DAC output voltage
DAC16_G6	J12-45	Un-buffered DAC output voltage
DAC15_G6	J12-47	Un-buffered DAC output voltage
DAC14_G6	J12-49	Un-buffered DAC output voltage
DAC14_G2	J13-2	Un-buffered DAC output voltage
DAC15_G2	J13-4	Un-buffered DAC output voltage
DAC21_G2	J13-6	Un-buffered DAC output voltage
DAC20_G2	J13-8	Un-buffered DAC output voltage
DAC16_G2	J13-10	Un-buffered DAC output voltage
DAC17_G2	J13-12	Un-buffered DAC output voltage
DAC22_G2	J13-14	Un-buffered DAC output voltage
DAC10_G1	J13-16	Un-buffered DAC output voltage
DAC7_G1	J13-18	Un-buffered DAC output voltage
DAC11_G1	J13-20	Un-buffered DAC output voltage
DAC8_G1	J13-22	Un-buffered DAC output voltage
DAC12_G1	J13-24	Un-buffered DAC output voltage
DAC9_G1	J13-26	Un-buffered DAC output voltage
DAC13_G1	J13-28	Un-buffered DAC output voltage
DAC19_G2	J13-30	Un-buffered DAC output voltage
DAC18_G2	J13-32	Un-buffered DAC output voltage

Table 6. DAC60096EVM DAC Signal Connections (continued)

Name	Connector	Description
DAC3_G1	J13-34	Un-buffered DAC output voltage
DAC23_G2	J13-36	Un-buffered DAC output voltage
DAC6_G1	J13-38	Un-buffered DAC output voltage
DAC5_G1	J13-40	Un-buffered DAC output voltage
DAC1_G1	J13-42	Un-buffered DAC output voltage
DAC4_G1	J13-44	Un-buffered DAC output voltage
DAC2_G1	J13-46	Un-buffered DAC output voltage
DAC13_G7	J14-1	Un-buffered DAC output voltage
DAC12_G7	J14-3	Un-buffered DAC output voltage
DAC4_G7	J14-5	Un-buffered DAC output voltage
DAC6_G7	J14-7	Un-buffered DAC output voltage
DAC11_G7	J14-9	Un-buffered DAC output voltage
DAC9_G7	J14-11	Un-buffered DAC output voltage
DAC3_G7	J14-13	Un-buffered DAC output voltage
DAC10_G7	J14-15	Un-buffered DAC output voltage
DAC8_G7	J14-17	Un-buffered DAC output voltage
DAC16_G8	J14-19	Un-buffered DAC output voltage
DAC17_G8	J14-21	Un-buffered DAC output voltage
DAC15_G8	J14-23	Un-buffered DAC output voltage
DAC18_G8	J14-25	Un-buffered DAC output voltage
DAC14_G8	J14-27	Un-buffered DAC output voltage
DAC21_G8	J14-29	Un-buffered DAC output voltage
DAC19_G8	J14-31	Un-buffered DAC output voltage
DAC24_G8	J14-33	Un-buffered DAC output voltage
DAC25_G8	J14-35	Un-buffered DAC output voltage
DAC20_G8	J14-37	Un-buffered DAC output voltage
DAC22_G8	J14-39	Un-buffered DAC output voltage
DAC2_G7	J14-41	Un-buffered DAC output voltage
DAC23_G8	J14-43	Un-buffered DAC output voltage
DAC26_G8	J14-45	Un-buffered DAC output voltage

4.5 SPI Communication Signals and Digital Inputs

The SPI signals are located on the J6 header and are described in Table 7, along with the digital input signals of the DAC60096 device.

Table 7. SPI Signal Definition

Name	Connector	Description
SCLK	J2-5	Serial interface clock
SDI	J2-3	Serial interface data input
SDO	J2-7	Serial interface data output
/CS	J2-8	Active low serial data enable
/CLEAR	J2-6	Asynchronous clear input
/RESET	J2-10	Reset input, active low
STATS	J2-9	DAC output status indicator
/LDAC	J2-4	Synchronous DAC load control input

4.6 External Trigger

The DAC60096 device also incorporates a trigger input signal. This signal enables all DAC outputs to toggle between the two DAC data registers associated with each DAC. This functionality enables the device to operate as a square-wave generator. The DAC registers are prepared for square-wave operation on a TRIGG rising edge and the outputs are toggled on each following TRIGG falling edge.

Table 8. External Trigger

Name	Connector	Description
Trigger	J10	Synchronous DAC load control input

5 DAC60096EVM Software Overview

This section discusses how to use the DAC60096EVM software.

5.1 Starting the DAC60096EVM Software

Once the hardware connections are established and jumper settings configured, launch the software located in the Texas Instruments folder of the *Start → All Programs* menu, and select the DAC60096 EVM icon (see Figure 9).

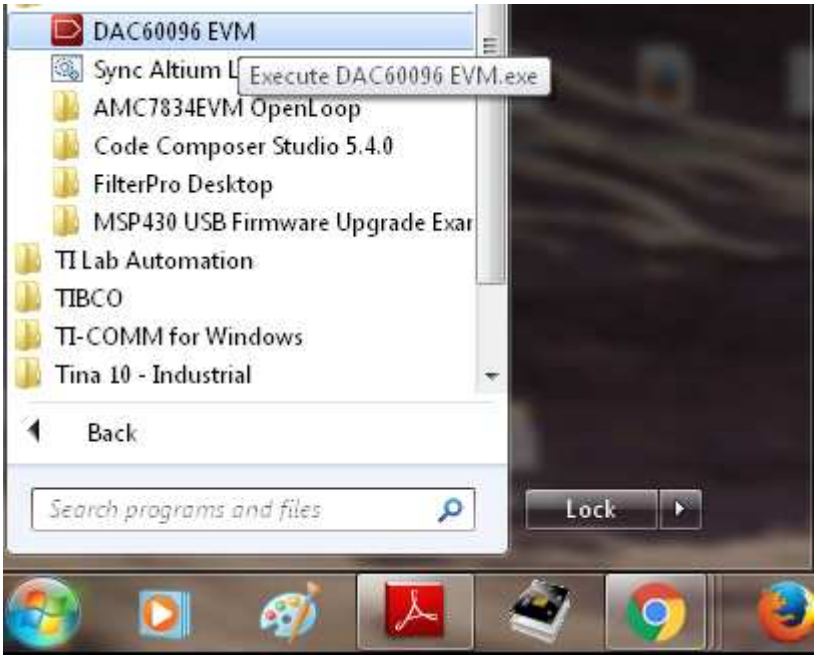

Figure 9. DAC60096EVM GUI Location

If the SDM-USB-DIG is properly connected to the DAC60096EVM, the GUI should automatically power the SDM-USB-DIG and display *HARDWARE CONNECTED* on the lower left of the GUI, as seen in Figure 10.

Figure 10. DAC60096EVM GUI – Power On

If the SDM-USB-DIG has a faulty connection, or is not connected at all, the GUI will launch in *DEMO* mode. If this text appears while the SDM-USB-DIG device is connected, then unplug the SDM-USB-DIG and close the GUI. Reconnect the SDM-USB-DIG, and ensure that the connectors are correctly aligned. After this, verify the USB extender cable is properly connected to both the SDM-USB-DIG and PC, and re-launch the GUI. This issue can also occur if the CDC driver is installed incorrectly, and so the DAC60096EVM software may need to be reinstalled.

5.2 DAC60096EVM Software Features

The following subsections describe the functionality of each page of the DAC60096EVM GUI.

5.2.1 DAC60096EVM Low Level Configuration Page

The DAC60096EVM features a *Register Map* page that allows access to low-level communication by directly writing to and reading from the DAC60096's registers. Selecting a register on the *Register Map* list presents a description of the values in that register, and also displays information such as the register's address, default value, size, and current value. The register values can be modified by either writing directly to the value column or selecting the bit individually. This is shown in Figure 11.

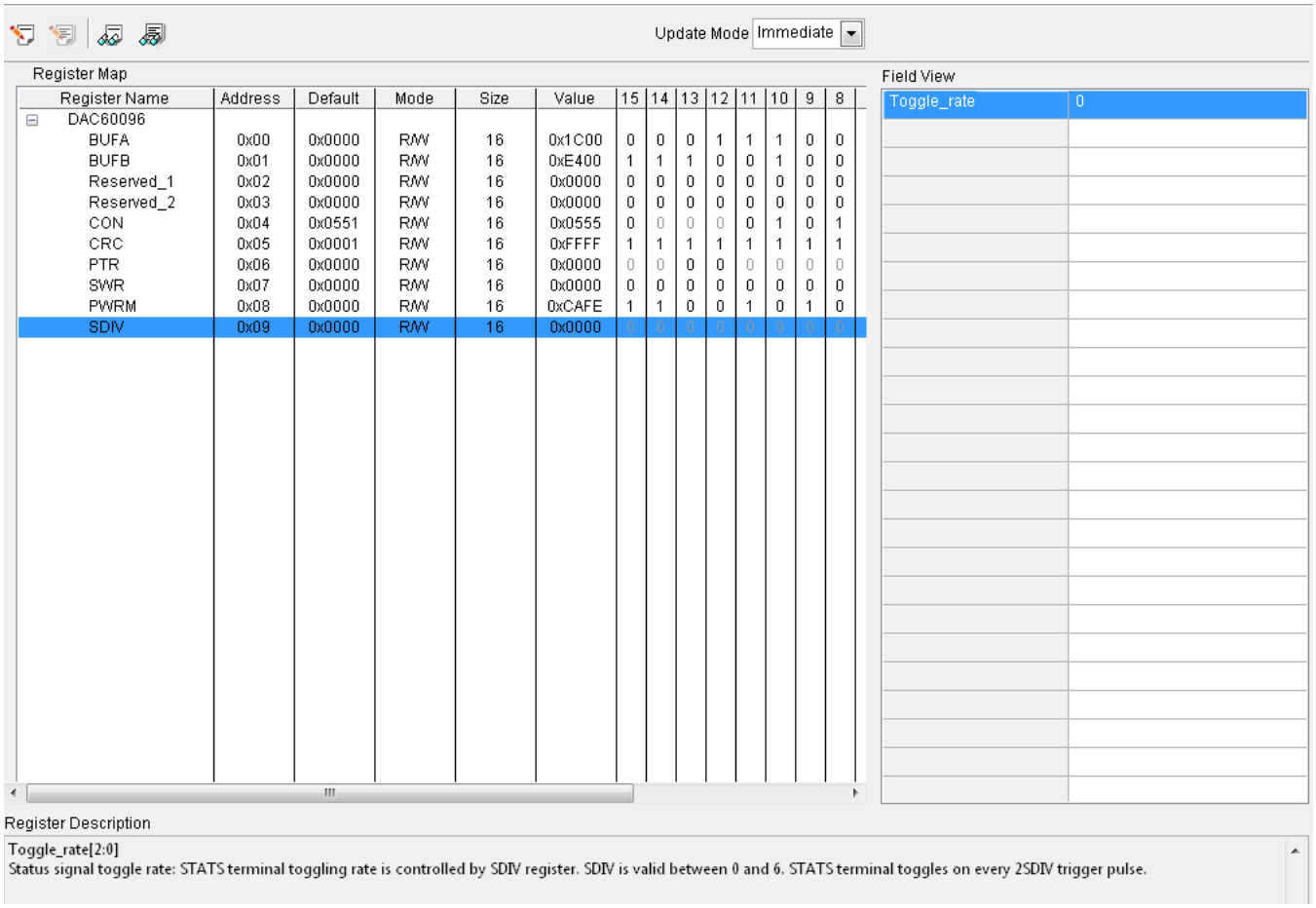

Figure 11. Low Level Configuration Page

The values of the register map can also be saved by pressing the *Save Configuration* button under the File menu option. Additionally, the configuration files can be accessed through the *Load Configuration* button.

Other options selectable by the user are the *Update Mode*, *Write Selected* (red box), *Read Selected* (orange box), *Write Modified* (gray box), and *Read All* (yellow box) buttons. All buttons are displayed in Figure 12.

Figure 12. Low Level Configuration Page Available Options

If *Update Mode* is selected to “Immediate”, all changes to register values update immediately, while “Deferred” allows the user to modify the value of a register without taking effect until the *Write Selected*, or *Write Modified* button is pressed.

The *Read Selected* button allows individual register reads, while the *Read All* button reads the status of all registers located in the register map.

5.2.2 DAC60096EVM High Level Configuration Page

The *High Level Configuration* page provides an interface to observe and control the different data registers, modes, and configurations available for the DAC60096 device. Figure 13 displays this page.

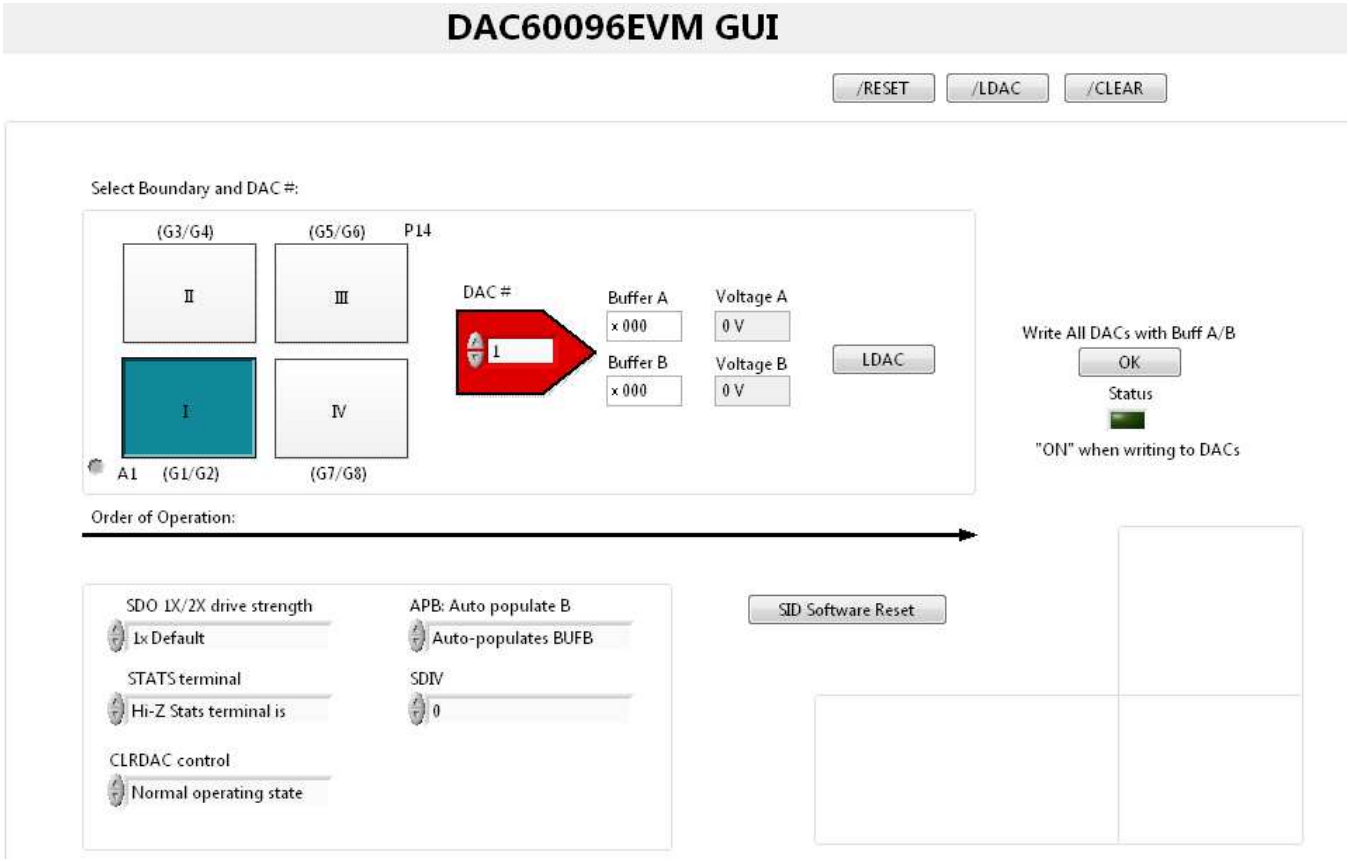

Figure 13. High Level Configuration Page

To write to a DAC channel of the device, the GUI is designed with 4 interactive inputs that are highlighted in Figure 14. The first four buttons, displayed within the red box, can be pressed to select any of the 4 quadrants of the DAC60096 device. Once the quadrant is chosen, the appropriate DAC channel is input in the *DAC Pointer* field, which is displayed in the gray box. The orange box displays the digital code inputs, Buffer A and Buffer B. Once an acceptable 12-bit code is written into the fields, the GUI updates the internal Buffer Registers and also provides a numeric display of the code represented as a voltage. Pressing the *LDAC* button issues a LDAC trigger at /CS rising edge, which enables the data to latch to the DAC Active Registers and output the programmed voltage.

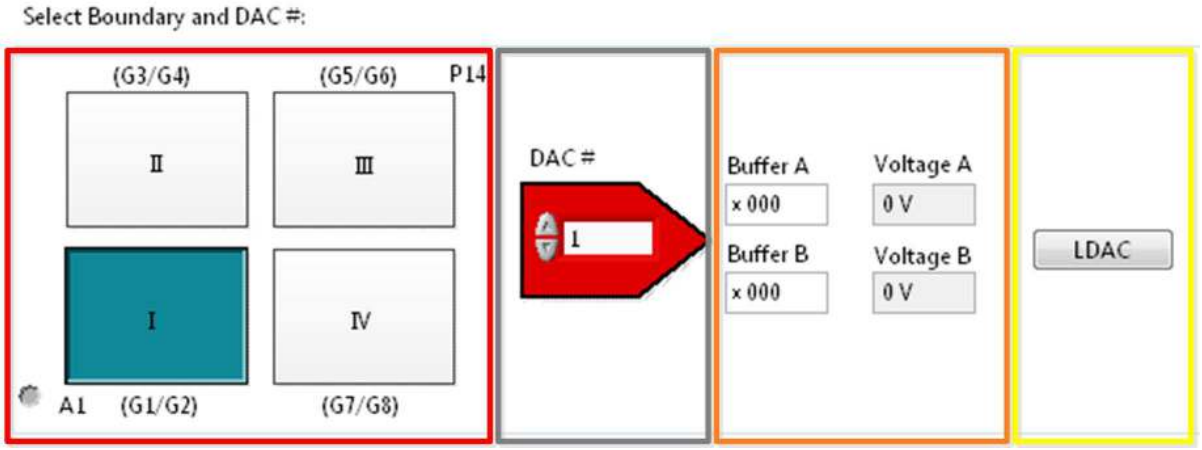

Figure 14. DAC Channel Write Order of Operation

An option to update all DAC Registers is provided with the “Write All DACs with Buff A/B” button. As the name suggests, this will write to all the DAC registers of the DAC60096 device, and issue the LDAC triggers for all quadrants. The *Status LED* keeps track of the status, once the GUI starts writing to the channels the LED turns ON and remains ON until all channels are updated.

Figure 15. Write All DACs Button

The remaining controls allow the user to adjust the register values for DAC60096 device settings. These controls are shown in Figure 16, and explained in Table 9.

Figure 16. Register Control Buttons

Table 9. Register Controls

Name	Register, Bit	Description
SDO 1x/2x	0x4, 11:10	'01': 1X (default) '10': 2X
STATS terminal	0x4, 9:8	'01': Hi-Z. STATS terminal is disabled '10': CMOS Push-pull output. Should only be enabled for sub-system 1.
PHAINV	0x4, 7:6	'01': SCLK NegEdge '10': SCLK PosEdge
CLRDAC	0x4, 5:4	'01': Normal operating state '10': Clear DAC state
APB	0x4, 1:0	'01': auto-populates BUFB with the negative value of BUFA after each BUFA register write. Writing to BUFB has no auto-populate effect. '10': disable auto populate B feature.
SDIV	0x9, 2:0	STATS terminal toggling rate is controlled by SDIV register. SDIV is valid between 0 and 6. STATS terminal toggles on every 2SDIV trigger pulse. The SDIV setting should only be updated after a device reset and before configuring the DAC outputs.

The High Level Configuration Page also provides a button interface to control different digital inputs, as shown in Figure 17. The digital inputs include the /RESET, /LDAC, and /CLEAR signals. Pressing any of the buttons creates an active low signal that asserts the functionality tied to the signal. The input signal remains low until the button is pressed a second time, bringing it to a high state.

Figure 17. Digital Input Buttons

A brief description of the digital inputs tied to the button interface is provided in Table 10.

Table 10. Digital Inputs

Digital Input	Description
/RESET	Reset input. Logic low on this terminal causes the device to perform a hardware reset.
/LDAC	Synchronous DAC load control input. When /LDAC is low, the DAC outputs are updated immediately after a register write. If left high during DAC register updates, a falling edge on /LDAC causes all DAC outputs to update simultaneously.
/CLEAR	Asynchronous clear input. When /CLR is activated, all DACs are loaded with code 000h. When /CLR is cleared, all DACs return to normal operation.

6 DAC60096EVM Documentation

This section contains the complete bill of materials and schematic diagram for the DAC60096EVM. Documentation information for the SDM-USB-DIG Platform can be found in the SDM-USB-DIG Platform User's Guide, SBOU136, available at the TI web site at www.ti.com.

6.1 DAC60096EVM Board Schematic

Figure 18 and Figure 19 illustrate the DAC60096EVM board schematics.

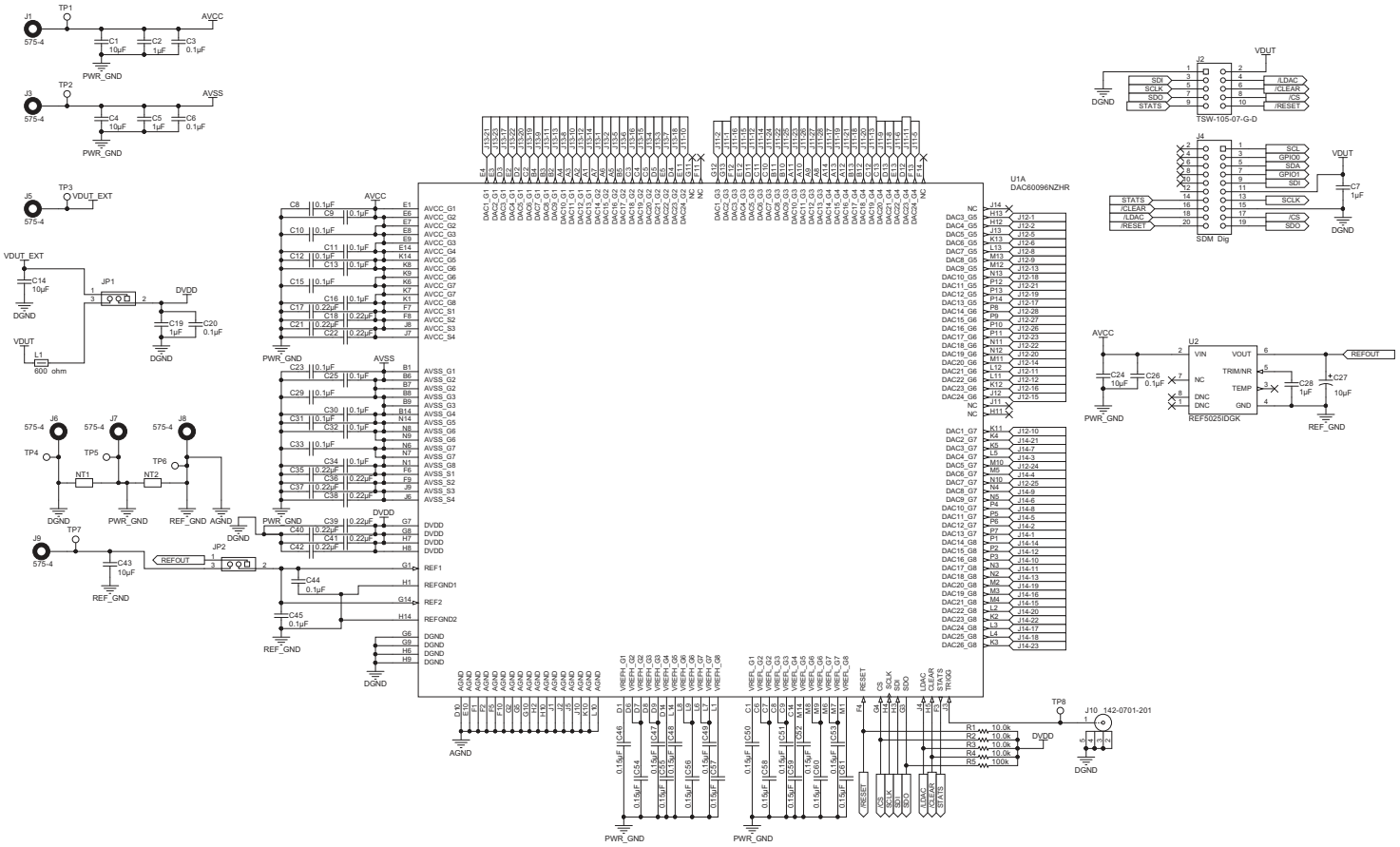

Figure 18. DAC60096EVM Board Schematic

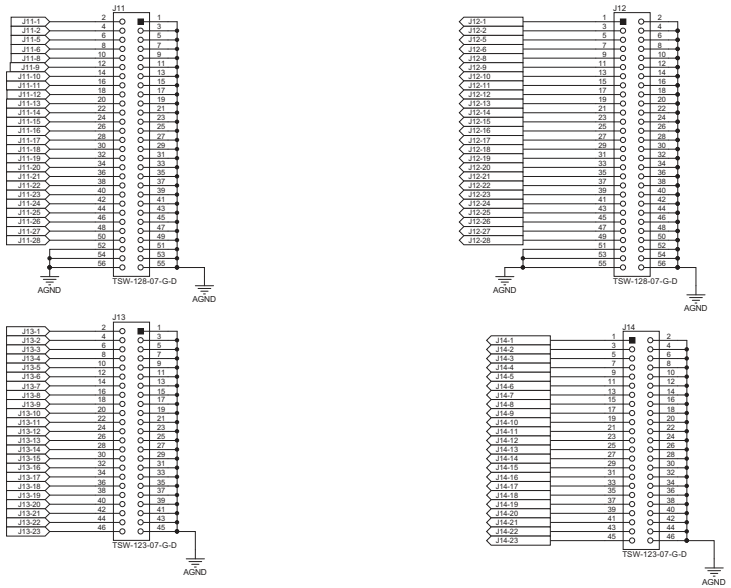

Figure 19. DAC60096EVM Board Schematic

6.2 DAC60096EVM PCB Components Layout

Figure 20 shows the layout of the components for the DAC60096EVM board.

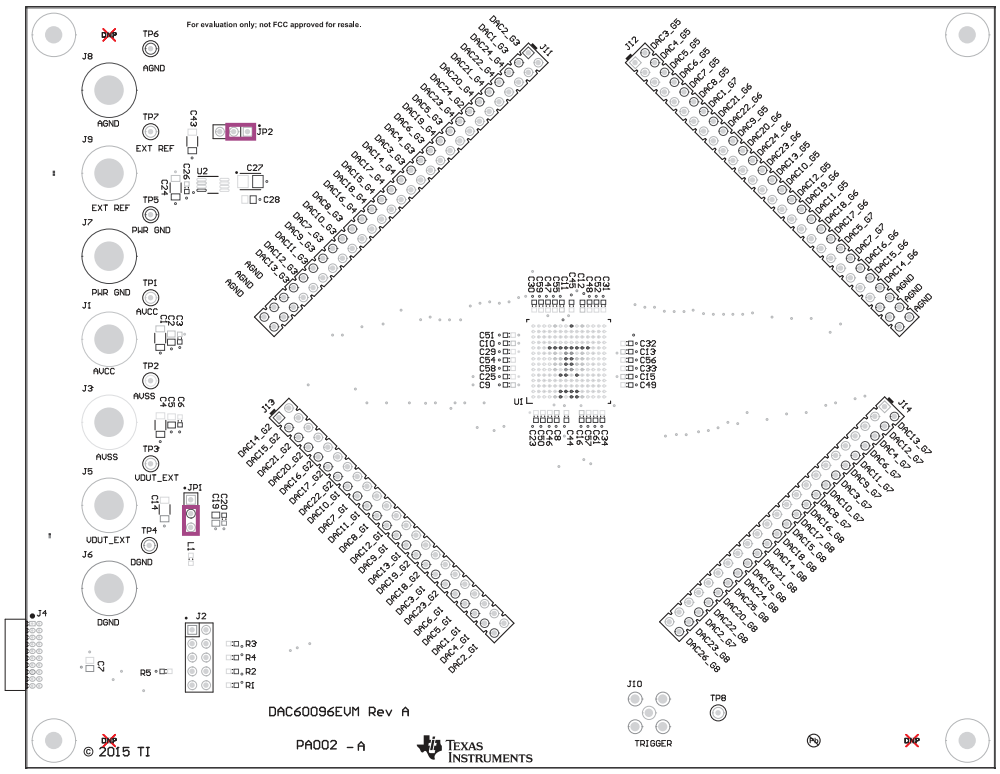

Figure 20. DAC60096EVM PCB Components Layout

6.3 DAC60096 Test Board Bill of Materials

Table 11 lists the DAC60096 test board bill of materials.

Table 11. DAC60096 Test Board Bill of Materials

Qty	Designator	Description	Part Number	Manufacturer
1	!PCB1	Printed Circuit Board	PA002	Any
5	C1, C4, C14, C24, C43	CAP, CERM, 10 µF, 50 V, +/- 10%, X5R, 1206_190	GRM31CR61H106KA12L	Murata
5	C2, C5, C7, C19, C28	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R, 0805	GRM21BR71H105KA12L	Murata
22	C3, C6, C8, C9, C10, C11, C12, C13, C15, C16, C20, C23, C25, C26, C29, C30, C31, C32, C33, C34, C44, C45	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	06035C104KAT2A	AVX
12	C17, C18, C21, C22, C35, C36, C37, C38, C39, C40, C41, C42	CAP, CERM, 0.22 µF, 16 V, +/- 10%, X7R, 0402	C1005X7R1C224K050BC	TDK
1	C27	CAP, TA, 10 µF, 16 V, +/- 10%, 0.5 ohm, SMD	TPSB106K016R0500	AVX
16	C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61	CAP, CERM, 0.15 µF, 25 V, +/- 10%, X7R, 0603	C1608X7R1E154K080AA	TDK
4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
7	J1, J3, J5, J6, J7, J8, J9	Standard Banana Jack, Uninsulated, 5.5mm	575-4	Keystone
1	J2	Header, 100mil, 5x2, Gold, TH	TSW-105-07-G-D	Samtec
1	J4	Receptacle, 50mil 10x2, R/A, TH	853-43-020-20-001000	Mill-Max
1	J10	Connector, TH, SMA	142-0701-201	Emerson Network Power
2	J11, J12	Header, 100mil, 28x2, Gold, TH	TSW-128-07-G-D	Samtec
2	J13, J14	Header, 2.54 mm, 23x2, Gold, TH	TSW-123-07-G-D	Samtec
2	JP1, JP2	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
1	L1	Ferrite Bead, 600 ohm @ 100 MHz, 0.2 A, 0603	BLM18HG601SN1D	Murata
4	R1, R2, R3, R4	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo America
1	R5	RES, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo America
2	SH-JP1, SH-JP2	Shunt, 100mil, Gold plated, Black	969102-0000-DA	3M
1	TP1	Test Point, Miniature, White, TH	5002	Keystone
1	TP2	Test Point, Miniature, Orange, TH	5003	Keystone
1	TP3	Test Point, Miniature, Yellow, TH	5004	Keystone
3	TP4, TP5, TP6	Test Point, Miniature, Black, TH	5001	Keystone
2	TP7, TP8	Test Point, Miniature, Red, TH	5000	Keystone
1	U1	96-Channel, 12-Bit Low-Power, Serial Input, Unbuffered, High-Voltage Output DAC with External Conversion Trigger, NZH0196A	DAC60096NZHR	Texas Instruments
1	U2	Low-Noise, Very Low Drift, Precision VOLTAGE REFERENCE, DGK0008A	REF5025IDGK	Texas Instruments

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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