HITFET™ +24V BTT3050EJ

Smart low-side power switch

Features

- Single channel device optimized for 24 V applications
- Electrostatic discharge protection (ESD)
- Overcurrent, active clamping and overtemperature protection
- Overtemperature latch shutdown
- Supply pin undervoltage protection
- Dedicated status signal
- Slew-rate control to adjust switching speed
- PWM switching capability of 20 KHz (duty cycle 10%-90%)
- Green product (RoHS compliant)
- AEC qualified

Potential applications

Suitable for resistive and inductive loads.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

BTT3050EJ is a 50 mΩ single channel smart low-side power switch within a PG-TDSO-8 package providing embedded protective functions. The power transistor is built by a N-channel vertical power MOSFET. BTT3050EJ is monolithically integrated, automotive qualified and optimized for 24 V automotive applications.

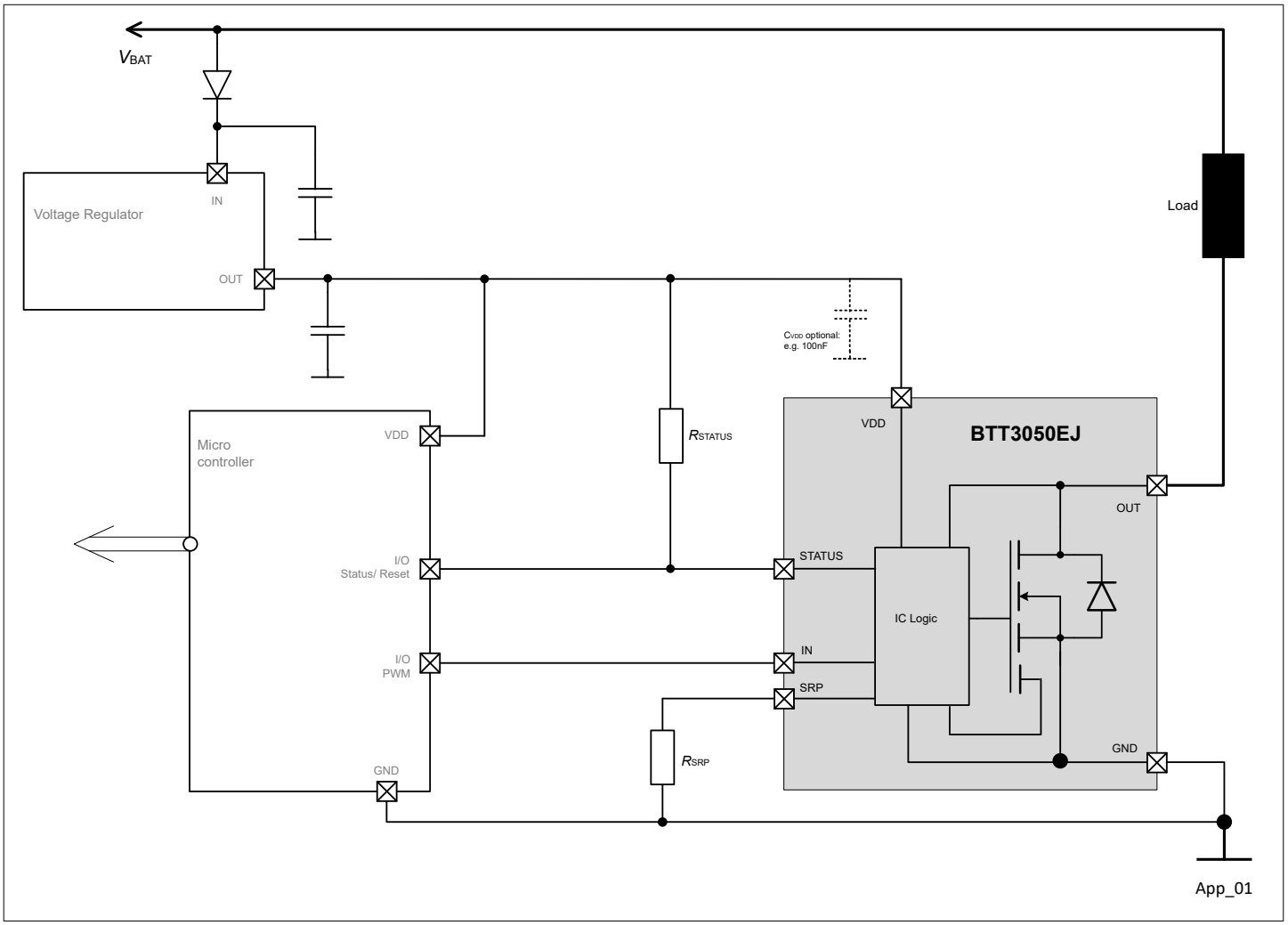

Table 1 Product summary

Parameter	Symbol	Values
Operating voltage range	V_{OUT}	0 … 36 V
Maximum load voltage	$V_{BAT(OUT)}$	63 V
ON-state resistance	$R_{DS(ON)\_25}$	50 mΩ
Nominal load current	$I_{L(NOM)}$	4 A
Minimum current limitation	$I_{L(LIM)}$	10 A

Product type	Package	Marking	Ordering code
BTT3050EJ	PG-TDSO-8	T3050EJ	BTT3050EJXUMA1

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1 Block diagram

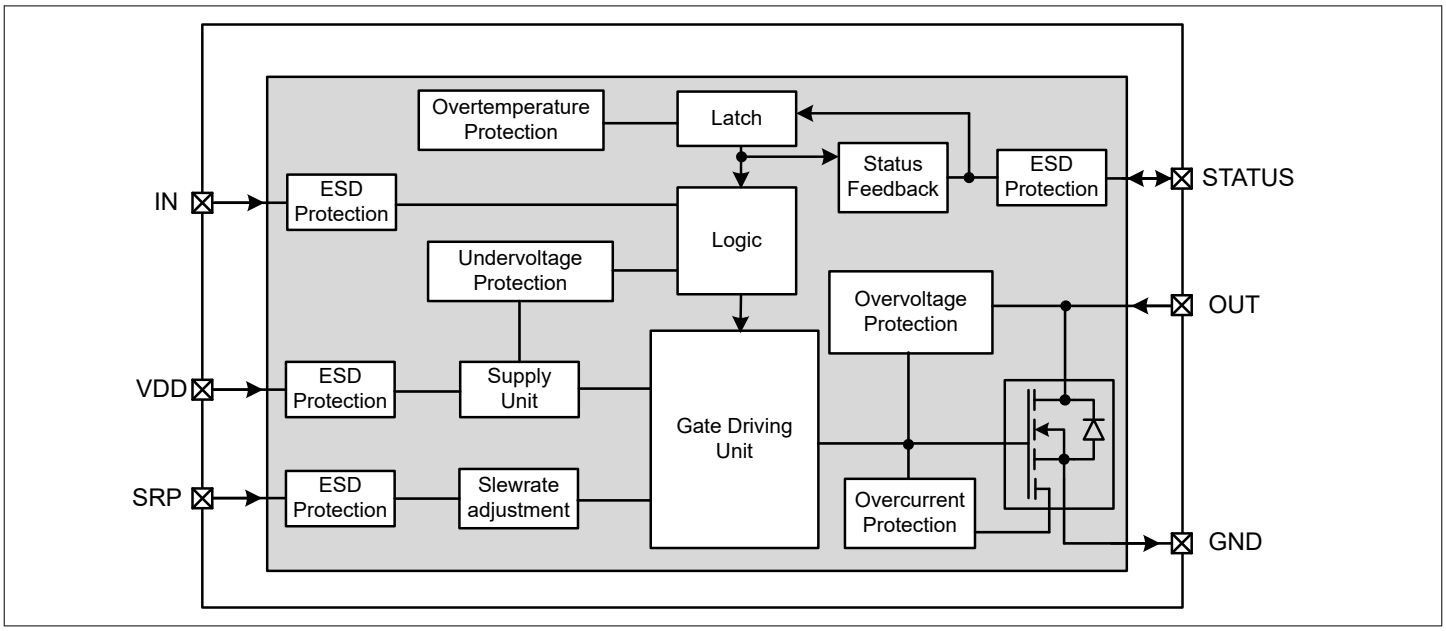

Figure 1 Block diagram of BTT3050EJ

2 Pin configuration

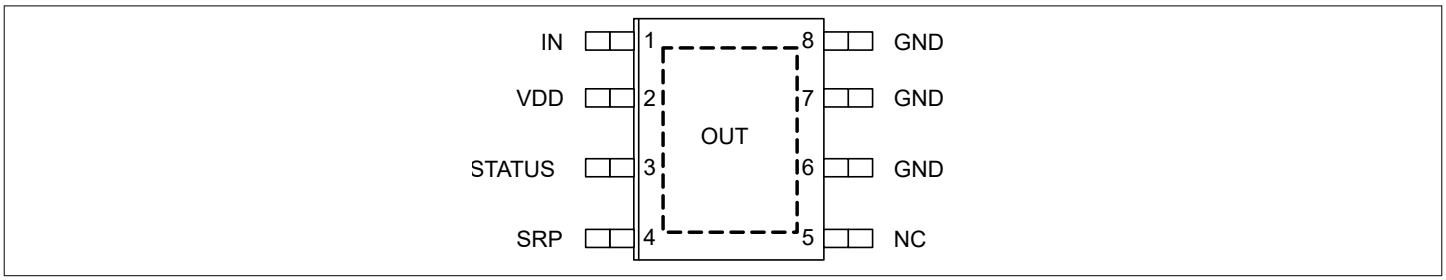

Figure 2 Pin configuration

Table 2 Pin definitions and functions

Pin	Symbol	I/O	Function
1	IN	I	If IN logic is high, switches ON the power DMOS If IN logic is low, switches OFF the power DMOS
2	VDD	I	Logic supply voltage pin, 3.3 V to 5.5 V
3	STATUS	I/O	RESET thermal latch function by microcontroller and pull-up If STATUS logic is high, device is in normal operation If STATUS logic is low, device is in overtemperature condition
4	SRP	I	Slew rate control with external resistor
5	NC	–	Pin internally not connected
6,7,8	GND	I/O	GND; source of power DMOS and logic [1)]
Cooling Tab	OUT	I/O	Load connection, drain of power DMOS

1) All GND pins must be connected together

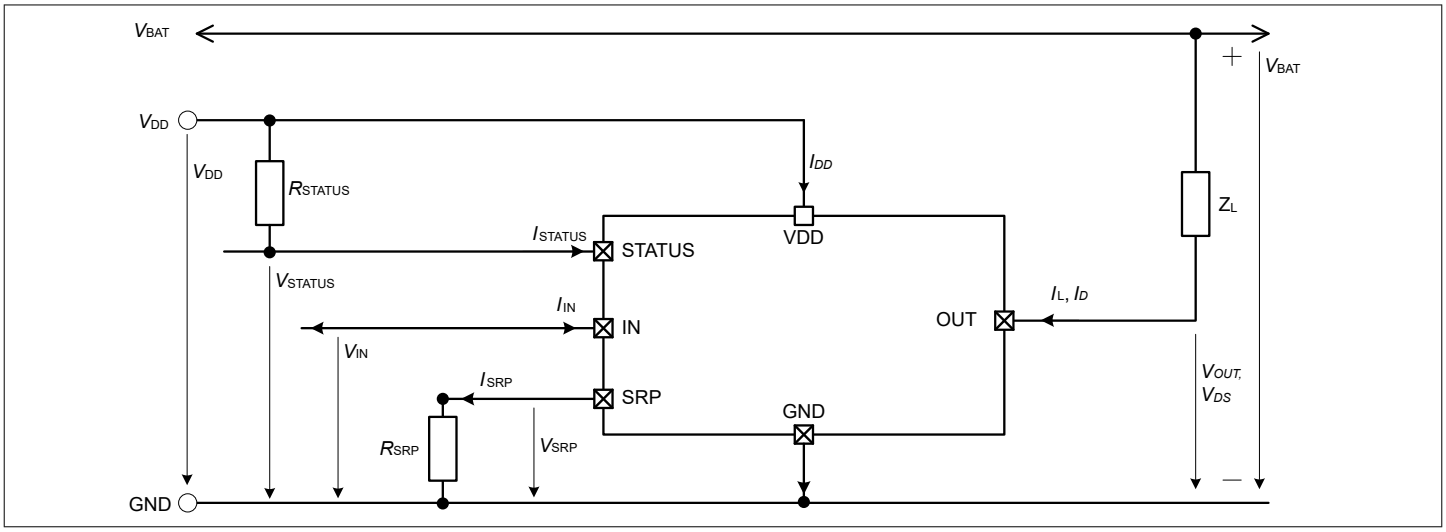

Figure 3 Naming definition of electrical parameters

3 General product characteristics

3.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

[1] T = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltages							
Output voltage	V_{OUT}	-0.3	–	63	V	Internally clamped	PRQ-296
Battery voltage for short circuit protection (extended range)	$V_{BAT(SC)}$	-0.3	–	36	V	V_{IN} = 5 V; T_A = 25°C, 125°C (3 samp./temp.); R_{ECU} (pin OUT) = 20 mΩ; R_{CABLE} (pin OUT) = 16 mΩ; L_{CABLE} (pin OUT) = 1 µH/m; L_{SC} (pin OUT) = 5 µH + L_{cable}; l = 40 m	PRQ-297
Power stage							
Load current	I_L	0	–	$I_{L(LIM)}$	A	–	PRQ-298
Logic pins							
Input voltage	V_{IN}	-0.3	–	5.5	V	–	PRQ-299
Status voltage	V_{STATUS}	-0.3	–	5.5	V	–	PRQ-300
SRP voltage	V_{SRP}	-0.3	–	5.5	V	–	PRQ-301
Supply voltage	V_{DD}	-0.3	–	6.5	V	–	PRQ-302
Energy capability							
Energy single pulse	E_{AS}	–	–	100	mJ	$I_{L(0)}$ = $I_{L(NOM)}$; V_{BAT} = 28 V; $T_{J(0)}$ = 150°C	PRQ-303
Energy repetitive pulse 20 M cycles	$E_{AR(20M)}$	–	–	50	mJ	$I_{L(0)}$ = $I_{L(NOM)}$; V_{BAT} = 28 V; $T_{J(0)}$ = 105°C	PRQ-306
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-308
Storage temperature	T_{STG}	-55	–	150	°C	–	PRQ-309
ESD susceptibility							
ESD susceptibility (all pins except OUT tab, to GND)	V_{ESD}	-2	–	2	kV	[2] HBM	PRQ-310
ESD susceptibility (OUT tab to GND)	V_{ESD_OUT}	-4	–	4	kV	[2] HBM	PRQ-311

(table continues...)

Table 3 (continued) Absolute maximum ratings

1) T = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ESD susceptibility (all pins)	V_{ESD_CDMA}	-500	–	500	V	3) CDM	PRQ-312
ESD susceptibility (corner pins)	V_{ESD_CDMC}	-750	–	750	V	3) CDM	PRQ-313

1) Not subject to production test, specified by design
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Battery voltage range for nominal operation	$V_{BAT(NOR)}$	6	–	36	V	1)	PRQ-314
Supply voltage range for nominal operation	$V_{DD(NOR)}$	3.3	–	5.5	V	1)	PRQ-316
Supply voltage range for extended_1 operation	$V_{DD(EXT1)}$	3.0	–	5.5	V	1) Parameter deviations possible	PRQ-315
Supply voltage range for extended_2 operation	$V_{DD(EXT2)}$	5.5	–	6.5	V	1) V_{BAT} < 46 V; Parameter deviations possible	PRQ-551
Junction temperature	T_J	-40	–	150	°C	1)	PRQ-318
External resistor range for adjustable slewrate operation	R_{SRP}	2.2	–	160	kΩ	1)	PRQ-319

1) Not subject to production test, specified by design

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical characteristics table.

3.3 Thermal resistance

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	3.0	–	K/W	1) 2)	PRQ-320
Junction to ambient 2s2p	$R_{thJA(2s2p)}$	–	35	–	K/W	1) 3)	PRQ-321
Junction to ambient (1s0p + 600 mm2Cu)	$R_{thJA(1s0p)}$	–	45	–	K/W	1) 4)	PRQ-322

1) Not subject to production test, specified by design
2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup. Bottom of the package is fixed to ambient temperature. T_{AMB} = 85°C. Device loaded with 1 W power.
3) Specified R_{thJA} value is according to Jedec JESD51-2, -7 at natural convection of FR4 2s2p board; the product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). T_{AMB} = 85°C. Device loaded with 1 W power.
4) Specified R_{thJA} value is according to Jedec JESD51-2, -7 at natural convection on FR4 1s0p board; the product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with additional heatspreading copper area of 600 m^2 and 70 µm thickness. T_{AMB} = 85°C. Device loaded with 1 W power.

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

3.4 Transient thermal impedance

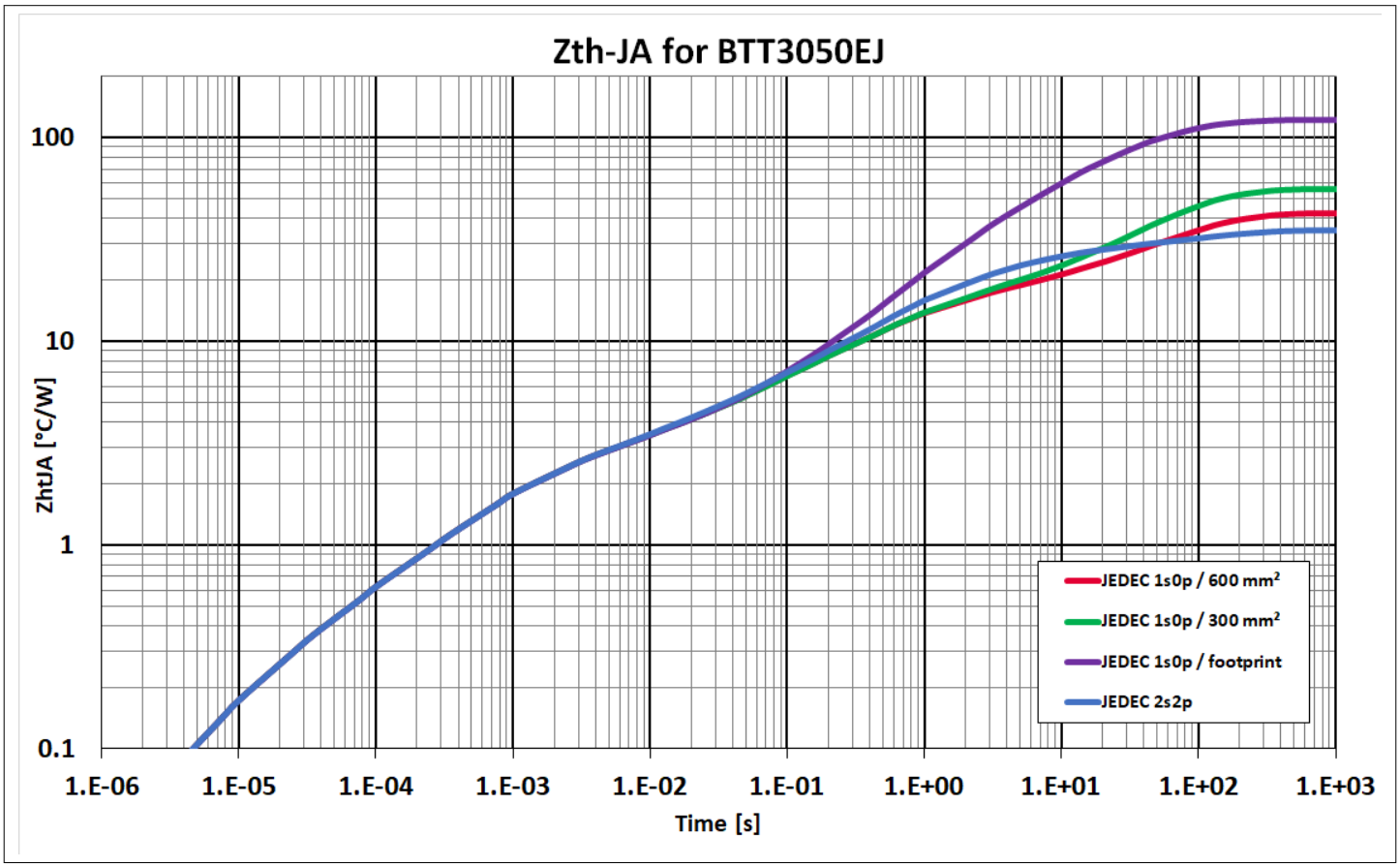

Figure 4 ZthJA = f(tp)

Typical transient thermal impedance $Z_{thJA} = f(t_p)$, $T_A = 85°C$.

In Figure 4 the value is according to Jedec JESD51-2, at natural convection on FR4 boards. Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. The device is dissipating 1 W power.

4 Power stage

4.1 Output on-state resistance

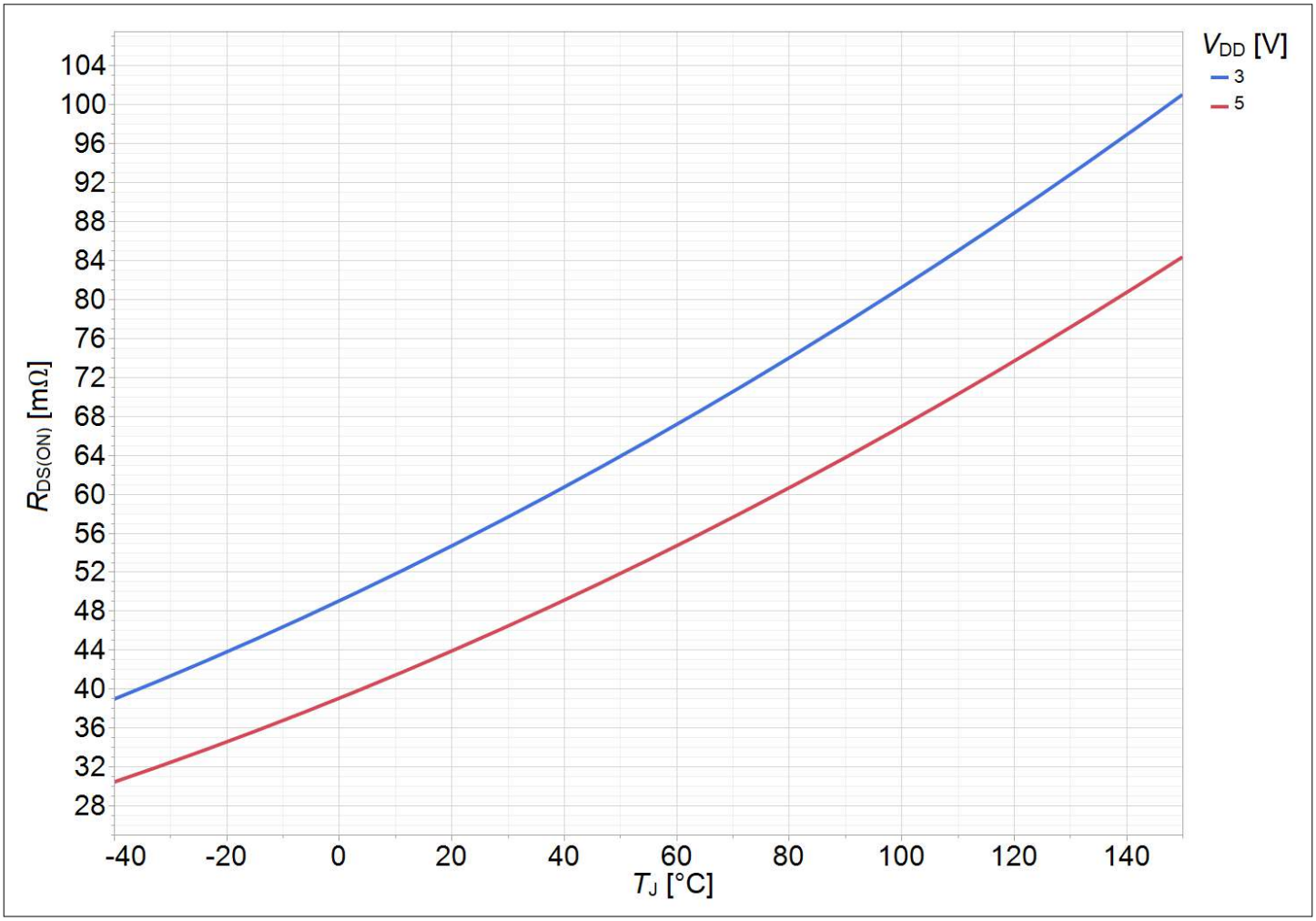

Figure 5 Typical on-state resistance $R_{DS(ON)}$ = f(T_J); V_{DD} = V_{IN} = 5 V, 3 V

Figure to be updated.

The on-state resistance depends on the supply voltage (V_{DD}) as well as on the junction temperature (T_J). Figure 5 shows these dependencies in terms of temperature and voltage for the typical on-state resistance $R_{DS(ON)}$. The behavior in reverse polarity is described in Reverse current capability.

4.2 Resistive load output timing

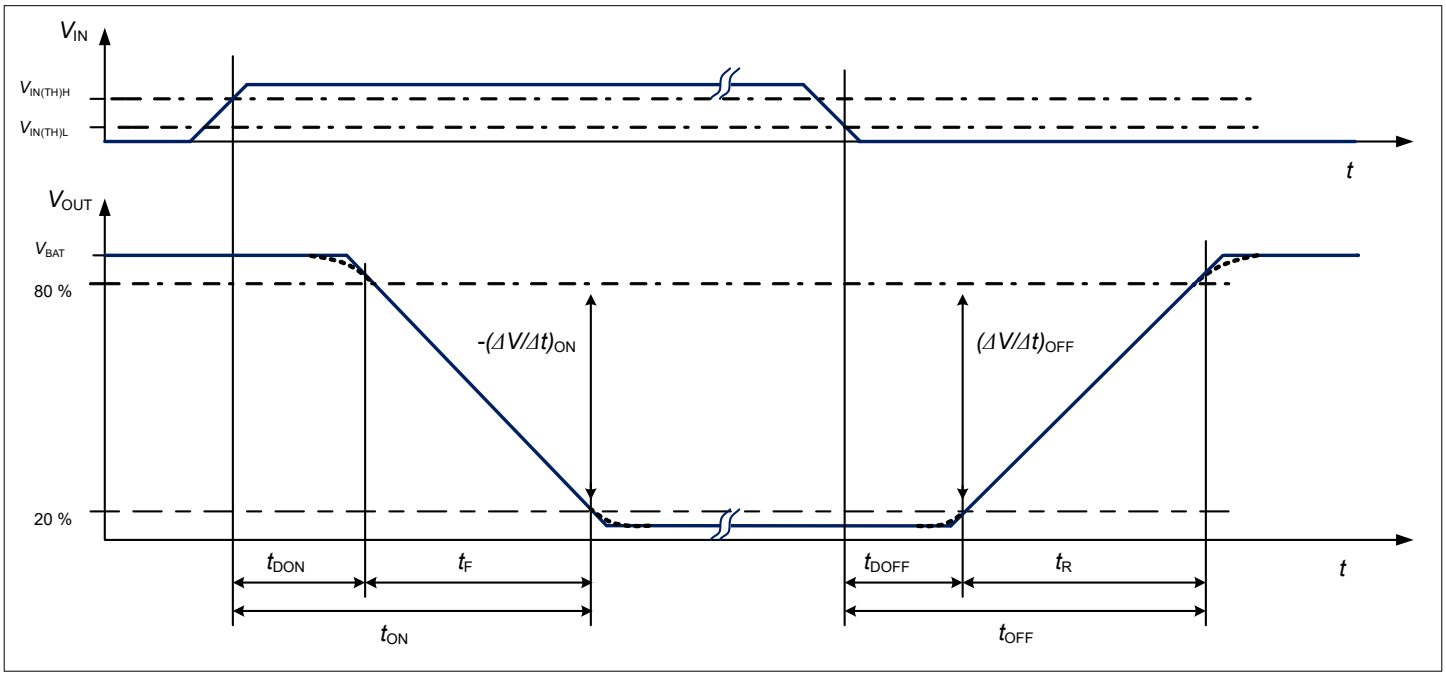

Figure 6 Definition of power output timing for resistive load

Figure 6 shows the typical timing when switching a resistive load.

Both -(Δ*V*/Δ*t*)ON and (Δ*V*/Δ*t*)OFF can be calculated using the following formulas:

- Turn-on slew rate: $-(\Delta V/\Delta t)_{ON} = (0.6 \times V_{BAT}) / t_F$
- Turn-off slew rate: $(\Delta V/\Delta t)_{OFF} = (0.6 \times V_{BAT}) / t_R$

NB: the coefficient 0.6 is based on 20% to 80% of V_{BAT}, this is how the measurement of Δ*V* is defined.

As shown in Figure 6 t_{ON} and t_{OFF} can be calculated from delay time (t_{DON}, t_{DOFF}) and falling/rising time (t_F, t_R) using the following formulas:

- Turn-on time: $t_{ON} = t_{DON} + t_F$
- Turn-off time: $t_{OFF} = t_{DOFF} + t_R$

4.3 Adjustable switching speed and slewrate

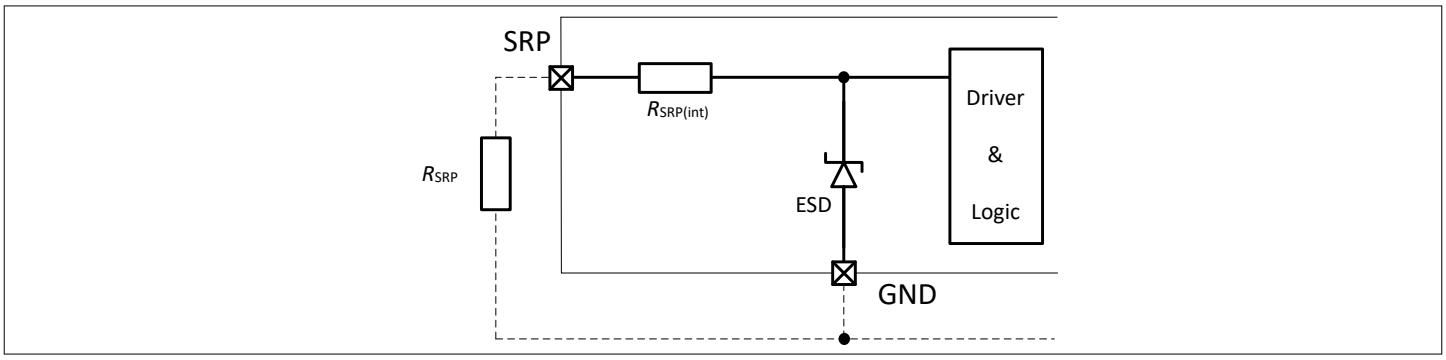

Figure 7 Simplified SRP circuit

Figure 7 shows the slew rate control circuit of BTT3050EJ. The circuit includes an ESD protection mechanism via a zener structure.

In order to optimize the switching speed of the MOSFET to a specific application, an external resistor can be connected between SRP pin and GND to select the desired slew rate (see switching timings in Power stage) . The adjustment of the slew rate also allows to balance between electromagnetic emissions and power dissipation.

To reduce the number of external components, the SRP pin can be connected directly to GND. This sets the slew rate at its largest value enabling fast switching timings.

It is not recommended to connect directly SRP pin to V_{DD} or to leave it floating (open).

The accuracy of the switching speed is dependent on the accuracy of the external resistor used. It is recommended to use short connections between the SRP pin and either R_{SRP}, GND bias.

Figure 8 shows the typical relation between switching speed and the external SRP resistor (R_{SRP}).

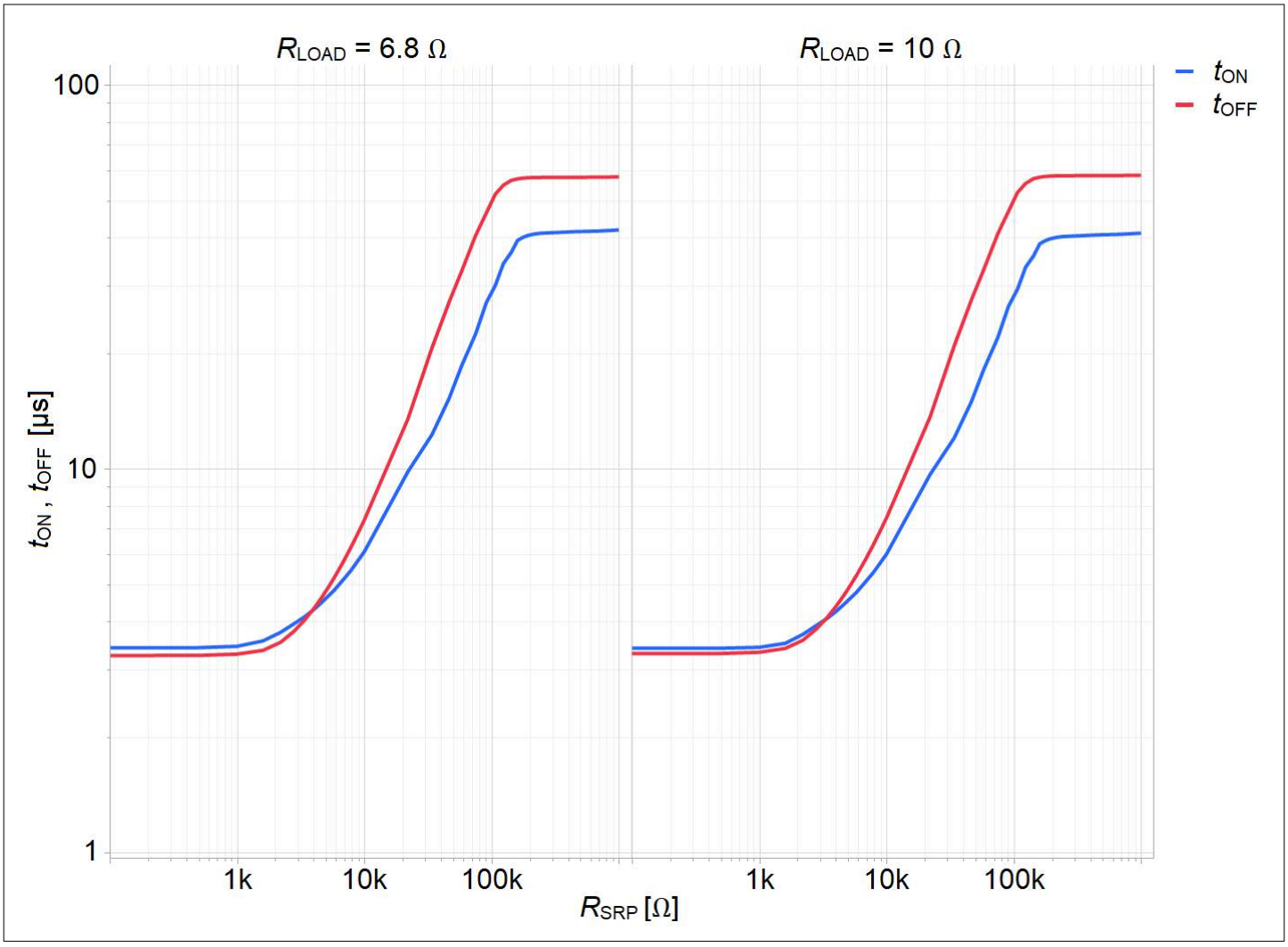

Figure 8 **Typical, simplified diagram representing the relation between R_{SRP} and t_{ON}, t_{OFF}; V_{DD} = 5 V; R_{Load} = 6.8 Ω, 10 Ω**

4.3.1 Output clamping

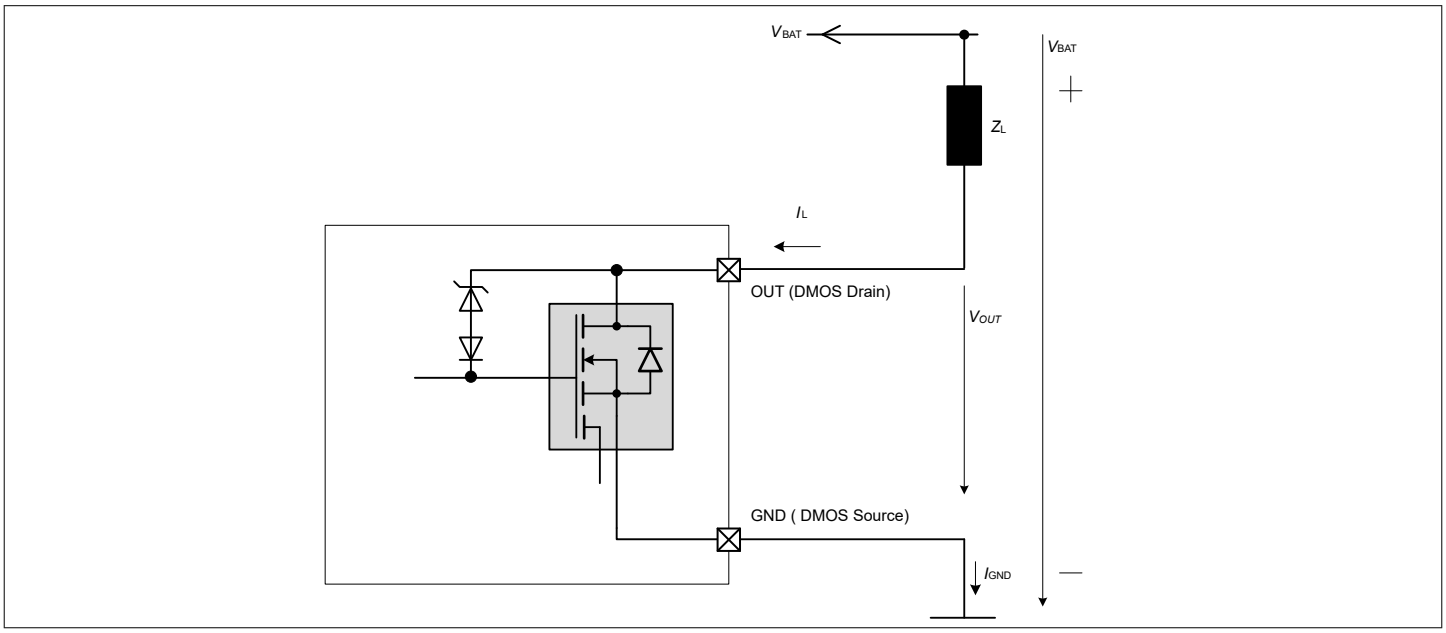

Figure 9 Output clamp circuitry

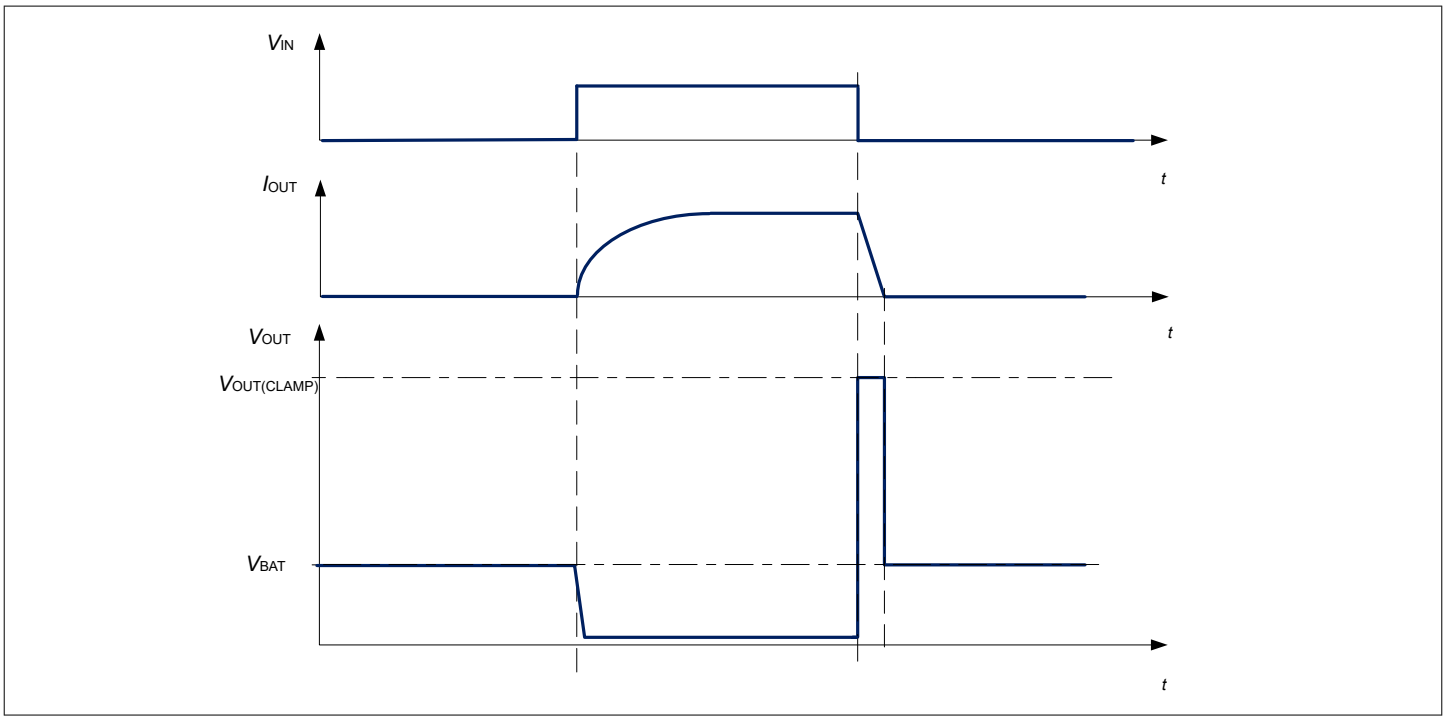

Figure 10 Switching an inductive load

When switching off inductive loads with low-side switches, the drain-source voltage V_{OUT} rises above the battery potential due to the inductance tendency to continue driving the current. To prevent unwanted high voltages the device has a voltage clamping mechanism to keep the voltage at $V_{OUT(CLAMP)}$. During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See Figure 9 and Figure 10 for more details.

Note: Repetitive switching of an inductive load by V_{DD} instead of using the input pin IN is a not recommended operation and may affect the device reliability and reduce the lifetime.

4.3.2 Maximum load inductance

During the demagnetization of inductive loads, energy has to be dissipated by the device.
This energy can be calculated by (1):

$$E = V_{OUT(CLAMP)} \times \left[\frac{V_{BAT} - V_{OUT(CLAMP)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_{BAT} - V_{OUT(CLAMP)}}\right) + I_L \right] \times \frac{L}{R_L} \quad (1)$$

The (2) is simplified under the assumption of $R_L = 0$:

$$E = \frac{1}{2} L I_L^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CLAMP)}}\right) \quad (2)$$

Figure 11 shows the inductance for a given current that the device BTT3050EJ can withstand.
For maximum single avalanche energy please refer to E_{AS} parameter in Table 3.

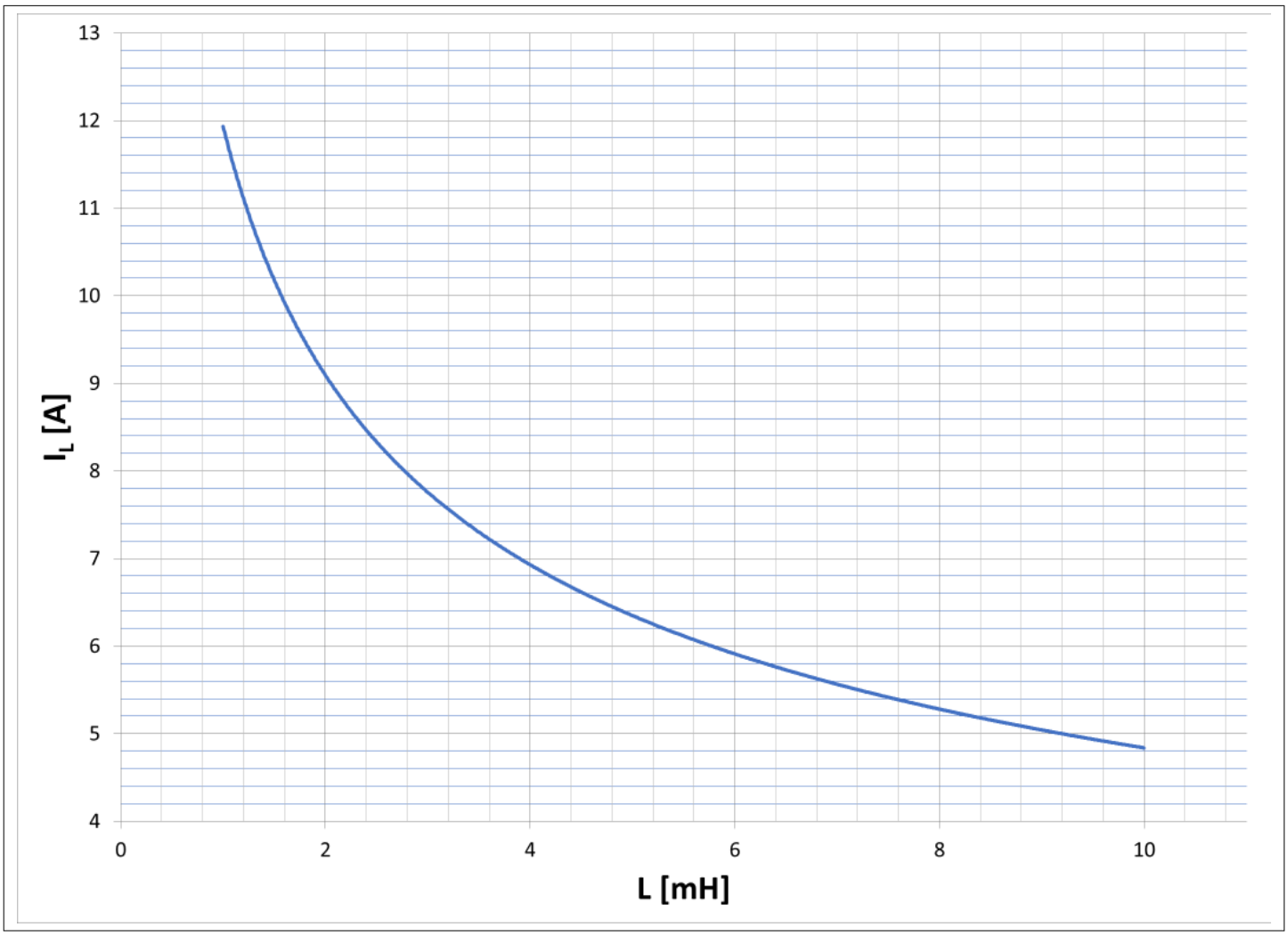

Figure 11 Maximum load inductance for single pulse: $L = f(I_L)$; $T_{J(0)} = 150°C$; $V_{BAT} = 28$ V

4.4 Reverse current capability

A reverse battery situation means that the device's drain is pulled below GND potential to $-V_{BAT}$. In this situation the load is driven by a current through the intrinsic body diode of BTT3050EJ and all protections, such as current limitation, overtemperature or overvoltage clamping, are not active.

In inverse or reverse operation via the reverse body diode, the device is dissipating a power loss which is defined by the driven current and the voltage drop on the body diode.

4.5 Characteristics

Please see Power stage for Electrical characteristics tables.

5 Diagnostics

BTT3050EJ provides a latching digital fault feedback signal on the STATUS pin triggered by an overtemperature shutdown.

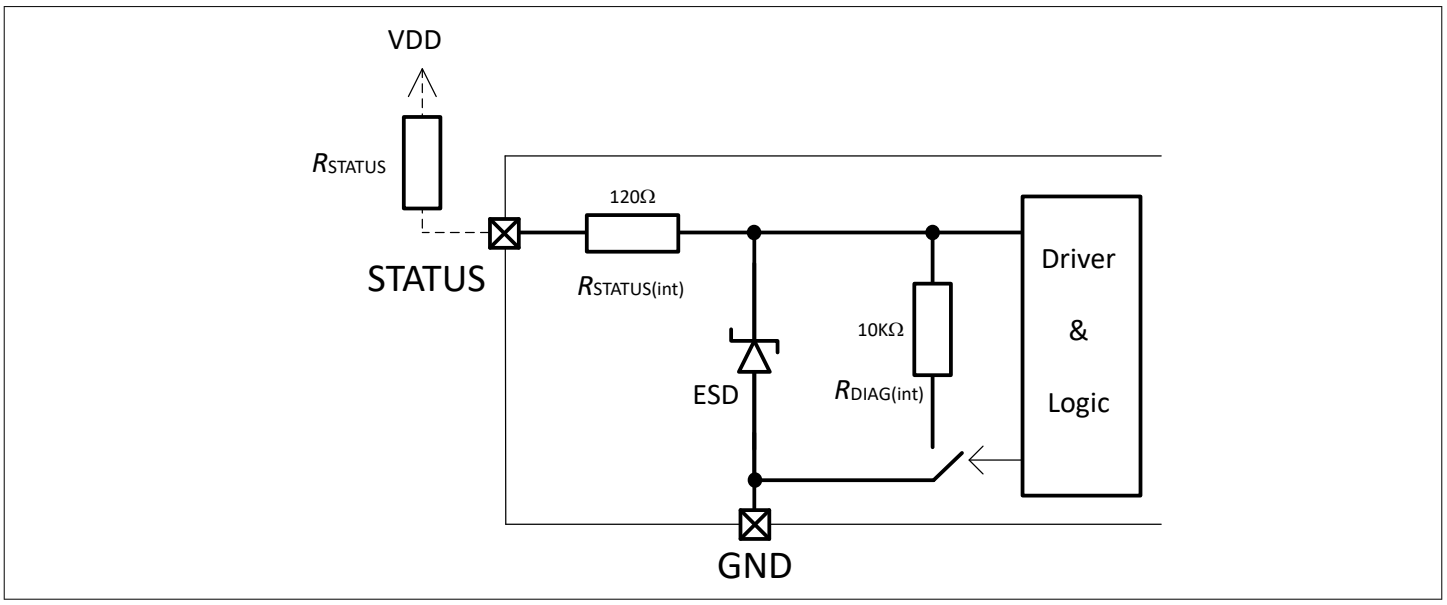

Figure 12 Simplified diagnosis circuit

Figure 12 shows the diagnosis circuit of BTT3050EJ. The circuit includes an ESD protection mechanism via a zener structure. Note that $R_{STATUS(int)} + R_{DIAG(int)} = R_{STATUS(LATCH)}$.

5.1 Functional description of the STATUS pin

BTT3050EJ provides digital status information via the STATUS pin to give feedback to a connected microcontroller.

The readout of the diagnosis signal is only possible if the STATUS pin has a dedicated connection to the microcontroller and the appropriate pull-up resistor R_{STATUS} is in place. See Figure 32 for recommended values of the external components.

The device is able to operate via STATUS pin and IN pin connected together, however, this condition will inhibit the readout of the diagnosis signal.

In normal operation (no thermal shutdown) the STATUS pin's logic is set "high". It is pulled up via an external resistor (R_{STATUS}) to V_{DD}.

Internally it is connected to an open drain MOSFET through an internal resistor.

In case of a thermal shutdown (fault) the internal MOSFET, connected to the STATUS pin, pulls its voltage down to GND providing a "low" level signal to the microcontroller $V_{STATUS(LATCH)}$.

Fault mode operation remains active independently from the INPUT pin state until it is reset.

To reset the latch fault signal of BTT3050EJ, the STATUS pin has to be externally pulled up. This behavior is shown in Figure 15. For other configurations and how to reset the latch OFF of the DMOS, please see Reset latch condition.

5.2 Characteristics

Please see Diagnostics for Electrical characteristics tables.

6 Supply and input stage

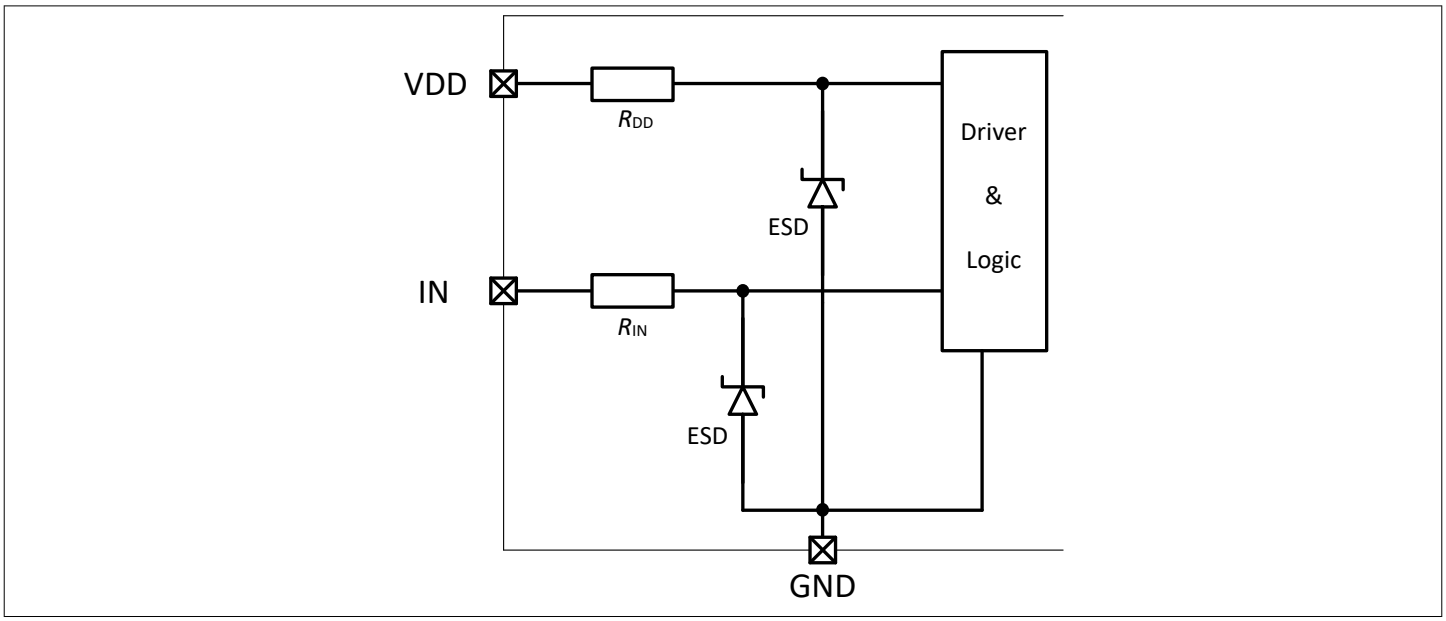

Figure 13 Simplified supply and input circuit

Figure 13 shows the supply and input circuit of BTT3050EJ. Both terminals include an ESD protection mechanism via a zener structure.

6.1 Supply circuit

The device's supply is not internally regulated but provided by an external supply. Therefore a reverse polarity protected and buffered (3.3 V..5.5 V) voltage supply is required at V_{DD} pin. To achieve the best $R_{DS(ON)}$ and the fastest switching speed a 5 V supply is required.

6.1.1 Undervoltage shutdown

In order to ensure a stable device behavior under all allowed conditions the supply voltage V_{DD} is monitored.

The output switches off if the supply voltage V_{DD} drops below the switch-off threshold $V_{DD(TH)L}$.

If the supply voltage V_{DD} drops below the supply voltage reset threshold $V_{DD(RESET)}$ a reset of the STATUS signal and the latch-off state will occur.

The device functions are only given for supply voltages above the supply voltage threshold $V_{DD(TH)H}$.

6.1.2 Supply current consumption

The supply current consumption is determined by the state of the input voltage, being low, with the $I_{DD(OFF)}$ and being high, with the $I_{DD(ON)}$.

After a thermal shutdown, when the device is in OFF latch mode, the current consumption values matches the normal ON state $I_{DD(ON)}$ as long as input is high.

However in PWM the consumption depends on the switching frequency. The higher the frequency, the higher the $I_{DD(PWM)}$.

Figure 14 shows the typical relation between the supply current consumption and the switching frequency considering a duty-cycle of 50%.

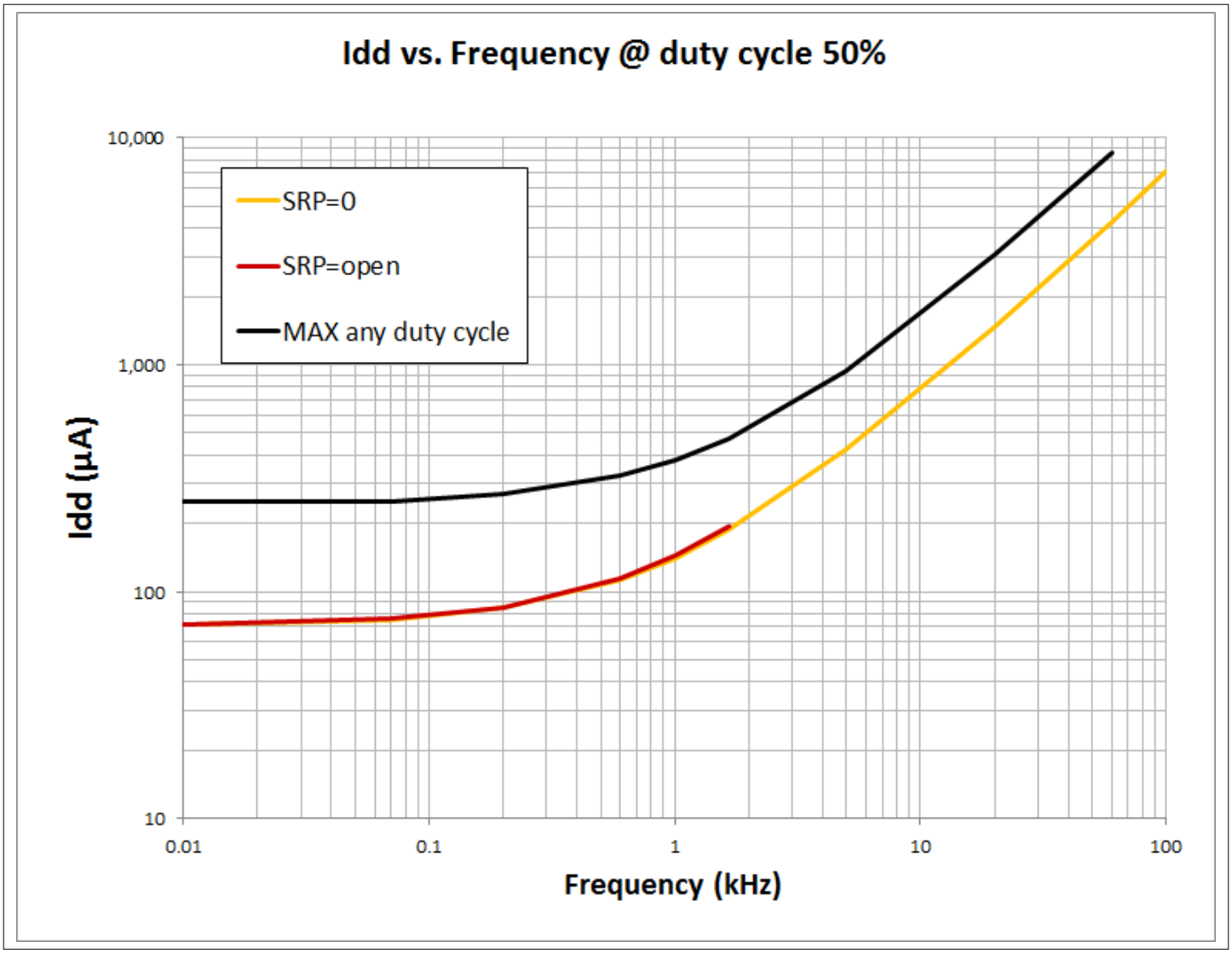

Figure 14 Typical $I_{DD(PWM)}$ versus switching frequency at 50% duty cycle

6.2 Characteristics

Please see Supply and input stage for Electrical characteristics tables.

7 Protection functions

BTT3050EJ provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operations. Protection functions are not to be used for continuous or repetitive operation. BTT3050EJ has implemented a latched overtemperature shutdown function.

In the event of overtemperature shutdown the device will remain OFF until the latch is reset via STATUS pin.

7.1 Overvoltage clamping on output

BTT3050EJ limits the drain-source voltage V_{DS} at a certain level $V_{OUT(CLAMP)}$.

The overvoltage clamping is overruling the other protection functions. Power dissipation has to be limited not to exceed the maximum allowed junction temperature.

This function is also used in terms of inductive clamping. Please see also Output clamping for more details.

7.2 Thermal protection

The device is protected against overtemperature due to overload and/or bad cooling conditions by an integrated temperature sensor.

The thermal protection is available when the device is active. In the event of overtemperature shutdown $T_{J(SD)}$, the device will remain OFF until the device is reset via STATUS pin.

Please see Figure 15 and Figure 16.

7.3 Overcurrent limitation and short circuit behavior

BTT3050EJ provides an overcurrent limitation intended to protect against short circuit or overcurrent conditions.

When the drain current reaches the current limitation level $I_{L(LIM)}$, the device will limit the current at that level.

While doing so, the power dissipation will heat up the device. Once the device reaches the overtemperature shutdown threshold $T_{J(SD)}$, it will automatically shutdown and remain OFF until it is reset via STATUS pin.

7.4 Reset latch condition

The reset of the latch OFF mode is done in two stages that need to be performed in the correct sequence.

During the first stage the voltage at the STATUS pin must be below the $V_{STATUS(RESET)L}$ threshold for a time $t > t_{STATUS(RESET)L}$.

In the second stage of the reset sequence, the STATUS pin voltage needs to be pulled-up above the $V_{STATUS(RESET)H}$ threshold for a time $t > t_{STATUS(RESET)H}$.

The total reset time needed is given by the sum of $t_{STATUS(RESET)L}$ and $t_{STATUS(RESET)H}$.

The following paragraphs explain more in detail the reset functionality in different conditions.

7.4.1 Reset via STATUS pin

If the temperature protection shutdowns the device, it will remain latched OFF independently of the input signal at IN pin. Simultaneously, the STATUS pin signal will be signalized low $V_{STATUS(LATCH)}$. In order to reset the latch condition, the STATUS pin needs to remain below $V_{STATUS(RESET)L}$ for a time $t > t_{STATUS(RESET)L}$ before being externally pulled-up to $V_{STATUS(RESET)H}$ for a time $t > t_{STATUS(RESET)H}$.

Please refer to Figure 15 and the application diagram in Figure 32.

This configuration allows the device to be driven with high frequency PWM signal via the IN pin without a risk of resetting the device in case it goes in protection shutdown mode (latch OFF).

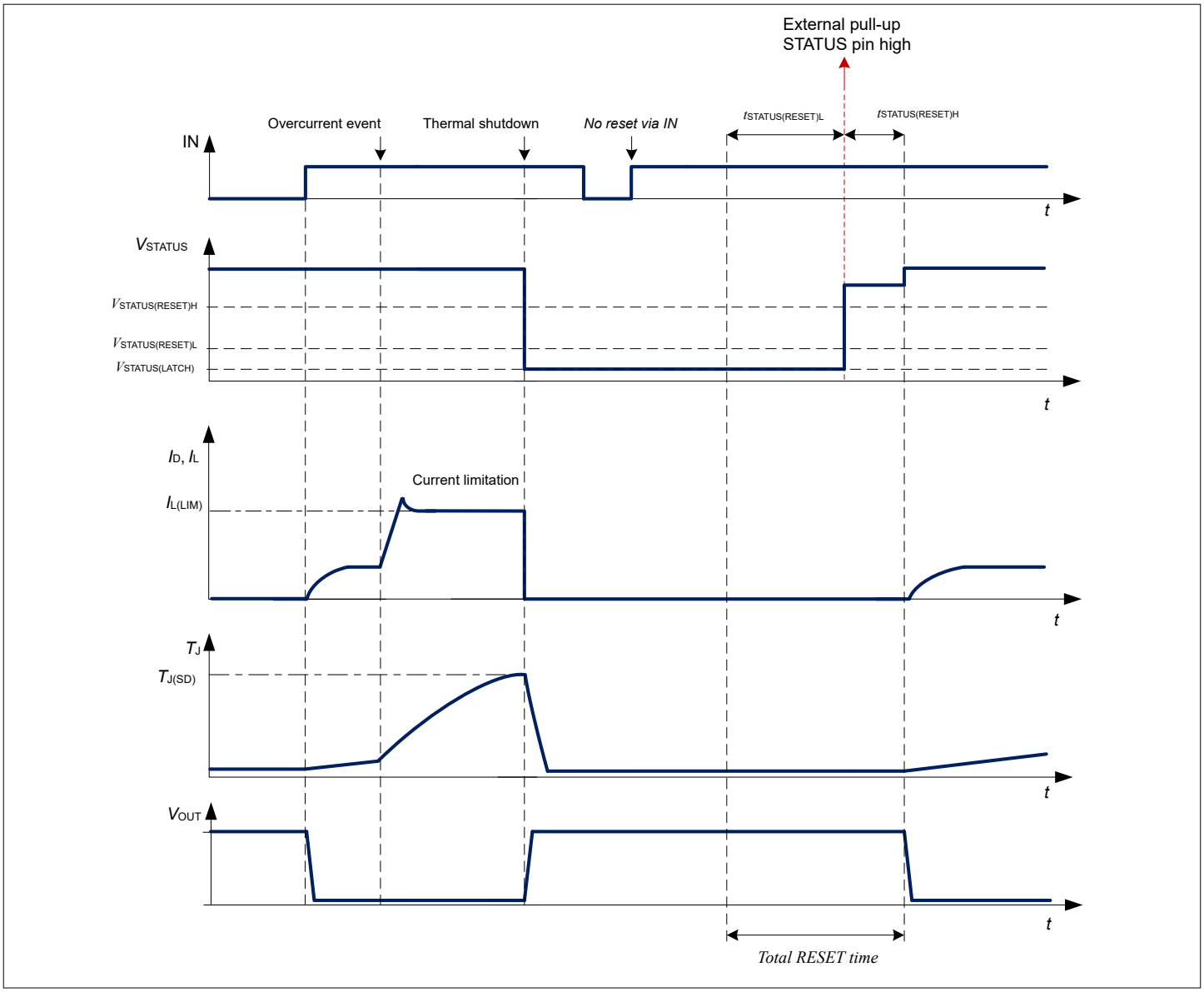

Figure 15 Mechanism to reset latch condition via STATUS pin

7.4.2 Reset via STATUS pin and IN pin connected together

If STATUS and IN pins are connected together (no R_{STATUS} pull-up external resistor), the voltage provided through the IN pin will prevent to signalize the STATUS low.

To reset the device under this condition, the STATUS – IN connection need to be pulled-down to $V_{STATUS(RESET)L}$ for a time $t > t_{STATUS(RESET)L}$ before being pulled-up to $V_{STATUS(RESET)H}$ for a time $t > t_{STATUS(RESET)H}$.

Please refer to Figure 16 and the application diagram in Figure 33.

If no diagnosis of the device is required, this configuration avoids the need of a dedicated I/O from the microcontroller for the STATUS pin. The maximum frequency allowed in PWM mode via IN pin preventing to reset the device is constrained by the $t_{STATUS(RESET)L}$ and $t_{STATUS(RESET)H}$ times.

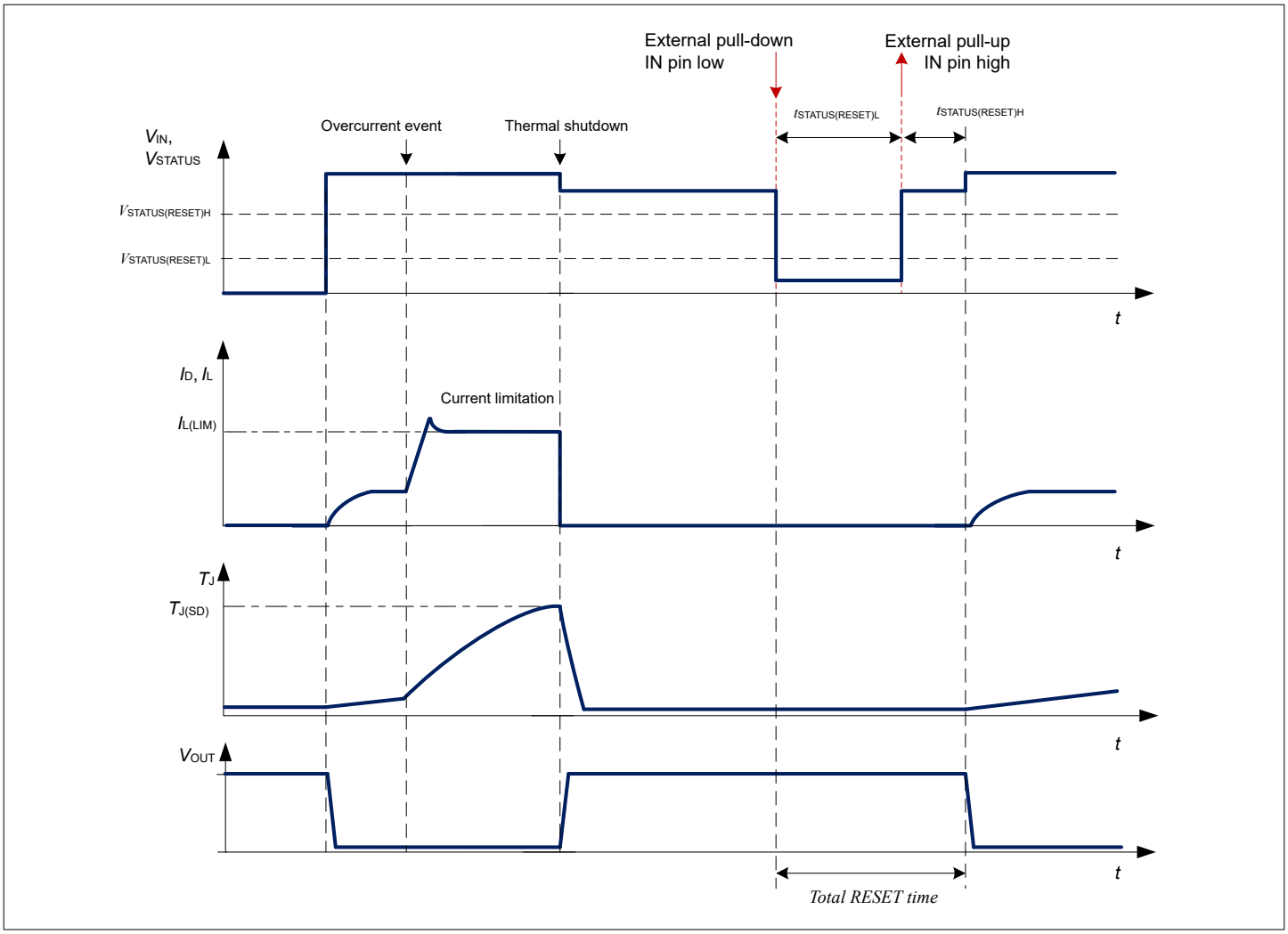

Figure 16 Mechanism to reset latch condition with STATUS pin and IN pin connected together

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependent and cannot be described.

7.5 Characteristics

Please see Protection for Electrical characteristic tables.

8 Electrical characteristics

Please note that Electrical characteristics shows the deviation of a parameter at a given input voltage and junction temperature. Typical values show the typical parameters expected from manufacturing and in typical application condition. All voltages and currents naming and polarity in accordance to Figure 3.

8.1 Power stage

Please see Power stage for parameters description and further details.

Table 6 Power stage

T_J = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Static characteristics							
On-state resistance at 5 V supply and 25°C	$R_{DS(ON)\_5\_25}$	–	50	63	mΩ	$I_L = I_{L(NOM)}$; V_{DD} = 5 V; T_J = 25°C	PRQ-168
On-state resistance at 5 V supply and 150°C	$R_{DS(ON)\_5\_150}$	–	85	100	mΩ	$I_L = I_{L(NOM)}$; V_{DD} = 5 V; T_J = 150°C	PRQ-169
On-state resistance at 3 V supply and 25°C	$R_{DS(ON)\_3\_25}$	–	63	78	mΩ	$I_L = I_{L(NOM)}$; V_{DD} = 3 V; T_J = 25°C	PRQ-172
On-state resistance at 3 V supply and 150°C	$R_{DS(ON)\_3\_150}$	–	105	130	mΩ	$I_L = I_{L(NOM)}$; V_{DD} = 3 V; T_J = 150°C	PRQ-173
Nominal load current	$I_{L(NOM)}$	–	4.0	–	A	[1] T_J < 150°C; T_A = 85°C; V_{DD} = 5 V	PRQ-174
OFF state load current, output leakage current	$I_{L(OFF)\_85}$	–	0	1	µA	[2] $T_J \leq$ 85°C	PRQ-175
OFF state load current, Output leakage current at 150°C	$I_{L(OFF)\_150}$	–	2	10	µA	T_J = 150°C	PRQ-176
Reverse diode							
Reverse diode forward voltage	$-V_{DS}$	–	0.6	1	V	V_{IN} = 0 V	PRQ-177
Switching times. RSRP = short to GND; VBAT = 28 V; VDD = 5 V; R_{Load} = 10 Ω.							
Turn-on delay time	$t_{DON\_5(0)}$	1.2	2.7	6.8	µs	–	PRQ-178
Turn-off delay time	$t_{DOFF\_5(0)}$	1.0	2.8	5.5	µs	–	PRQ-179
Turn-on output fall time	$t_{F\_5(0)}$	0.5	1.4	2.5	µs	–	PRQ-180
Turn-off output rise time	$t_{R\_5(0)}$	0.3	0.8	2.0	µs	–	PRQ-181

(table continues...)

Table 6 (continued) Power stage

T_J = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching times. RSRP = 5.8 KΩ; VBAT = 28 V; VDD = 5 V; R_{Load} = 10 Ω.							
Turn-on delay time	$t_{DON\_5(5K8)}$	1.7	3.1	6.9	µs	–	PRQ-182
Turn-off delay time	$t_{DOFF\_5(5K8)}$	1.4	4.5	7.6	µs	–	PRQ-183
Turn-on output fall time	$t_{F\_5(5K8)}$	1.1	2.1	3.6	µs	–	PRQ-184
Turn-off output rise time	$t_{R\_5(5K8)}$	1.0	1.7	2.9	µs	–	PRQ-328
Switching times. RSRP = 58 KΩ; VBAT = 28 V; VDD = 5 V; R_{Load} = 10 Ω.							
Turn-on delay time	$t_{DON\_5(58K)}$	5.5	10.5	15.3	µs		PRQ-329
Turn-off delay time	$t_{DOFF\_5(58K)}$	6.6	20.4	40.9	µs		PRQ-330
Turn-on output fall time	$t_{F\_5(58K)}$	5.7	11.3	18.6	µs		PRQ-331
Turn-off output rise time	$t_{R\_5(58K)}$	6.9	12.8	19.3	µs		PRQ-332
Switching times. RSRP = 1 MΩ; VBAT = 28 V; VDD = 5 V; R_{Load} = 10 Ω.							
Turn-on delay time	$t_{DON\_5(1M)}$	9.3	17.0	42.2	µs	–	PRQ-337
Turn-off delay time	$t_{DOFF\_5(1M)}$	10.4	44.2	139	µs	–	PRQ-338
Turn-on output fall time	$t_{F\_5(1M)}$	8.9	26.7	64.7	µs	–	PRQ-339
Turn-off output rise time	$t_{R\_5(1M)}$	8.9	27.1	68.2	µs	–	PRQ-340

1) Not subject to production test, calculated by R_{thJA} and $R_{DS(ON)}$
2) Not subject to production test, specified by design

8.2 Protection

Please see Protection functions for parameter description and further details.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Table 7 Protection

T_J = -40°C to +150°C, V_{BAT} = 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal shutdown							
Thermal shutdown junction temperature	$T_{J(SD)}$	150	175	200	°C	1) V_{DD} = 5 V	PRQ-185
Overtemperature shutdown STATUS delay at 5 V	$t_{TJ(SD)5}$	–	4.5	–	µs	1) Delay time to trigger STATUS signal; V_{DD} = 5 V; T_{AMB} = 25°C	PRQ-189
Overtemperature shutdown STATUS delay at 3 V	$t_{TJ(SD)3}$	–	4.2	–	µs	1) Delay time to trigger STATUS signal; V_{DD} = 3 V; T_{AMB} = 25°C	PRQ-191
Overvoltage protection/clamping							
Drain clamp voltage	$V_{OUT(CLAMP)}$	63	72	83	V	V_{IN} = 0 V; I_D > 50 mA	PRQ-193
Current limitation							
Current limitation level	$I_{L(LIM)\_5}$	10	16	22	A	2) V_{DD} = 5 V	PRQ-196

1) Not subject to production test, specified by design
2) Parameter tested at V_{BAT} = 5 V; specified up to V_{BAT} = 36 V

8.3 Supply and input stage

Please see Supply and input stage for description and further details.

Table 8 Supply and input stage

T_J = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply							
Supply on threshold voltage high	$V_{DD(TH)H}$	2.4	2.8	3	V	–	PRQ-202
Supply off threshold voltage low	$V_{DD(TH)L}$	2.3	2.7	2.9	V	1) DMOS switches OFF below threshold	PRQ-203

(table continues...)

Table 8 (continued) Supply and input stage

T_J = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply current, continuous ON operation	$I_{DD(ON)}$	–	150	250	µA	ON-state; V_{DD} = 5.5 V; V_{IN} = 5 V; $I_{L(0)} = I_{L(NOM)}$	PRQ-206
Standby supply current	$I_{DD(OFF)}$	–	0.3	3	µA	2) V_{IN} = 0 V; V_{DD} = 5.5 V	PRQ-212
Input							
Input on threshold voltage; 5.5 V supply	$V_{IN(TH)H\_5.5}$	1.9	2.4	2.8	V	V_{DD} = 5.5 V	PRQ-213
Input off threshold voltage; 5.5 V supply	$V_{IN(TH)L\_5.5}$	1.2	1.5	1.8	V	V_{DD} = 5.5 V	PRQ-214
Input on threshold voltage; 3 V supply	$V_{IN(TH)H\_3}$	1.2	1.5	1.8	V	V_{DD} = 3 V	PRQ-219
Input off threshold voltage; 3 V supply	$V_{IN(TH)L\_3}$	0.7	1	1.2	V	V_{DD} = 3 V	PRQ-220
Input pull down current	I_{IN}	20	45	80	µA	$V_{IN} \leq$ 5.5 V; $V_{DD} \leq$ 5.5 V	PRQ-222

1) Undervoltage shutdown protection doesn't reset the OFF latch mode
2) Not subject to production test, specified by design

8.4 Diagnostics

Please see Diagnostics for parameters description and further details.

Table 9 Diagnostics

T_J = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Diagnostics							
Status pin latch voltage	$V_{STATUS(LATCH)}$	–	–	1	V	6) 1) V_{DD} = 5 V; R_{STATUS} = 100 kOhm; 3 V ≤ V_{IN} ≤ 5 V; latched fault signal	PRQ-227
Status pin reset threshold low	$V_{STATUS(RESET)L\_5}$	1	1.4	1.7	V	2) V_{DD} = 5 V	PRQ-228
Status pin reset threshold high	$V_{STATUS(RESET)H\_5}$	1.7	2.2	2.6	V	3) V_{DD}= 5 V	PRQ-229
Status reset low time	$t_{STATUS(RESET)L\_5}$	1	1.6	2.4	ms	6) 4) V_{DD} = 5 V	PRQ-230
Status reset high time	$t_{STATUS(RESET)H\_5}$	20	35	70	µs	6) 5) V_{DD} = 5 V	PRQ-231

(table continues...)

Table 9 (continued) Diagnostics

T_J = -40°C to +150°C, V_{BAT} = 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Status pin reset threshold low	$V_{STATUS(RESET)L\_3}$	0.7	1	1.2	V	2) V_{DD} = 3 V	PRQ-232
Status pin reset threshold high	$V_{STATUS(RESET)H\_3}$	1.2	1.6	1.9	V	3) V_{DD} = 3 V	PRQ-233
Status reset low time	$t_{STATUS(RESET)L\_3}$	0.5	1	2.3	ms	6) 4) V_{DD} = 3 V	PRQ-234
Status reset high time	$t_{STATUS(RESET)H\_3}$	8	15	50	µs	6) 5) V_{DD} = 3 V	PRQ-235
Status pin leakage current (no latch)	$I_{STATUS(NOLATCH)}$	–	–	1	µA	6) 3 V ≤ V_{DD} ≤ 5.5 V; V_{STATUS} ≤ 5.5 V; 0 V ≤ V_{IN} ≤ 5.5 V	PRQ-236
Status pin internal resistance (latch active)	$R_{STATUS(LATCH)}$	7	10	15	KΩ	$R_{STATUS(LATCH)}$ = $R_{STATUS(int)}$ + $R_{DIAG(int)}$	PRQ-237

1) Latch feedback signal voltage drop considering V_{DD} = 5 V and R_{STATUS} = 100 kΩ.
2) Voltage threshold needed at the STATUS pin to initialize the reset sequence of the latch OFF mode. If STATUS pin and IN pin are connected together, same voltage threshold applies.
3) Voltage threshold needed at the STATUS pin to complete the reset sequence of the latch OFF mode. If STATUS pin and IN pin are connected together, same voltage range applies.
4) Time needed to remain below $V_{STATUS(RESET)L}$ to initialize the reset sequence of the latch OFF mode. See Chapter 6.4 for more information.
5) Time needed to remain above $V_{STATUS(RESET)H}$ after $V_{STATUS(RESET)L}$ is applied to conlude the reset sequence. See Chapter 6.4 for more information.
6) Not subject to production test, specified by design.

9 Characterization results

Typical performance characteristics.

9.1 Power stage

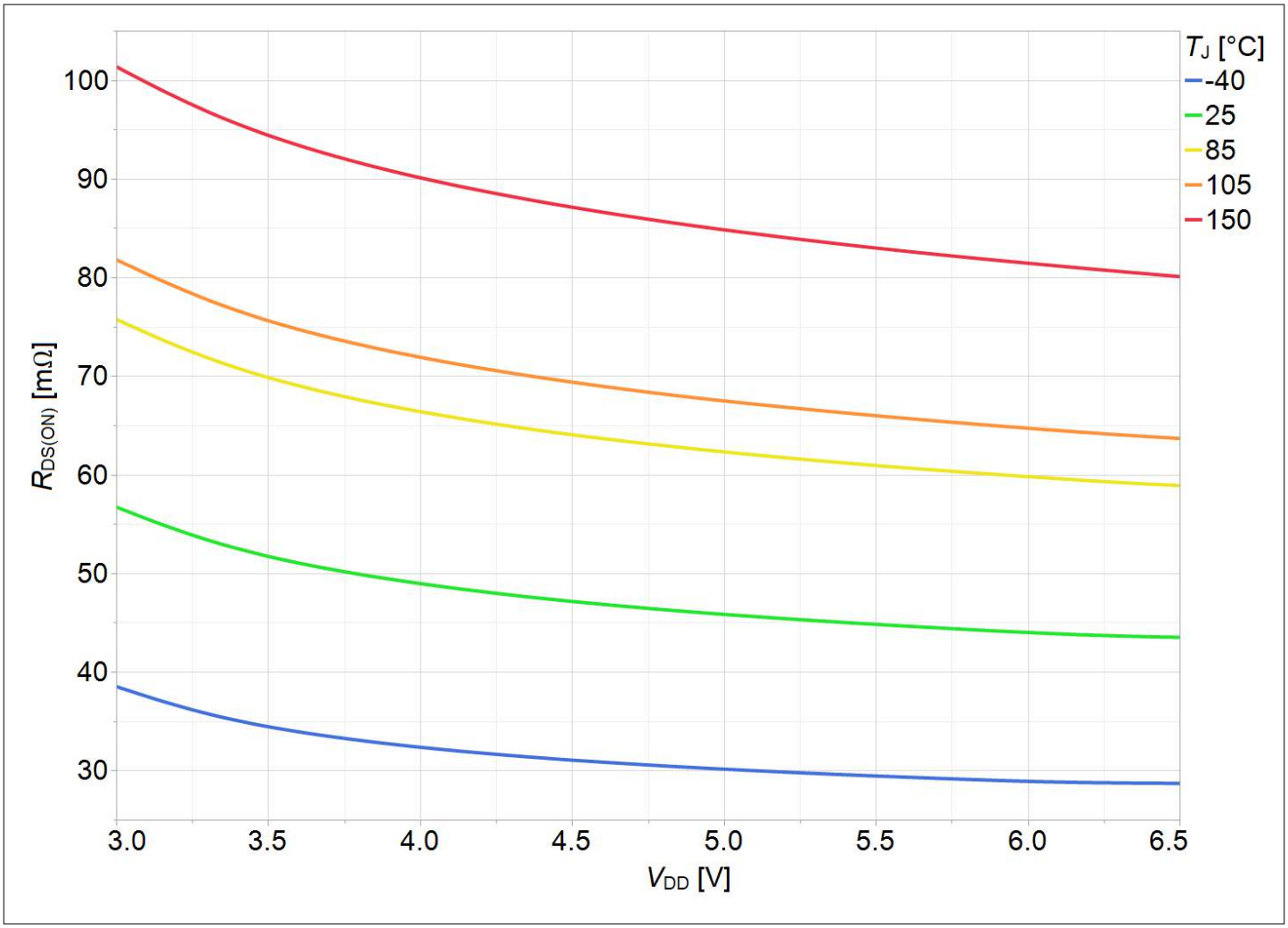

Figure 17 **Typical $R_{DS(ON)}$ vs. V_{DD}; $I_L = I_{L(NOM)}$; V_{IN} = 3 V; V_{DD} = 3.. 5.5 V; V_{BAT} = 28 V; R_{SRP} = 0 Ω**

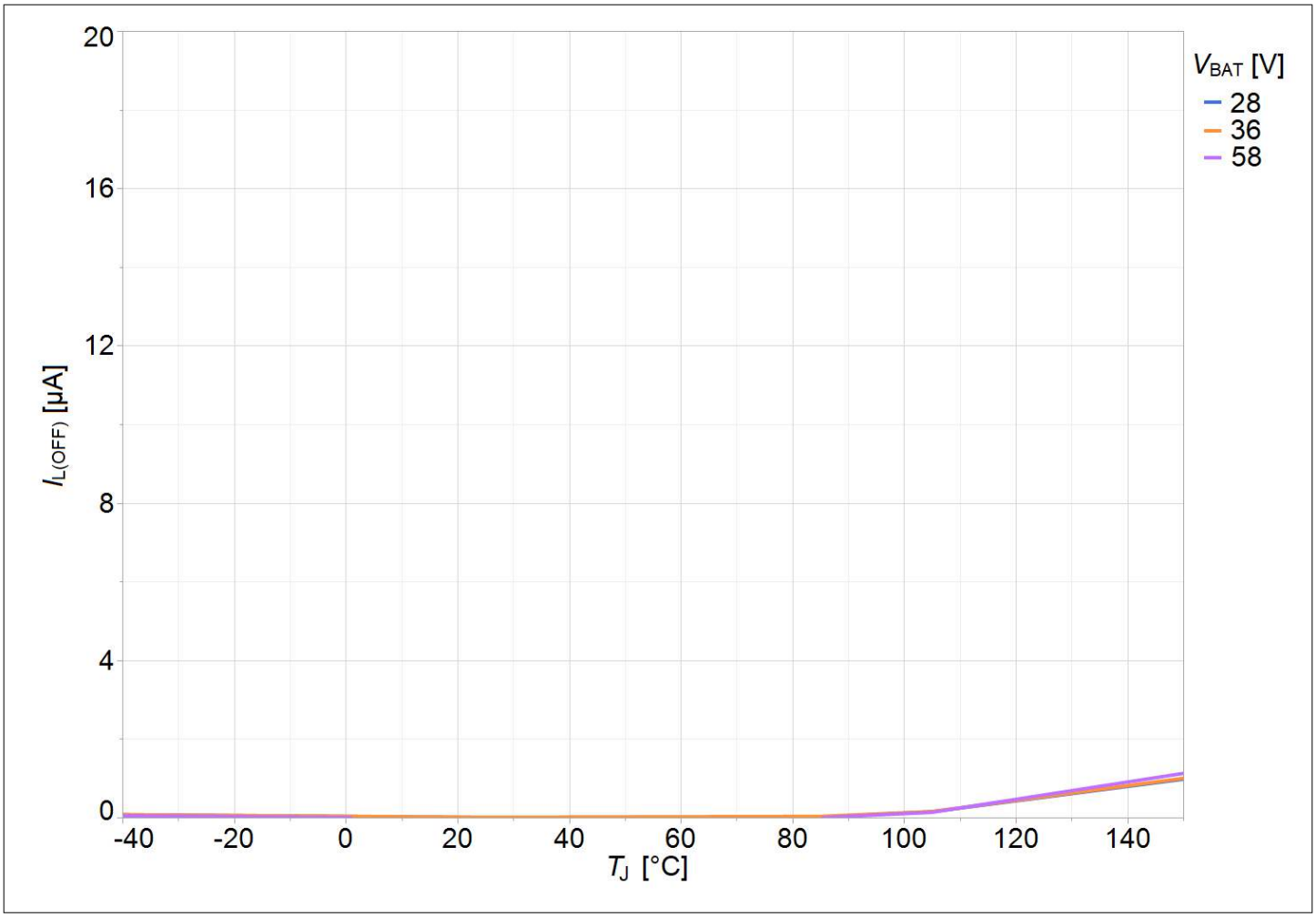

Figure 18 **Typical $I_{L(OFF)}$ vs. T_J at V_{IN} = 0 V; V_{DD} = 0 V, 5 V; V_{BAT} = 28, 36, 58 V; T_J = -40, 25, 85, 105, 150°C**

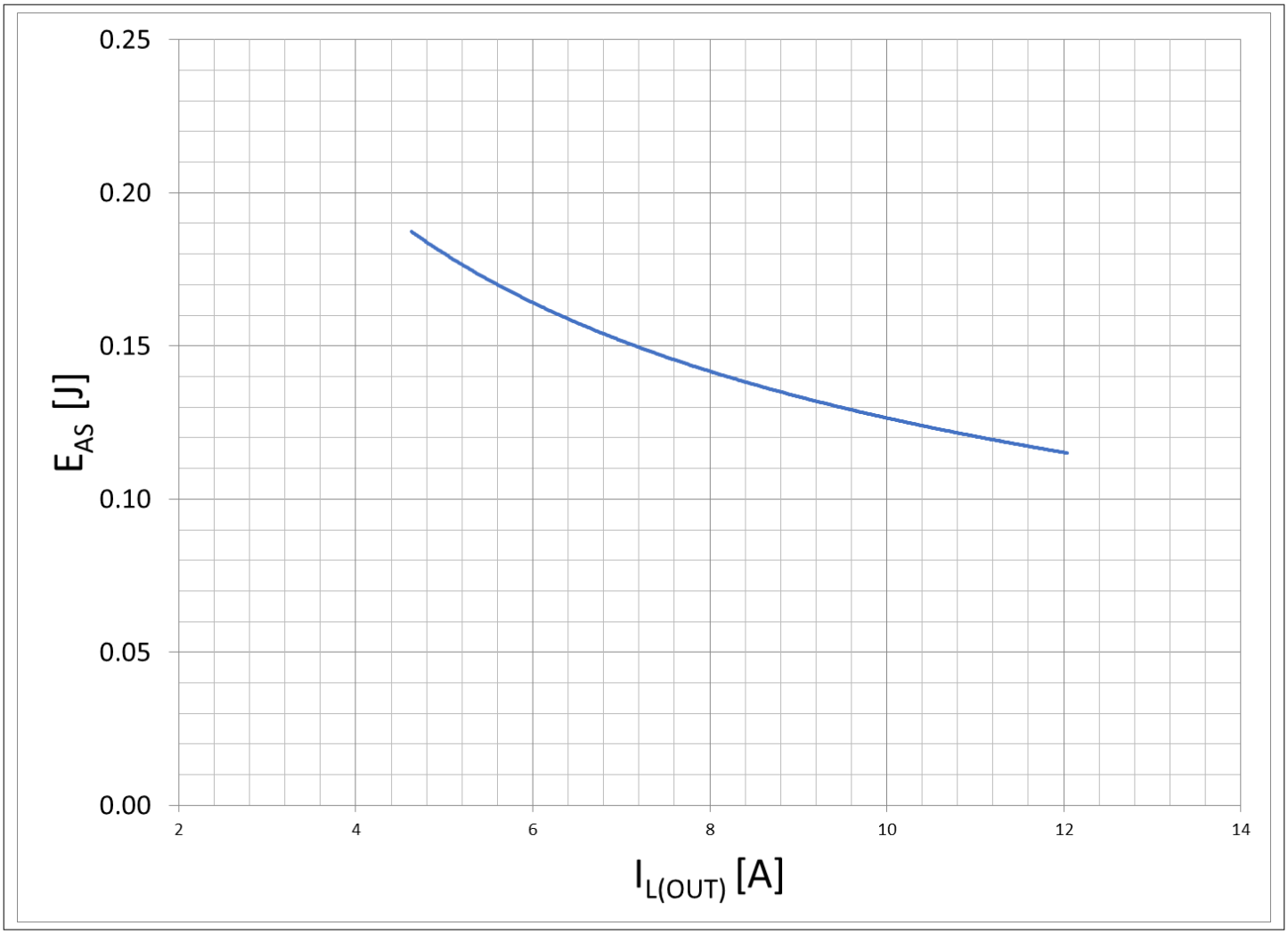

Figure 19 **Typical destruction point E_{AS} versus I_L at $T_{J(0)}$ = 150°C, V_{BAT} = 28 V; $I_{L(NOM)}$, 2 x $I_{L(NOM)}$**

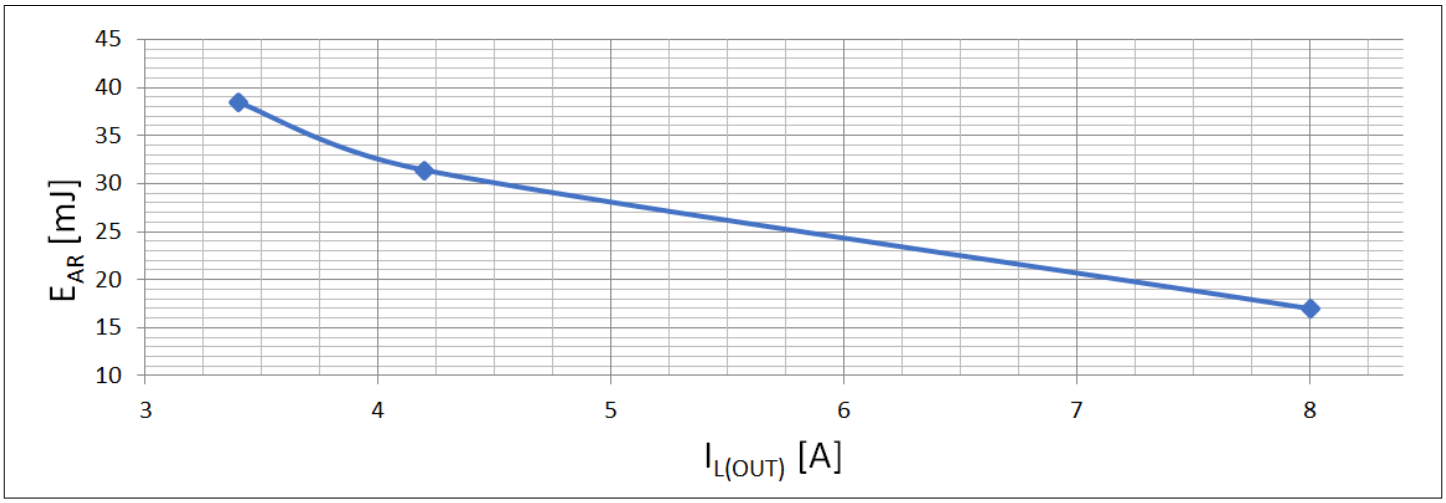

Figure 20 **Typical E_{AR} versus I_L at $T_{J(0)}$ = 25, 105°C, V_{BAT} = 28 V; Nr. cycles = 20 Mio cycles; I_L = $I_{L(NOM)}$, 2 x $I_{L(NOM)}$**

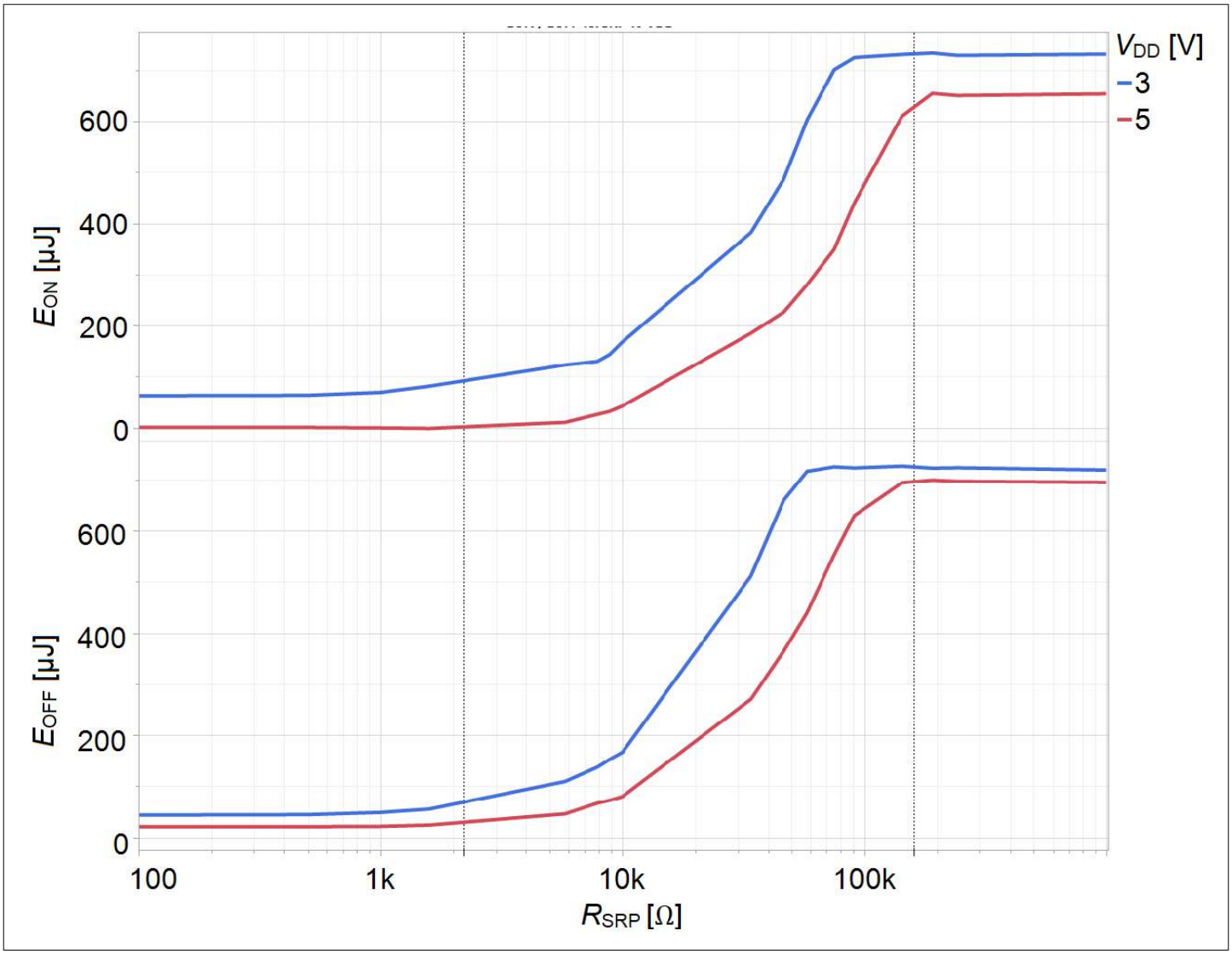

Figure 21 **Typical E_{ON} and E_{OFF} vs. R_{SRP} at T_A = 25°C, V_{DD} = 3 V and 5.5 V; V_{BAT} = 28 V; IN = 5 V; STATUS = pulled-up to VDD; R_{LOAD} = 6.8Ω**

Dynamic characteristics

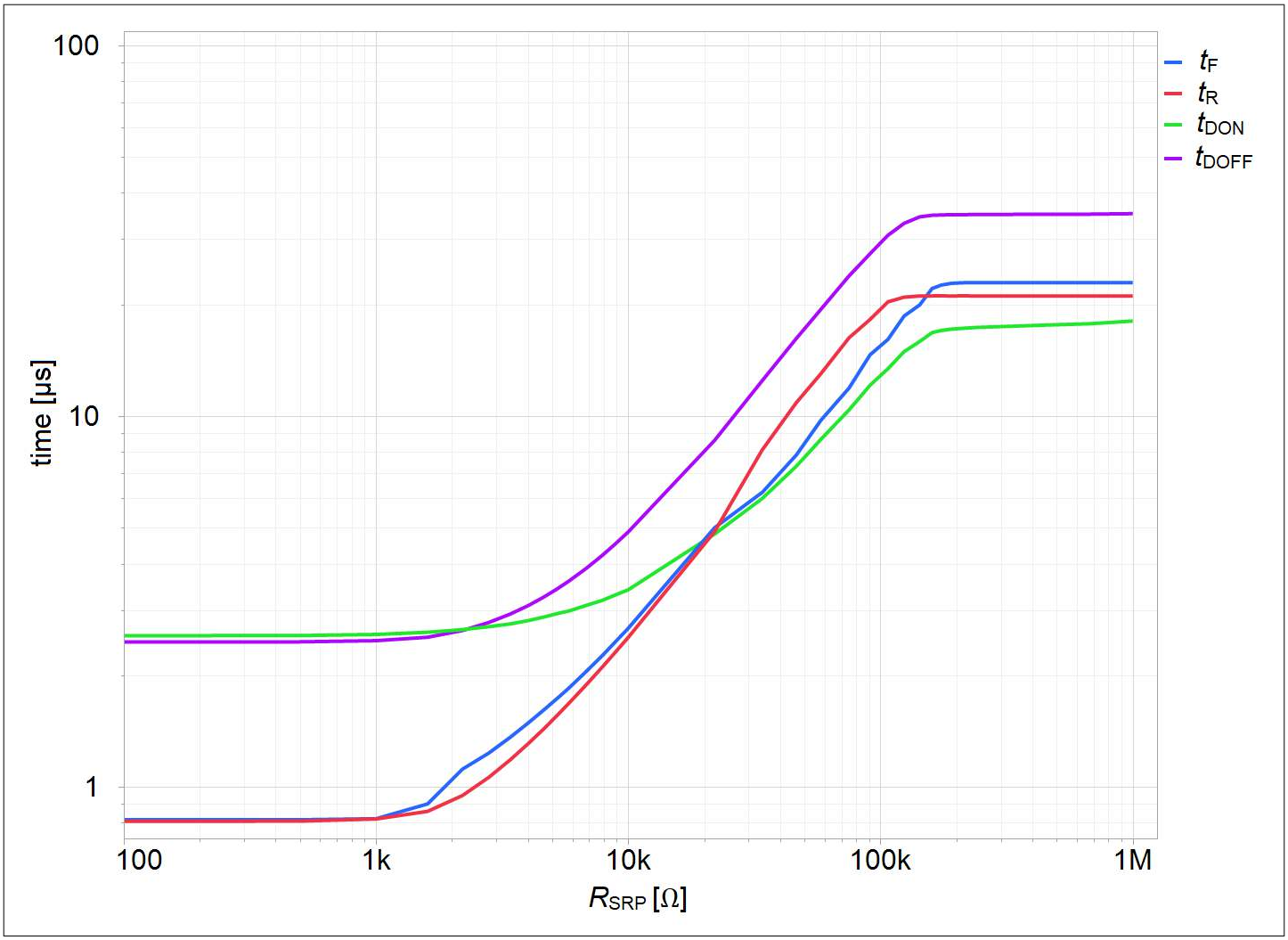

Figure 22 **Typical t_F, t_R, t_{DON}, t_{DOFF} versus R_{SRP} at V_{IN} = 5 V; V_{DD} = 5 V; V_{BAT} = 28 V; R_L= 6.8 Ω, 10 Ω; R_{SRP} = (0 kΩ, 2.2 kΩ,5.8 kΩ, 10 kΩ,58 kΩ, 160 kΩ, open); T_J = -40 .. 150°C**

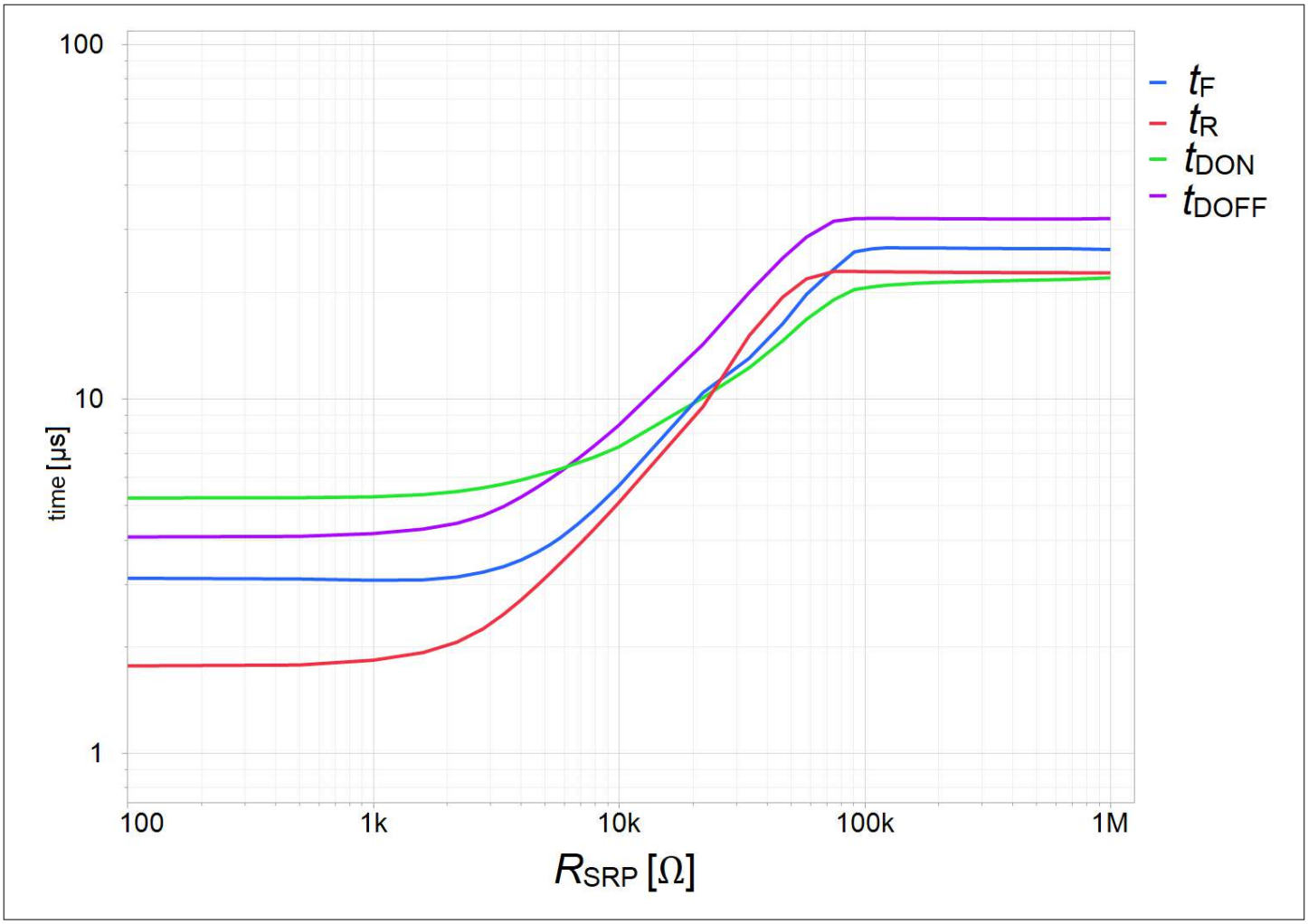

Figure 23 **Typical t_F, t_R, t_{DON}, t_{DOFF} versus R_{SRP} at V_{IN} = 3 V; V_{DD} = 3 V; V_{BAT} = 28 V; R_L = 6.8 Ω, 10 Ω; R_{SRP} = (0 kΩ, 2.2 kΩ, 5.8 kΩ, 10 kΩ,58 kΩ, 160 kΩ, open); T_J = -40 .. 150°C**

9.2 Protection

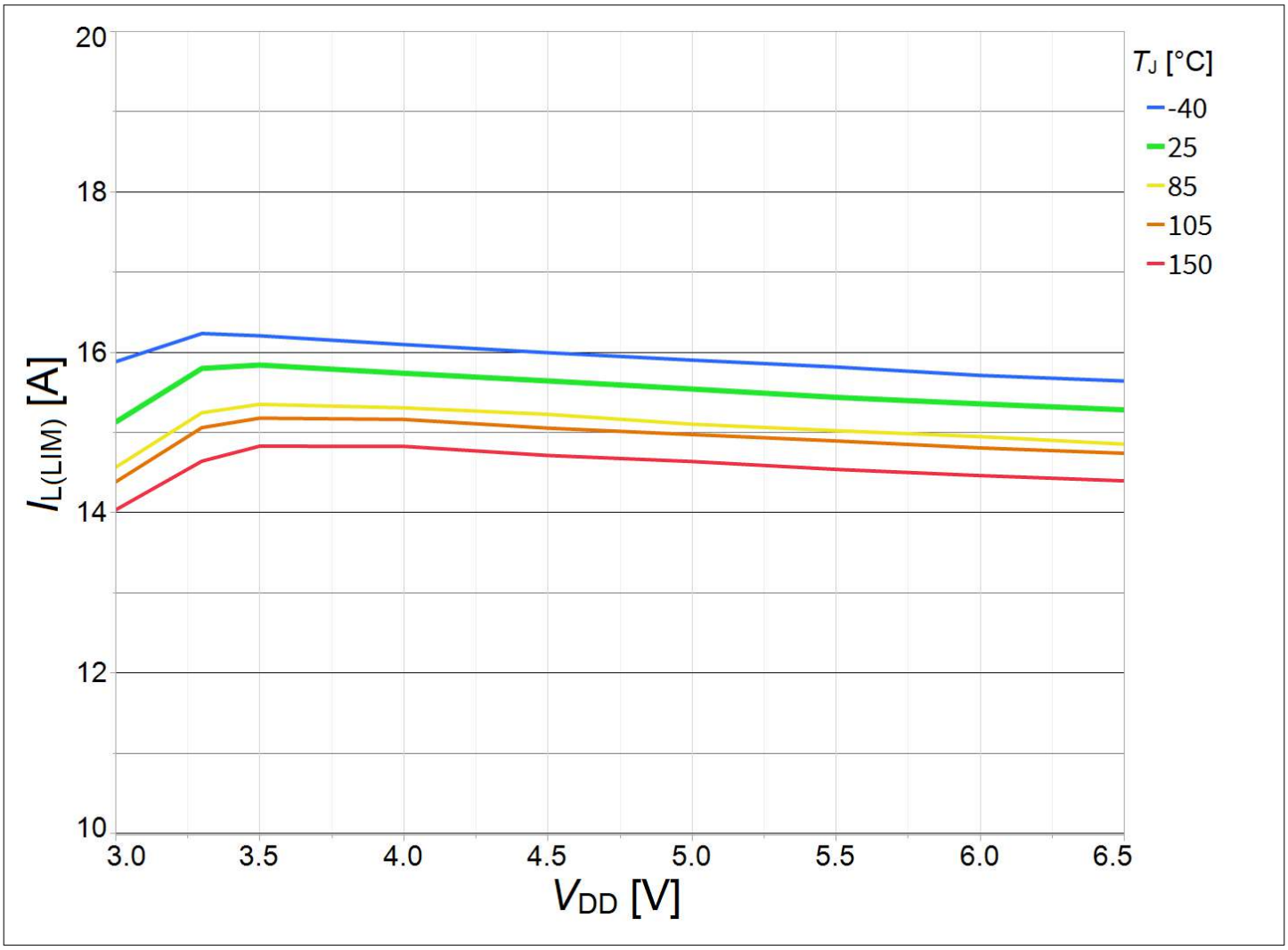

Figure 24 **Typical $I_{L(LIM)}$ versus V_{DD} = 3, 6.5 V; V_{IN} = 5 V; V_{BAT} = 0 .. 63 V; T_J = -40, 25, 85, 105, 150°C**

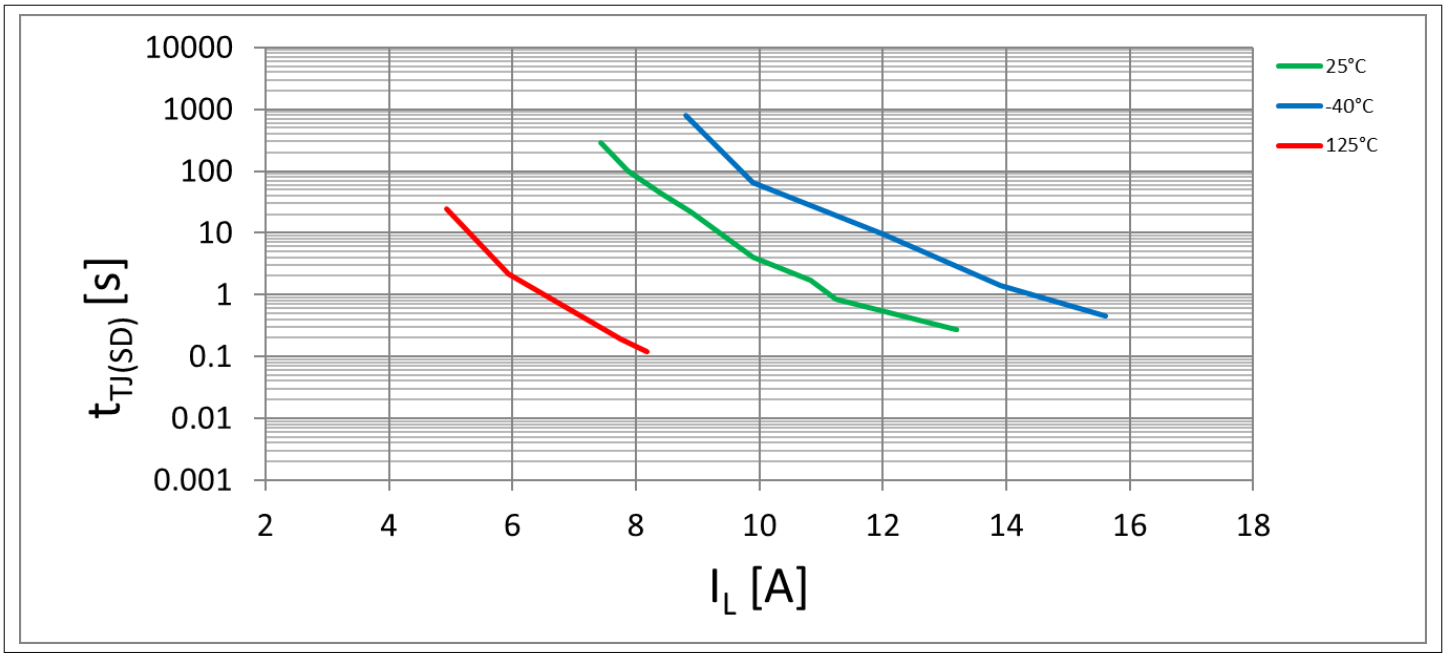

Figure 25 **Typical *time to shut down* $t_{TJ(SD)}$ versus I_L; V_{BAT}= 28 V; V_{DD} = 3.3, 5 V; V_{IN} = 5 V; RthJA(2s2p)**

9.3 Supply and input stage

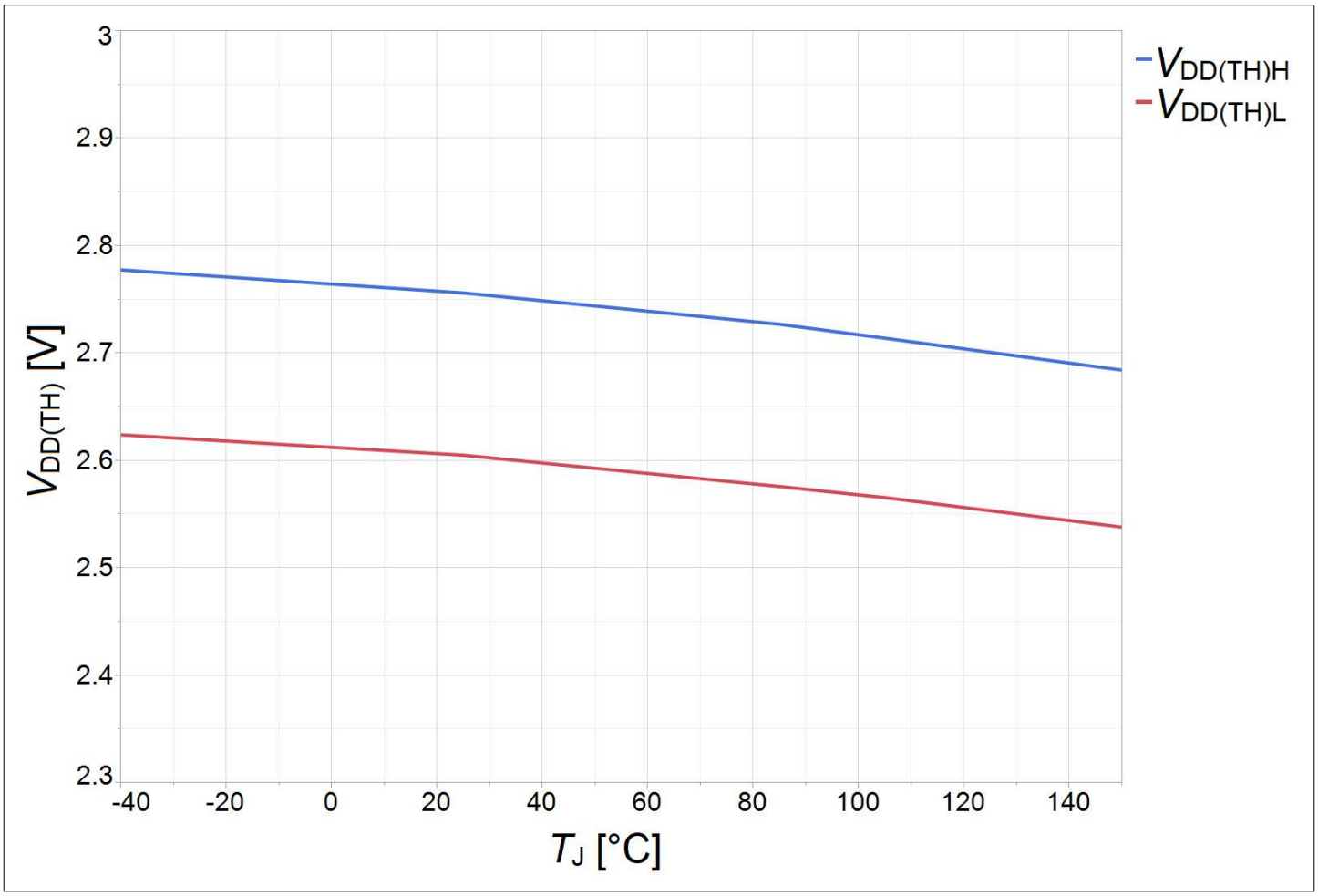

Figure 26 **Typical $V_{DD(TH)}$ versus T_J at T_J = -40 .. 150°C; $V_{DD(TH)H}$ and $V_{DD(TH)L}$; V_{IN} = 3 V; R_{LOAD} = 150 kΩ; R_{SRP} = *GND*; V_{BAT} = 28 V**

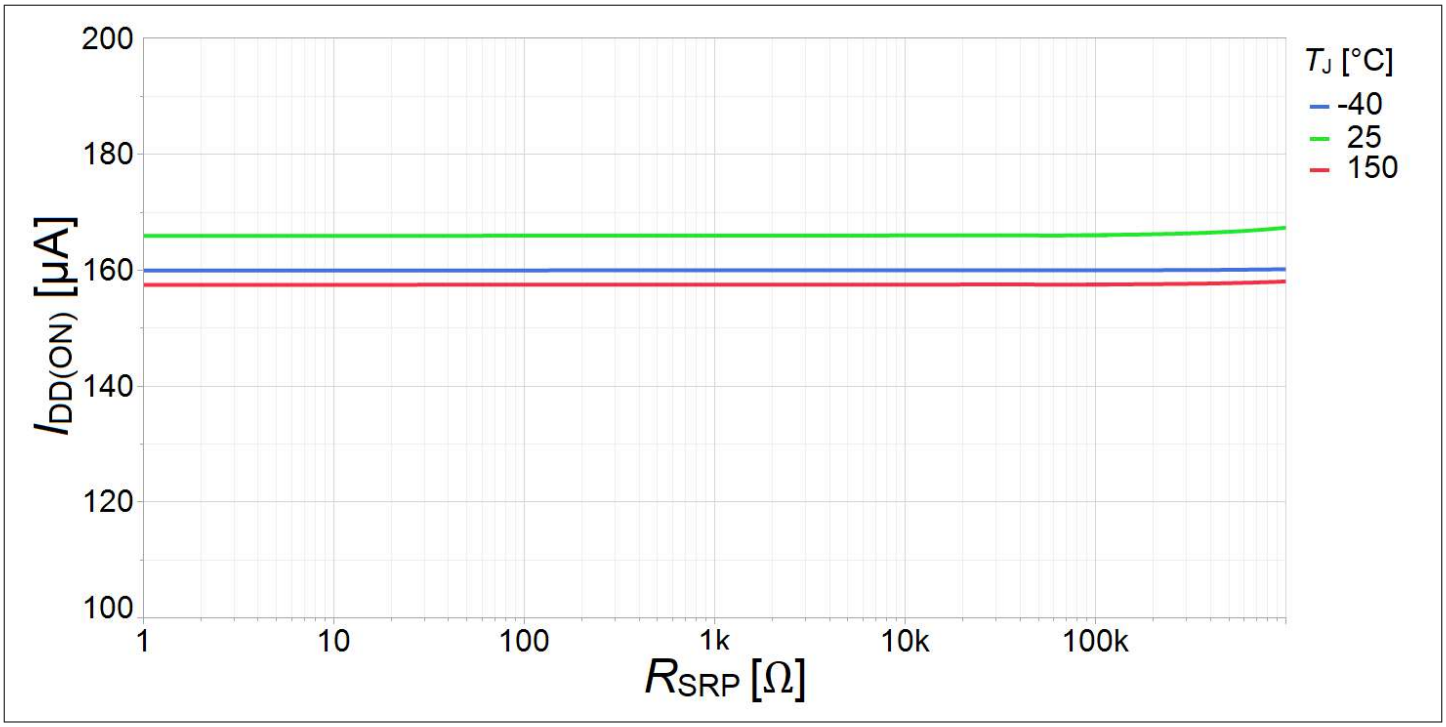

Figure 27 **Typical $I_{DD(ON)}$ versus R_{SRP} at T_J = -40 .. 150°C, I_L = $I_{L(NOM)}$; V_{IN} = 3 V; V_{DD} = 5 V; V_{BAT} = 28 V; R_{SRP} = *GND***

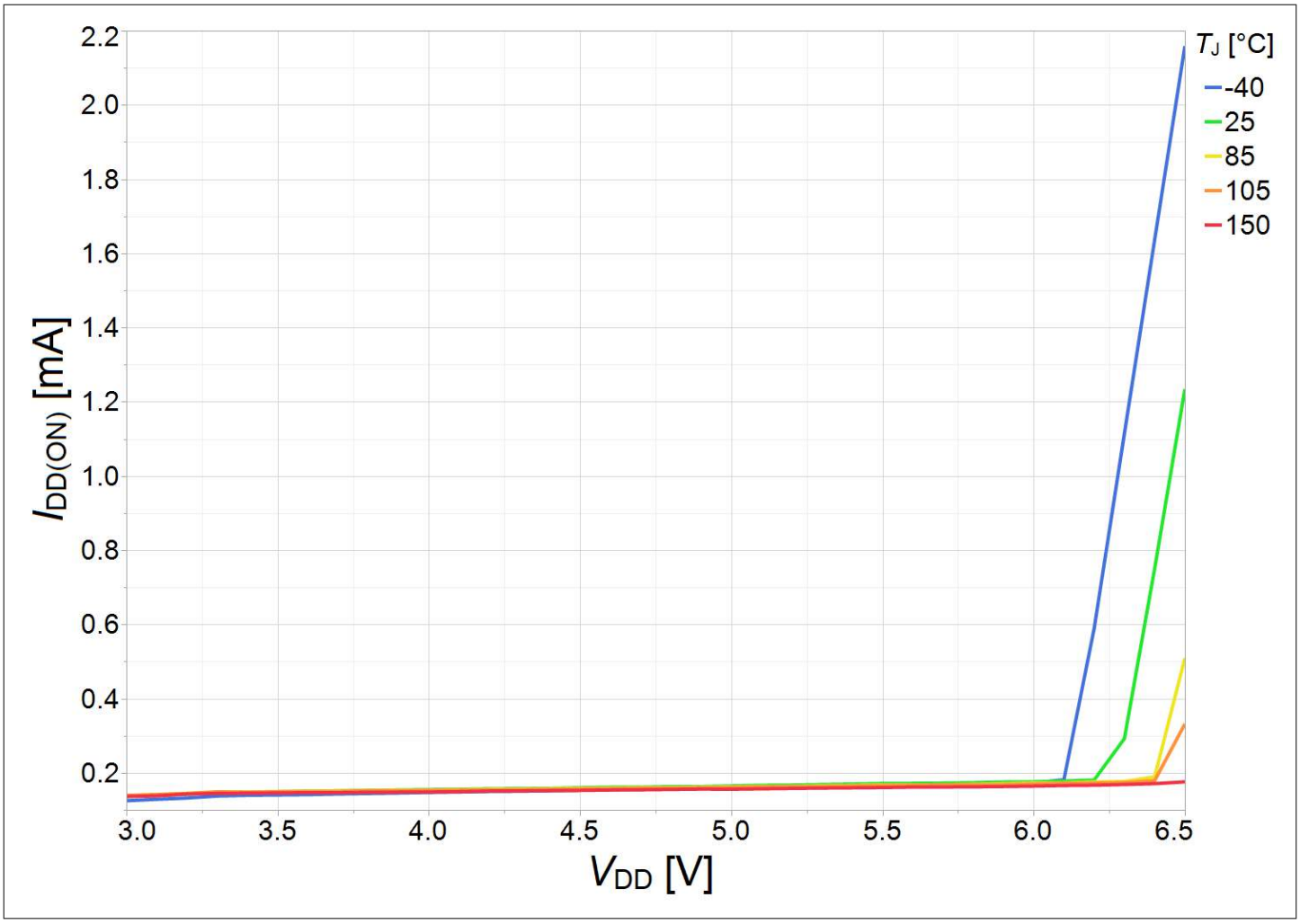

Figure 28 **Typical $I_{DD(ON)}$ versus V_{DD} at V_{DD} = 3 .. 6.5 V; T_J = -40 .. 150°C; I_L = $I_{L(NOM)}$; V_{IN} = 3 V; V_{BAT} = 28 V; R_{SRP} = *GND***

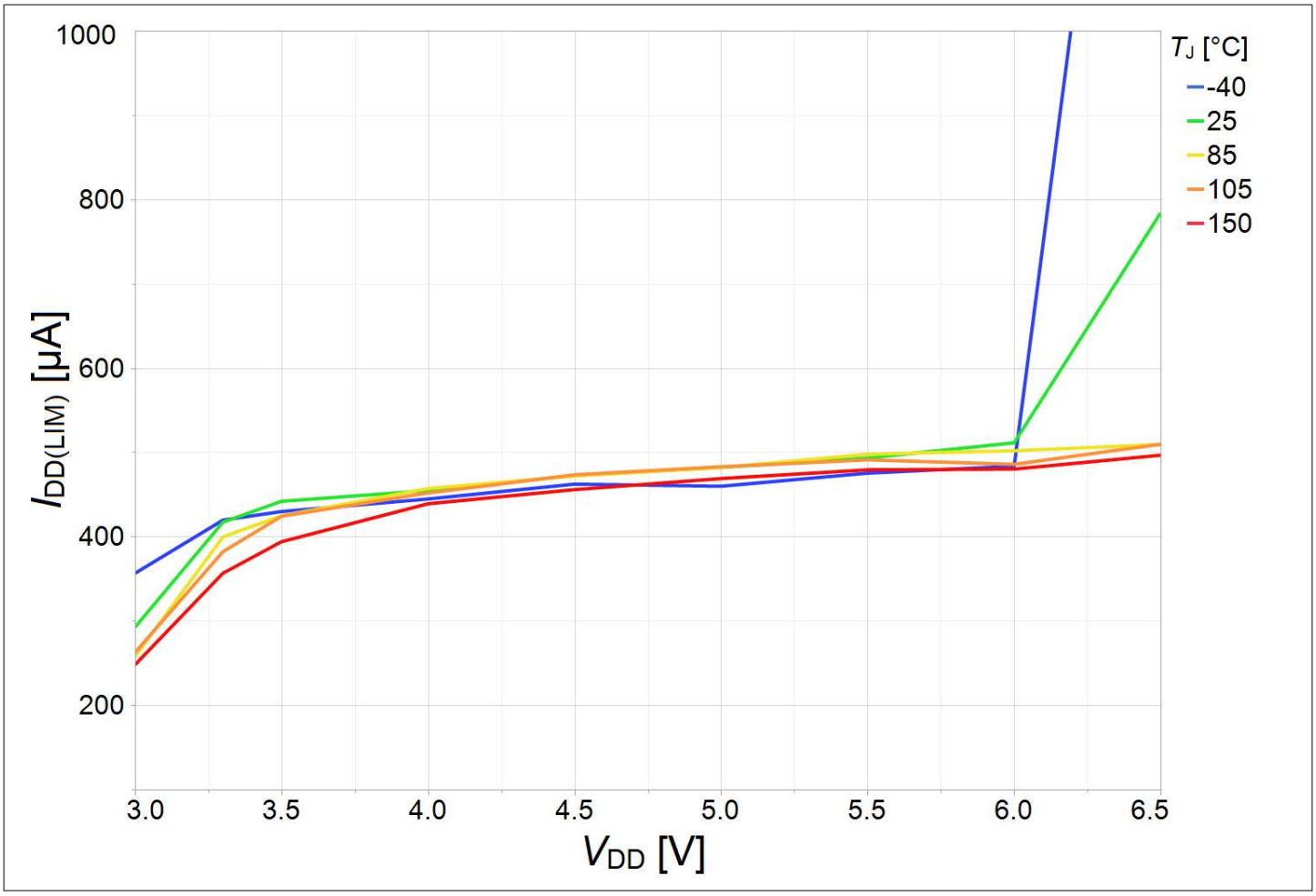

Figure 29 **Typical $I_{DD(LIM)}$ versus V_{DD} at V_{DD} = 3 .. 6.5 V; T_J = -40 .. 150°C; V_{IN} = 3 V; R_{SRP} = *GND*; V_{BAT} = 5 V**

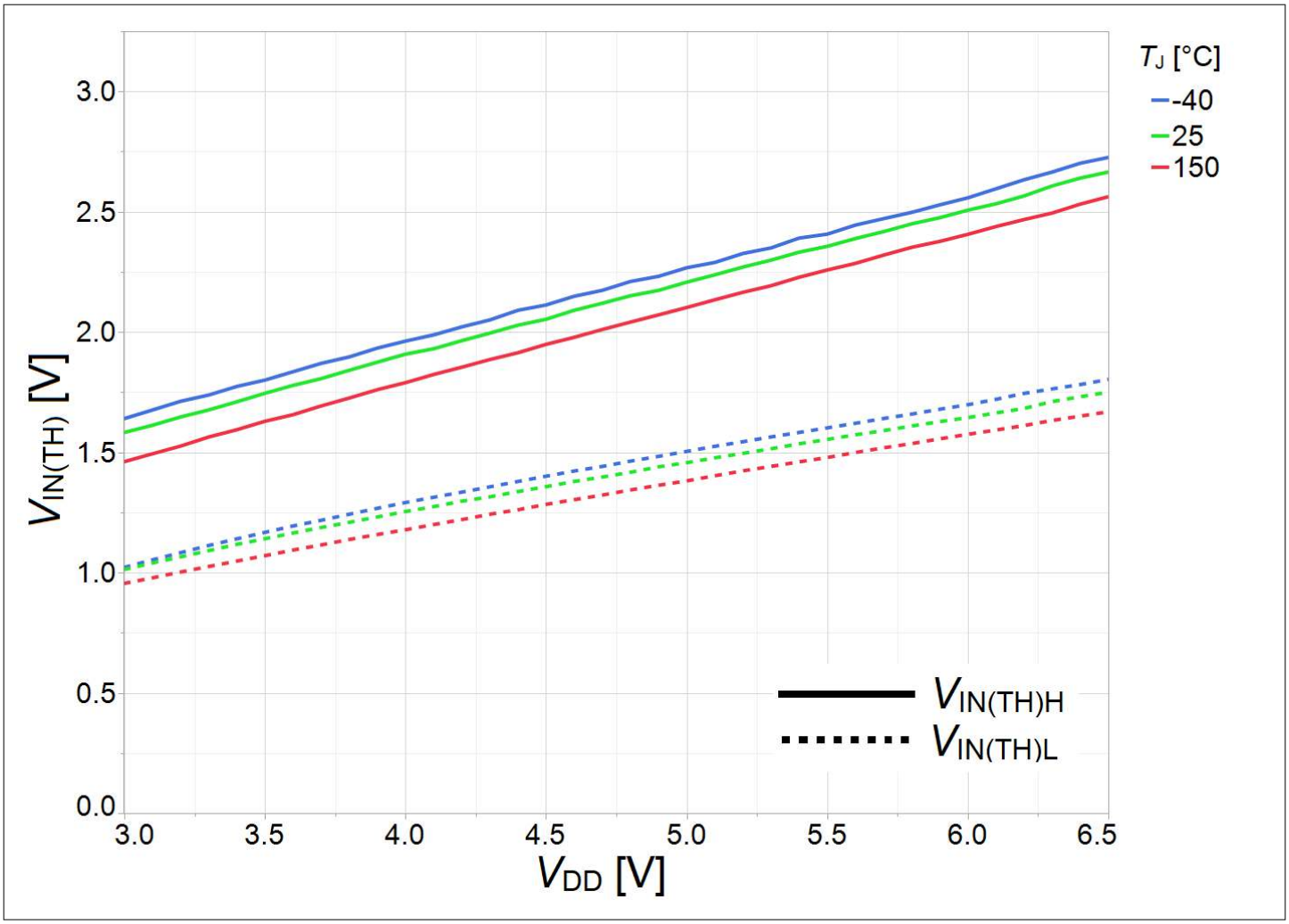

Figure 30 **Typical $V_{IN(TH)}$ versus V_{DD} $V_{IN(TH)H}$ and $V_{IN(TH)L}$; V_{DD} = 3 .. 6.5 V; T_J =-40 ... 150°C; R_{LOAD} = 150 kΩ; R_{SRP} = *GND*; V_{BAT} = 28 V**

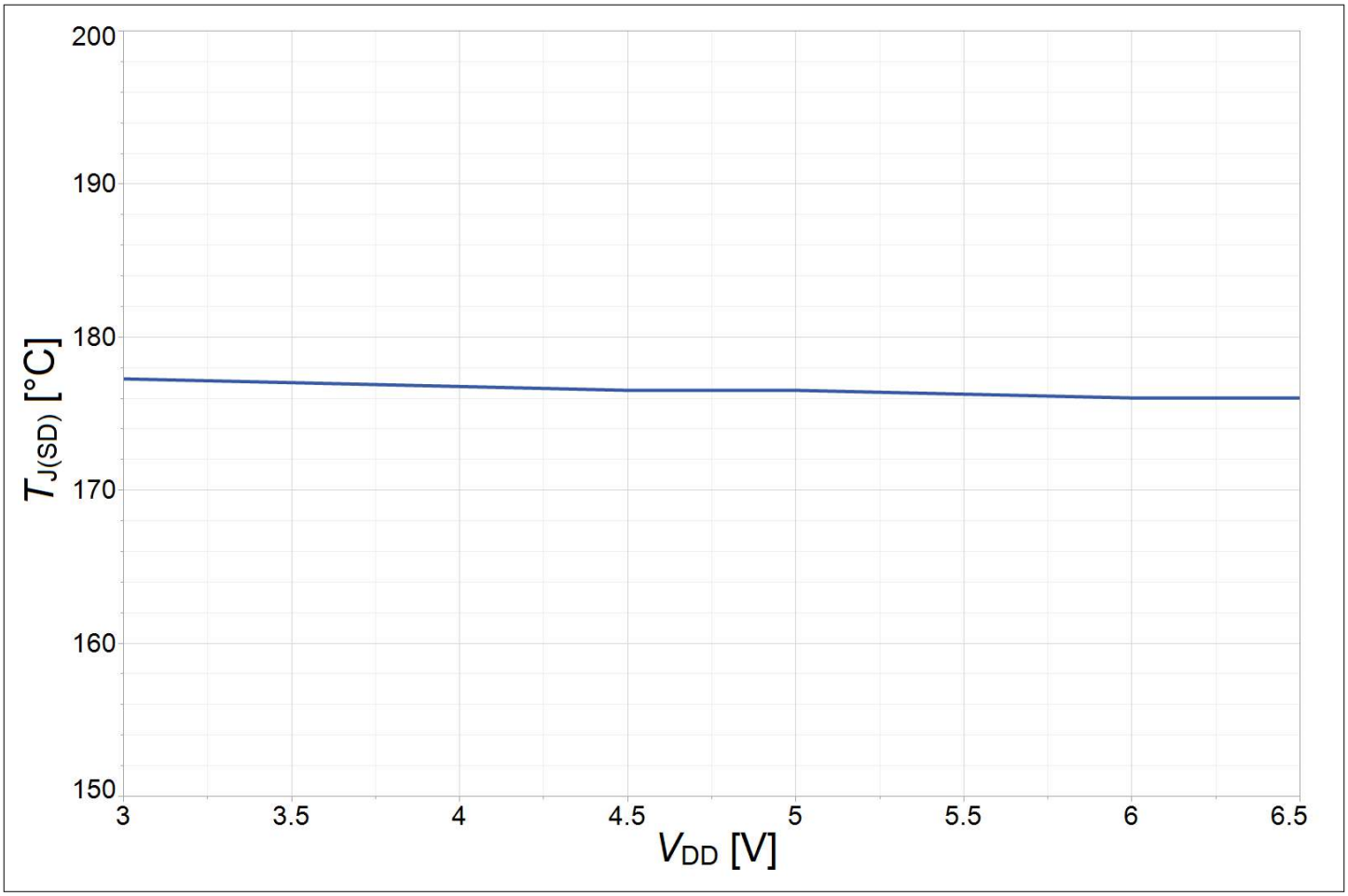

Figure 31 **Typical ITj_{SD} versus V_{DD} at V_{IN} = 3 .. 5.5 V; V_{DD} = 3, 6.5 V; I_L = $I_{L(NOM)}$; V_{BAT} = 28 V**

10 Application information

10.1 Layout recommendations and considerations

As consequences of the fast switching times for high currents (I_{NOM} and above), special care has to be taken to the PCB layout. Stray inductances have to be minimized, as BTT3050EJ has no separate pin for power ground and logic ground. Therefore, it is recommended:

- To ensure that the offset between the ground connection of the SRP resistor and ground pins of the device is minimized. R_{SRP} should be placed next to the device and directly connected to the GND pins, to avoid any influence of GND shift to SRP functionality.
- To ensure that the offset between the ground of the V_{DD} supply and the ground of the pins of the device is minimized.

The maximum parasitic capacitance between the SRP line and GND (C_{SRP}) has to be less than 10 pF to avoid any influence on SRP functionality (e.g. switching times).

10.2 Application diagrams

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Recommended values for $V_{IN} = V_{DD} = 5$ V: $R_{STATUS} = 100$ kΩ.

Table 10 R_{SRP} switching modes

R_{SRP_min}	R_{SRP_max}	Unit	Behavior
0	2.2	kΩ	Fast switching mode. SRP pin can be connected to GND.
2.2	160	kΩ	Adjustable switching mode
160	1000	kΩ	Slow switching mode

For switching timings, please refer to Power stage.

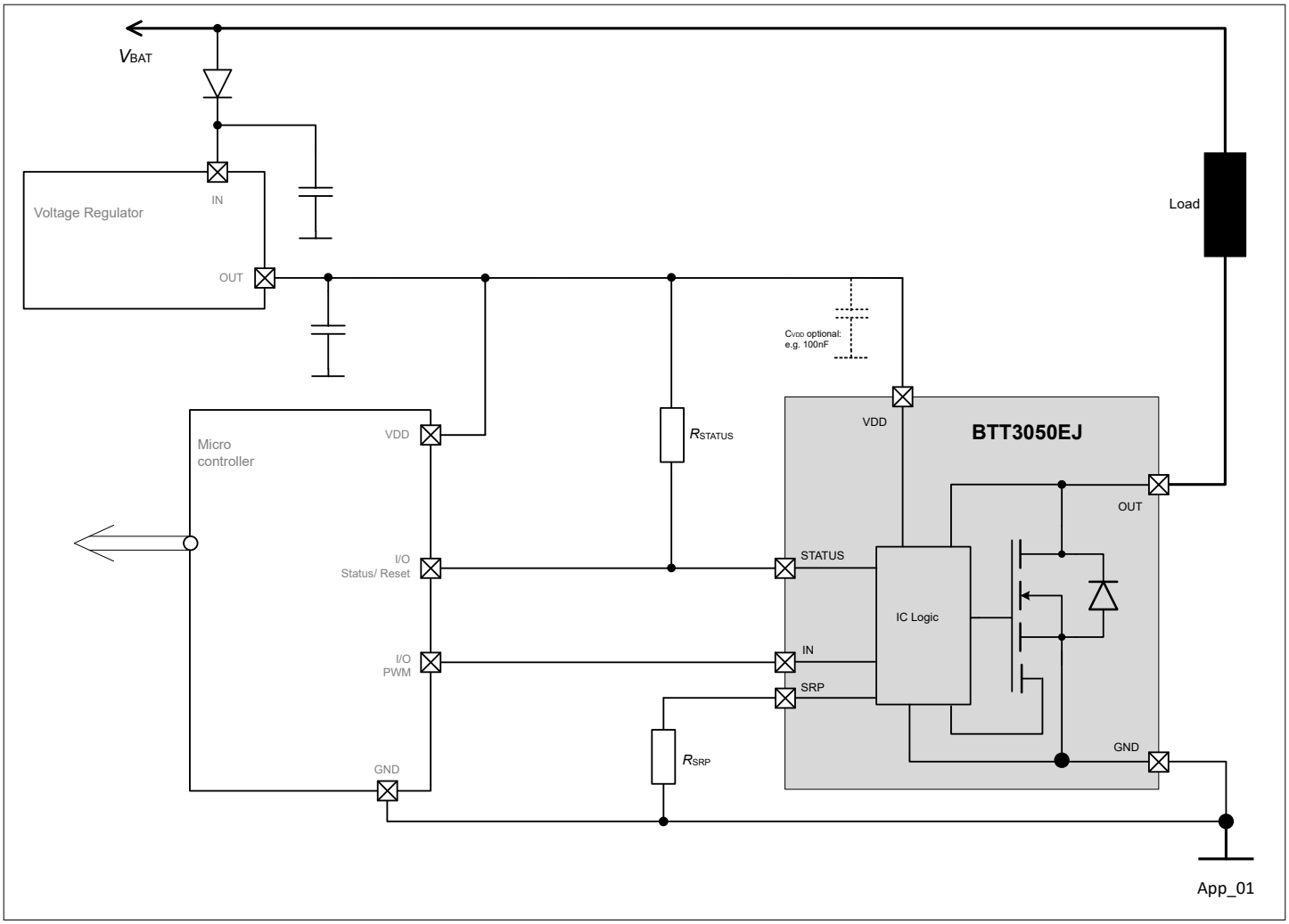

Figure 32 Application diagram to use IN pin and STATUS pin independently

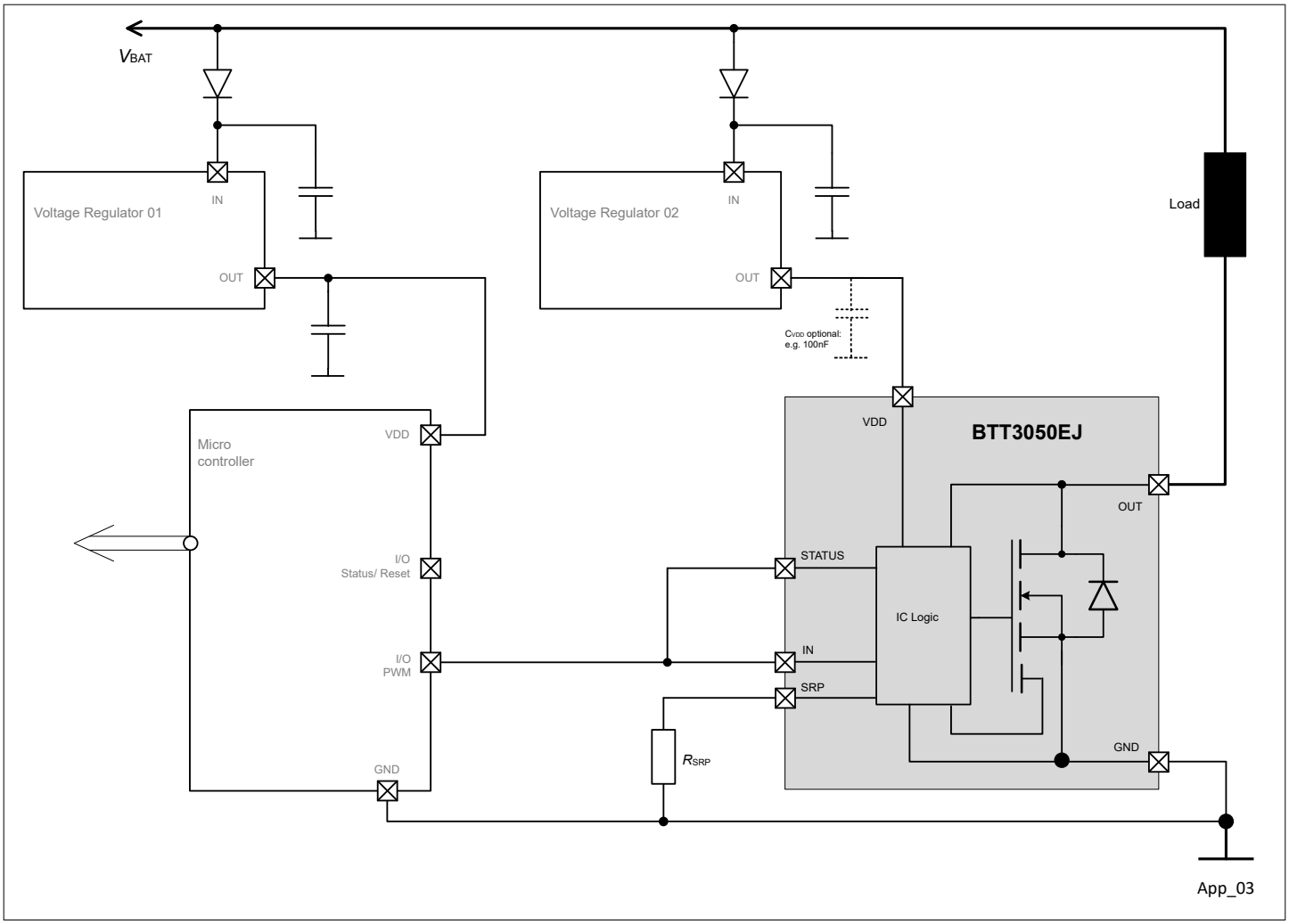

Figure 33 Application diagram to use IN pin and STATUS pin simultaneously with different supply and microcontroller voltage class

Example given for V_{IN} = 3.3 V; V_{DD} = 5 V allows to maintain an optimal $R_{DS(ON)}$ while driving the input with a 3.3 V microcontroller. This configuration does not make possible the readout of the fault signal and will reset the latch OFF via IN pin (see parameters in Diagnostics).

For R_{SRP} recommended values, please see Table 10.

Note: This are very simplified examples of an application circuit. The function must be verified in the real application.

11 Package

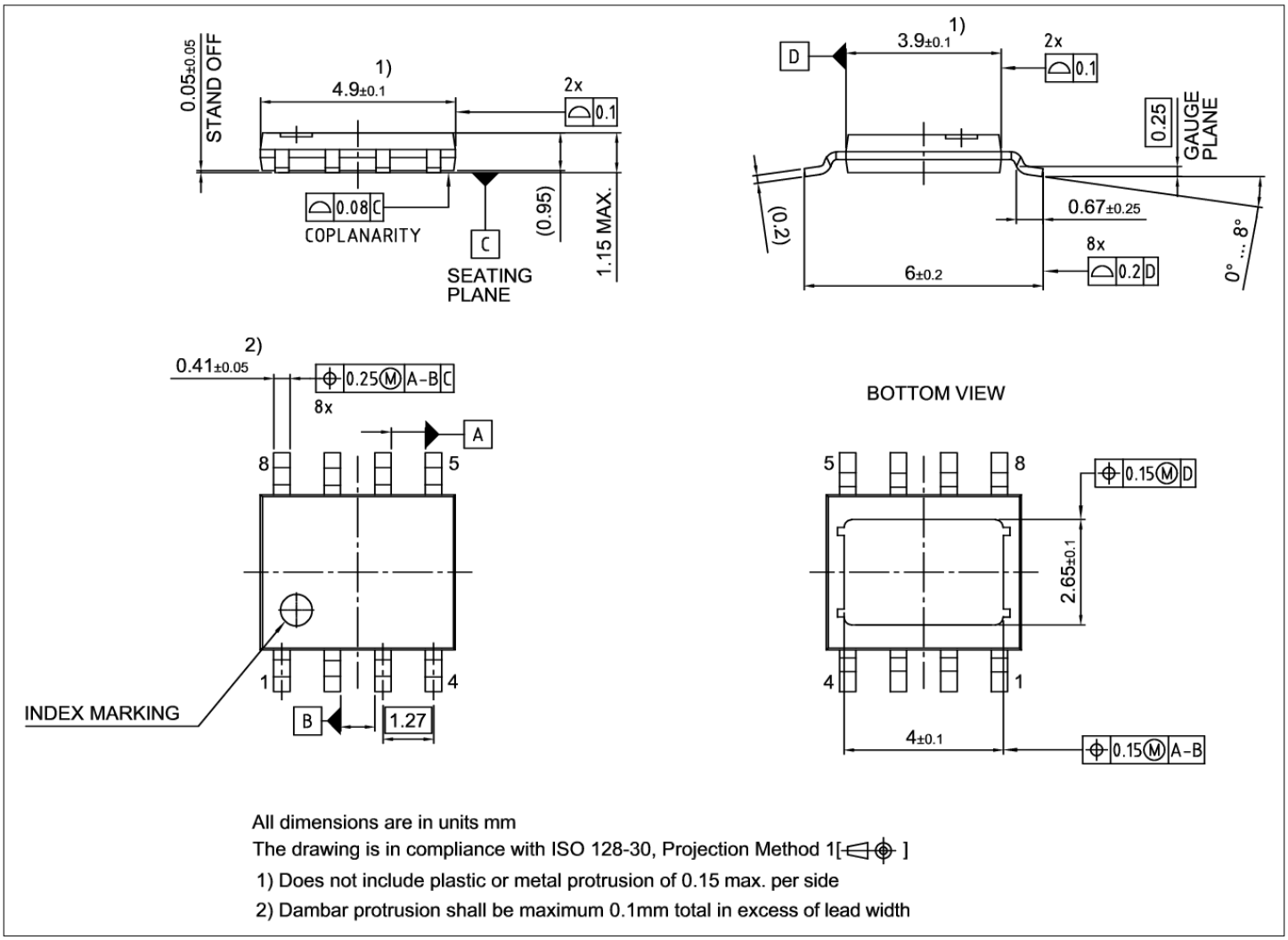

Figure 34 PG-TDSO-8

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision history

Document version	Date of release	Description of changes
Rev.1.00	2022-01-18	• Datasheet creation

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