

## N-channel 80 V, 3.5 mΩ typ., 90 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data

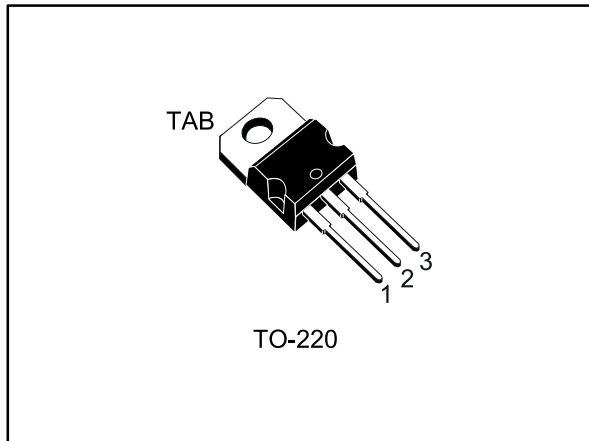
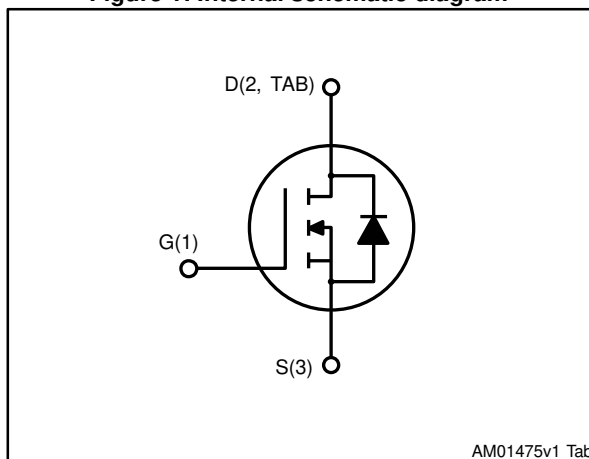


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STP140N8F7	80 V	4.3 mΩ	90 A	200 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP140N8F7	140N8F7	TO-220	Tube

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	80	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	90 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	90	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	360	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	200	W
$E_{AS}$ <sup>(3)</sup>	Single pulse avalanche energy	515	mJ
$T_j$	Operating junction temperature	- 55 to 175	°C
$T_{stg}$	Storage temperature		

**Notes:**

<sup>(1)</sup>Limited by package

<sup>(2)</sup>Pulse width is limited by safe operating area

<sup>(3)</sup>Starting  $T_j = 25\text{ °C}$ ,  $I_D = 18.5\text{ A}$ ,  $V_{DD} = 50\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.75	°C/W
$R_{thj-amb}$	thermal resistance junction-ambient	62.5	°C/W

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA	80			V
I <sub>DSS</sub>	Zero gate voltage Drain current	V <sub>GS</sub> = 0, V <sub>DS</sub> = 80 V			1	μA
		V <sub>GS</sub> = 0, V <sub>DS</sub> = 80 V, T <sub>J</sub> =125 °C			10	μA
I <sub>GSS</sub>	Gate-source leakage current	V <sub>DS</sub> = 0, V <sub>GS</sub> = ±20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5		4.5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> =10 V, I <sub>D</sub> = 45 A		3.5	4.3	mΩ

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>ISS</sub>	Input capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 40 V, f = 1 MHz	-	6340	-	pF
C <sub>OSS</sub>	Output capacitance		-	1195	-	pF
C <sub>RSS</sub>	Reverse transfer capacitance		-	105	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 64 A, V <sub>GS</sub> = 10 V	-	96	-	nC
Q <sub>gs</sub>	Gate-source charge		-	30	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	26	-	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 45 A R <sub>G</sub> =4.7 Ω, V <sub>GS</sub> = 10 V	-	26	-	ns
t <sub>r</sub>	Rise time		-	51	-	ns
t <sub>d(off)</sub>	Turn-off-delay time		-	82	-	ns
t <sub>f</sub>	Fall time		-	44	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		90	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		360	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 90 \text{ A}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 64 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 60 \text{ V}$ $T_j = 150 \text{ }^\circ\text{C}$	-	58		ns
$Q_{rr}$	Reverse recovery charge		-	92		nC
$I_{RRM}$	Reverse recovery current		-	3.2		A

**Notes:**

(1) Pulse width is limited by safe operating area

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

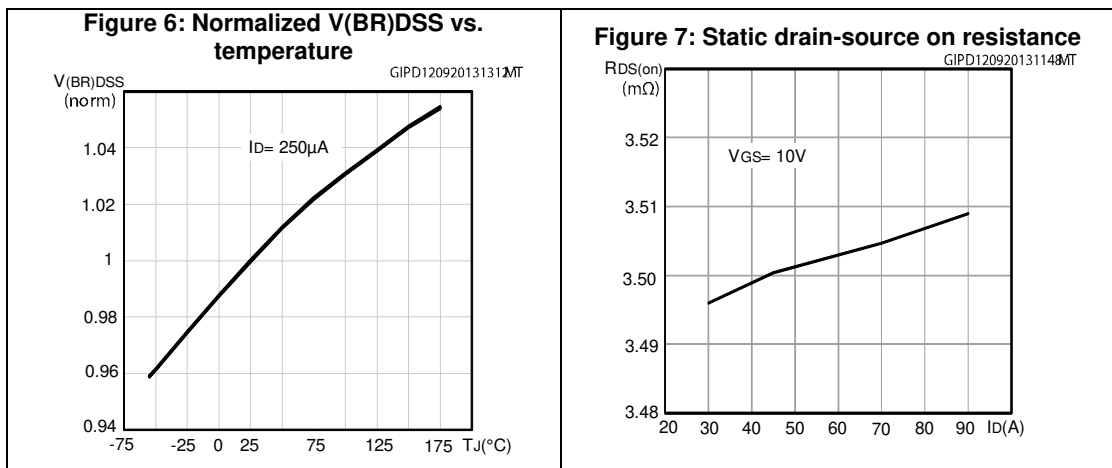
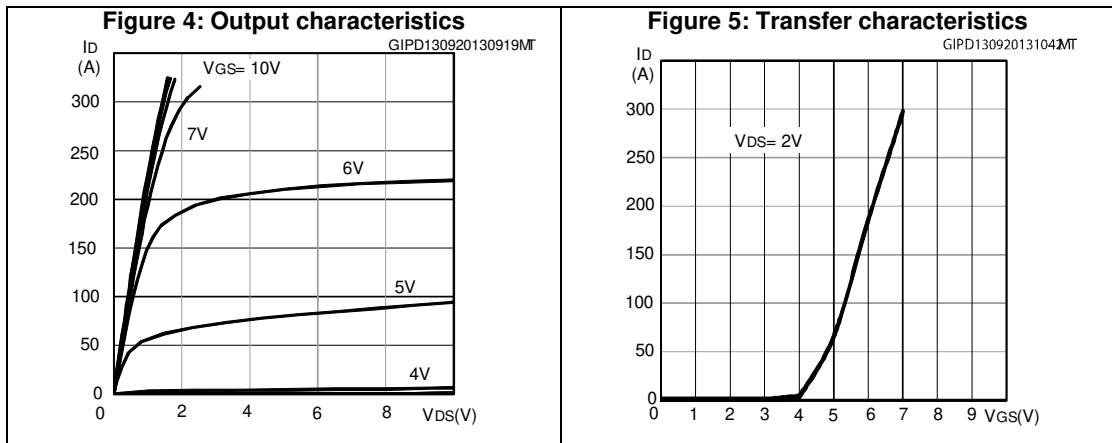
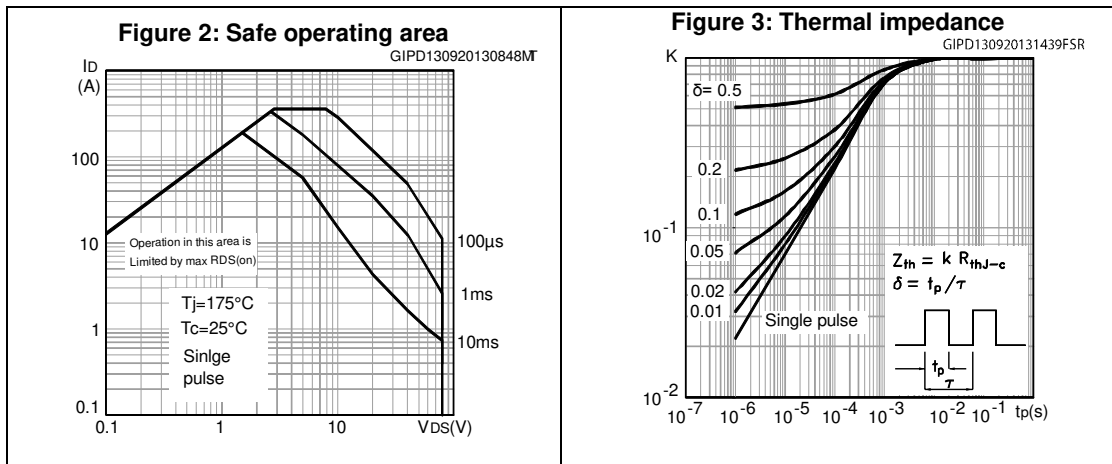


Figure 8: Gate charge vs. gate-source voltage

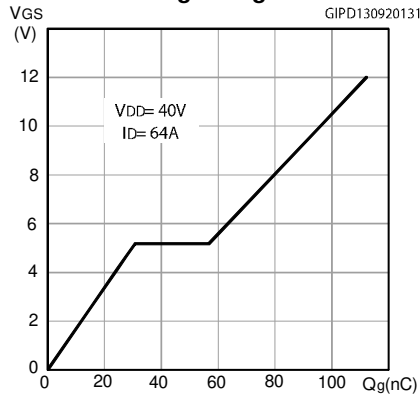


Figure 9: Capacitance variations

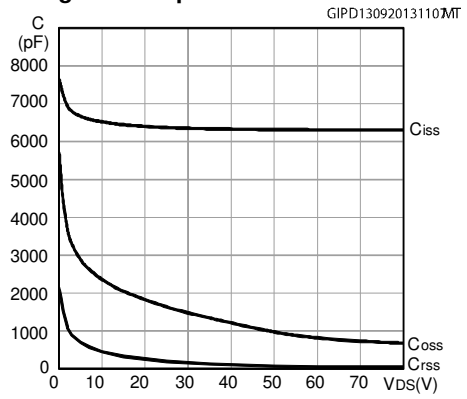


Figure 10: Normalized gate threshold voltage vs. temperature

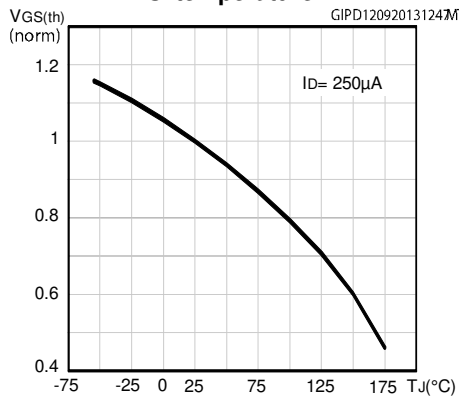


Figure 11: Normalized on resistance vs. temperature

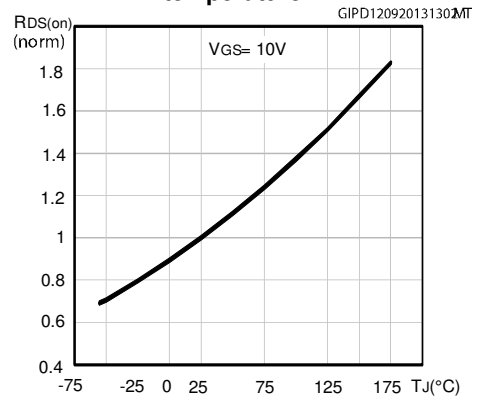
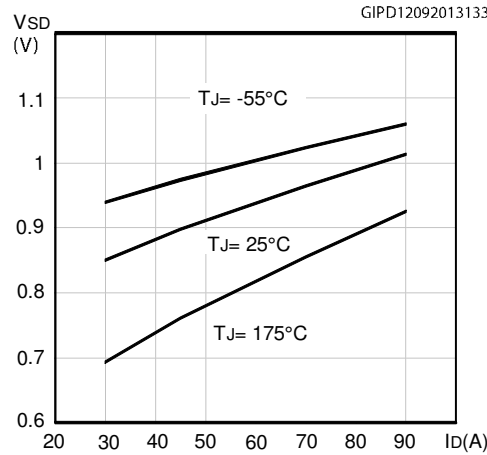
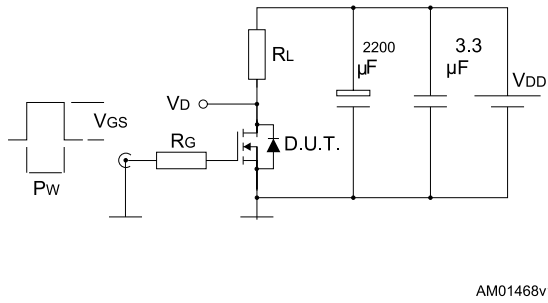


Figure 12: Source-drain diode forward characteristics

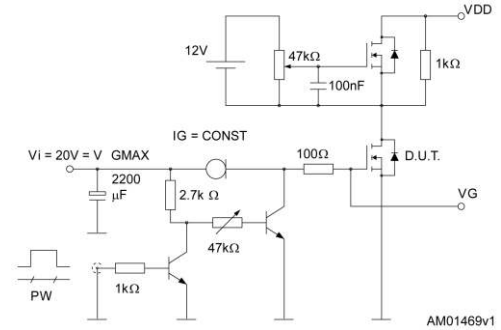


### 3 Test circuits

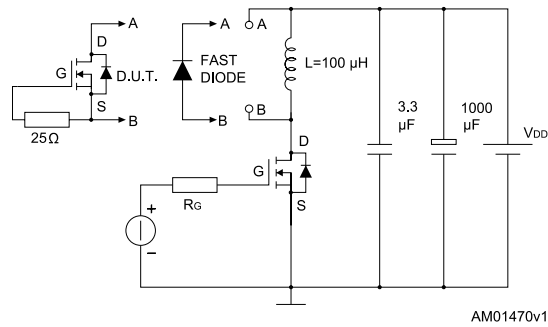
**Figure 13: Switching times test circuit for resistive load**



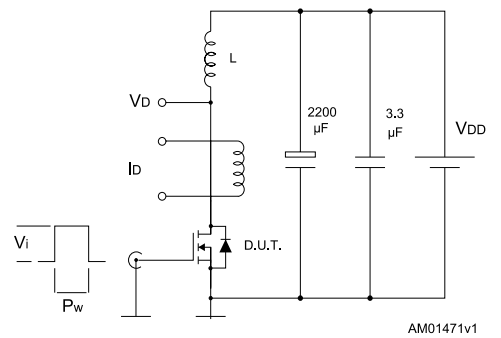
**Figure 14: Gate charge test circuit**



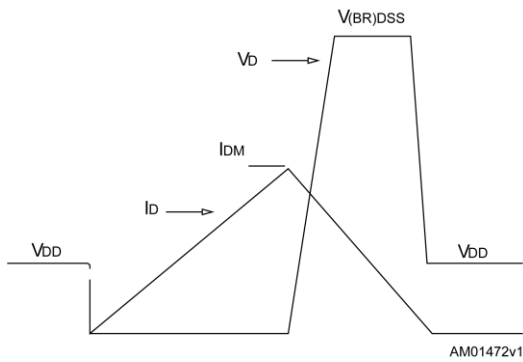
**Figure 15: Test circuit for inductive load switching and diode recovery times**



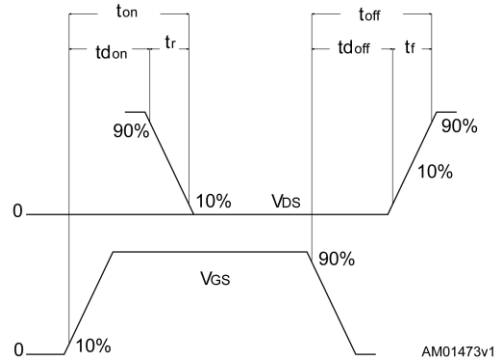
**Figure 16: Unclamped inductive load test circuit**



**Figure 17: Unclamped inductive waveform**



**Figure 18: Switching time waveform**



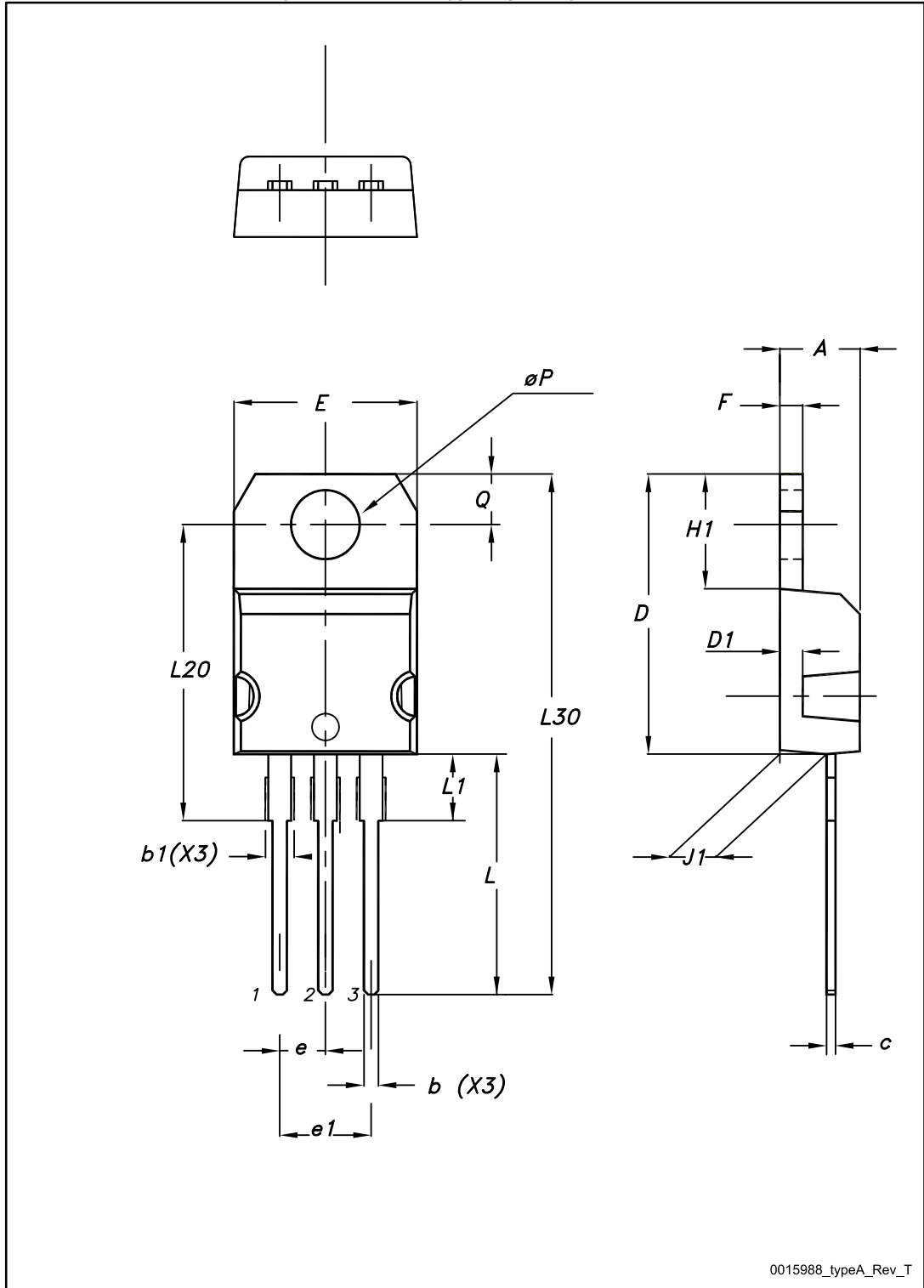


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220 type A package information

Figure 19: TO-220 type A package outline



0015988\_typeA\_Rev\_T

Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ÆP	3.75		3.85
Q	2.65		2.95

## 5 Revision history

Table 9: Document revision history

Date	Revision	Changes
25-Aug-2014	1	First release.
09-Oct-2014	2	Updated <a href="#">Figure 3: "Thermal impedance"</a>

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