

Specifications HC-5524

Absolute Maximum Ratings (Note 1)

Maximum Supply Voltages (V_{B+})	-0.5V to +7V
(V_{B+}) - (V_{B-})	+40V
Relay Drive Voltage	-0.5V to +15V
Junction Temperature	+175°C
Junction Temperature (Plastic Package)	+150°C
Lead Temperature (Soldering 10 Sec.)	+300°C

Operating Conditions

Operating Temperature Range	$0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$
HC-5524-5	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
HC-5524-9	$-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$
Storage Temperature Range	$-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$
Relay Driver Voltage	+5V to +12V
Positive Power Supply (V_{B+})	+5V \pm 5%
Negative Power Supply (V_{B-})	-20V to -28V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Typical Parameters are at $T_A = +25^{\circ}\text{C}$, $V_{B+} = +5\text{V}$, $V_{B-} = -24\text{V}$, $AG = DG = BG = 0\text{V}$. Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Operating Temperature Range. All Parameters are Specified at 600 Ω 2-Wire Terminating Impedance, Unless Otherwise Specified.

PARAMETER	CONDITIONS	LIMITS			UNITS	
		MIN	TYP	MAX		
AC TRANSMISSION PARAMETERS						
RX Input Impedance	300Hz to 3.4kHz (Note 2)	-	100	-	k Ω	
TX Output Impedance		-	-	20	Ω	
4W Input Overload Level	300Hz to 3.4kHz, 600 Ω Reference	+1.0	-	-	V_{PEAK}	
2W Return Loss	Matched for 600 Ω (Note 2)					
SRL LO		26	35	-	dB	
ERL		30	40	-	dB	
SRL HI		30	40	-	dB	
2W Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 2), 300Hz to 3400Hz	58	63	-	dB	
4W Longitudinal Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 2), 300Hz to 3400Hz (Note 2)	50	55	-	dB	
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-80	-67	dBmp	
	$I_{LINE} = 40\text{mA}$, $T_A = +25^{\circ}\text{C}$ (Note 2)	-	10	23	dBmC	
Longitudinal Current Capability	$I_{LINE} = 40\text{mA}$, $T_A = +25^{\circ}\text{C}$ (Note 2)	-	-	40	mArms	
Insertion Loss						
	2W/4W	-1.58dBm at 1kHz, Referenced 600 Ω	-	± 0.05	± 0.2	dB
	4W/2W	0dBm at 1kHz, Referenced 600 Ω	-	± 0.05	± 0.2	dB
4W/4W	-1.58dBm at 1kHz, Referenced 600 Ω	-	-	± 0.2	dB	
Frequency Response	300Hz to 3400Hz (Note 2), Referenced to Absolute Level at 1kHz, 0dBm Referenced 600 Ω	-	± 0.02	± 0.06	dB	
Level Linearity 2W to 4W and 4W to 2W	Referenced to -10dBm (Note 2)					
	+3 to -40dBm	-	-	± 0.08	dB	
	-40 to -50dBm	-	-	± 0.12	dB	
-50 to -55dBm	-	-	± 0.3	dB		
Absolute Delay	(Note 2)					
	2W/4W	300Hz to 3400Hz	-	-	1	μs
	4W/2W	300Hz to 3400Hz	-	-	1	μs
	4W/4W	300Hz to 3400Hz	-	0.95	1.5	μs
Total Harmonic Distortion 2W/4W, 4W/2W, 4W/4W	Reference Level 0dBm at 600 Ω , 300Hz to 3400Hz (Note 2)	-	-	-50	dB	

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PARAMETER	CONDITIONS	LIMITS			UNITS	
		MIN	TYP	MAX		
AC TRANSMISSION PARAMETERS (Continued)						
Idle Channel Noise 2W and 4W	(Note 2)					
	C-Message	-	-	5	dBrnC	
	Psophometric	-	-	-85	dBmp	
	3kHz Flat	-	-	16	dBrn	
Open Loop Voltage ($V_{TIP} - V_{RING}$)	$V_{B+} = +5\text{V}$, $V_{B-} = -24\text{V}$	-	15.8	-	V	
Power Supply Rejection Ratio	(Note 2)					
	V_{B+} to 2W	30Hz to 200Hz, $R_L = 600\Omega$	20	40	-	dB
	V_{B+} to 4W		20	40	-	dB
	V_{B-} to 2W		20	40	-	dB
	V_{B-} to 4W		20	50	-	dB
	V_{B+} to 2W	200Hz to 16kHz, $R_L = 600\Omega$	30	40	-	dB
	V_{B+} to 4W		20	28	-	dB
	V_{B-} to 2W		20	50	-	dB
Ring Sync Pulse Width		50	-	500	μs	
DC PARAMETERS						
Loop Current Programming		20	40	60	mA	
						Limit Range
Accuracy		10	-	-	%	
Loop Current During Power Denial	$R_L = 200\Omega$	-	± 4	± 7	mA	
Fault Currents		-	30	-	mA	
						TIP to Ground
						RING to Ground
TIP and RING to Ground		-	150	-	mA	
Switch Hook Detection Threshold		-	12	15	mA	
Ground Key Detection Threshold		-	10	-	mA	
Thermal ALM Output	Safe Operating Die Temperature Exceeded	140	-	160	$^\circ\text{C}$	
Ring Trip Detection Threshold	$V_{RING} = 105V_{RMS}$, $f_{RING} = 20\text{Hz}$	-	10	-	mA	
Ring Trip Detection Period		-	100	150	ms	
Dial Pulse Distortion		-	0.1	0.5	ms	
Relay Driver Outputs		-	0.2	0.5	V	
						On Voltage V_{OL}
Off Leakage Current	$V_{OH} = 13.2\text{V}$	-	± 10	± 100	μA	
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{\text{TST}}$, PRI)		-	-	0.8	V	
						Logic '0' V_{IL}
Logic '1' V_{IH}		2.0	-	5.5	V	

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PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
DC PARAMETERS (Continued)					
Input Current (F0, F1, RS, TST, PRI)	$0\text{V} \leq V_{IN} \leq 5\text{V}$	-	-	± 100	μA
Logic Outputs					
Logic '0' V_{OL}	$I_{LOAD} = 800\mu\text{A}$	-	0.1	0.5	V
Logic '1' V_{OH}	$I_{LOAD} = 40\mu\text{A}$	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	60	-	mW
I_{B+}	$V_{B+} = +5.25\text{V}$, $V_{B-} = -28\text{V}$, $R_{LOOP} = \infty$	-	-	4	mA
I_{B-}	$V_{B+} = +5.25\text{V}$, $V_{B-} = -28\text{V}$, $R_{LOOP} = \infty$	-4	-	-	mA
I_{B+}	$V_{B+} = +5\text{V}$, $V_{B-} = -24\text{V}$, $R_{LOOP} = 600\Omega$	-	3	6	mA
I_{B-}	$V_{B+} = +5\text{V}$, $V_{B-} = -24\text{V}$, $R_{LOOP} = 600\Omega$	-28	-24	-	mA
UNCOMMITTED OP AMP PARAMETERS					
Input Offset Voltage		-	± 5	-	mV
Input Offset Current		-	± 10	-	nA
Differential Input Resistance	(Note 2)	-	1	-	M Ω
Output Voltage Swing	$R_L = 10\text{k}\Omega$	-	± 3	-	$V_{P,P}$
Small Signal GBW	(Note 2)	-	1	-	MHz

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
1	2	AG	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	3	VB+	Positive Voltage Source - Most Positive Supply.
3	4	C1	Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	8	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page. F1 should be toggled high after power is applied.
5	9	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on front page.
6	10	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500 μs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.

Pin Descriptions (Continued)

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
7	11	$\overline{\text{SHD}}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	12	$\overline{\text{GKD}}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	13	$\overline{\text{TST}}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep ALM low. See Truth Table on front page.
10	17	ALM	A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{\text{TST}}$ is forced low by an external control signal, ALM is latched low until the proper F1, F0 state and $\overline{\text{TST}}$ input is brought high. The ALM can be tied directly to the $\overline{\text{TST}}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on front page. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{\text{TST}}$ pin from the ALM. Care must be exercised in attempting this as continued thermal overstress may reduce component life.
11	18	ILMT	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	19	OUT1	The analog output of the spare operational amplifier.
13	20	-IN1	The inverting analog input of the spare operational amplifier.
14	22	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purposes.
15	24	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	25	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring Injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	27	VRX	Receive Input, Four Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	31	C2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.
19	32	VTX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	33	PRI	A TTL compatible input used to control $\overline{\text{PR}}$. PRI active High = $\overline{\text{PR}}$ active low.
21	34	$\overline{\text{PR}}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	35	DG	Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.
23	36	$\overline{\text{RD}}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2 wire line.
24	37	VFB (Note 2)	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op-amp to accommodate 2W line impedance matching. (This is not used in the typical applications circuit).
25	38	TF2	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF1.
NA	39	TF1	Tie directly to TF2 in the PLCC application.
26	41	RF1	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.

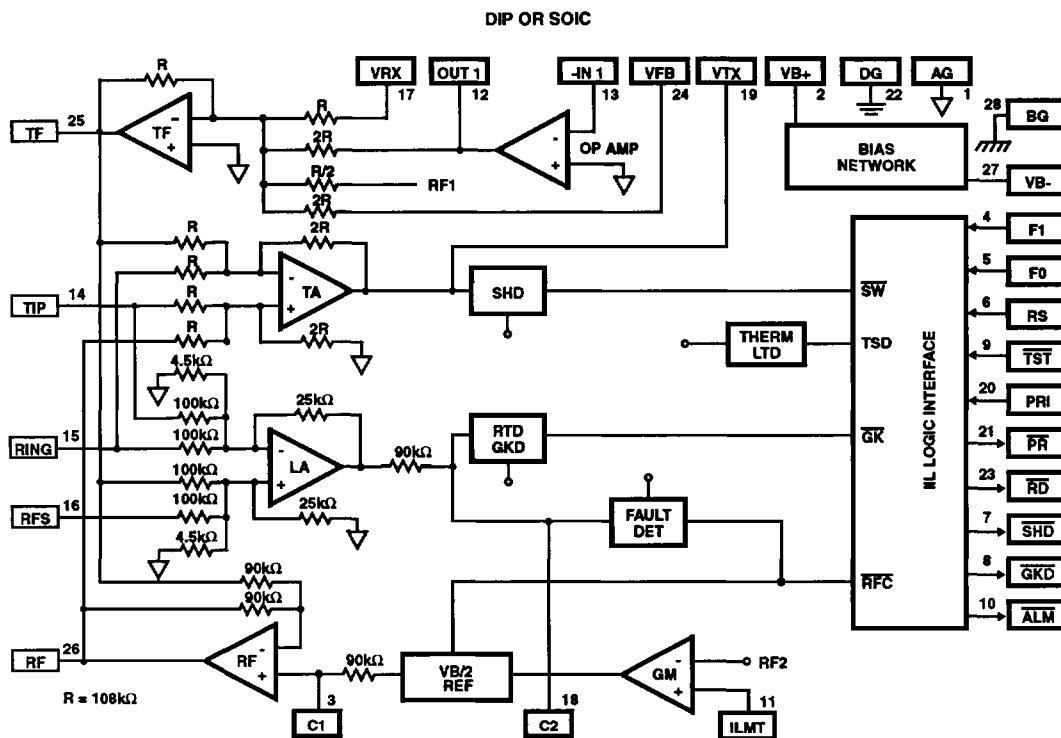
Pin Descriptions (Continued)

DIP/ SOIC	PLCC	SYMBOL	DESCRIPTION
NA	42	RF2	Tie directly to RF1 in the PLCC application.
27	43	VB-	The battery voltage source. The most negative supply.
28	44	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
	1, 5, 6, 7, 14, 15, 16, 21, 23, 26, 28, 29, 30, 40	NC	No internal connection.

NOTES:

1. All grounds (AG, BG, DG) must be applied before V_{B+} or V_{B-} . Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
2. Although not used in the typical applications circuit, V_{FB} may be used in matching complex 2-Wire impedances.

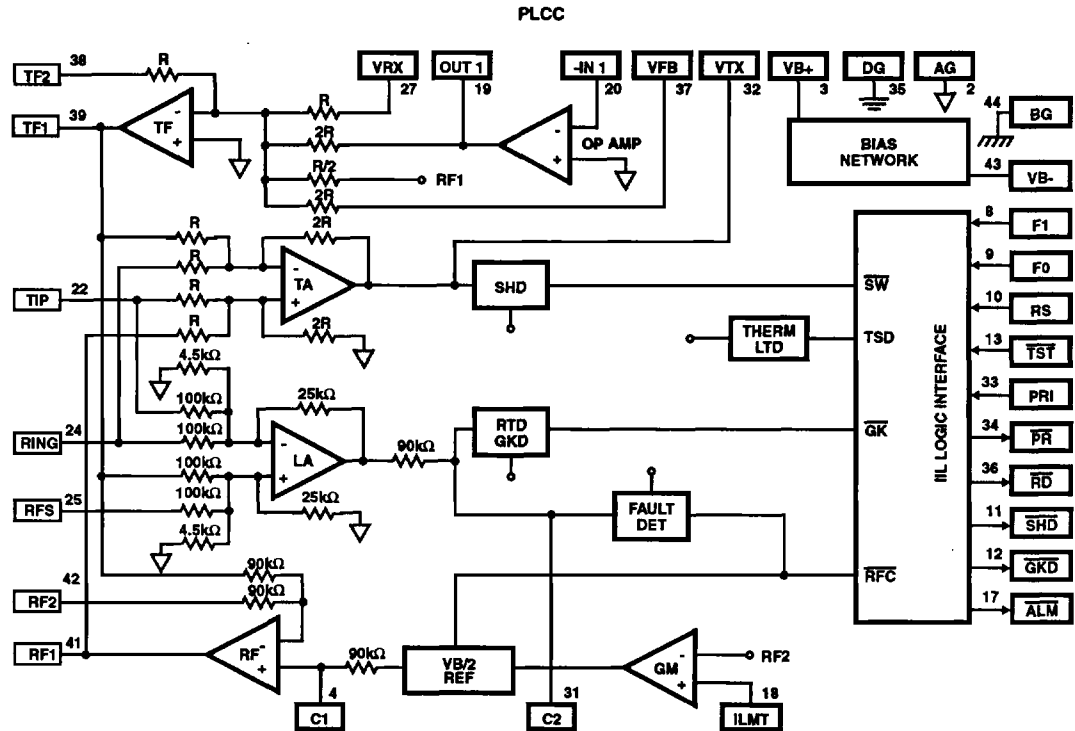
Functional Diagram



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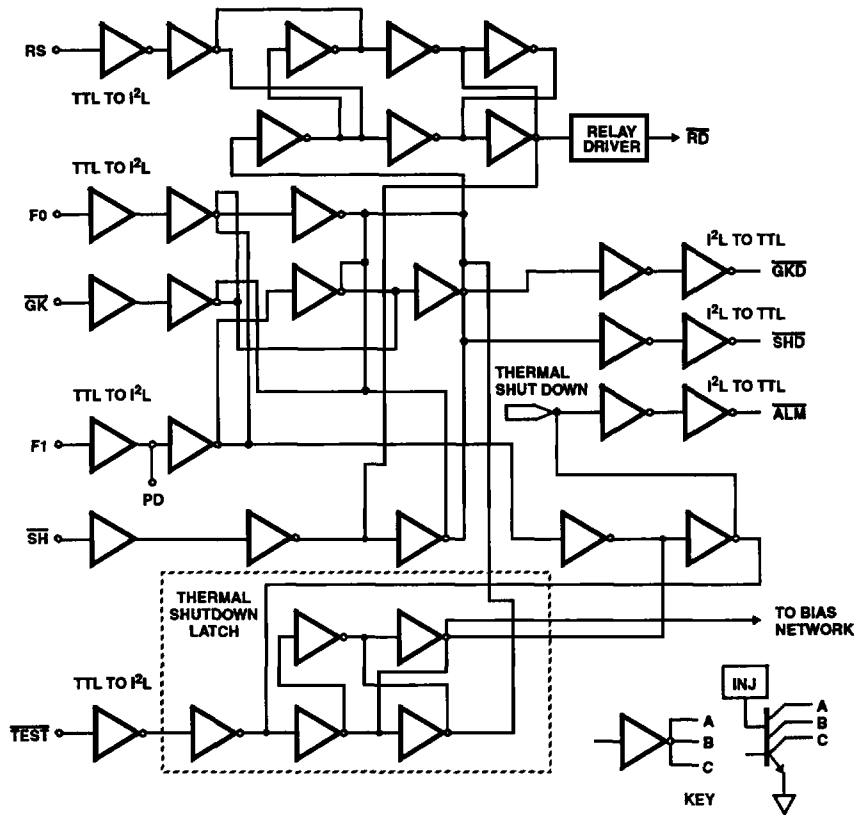
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Functional Diagram (Continued)



NOTE:
 $R = 108k\Omega$
 $NC = 1, 5, 6, 7, 14, 15, 16, 21$
 $23, 26, 28, 29, 30, 40$

Logic Diagram



Die Characteristics

Transistor Count	224	
Diode Count	28	
Die Dimensions	174 x 120 mils	
Substrate Potential	Connected	
Process	Bipolar-DI	
Thermal Constants (°C/W)	θ_{JA}	θ_{JC}
Ceramic DIP	48	12
Plastic DIP	51	21
PLCC	47	17
SOIC	72	22

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 40Arms, 20Arms per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10 μ s Rise/	\pm 1000 (Plastic)	V_{PEAK}
	1000 μ s Fall	\pm 500 (Ceramic)	V_{PEAK}
Metallic Surge	10 μ s Rise/	\pm 1000 (Plastic)	V_{PEAK}
	1000 μ s Fall	\pm 500 (Ceramic)	V_{PEAK}
T/GND	10 μ s Rise/	\pm 1000 (Plastic)	V_{PEAK}
R/GND	1000 μ s Fall	\pm 500 (Ceramic)	V_{PEAK}
50/60Hz Current	T/GND	700 (Plastic)	V_{RMS}
	R/GND	Limited to 10Arms	350 (Ceramic)

Applications Diagram

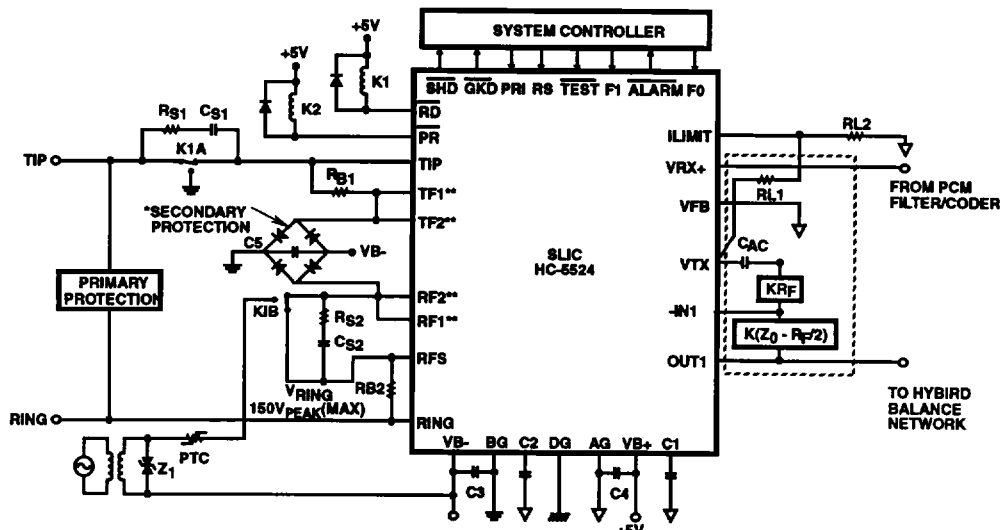


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

TYPICAL COMPONENT VALUES

C1 = 0.5μF, 20V

C2 = 0.5μF-1.0μF ±10%, 20V (Should be nonpolarized)

C3 = 0.01μF, 50V ±20%

C4 = 0.01μF, 50V ±20%

C5 = 0.01μF, 50V ±20%

CAC = 0.5μF, 20V

$K(Z_0 - R_F/2) = 50k\Omega$ ($Z_0 = 600\Omega$, $K = \text{Scaling Factor} = 100$)

RL1, RL2; Current Limit Setting Resistors

$$RL1 + RL2 > 90k\Omega$$

$$I_{LIMIT} = (.6) (RL1 + RL2) / (200 \times RL2), \text{ RL1 typically } 100k\Omega$$

$$KR_F = 20k\Omega, R_F = 2(R_{B1} + R_{B2}), K = \text{Scaling Factor} = 100$$

$RB_1 = RB_2 = 50\Omega$ (1% absolute, matching requirements covered in a Tech Brief)

$RS_1 = RS_2 = 1k\Omega$ typically

$CS_1 = CS_2 = 0.1\mu F$, 200V typically, depending on V_{RING} and line length.

$Z_1 = 150V$ to $200V$ transient protector. PTC used as ring generator ballast.

* Secondary protection diode bridge recommended is 3A, 200V type.

** TF1, TF2 and RF1, RF2 are on PLCC only and should be connected together as shown.

NOTES:

1. All grounds (AG, BG, & DG) must be applied before V_{B+} or V_{B-} . Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first
2. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.

Additional information is contained in Application Note 549, "The HC-550X Telephone SLICs" By Geoff Phillips