HMC683LP6C / 683LP6CE

v02.0808

HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ LO SWITCH, 0.7 - 1.0 GHz

Typical Applications

The HMC683LP6C(E) is Ideal for:

- Cellular/3G & LTE/WiMAX/4G
- Basestations & Repeaters
- GSM, CDMA & OFDM
- Dual Density Receivers

Features

High Input IP3: +23 dBm

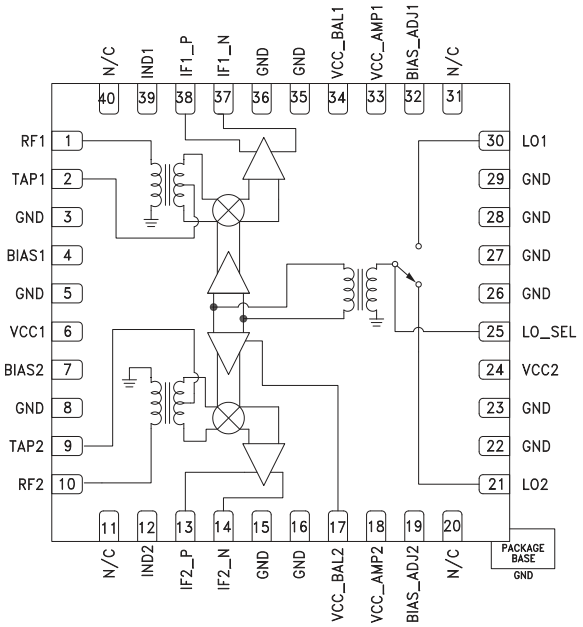
Conversion Gain: 7.5 dB

Low LO Drive: 0 dBm

High Channel Isolation

40 Lead 6x6mm SMT Package: $36mm^2$

Functional Diagram



General Description

The HMC683LP6C(E) is a high linearity, dual channel downconverter with integrated LO amplifier in a 6x6 SMT QFN package covering 0.7 - 1.0 GHz. Excellent input IP3 performance of +23 dBm for down conversion is provided for 3G & 4G GSM/CDMA applications at an LO drive of 0 dBm. With an input 1 dB compression of +11 dBm, the RF port will accept a wide range of input signal levels. Conversion gain is 7.5 dB typical. The 60 - 500 MHz IF frequency response will satisfy various GSM/CDMA receive frequency plans.

Electrical Specifications, T_A = +25 °C, IF - 100 MHz, LO = 0 dBm

Vcc1, 2 = Vcc_BAL1, 2 = Vcc_AMP1, 2 [1] = Vcc_IF1P, N = Vcc_IF2P, N = +5V, BIAS1, 2 = +2.5V

Parameter	Min.	Typ.	Max.	Units
Frequency Range, RF		700 - 1000		MHz
Frequency Range, LO		570 - 900		MHz
Frequency Range, IF		60 - 500		MHz
Conversion Gain	5	7.5		dB
Noise Figure (SSB)		11		dB
LO to RF Isolation	10	16		dB
LO to IF Isolation	15	20		dB
RF to IF Isolation	19	28		dB
IP3 (Input)		23		dBm
1 dB Compression (Input)		11		dBm
Channel to Channel Isolation		50		dB
LO Drive Input Level (Typical)		-3 to +3		dBm
Supply Current (Icc)		420	520	mA

[1] See Application Circuit [2] Unless otherwise noted all measurements with low side LO & IF = 100 MHz.

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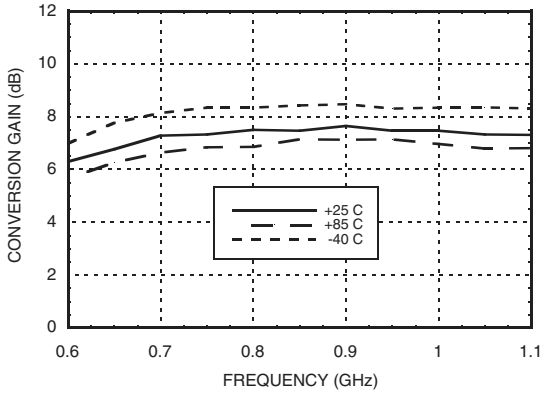
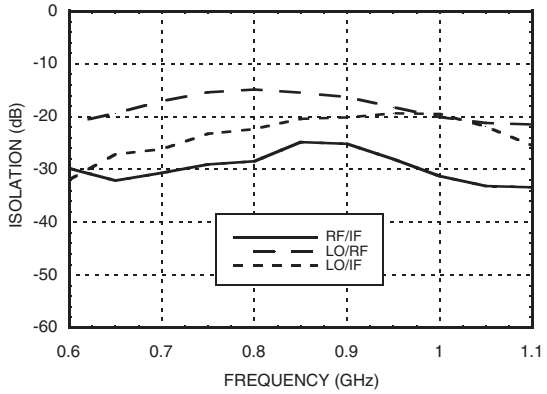
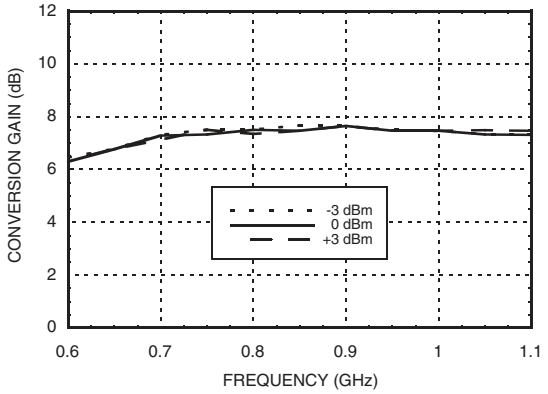
Single Channel: Conversion Gain vs. Temperature



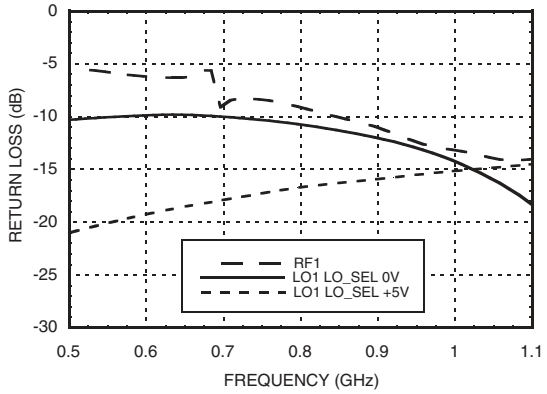
Single Channel: Isolation



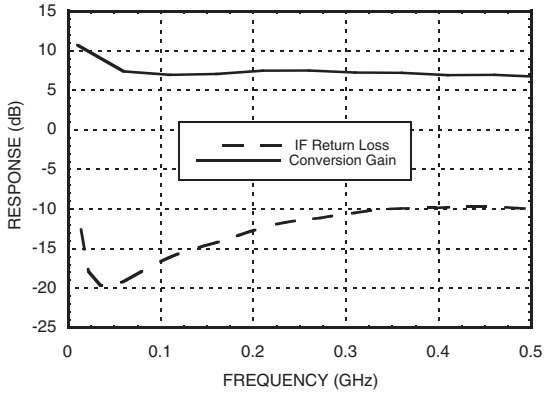
Single Channel: Conversation Gain vs. LO Drive



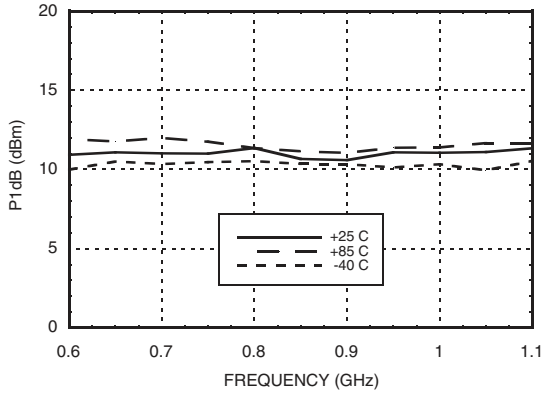
Single Channel: Return Loss



Single Channel: IF Bandwidth



Single Channel: Input P1dB vs. Temperature



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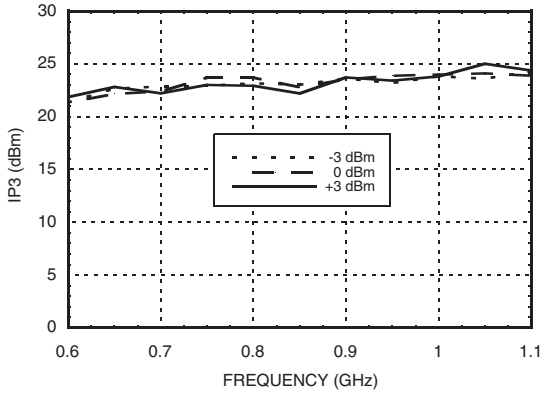
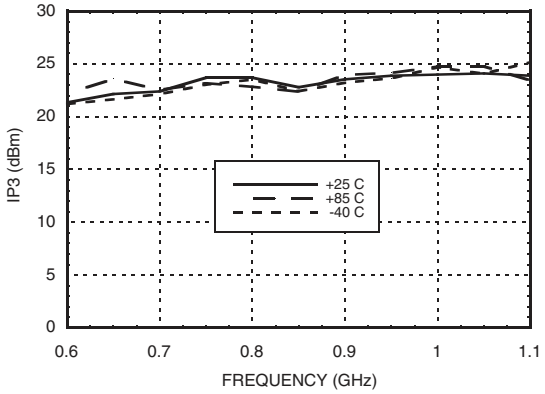
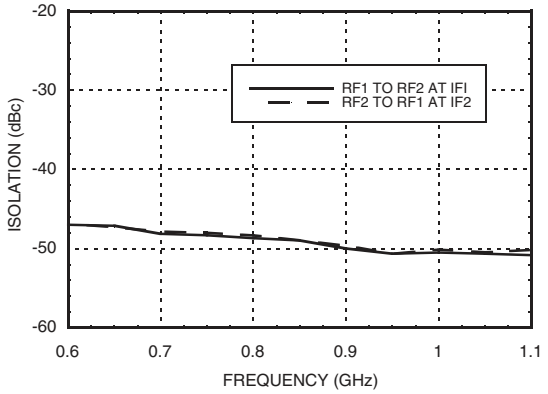
Single Channel: Input IP3 vs. LO Drive



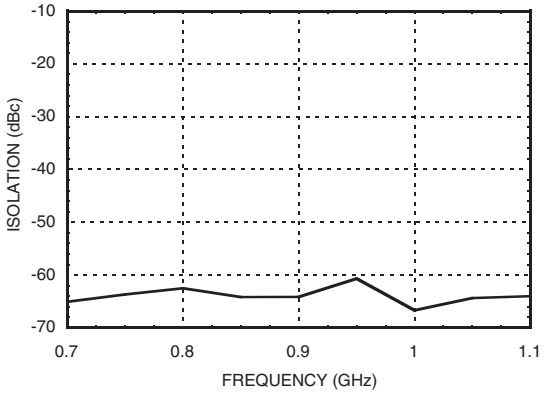
Single Channel: Input IP3 vs. Temperature



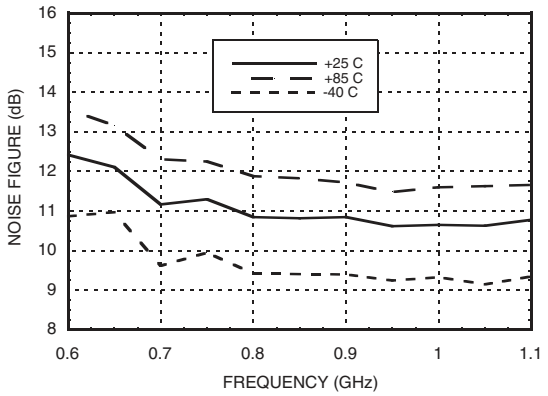
Dual Channel: Channel to Channel Isolation [1]



Dual Channel: LO1 to LO2 Isolation [2]



Noise Figure vs. Temperature



[1] For 900 MHz, RF1 = 900 MHz @ 0 dBm, RF2 = 901 MHz @ 0 dBm, LO = 800 MHz @ 0 dBm, IF2 terminated with 50 Ohms. Channel isolation is the dBc difference at IF1 port between the fundamental tone @ 100 MHz and the leakage tone @ 101 MHz.

[2] For 900 MHz, LO1 = 800 MHz @ 0 dBm, LO2 = 799 MHz @ 0 dBm, LO1 is selected, RF1 = RF2 = 900 MHZ @ 0 dBm, IF2 terminated with 50 Ohms. LO1-LO2 isolation is the dBc difference measured at the IF1 port between the fundamental tone at 100 MHz and the leakage tone @ 101 MHz.

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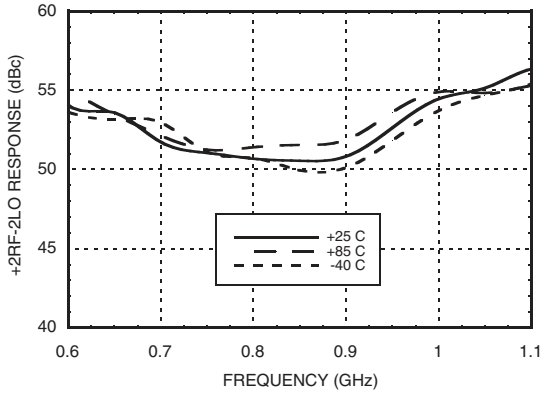
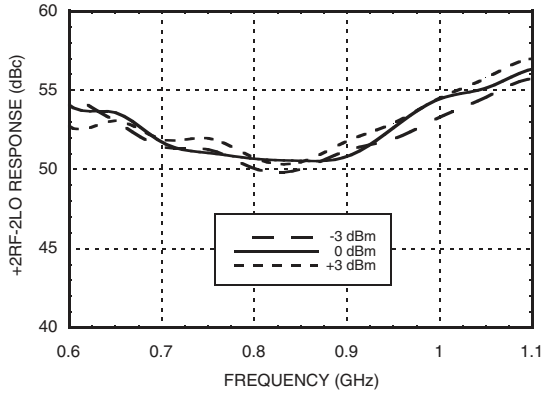
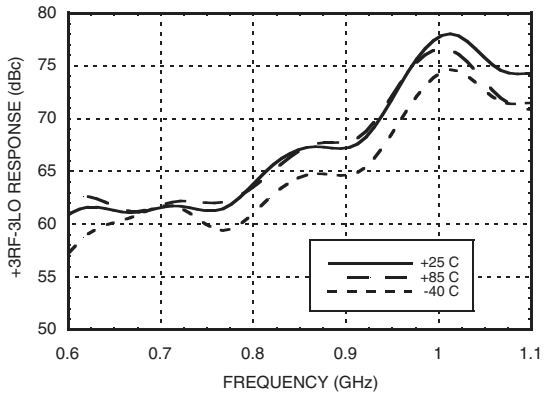
+2RF -2LO Response vs. Temperature [3]



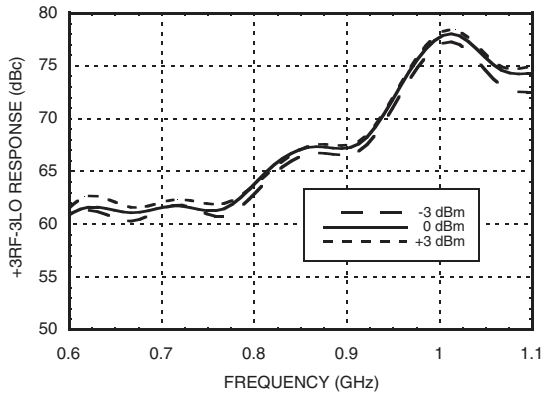
+2RF -2LO Response vs. LO Drive [3]



+3RF -3LO Response vs. Temperature [3]



+3RF -3LO Response vs. LO Drive [3]



[1] Referenced to RF Input Power @ 0 dBm

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MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	23	16	22	28
1	34	0	38	16	45
2	55	50	56	59	82
3	88	57	82	63	88
4	93	94	92	94	94

RF Freq. = 0.9 GHz @ -5 dBm
LO Freq. = 0.8 GHz @ 0 dBm
All values in dBc below IF power level (1RF - 1LO).

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
0.6	17	33	36	37
0.7	15	25	34	39
0.8	17	24	33	30
0.9	20	26	35	25
1.0	21	28	41	54
1.1	23	29	53	57

LO = 0 dBm
All values in dBc below input LO level measured at RF port.

Typical Supply Current vs. Vcc

Vcc	Icc (A)
4.75	390
5.00	420
5.25	450

Downconverter will operate over full voltage range shown above.

Truth Table

LO_SEL (V)	LO Signal Path
0	LO1
5	LO2

Absolute Maximum Ratings

RF / IF Input (Vcc= +5V)	+15 dBm
LO Drive (Vcc= +5V)	+6 dBm
Vcc (LO or IF)	5.5V
Channel Temperature	12.5°C
Continuous Pdiss (T = 85°C) (derate 110.53 mW/°C above 85°C)	4.42 W
Thermal Resistance (channel to ground paddle)	9.05 °C/W
Storage Temperature	-65 to 150°C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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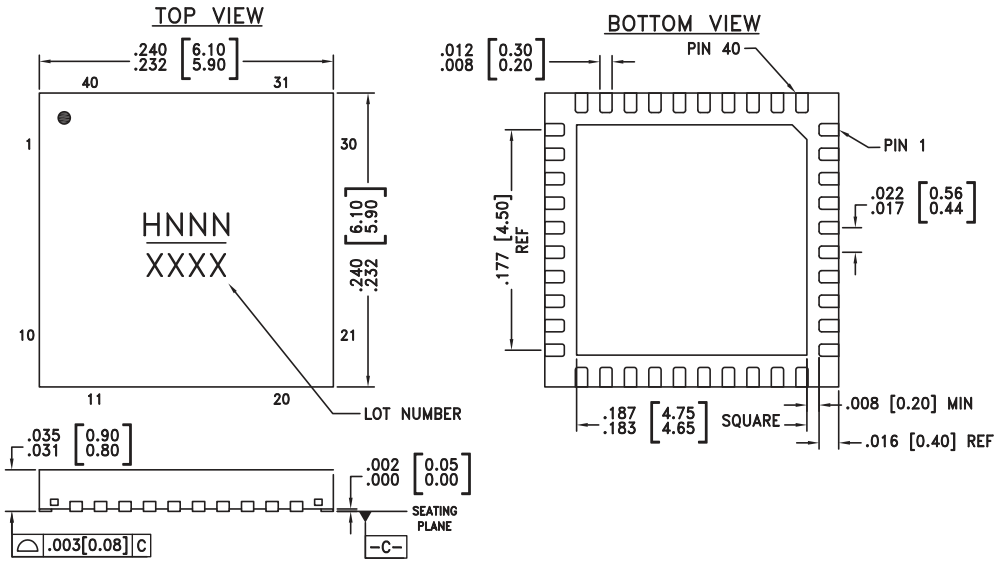
Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC683LP6C	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H683 XXXX
HMC683LP6CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H683 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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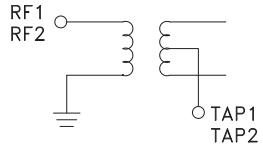
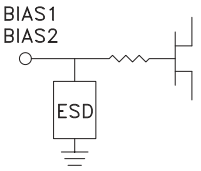
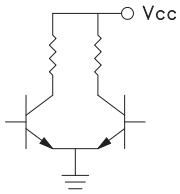
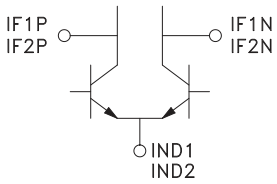
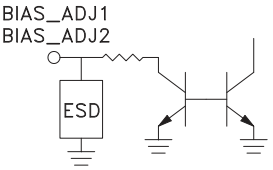
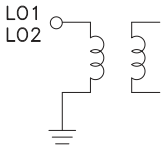
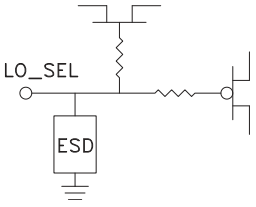
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 10	RF1, RF2	These are the RF inputs of the mixers. See application circuit for the off-chip matching components	
2, 9	TAP1, TAP2	These are the center taps of the internal RF baluns. Connect these pins to the AC ground via external capacitors. See application circuit.	
3, 5, 8, 15, 16, 22, 23, 26 - 29, 35, 36	GND	These pins must be connected to RF ground.	
4, 7	BIAS1, BIAS2	Bias pins for mixer cores. See application circuit for the nominal value.	
6, 17, 18, 24, 33, 34	Vcc1, Vcc_BAL2, Vcc_AMP2, Vcc2, Vcc_AMP1, Vcc_BAL1	Power supply voltage pins. See application circuit for bypass capacitors required.	
11, 20, 31, 40	N/C	No Connection required. These pins may be connected to RF GND without affecting performance.	
12, 39	IND1, IND2	Current source inductors for IF amplifiers.	
13, 14, 38, 37	IF2P, IF2N, IF1P, IF1N	Differential IF outputs and DC bias for IF amplifiers.	
19, 32	BIAS_ADJ1, BIAS_ADJ2	Adjusts LO buffer amplifies current via external resistor. See application circuit.	
21, 30	LO2, LO1	These are LO inputs of the mixers. See application circuit for off-chip matching components.	
25	LO_SEL	Control voltage for LO1 or LO2 selection. LO1 is selected when LO SEL is set low. LO2 is selected when LO SEL is set high. See application circuit and truth table for low and high voltage levels.	

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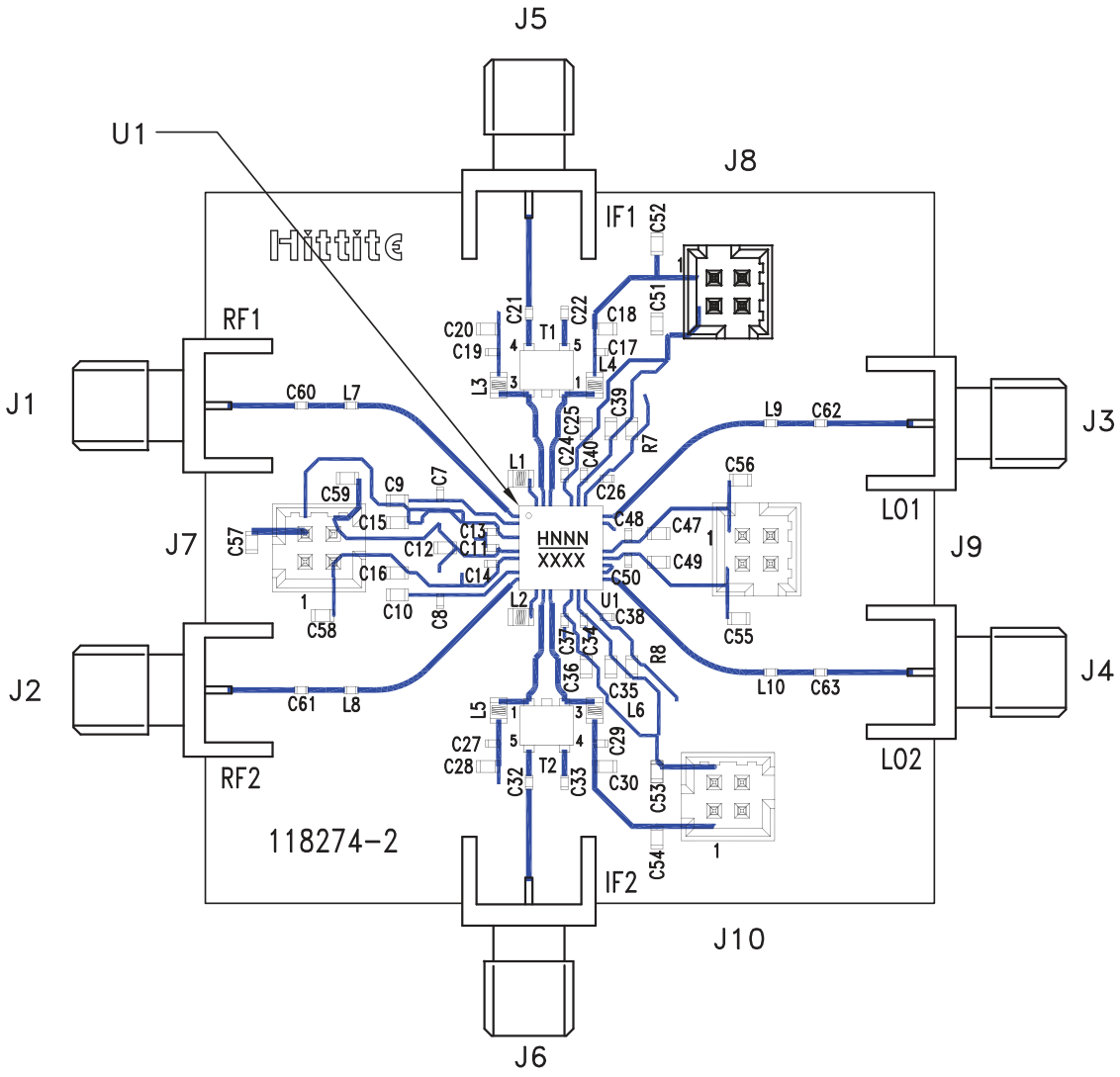
Evaluation PCB



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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List of Materials for Evaluation PCB 119926 [1]

Item	Description
J1 - J6	PCB Mount SMA Connector
J7 - J10	2mm Vertical Molex 8pc Connector
L1, L2	51 nH Inductor, 0603 Pkg.
L3 - L6	390 nH Inductor, 0603 Pkg.
L7, L8	5.1 nH Inductor, 0402 Pkg.
L9, L10	3.6 nH Inductor, 0402 Pkg.
C7, C8, C26, C38	22 pF Capacitor, 0402 Pkg.
C9, C10	10 nF Capacitor, 0603 Pkg.
C11, C17, C19, C24, C27, C29, C34, C37, C40, C48, C50	1 nF Capacitor, 0402 Pkg.
C12, C15, C16, C18, C20, C25, C28, C30, C35, C36, C39, C47, C49	0.1 µF Capacitor, 0603 Pkg.
C13, C14, C60 - C63	100 pF Capacitor, 0402 Pkg.
C21, C22, C32, C33	0.01 µF Capacitor, 0402 Pkg.
C51 - C59	0.47 µF Capacitor, 0603 Pkg.
R7, R8	330 Ohm Resistor, 0603 Pkg.
T1, T2	1:1 Transformer - Tyco ETC1-IT
U1	HMC683LP6C(E)
PCB [2]	118274 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon-25FR adn FR4

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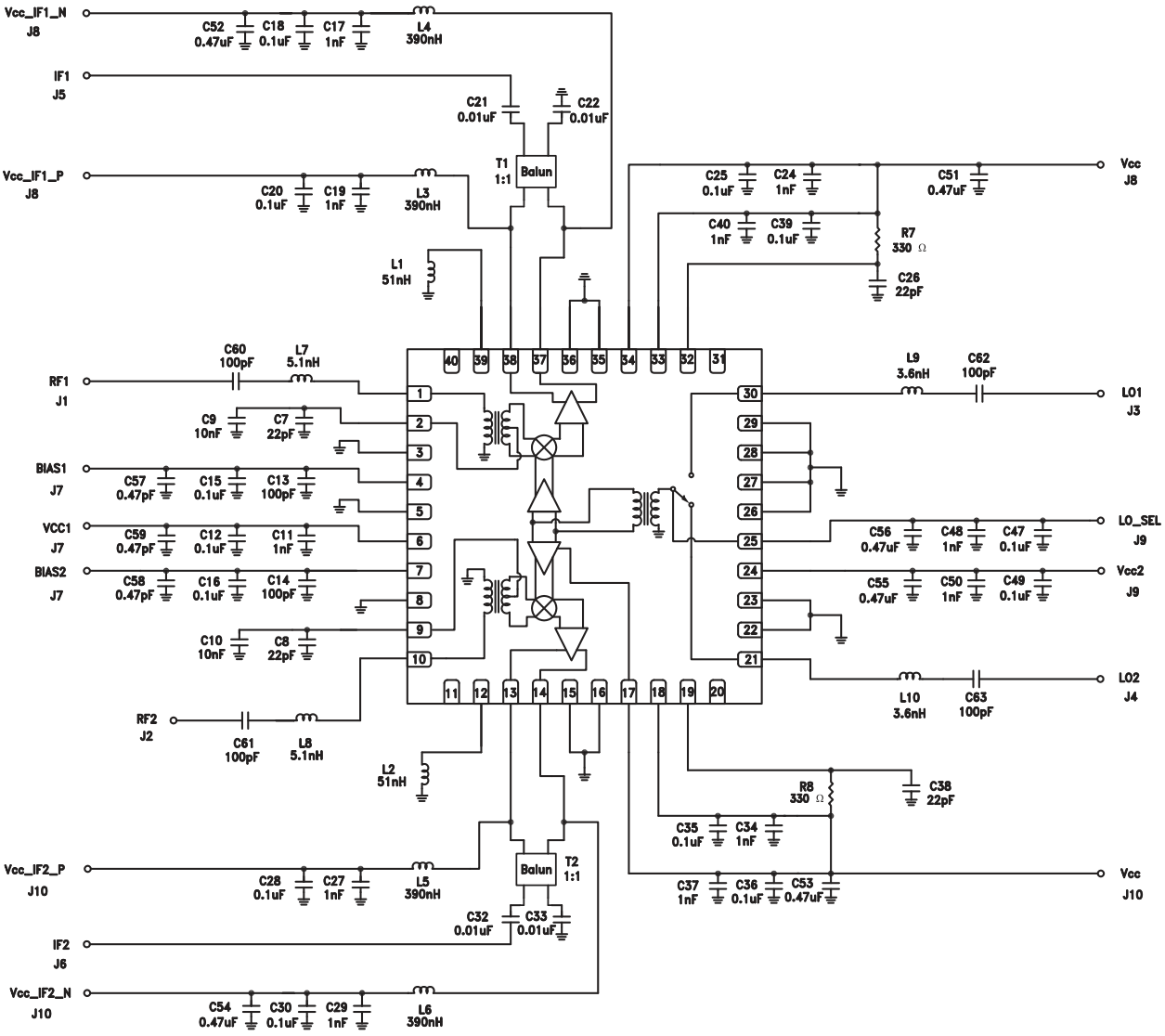
Application Circuit



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