

EC2x&EG25-G&UC20

Compatible Design

UMTS/HSPA+/LTE Module Series

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About the Document

History

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1.1	2019-01-03	Lorry XU	<ol style="list-style-type: none">1. Added EG25-G in the compatible design2. Updated Figure 1 and 153. Updated Table 1, 2, 3, 6 and 84. Updated description of Chapter 4 and 5

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1 Introduction

Quectel LTE EC2x module (contains EC25, EC21, EC20, EC20 R2.0 and EC20 R2.1) and EG25-G module are compatible with UMTS/HSPA+ UC20 module. This document briefly describes the compatible design among EC2x, EG25-G and UC20, which can help customers easily migrate from one to either of the others in their design and manufacturing.

2 General Descriptions

2.1. Product Description

EC25, EC21, EC20, EC20 R2.0, EC20 R2.1 and UC20 modules have some serial products. The following tables show the frequency bands and module general information.

Table 1: Module Frequency Bands

Module	LTE	UMTS	GSM	Rx-diversity	GNSS
EC25-E	FDD: B1/B3/B5/B7/B8/B20 TDD: B38/B40/B41	WCDMA: B1/B5/B8	900/1800MHz	Y	
EC25-EU	FDD: B1/B3/B7/B8/B20/ B28A TDD: B38/B40/B41	WCDMA: B1/B8	900/1800MHz	Y	
EC25-A	FDD: B2/B4/B12	WCDMA: B2/B4/B5		Y	
EC25-V	FDD: B4/B13			Y	GPS GLONASS
EC25-AF	FDD: B2/B4/B5/B12/B13/B14 /B66/B71	WCDMA: B2/B4/B5		Y	BeiDou Galileo QZSS
EC25-AU	FDD: B1/B2 ¹⁾ /B3/B4/B5/B7/ B8/B28 TDD: B40	WCDMA: B1/B2/B5/B8	850/900/ 1800/1900MHz	Y	
EC25-AUT	FDD: B1/B3/B5/B7/B28	WCDMA: B1/B5		Y	
EC25-J	FDD: B1/B3/B8/B18/B19/B26 TDD: B41	WCDMA: B1/B6/B8/B19		Y	
EC25-EC	FDD: B1/B3/B7/B8/B20/	WCDMA: B1/B8	900/1800MHz	Y	N

	B28A				
EC25-AUTL	FDD: B3/B7/B28			Y	N
EC21-E	FDD: B1/B3/B5/B7/B8/B20	WCDMA: B1/B5/B8	900/1800MHz	Y	
EC21-EU	FDD: B1/B3/B7/B8/B20/ B28A	WCDMA: B1/B8	900/1800MHz	Y	
EC21-A	FDD: B2/B4/B12	WCDMA: B2/B4/B5		Y	GPS GLONASS
EC21-V	FDD: B4/B13			Y	BeiDou Galileo
EC21-AU	FDD: B1/B2 ¹⁾ / B3/B4/B5/B7/ B8/B28 TDD: B40	WCDMA: B1/B2/B5/B8	850/900/ 1800/1900MHz	Y	QZSS
EC21-AUT	FDD: B1/B3/B5/B7/B28	WCDMA: B1/B5		Y	
EC21-EC	FDD: B1/B3/B7/B8/B20/ B28A	WCDMA: B1/B8	900/1800MHz	Y	N
EC21-AUV	FDD: B1/B3/B5/B8/B28	WCDMA: B1/B5/B8		Y	N
EC21-J	FDD: B1/B3/B8/B18/B19/B26				N
EC21-KL	FDD: B1/B3/B5/B7/B8				N
EC20-C R2.0	FDD: B1/B3/B8 TDD: B38/B39/B40/B41	WCDMA: B1/B8 TD-SCDMA: B34/B39	900/1800MHz	Y	
EC20-CE R2.0	FDD: B1/B3/B8 TDD: B38/B39/B40/B41	WCDMA: B1/B8 TD-SCDMA: B34/B39 CDMA: BC0	900/1800MHz	Y	GPS GLONASS BeiDou Galileo QZSS
EC20-CE R2.1	FDD: B1/B3/B5/B8 TDD: B38/B39/B40/B41	WCDMA: B1/B8 TD-SCDMA: B34/B39 CDMA: BC0	900/1800MHz	Y	
EC20-C	FDD: B1/B3/B8 TDD: B38/B39/B40/B41	WCDMA: B1/B8 TD-SCDMA: B34/B39	900/1800MHz	Y	GPS
EC20-CE	FDD: B1/B3 TDD: B38/B39/B40/B41	WCDMA: B1 TD-SCDMA: B34/B39	900/1800MHz	Y	GLONASS



CDMA: BC0					
EC20-A	FDD: B2/B4/B5/B12/B17	WCDMA: B2/B4/B5	850/1900MHz	Y	
EC20-E	FDD: B1/B3/B5/B7/B8/B20	WCDMA: B1/B5/B8	850/900/ 1800/1900MHz	Y	
EG25-G	FDD: B1/B2/B3/B4/B5/B7/ B8/B12/B13/B18/B19/B 20/B25/B26/B28 TDD: B38/B39/B40/B41	WCDMA: B1/B2/B4/B5/B6/B 8/B19	850/900/ 1800/1900MHz	Y	GPS GLONASS BeiDou Galileo QZSS
UC20-A		WCDMA: B2/B5		Y	
UC20-E		WCDMA: B1/B8	850/900/ 1800/1900MHz	Y	GPS GLONASS
UC20-G		WCDMA: B1/B2/B5/B6/B8	850/900/ 1800/1900MHz	Y	

NOTES

- Y = supported (including LTE and UMTS)
- ¹⁾ B2 band on EC21-AU/EC25-AU module does not support Rx-diversity.

Table 2: Module General Information

Module Name	Picture	Packaging	Dimensions	Description
EG25-G		144 LGA pads	29mm × 32mm × 2.4mm	LTE module
EC25		80 LCC pads + 64 LGA pads	29mm × 32mm × 2.4mm	LTE module (EC25-E, EC25-EU, EC25-EC, EC25-A, EC25-V, EC25-AF, EC25-AU, EC25-AUT, EC25-AUTL and EC25-J)
EC21		80 LCC pads + 64 LGA pads	29mm × 32mm × 2.4mm	LTE module (EC21-E, EC21-EU, EC21-EC, EC21-A, EC21-V, EC21-AU, EC21-AUT, EC21-AUV, EC21-J and EC21-KL)

EC20 R2.0		80 LCC pads + 64 LGA pads	29mm × 32mm × 2.4mm	LTE module (EC20-C R2.0 and EC20-CE R2.0)
EC20 R2.1		80 LCC pads + 64 LGA pads	29mm × 32mm × 2.4mm	LTE module (EC20-CE R2.1)
EC20		76 LCC pads + 64 LGA pads	29mm × 32mm × 2.4mm	LTE module (EC20-C, EC20-CE, EC20-A and EC20-E)
UC20		72 LCC pads + 40 LGA pads	29mm × 32mm × 2.5mm	UMTS/HSPA+ module (UC20-A, UC20-E and UC20-G)

2.2. Feature Overview

The following table compares the general features of EC2x, EG25-G and UC20.

Table 3: Feature Overview

Feature	UC20	EC20	EC25/EC21/EC20 R2.0/ EC20 R2.1/EG25-G
Power Supply	3.3V~4.3V, Typ.=3.8V	3.3V~4.3V, Typ.=3.8V	3.3V~4.3V, Typ.=3.8V
Peak Current	VBAT_BB&RF: max 2.0A	VBAT_BB&RF: max 2.0A	VBAT_BB&RF: max 2.0A < 4mA.
Sleep Current (USB Suspended)	2G: 3.7mA @DRX=2 3G: 3.0mA @DRX=6	2G: 3.7mA @DRX=2 3G: 3.0mA @DRX=6	For details, please refer to the Hardware Design document of these modules respectively.
LTE Features		Support 3GPP R9 Cat 3 FDD: Max 100Mbps (DL), Max 50Mbps (UL) TDD: Max 61Mbps (DL), Max 18Mbps (UL)	EC25/EC20 R2.0/ EC20 R2.1/EG25-G: Support up to LTE Cat 4. FDD: Max 150Mbps (DL), Max 50Mbps (UL) EC21:

			Support up to LTE Cat 1. FDD: Max 10Mbps (DL), Max 5Mbps (UL)
Temperature Range	Operating temperature range: -35°C ~ +75°C ¹⁾ Extended temperature range: -40°C ~ +85°C ²⁾ Storage temperature range: -40°C ~ +90°C	Operating temperature range: -35°C ~ +75°C ¹⁾ Extended temperature range: -40°C ~ +85°C ²⁾ Storage temperature range: -40°C ~ +90°C	Operating temperature range: -35°C ~ +75°C ¹⁾ Extended temperature range: -40°C ~ +85°C ²⁾ Storage temperature range: -40°C ~ +90°C
UART Interface	Baud rate: reach up to 921600bps Flow control: RTS/CTS	Baud rate: reach up to 921600bps Flow control: RTS/CTS	Baud rate: reach up to 921600bps Flow control: RTS/CTS
USB Interface	USB 2.0 HS (Slave only)	USB 2.0 HS (Slave only)	USB 2.0 HS (Slave only)
Digital Audio	PCM interface	PCM interface	PCM interface
I2C Interface	Supported	Supported	Supported
(U)SIM Detection	YES	YES	YES
GNSS	GPS+GLONASS	GPS+GLONASS	GPS, GLONASS, BeiDou, Galileo, QZSS
Firmware Upgrade	USB interface and DFOTA*	USB interface and DFOTA*	USB interface and DFOTA*

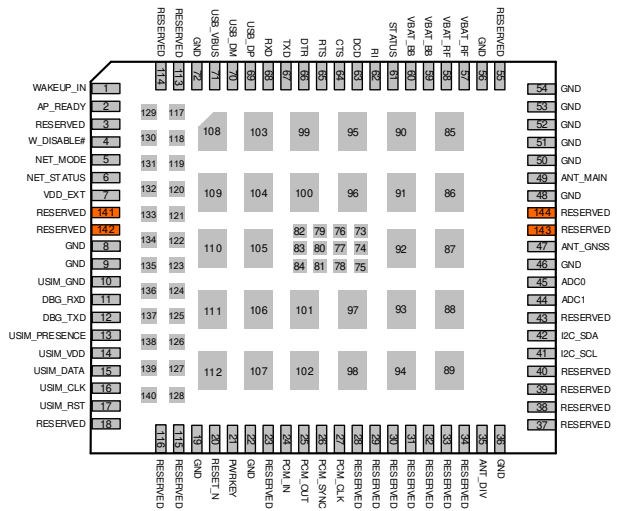
NOTES

- ¹⁾ Within operating temperature range, the module is 3GPP compliant.
- ²⁾ Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction; there are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module is compliant with 3GPP specification again.
- ³⁾ means under development.

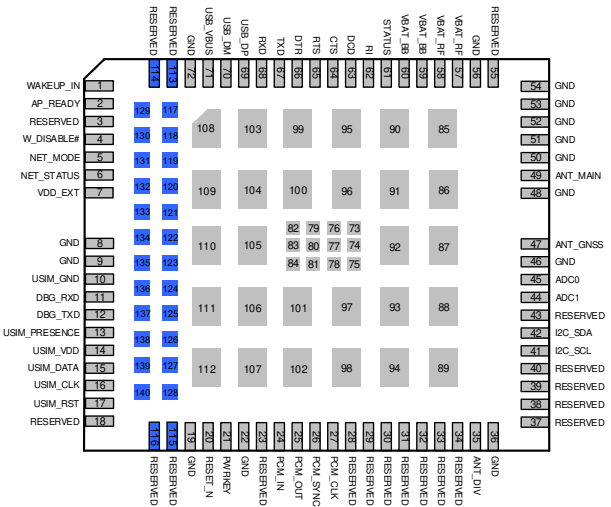
2.3. Pin Assignment

The following figures show the pin assignment of EC2x, EG25-G and UC20.

EC25/EC21/EC20 R2.0/EC20 R2.1/EG25-G Top View



EC20 Top View



UC20 Top View

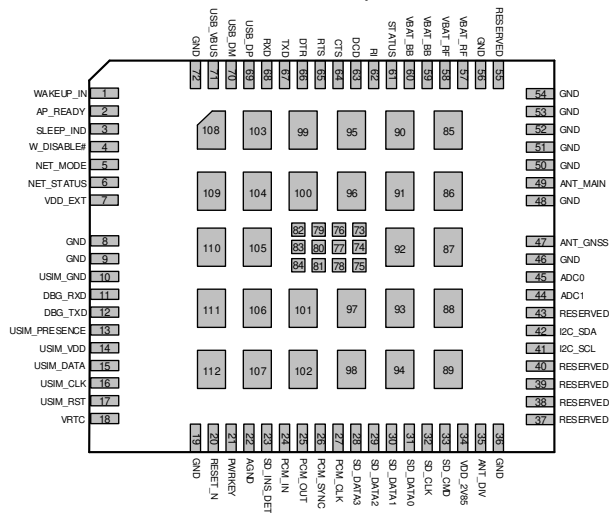


Figure 1: EC2x&EG25-G&UC20 Pin Assignment

NOTES

1. The orange pins are the additional pins of EC25/EC21/EC20 R2.0/EC20 R2.1/EG25-G as compared with EC20.
2. The blue pins are the additional pins of EC20 as compared with UC20.

3 Pin Description

This chapter describes the pin definition of EC2x, EG25-G and UC20.

Table 4: I/O Parameters Definition

Symbol	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

3.1. Common Pins

The following table shows EC2x, EG25-G and UC20's common pins with the same function.

Table 5: Common Pins

EC2x/EG25-G				UC20			
Pin No.	Pin Name	I/O	Power Domain	Pin No.	Pin Name	I/O	Power Domain
1	WAKEUP_IN	DI	1.8V	1	WAKEUP_IN	DI	1.8V
2	AP_READY	DI	1.8V	2	AP_READY	DI	1.8V

4	W_DISABLE#	DI	1.8V	4	W_DISABLE#	DI	1.8V
5	NET_MODE	DO	1.8V	5	NET_MODE	DO	1.8V
6	NET_STATUS	DO	1.8V	6	NET_STATUS	DO	1.8V
7	VDD_EXT	PO	1.8V	7	VDD_EXT	PO	1.8V
8	GND	-	Ground	8	GND	-	Ground
9	GND	-	Ground	9	GND	-	Ground
10	USIM_GND	-	Ground	10	USIM_GND	-	Ground
11	DBG_RXD	DI	1.8V	11	DBG_RXD	DI	1.8V
12	DBG_TXD	DO	1.8V	12	DBG_TXD	DO	1.8V
13	USIM_PRESENCE	DI	1.8V	13	USIM_PRESENCE	DI	1.8V
14	USIM_VDD	PO	1.8V/3.0V	14	USIM_VDD	PO	1.8V/3.0V
15	USIM_DATA	IO	1.8V/3.0V	15	USIM_DATA	IO	1.8V/3.0V
16	USIM_CLK	DO	1.8V/3.0V	16	USIM_CLK	DO	1.8V/3.0V
17	USIM_RST	DO	1.8V/3.0V	17	USIM_RST	DO	1.8V/3.0V
19	GND	-	Ground	19	GND	-	Ground
20	RESET_N	DI	1.8V	20	RESET_N	DI	1.8V
21	PWRKEY	DI	1.8V	21	PWRKEY	DI	1.8V
22	GND	-	Ground	22	AGND	-	Ground
23	RESERVED	-	-	23	RESERVED	-	-
24	PCM_IN	DI	1.8V	24	PCM_IN	DI	1.8V
25	PCM_OUT	DO	1.8V	25	PCM_OUT	DO	1.8V
26	PCM_SYNC	IO	1.8V	26	PCM_SYNC	IO	1.8V
27	PCM_CLK	IO	1.8V	27	PCM_CLK	IO	1.8V
28	RESERVED	-	-	28	RESERVED	-	-
29	RESERVED	-	-	29	RESERVED	-	-
30	RESERVED	-	-	30	RESERVED	-	-

31	RESERVED	-	-	31	RESERVED	-	-
32	RESERVED	-	-	32	RESERVED	-	-
33	RESERVED	-	-	33	RESERVED	-	-
34	RESERVED	-	-	34	RESERVED	-	-
35	ANT_DIV	AI	-	35	ANT_DIV	AI	-
36	GND	-	Ground	36	GND	-	Ground
37	RESERVED	-	-	37	RESERVED	-	-
38	RESERVED	-	-	38	RESERVED	-	-
39	RESERVED	-	-	39	RESERVED	-	-
40	RESERVED	-	-	40	RESERVED	-	-
41	I2C_SCL	OD	1.8V only	41	I2C_SCL	OD	1.8V only
42	I2C_SDA	OD	1.8V only	42	I2C_SDA	OD	1.8V only
43	RESERVED	-	-	43	RESERVED	-	-
44	ADC1	AI	0.3V~ VBAT_BB	44	ADC1	AI	0.2V~4.2V
45	ADC0	AI	0.3V~ VBAT_BB	45	ADC0	AI	0.2V~2.1V
46	GND	-	Ground	46	GND	-	Ground
47	ANT_GNSS	AI	-	47	ANT_GNSS	AI	-
48	GND	-	Ground	48	GND	-	Ground
49	ANT_MAIN	IO	-	49	ANT_MAIN	IO	-
50	GND	-	Ground	50	GND	-	Ground
51	GND	-	Ground	51	GND	-	Ground
52	GND	-	Ground	52	GND	-	Ground
53	GND	-	Ground	53	GND	-	Ground
54	GND	-	Ground	54	GND	-	Ground
55	RESERVED	-	-	55	RESERVED	-	-
56	GND	-	Ground	56	GND	-	Ground

57	VBAT_RF	PI	3.3V~4.3V	57	VBAT_RF	PI	3.3V~4.3V
58	VBAT_RF	PI	3.3V~4.3V	58	VBAT_RF	PI	3.3V~4.3V
59	VBAT_BB	PI	3.3V~4.3V	59	VBAT_BB	PI	3.3V~4.3V
60	VBAT_BB	PI	3.3V~4.3V	60	VBAT_BB	PI	3.3V~4.3V
61	STATUS	OD	-	61	STATUS	OD	-
62	RI	DO	1.8V	62	RI	DO	1.8V
63	DCD	DO	1.8V	63	DCD	DO	1.8V
64	CTS	DO	1.8V	64	CTS	DO	1.8V
65	RTS	DI	1.8V	65	RTS	DI	1.8V
66	DTR	DO	1.8V	66	DTR	DI	1.8V
67	TXD	DI	1.8V	67	TXD	DO	1.8V
68	RXD	DI	1.8V	68	RXD	DI	1.8V
69	USB_DP	IO	-	69	USB_DP	IO	-
70	USB_DM	IO	-	70	USB_DM	IO	-
71	USB_VBUS	PI	Typ. 5V	71	USB_VBUS	PI	Typ. 5V
72	GND	-	Ground	72	GND	-	Ground
73~84	RESERVED	-	-	73~84	RESERVED	-	-
85~112	GND	-	Ground	85~112	GND	-	Ground

3.2. Different Pins

The following table shows the different functional pins of EC2x, EG25-G and UC20.

Table 6: Different Functional Pins among EC2x, EG25-G and UC20

EC2x/EG25-G				UC20			
Pin No.	Pin Name	I/O	Power Domain	Pin No.	Pin Name	I/O	Power Domain
3	RESERVED	-	-	3	SLEEP_IND	DO	1.8V
18	RESERVED	-	-	18	VRTC	IO	1.5V~3.25V
113, 114, 116	RESERVED	-	-	-	-	-	-
115	EC25/EC21/ EC20R2.0/ EC20 R2.1/ EG25-G: USB_BOOT EC20: RESERVED	-	-	-	-	-	-
117~140	EC25/EC21/ EC20R2.0/ EC20 R2.1/ EG25-G: Wi-Fi&BT& SGMII EC20: RESERVED	-	-	-	-	-	-

The following table shows the additional pins of EC25/EC21/EC20 R2.0/EC20 R2.1/EG25-G as compared with EC20.

Table 7: Additional Pins of EC25/EC21/EC20 R2.0/EC20 R2.1/EG25-G as Compared with EC20

PIN No.	Pin Name	I/O	Pin Description
141~144	RESERVED	-	-

NOTES

1. Keep all reserved and unused pins unconnected.
2. All GND pins should be connected to ground.
3. Detail definition of pin 117~140, please refer to EC25/EC21/EC20 R2.0/EC20 R2.1 and EG25-G Hardware Design document respectively.

4 Hardware Reference Design

4.1. Power Supply

The power supply range of EC2x, EG25-G and UC20 is from 3.3V to 4.3V. Attention should be paid to the range of power source to make sure that the input voltage will never drop below 3.3V or exceed 4.3V. The typical power supply is 3.8V. The following figure shows a reference design for a 5V input power source. The designed output for the power supply is 3.88V and the maximum load current is 3A. The VBAT_BB and VBAT_RF pins should be divided into two separated paths in star structure.

In addition, in order to avoid the damage caused by electric surge and ESD, it is suggested that a TVS diode with low reverse stand-off voltage V_{RWM} , low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figures show a reference design for +5V input power source and the star structure of the power supply.

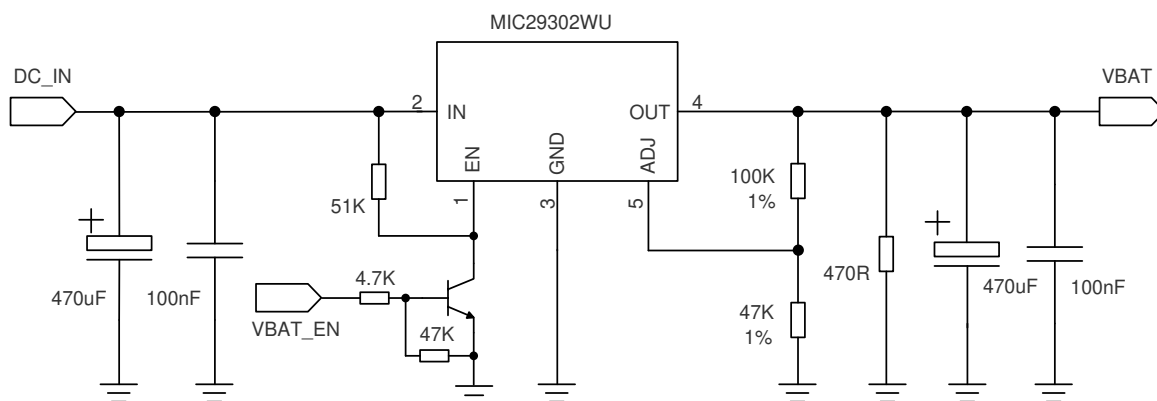


Figure 2: Reference Circuit of Power Supply

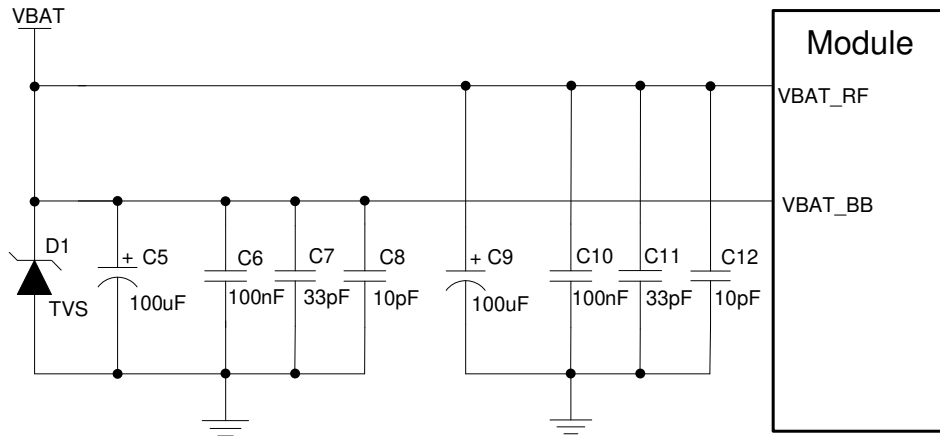


Figure 3: Star Structure of the Power Supply

4.2. Power-on and off Circuit

The following is a reference design for EC2x, EG25-G and UC20's power-on and off circuit.

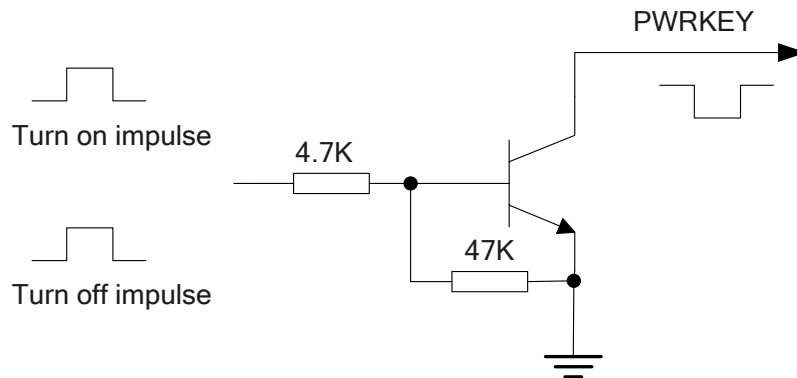


Figure 4: Turn on and off the Module Using Driving Circuit

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to **document [14]** for details about **AT+QPOWD** command.

4.3. Reset Circuit

When it is failed to turn off the module by both command **AT+QPOWD** and PWRKEY pin, the RESET_N can be used to reset the module. The following is a reference design for EC2x, EG25-G and UC20's reset circuit.

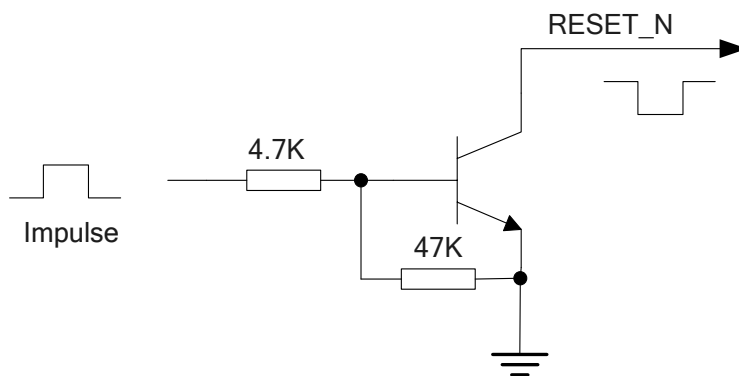


Figure 5: Reset the Module Using Driving Circuit

4.4. (U)SIM Interface

The (U)SIM interface of EC2x, EG25-G and UC20 circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported. The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector

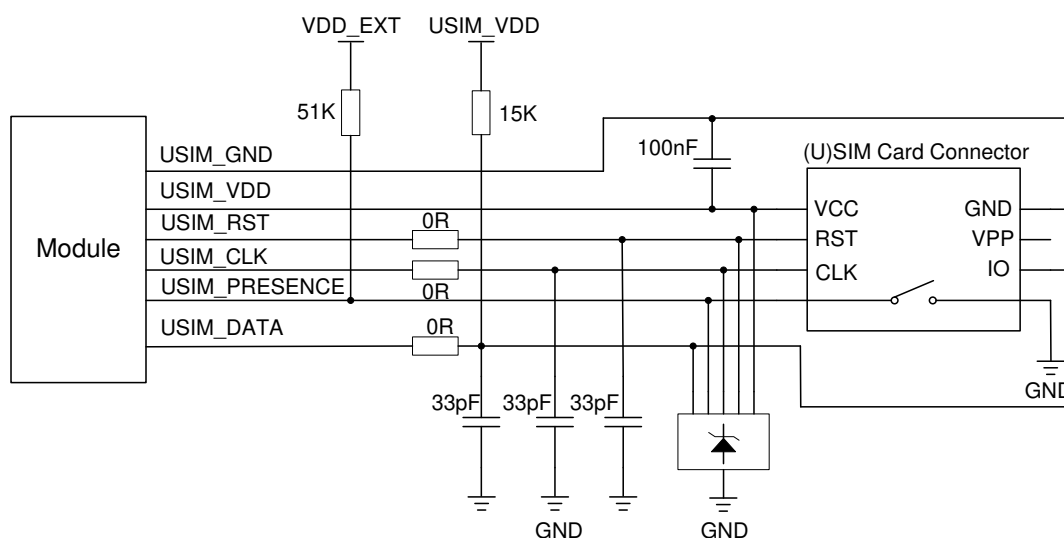


Figure 6: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

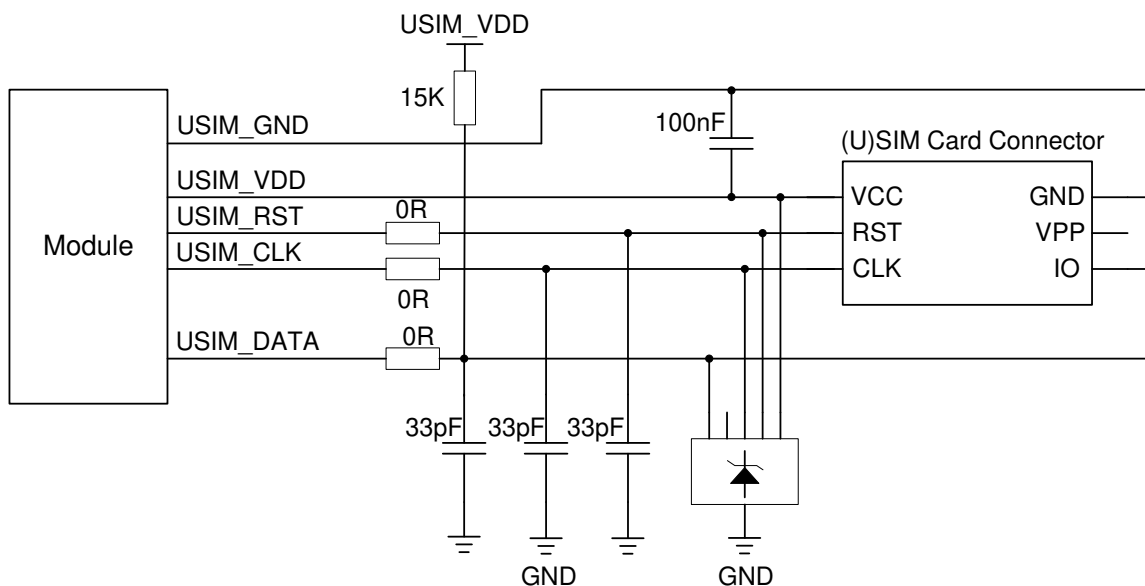


Figure 7: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

4.5. USB Interface

EC2x, EG25-G and UC20 contain one integrated Universal Serial Bus (USB) interface which complies with USB 2.0 specification, supports high-speed (480Mbps) and full-speed (12Mbps) modes; UC20 additionally supports low-speed (1.5Mbps) mode. The USB interface can be used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade.

The USB interface is recommended to be reserved for firmware upgrade in customers' design. The following figure shows the reference circuit of USB interface.

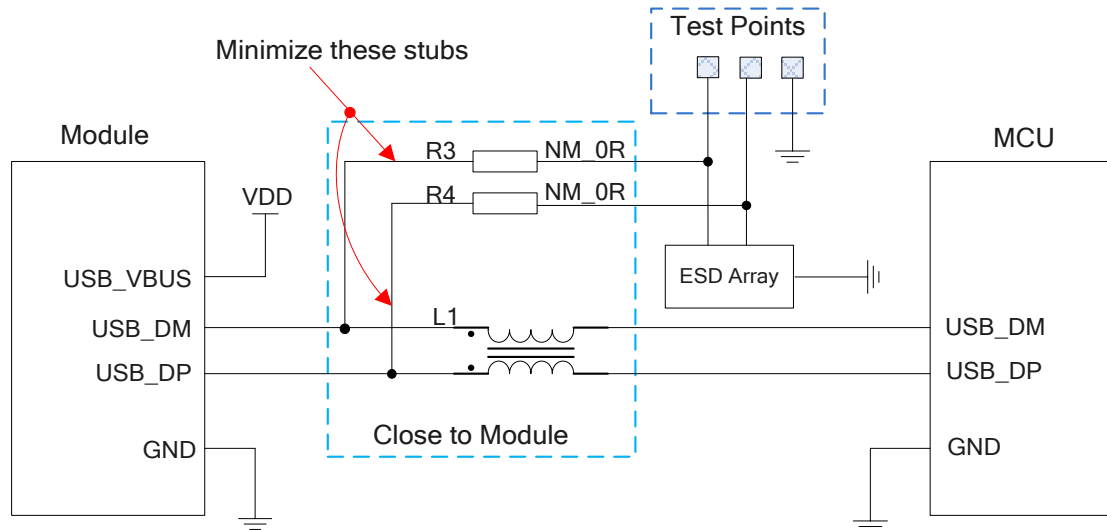


Figure 8: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

NOTE

EC2x, EG25-G and UC20 modules can only be used as a USB device.

4.6. PCM Interface

EC2x, EG25-G and UC20 support one PCM interface used for audio applications with the same feature. The following figure shows a reference design of PCM interface with external codec IC.

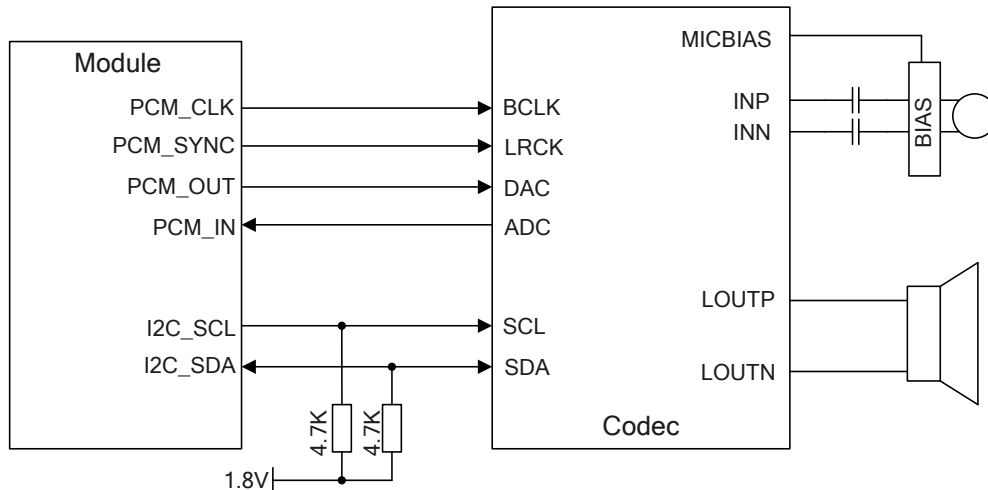


Figure 9: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve the RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. EC2x, EG25-G and UC20 modules work as master device pertaining to I2C interface.

4.7. UART Interface

EC2x, EG25-G and UC20 support a main UART and a debug UART interface. The main UART interface can be used for data transmission, AT command communication and firmware upgrade; the debug UART interface can be used for GNSS NMEA sentences output.

EC2x, EG25-G and UC20 provide 1.8V UART interface. A level translator should be used if customers' application is equipped with a 3.3V UART interface. Level translator TXS0108EPWR provided by *Texas Instrument* is recommended. The following figure shows a reference design.

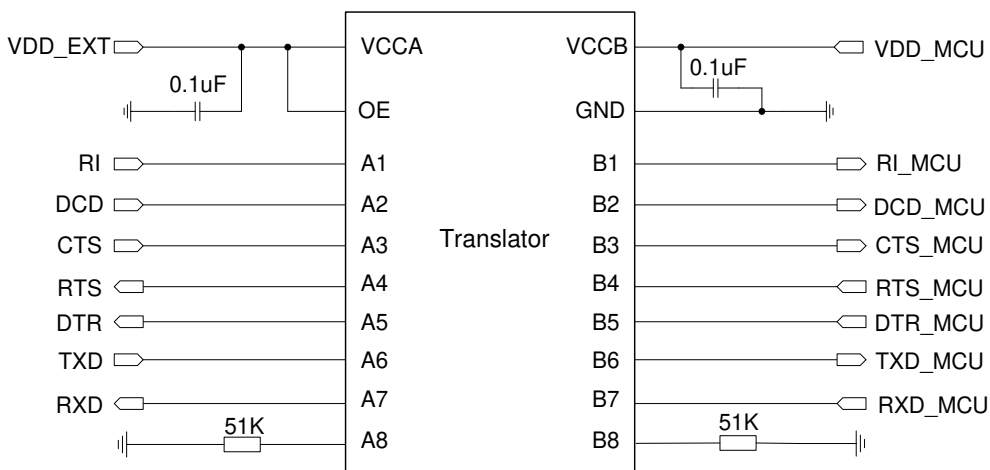


Figure 10: Reference Circuit with Level Translator Chip

Please visit <http://www.ti.com> for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module's input and output circuit designs; but please pay attention to the direction of connection.

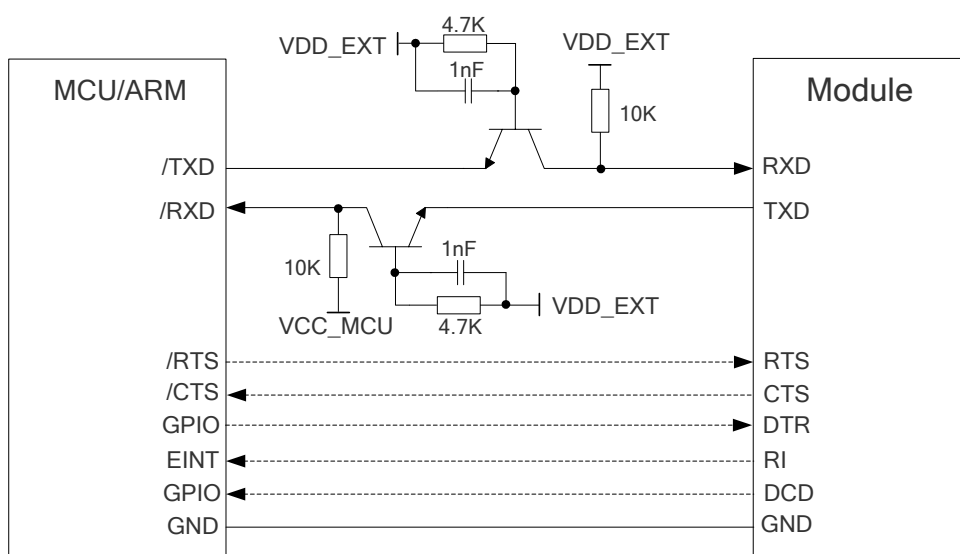


Figure 11: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rate exceeding 460Kbps.

4.8. Antenna Interfaces

EC2x, EG25-G and UC20 have the same antenna interfaces: ANT_MAIN, ANT_GNSS and ANT_DIV. For better RF performance, a π -type matching circuit should be reserved. The following figure shows a reference circuit.

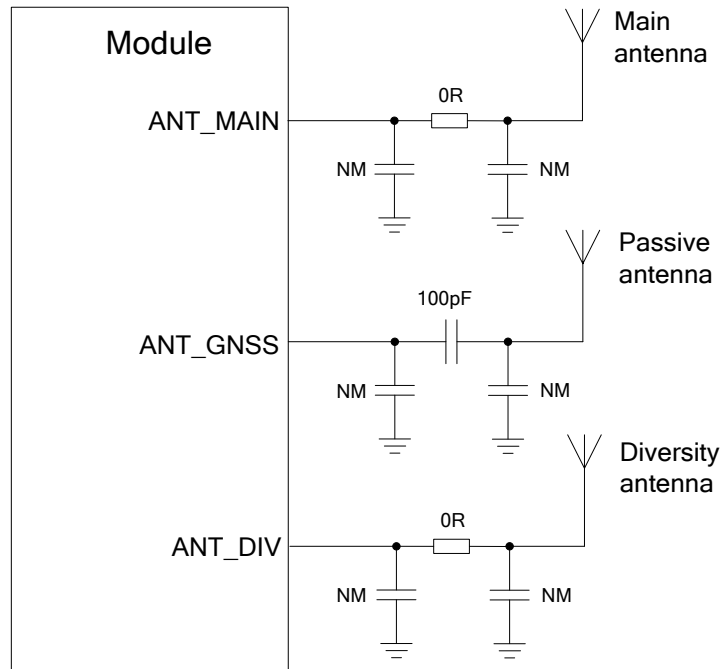


Figure 12: Reference Circuit of Antenna Interfaces

5 Recommended Footprint

The following figure shows the recommended compatible footprint of EC2x, EG25-G and UC20. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are $\pm 0.05\text{mm}$.

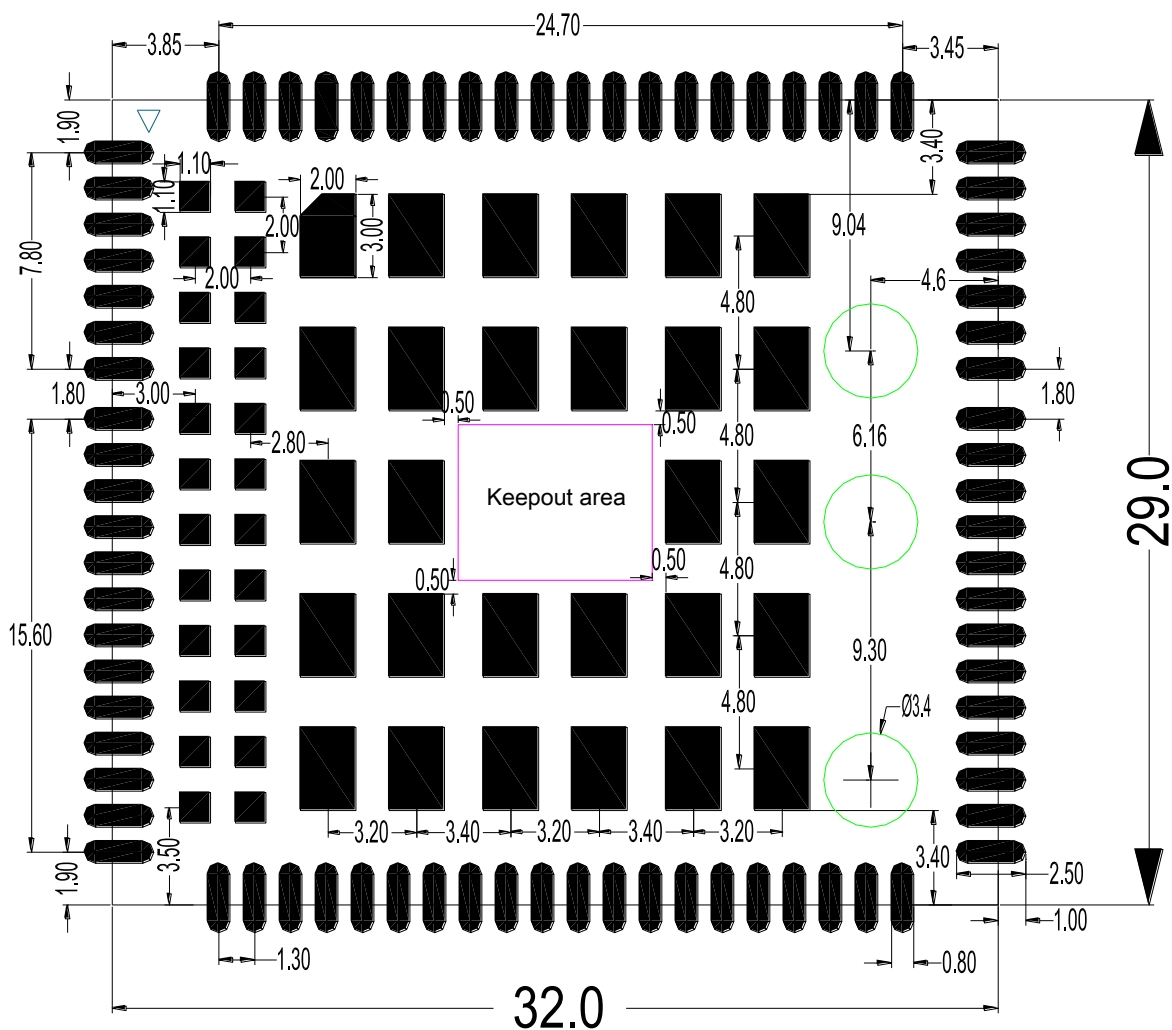


Figure 13: Recommended Compatible Footprint (Unit: mm)

If SGMII or Wi-Fi function is not needed, it is recommended to keep out the area for pins 117~140. The following figure shows the recommended compatible footprint without SGMII or Wi-Fi function.

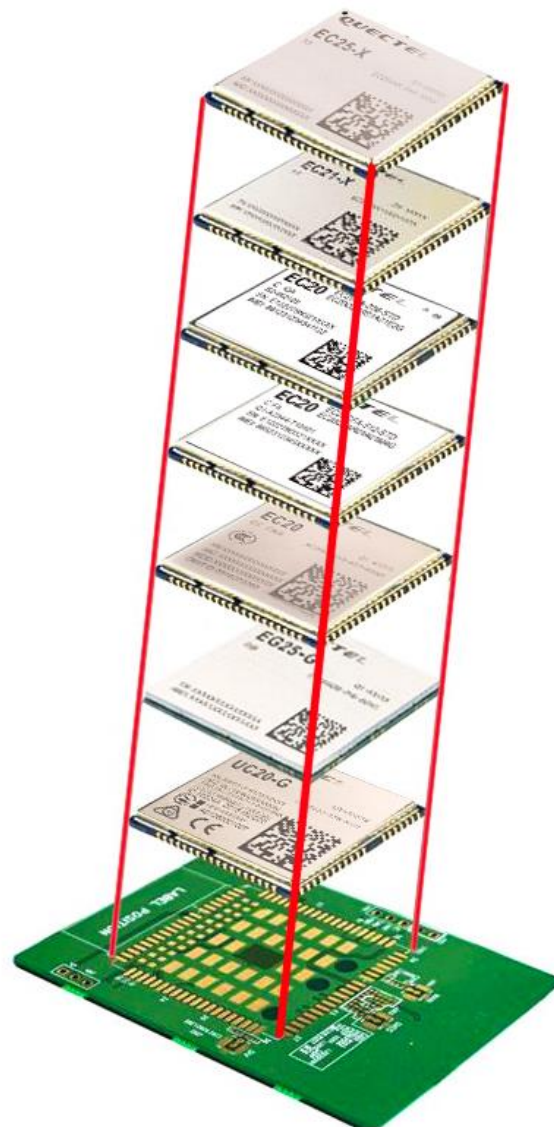


Figure 15: Installation Sketch Map for EC2x, EG25-G and UC20

6 Appendix References

Table 8: Related Documents

SN	Document Name	Remark
[1]	Quectel_UC20_Hardware_Design	UC20 Hardware Design
[2]	Quectel_EC20_Hardware_Design	EC20 Hardware Design
[3]	Quectel_EC25_Hardware_Design	EC25 Hardware Design
[4]	Quectel_EC20_R2.0_Hardware_Design	EC20 R2.0 Hardware Design
[5]	Quectel_EC20_R2.1_Hardware_Design	EC20 R2.1 Hardware Design
[6]	Quectel_UC20_Reference_Design	UC20 Reference Design
[7]	Quectel_EC20_Reference_Design	EC20 Reference Design
[8]	Quectel_EC25_Reference_Design	EC25 Reference Design
[9]	Quectel_EC20_R2.0_Reference_Design	EC20 R2.0 Reference Design
[10]	Quectel_EC20_R2.1_Reference_Design	EC20 R2.1 Reference Design
[11]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[12]	Quectel_EG25-G_Hardware_Design	EG25-G Hardware Design
[13]	Quectel_EG25-G_Reference_Design	EG25-G Reference Design
[14]	Quectel_EC25&EC21_AT_Commands_Manual	EC25&EC21 AT Commands Manual