ASM5P2308A

3.3 V Zero-Delay Buffer

Description

ASM5P2308A is a versatile, 3.3 V zero−delay buffer designed to distribute high−speed clocks. It is available in a 16−pin package. The part has an on−chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven to FBK pin, and can be obtained from one of the outputs. The input−to−output propagation delay is guaranteed to be less than ±250 pS, and the output−to−output skew is guaranteed to be less than 200 pS.

The ASM5P2308A has two banks of four outputs each, which can be controlled by the select inputs as shown in the *Select Input Decoding Table*. If all the output clocks are not required, Bank B can be three−stated. The select input also allows the input clock to be directly applied to the outputs for chip and system testing purposes.

Multiple ASM5P2308A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700 pS.

ASM5P2308A is available in five different configurations. Refer to *ASM5P2308A Configurations Table*. The ASM5P2308A−1 is the base part, where the output frequencies equal the reference clock input. The ASM5P2308A−1H is the high−drive version of the −1 and the rise and fall times on this device are faster.

ASM5P2308A−2 allows the user to obtain 2x and 1x frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin. ASM5P2308A−3 allows the user to obtain 4x and 2x frequencies on the outputs.

ASM5P2308A−4 enables the user to obtain 2x clocks on all outputs.

The ASM5P2308A−5H is a high−drive version with REF/2 output on both banks.

ASM5P2308A is an extremely versatile part, and can be used in a variety of applications.

Features

- Zero Input−output Propagation Delay, Adjustable by Capacitive Load on FBK Input
- Multiple Configurations –
  Refer to *ASM5P2308A Configurations Table*
- Input Frequency Range: 10 MHz to 133 MHz
- Multiple Low−skew Outputs
  - Output−output Skew less than 200 pS
  - Device−device Skew less than 700 pS
  - Two Banks of Four Outputs Each, Three−state by Two Select Inputs
- Less than 200 pS Cycle−to−Cycle Jitter (−1, −1H, −2, −3, −4, −5H)
- 16−pin SOIC and TSSOP Packages
- 3.3 V Operation
- Commercial and Industrial Temperature Range
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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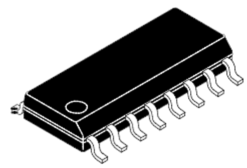
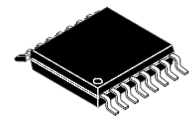
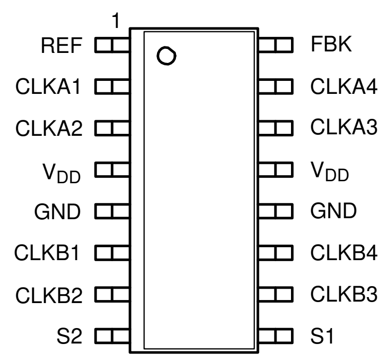


SOIC−16
S SUFFIX
CASE 751BG



TSSOP−16
T SUFFIX
CASE 948AN

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

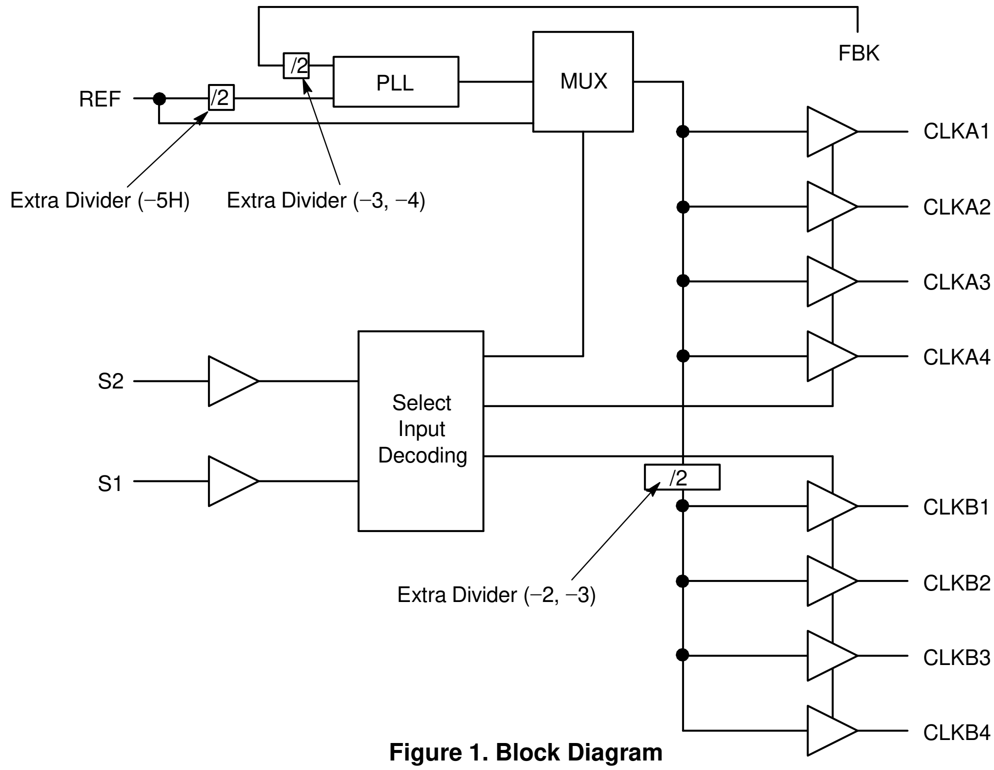


Figure 1. Block Diagram

Table 1. SELECT INPUT DECODING FOR ASM5P2308A

S2	S1	Clock A1 − A4	Clock B1 − B4	Output Source	PLL Shut−Down
0	0	Three−state	Three−state	PLL	Y
0	1	Driven	Three−state	PLL	N
1	0	Driven (Note 1)	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

1. Outputs are non−inverted on 2308A−2 and 2308A−3 in bypass mode, S2 = 1 and S1 = 0.

Table 2. ASM5P2308A CONFIGURATIONS (This table is applicable when PLL is not Shut Down.)

Device	Feedback From	Bank A Frequency	Bank B Frequency
ASM5P2308A (−1, −1H)	Bank A or Bank B	Reference	Reference
ASM5P2308A−2	Bank A	Reference	Reference /2
ASM5P2308A−2	Bank B	2 X Reference	Reference
ASM5P2308A−3	Bank A	2 X Reference	Reference or $\overline{\text{Reference}}$ (Note 2)
ASM5P2308A−3	Bank B	4 X Reference	2 X Reference
ASM5P2308A−4	Bank A or Bank B	2 X Reference	2 X Reference
ASM5P2308A−5H	Bank A or Bank B	Reference /2	Reference /2

2. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the ASM5P2308A−2.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output.

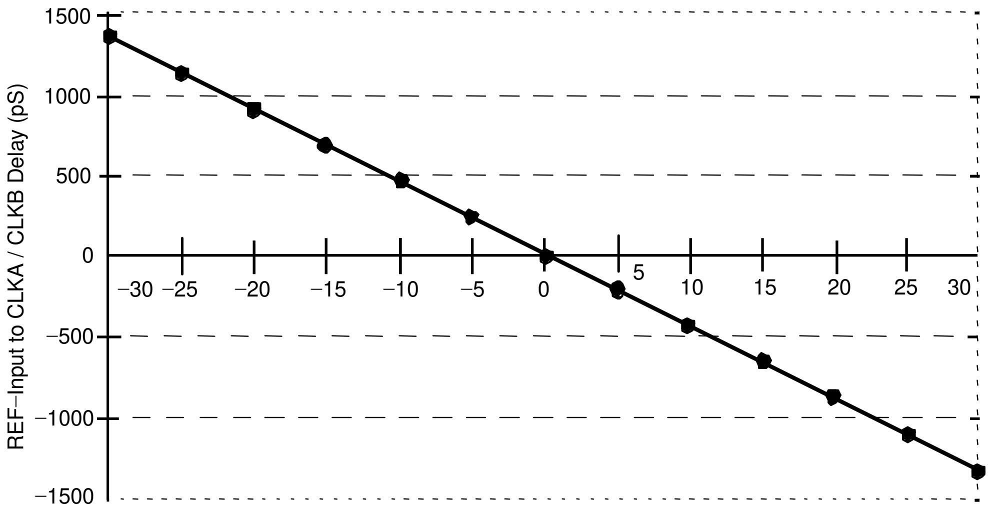


Figure 2. Output Load Difference: FBK Load − CLKA/CLKB Load (pF)

To close the feedback loop of the ASM5P2308A, the FBK can be driven from any of the eight available clock outputs. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input−output delay. This is shown in the above graph.

For applications requiring zero input−output delay, all outputs including the one providing feedback should be equally loaded. If input−output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs. For zero output−output skew, be sure to load outputs equally.

Table 3. PIN DESCRIPTION FOR ASM5P2308A

Pin #	Pin Name	Description
1	REF (Note 3)	Input reference clock frequency, 5 V tolerant input
2	CLKA1 (Note 4)	Buffered clock output, bank A
3	CLKA2 (Note 4)	Buffered clock output, bank A
4	V_{DD}	3.3 V supply
5	GND	Ground
6	CLKB1 (Note 4)	Buffered clock output, bank B
7	CLKB2 (Note 4)	Buffered clock output, bank B
8	S2 (Note 5)	Select input, bit 2
9	S1 (Note 5)	Select input, bit 1
10	CLKB3 (Note 4)	Buffered clock output, bank B
11	CLKB4 (Note 4)	Buffered clock output, bank B
12	GND	Ground
13	V_{DD}	3.3 V supply
14	CLKA3 (Note 4)	Buffered clock output, bank A
15	CLKA4 (Note 4)	Buffered clock output, bank A
16	FBK	PLL feedback input

3. Weak pull−down.
4. Weak pull−down on all outputs.
5. Weak pull−up on these inputs.

Table 4. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	−0.5	+4.6	V
DC Input Voltage (Except REF)	−0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	−0.5	7	V
Storage Temperature	−65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD22− A114−B)		2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. OPERATING CONDITIONS

Parameter	Description		Min	Max	Unit
V_{DD}	Supply Voltage		3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	Commercial temperature	0	70	°C
		Industrial temperature	−40	85	
C_L	Load Capacitance, below 100 MHz			30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz			15	pF
C_{IN}	Input Capacitance (Note 6)			7	pF

6. Applies to both Ref Clock and FBK.

Table 6. ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions		Min	Max	Unit
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage			2.2		V
I_{IL}	Input LOW Current	V_{IN} = 0 V			50	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$			100	μA
V_{OL}	Output LOW Voltage (Note 7)	I_{OL} = 8 mA (−1, −2, −3, −4) I_{OL} = 12 mA (−1H, −5H)			0.4	V
V_{OH}	Output HIGH Voltage (Note 7)	I_{OH} = −8 mA (−1, −2, −3, −4) I_{OH} = −12 mA (−1H, −5H)		2.4		V
I_{DD}	Supply Current (Note 8)	Unloaded outputs at 100 MHz, Select inputs at V_{DD} or GND (−1, −1H, −2,−3,−4)	Commercial temp.		40	mA
			Industrial temp.		45	
		Unloaded outputs; 100 MHz REF, Select inputs at V_{DD} or GND (−5H)	Commercial temp.		30	
			Industrial temp.		35	
		Unloaded outputs at 66 MHz	Commercial temp.		32	
			Industrial temp.		34	
		Unloaded outputs at 33 MHz	Commercial temp.		18	
			Industrial temp.		20	

7. Parameter is guaranteed by design and characterization. Not 100% tested in production.
8. Supply Currents are measured for PLL−Driven Mode (S2 = 1, S1 = 1).

Table 7. SWITCHING CHARACTERISTICS (For all measurements use Test Circuit #1.) (Note 9)

Parameter	Test Conditions		Min	Typ	Max	Unit
Output Frequency (Refer to *ASM5P2308A Configurations Table*)	30 pF load	(−1, −1H)	10		100	MHz
		(−2)	12		100	
		(−3)	15		100	
		(−4)	20		100	
		(−5H)	5		66.67	
	15 pF load	(−1, −1H)	10		133	MHz
		(−2)	12		133	
		(−3)	15		133	
		(−4)	20		133	
Duty Cycle (Note 10) (−1, −2, −3, −4, −1H, −5H)	Measured at 1.4 V, F_{OUT} ≤ 66.66 MHz, 30 pF load		40	50	60	%
Duty Cycle (Note 10) (−1, −2, −3, −4, −1H, −5H)	Measured at 1.4 V, F_{OUT} ≤ 50 MHz, 15 pF load		45	50	55	%
Output Rise Time (Note 10) (−1, −2, −3, −4)	Measured between 0.8 V and 2.0 V, 30 pF load	Commercial temp.			2.2	nS
		Industrial temp.			2.5	
Output Rise Time (Note 10) (−1, −2, −3, −4)	Measured between 0.8 V and 2.0 V, 15 pF load	Commercial temp., Industrial temp.			1.5	nS
Output Rise Time (Note 10) (−1H, −5H)	Measured between 0.8 V and 2.0 V, 30 pF load			1.5	2	nS
Output Fall Time (Note 10) (−1, −2, −3, −4)	Measured between 2.0 V and 0.8 V, 30 pF load	Commercial temp.			2.2	nS
		Industrial temp.			2.5	
Output Fall Time (Note 10) (−1, −2, −3, −4)	Measured between 2.0 V and 0.8 V, 15 pF load	Commercial temp., Industrial temp.			1.5	nS
Output Fall Time (Note 10) (−1H, −5H)	Measured between 2.0 V and 0.8 V, 30 pF load			1.25	1.5	nS
Output−to−output skew on same bank (Note 10) (−1, −2, −3, −4)		All outputs equally loaded			200	pS
Output−to−output skew (Note 10) (−1H, −5H)		All outputs equally loaded			200	pS
Output bank A −to− output Bank B skew (Note 10) (−1, −4, −5H)		All outputs equally loaded			200	pS
Output bank A −to− output Bank B skew (Note 10) (−2, −3)	All outputs equally loaded				400	pS
Delay, REF Rising Edge to FBK Rising Edge (Notes 10, 11)	Measured at V_{DD} /2			0	±250	pS
Device−to−Device Skew (Note 10)	Measured at V_{DD}/2 on the FBK pins of the device			0	700	
Cycle−to−Cycle Jitter (Note 10) (−1, −1H, −4, −5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load				200	
	Measured at 66.67 MHz, loaded outputs, 30 pF load				200	
	Measured at 133.3 MHz, loaded outputs, 15 pF load (Note 12)				125	
Cycle−to−Cycle Jitter (Note 10) (−2, −3)	Measured at 66.67 MHz, loaded outputs, 15 pF load				400	
	Measured at 66.67 MHz, loaded outputs, 30 pF load					
PLL Lock Time (Note 10)	Stable power supply, valid clock presented on REF and FBK pins				1.0	mS

9. All parameters are specified at Commercial and Industrial temperature unless stated otherwise.
10. Parameter is guaranteed by design and characterization. Not 100% tested in production.
11. Refer to Test Circuit #2 *Not applicable for (−1, −2, −1H, −2H).
12. Not applicable for −5H.

Switching Waveforms

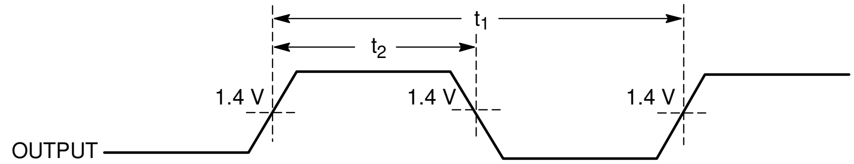


Figure 3. Duty Cycle Timing

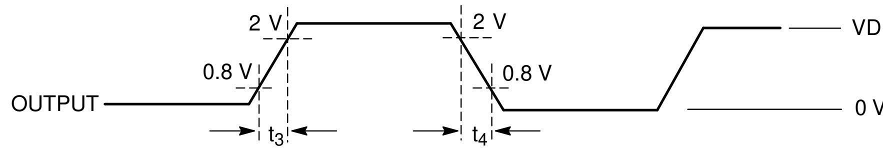


Figure 4. All Outputs Rise/Fall Time

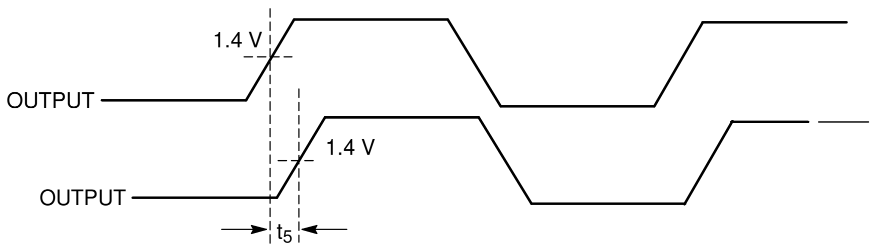


Figure 5. Output−Output Skew

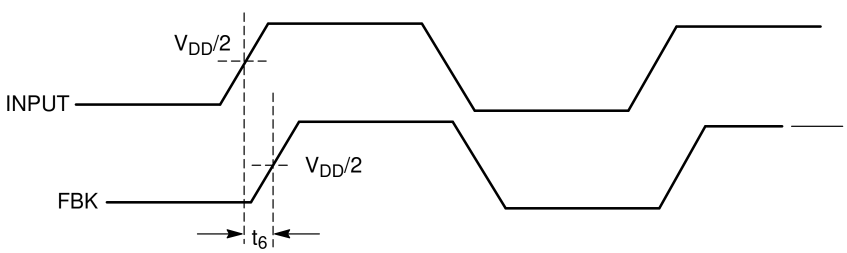


Figure 6. Input−Output Propagation Delay

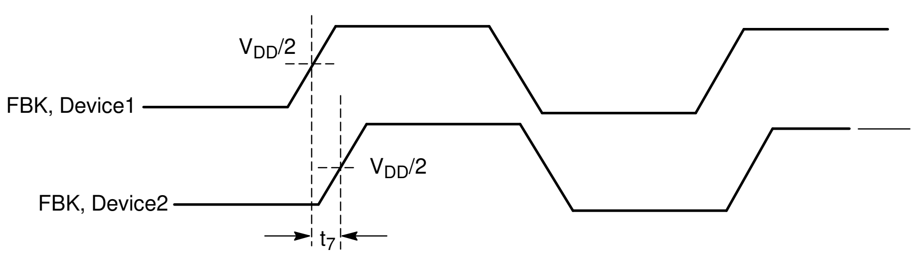
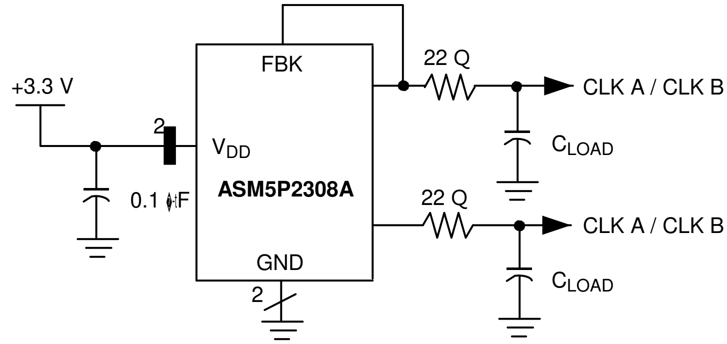


Figure 7. Device−Device Skew

TEST CIRCUIT #1



TEST CIRCUIT #2

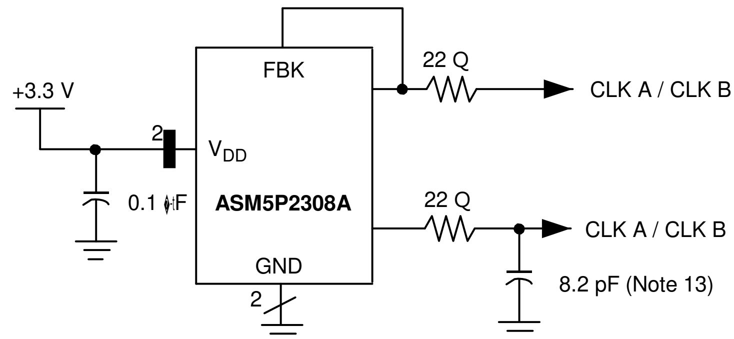
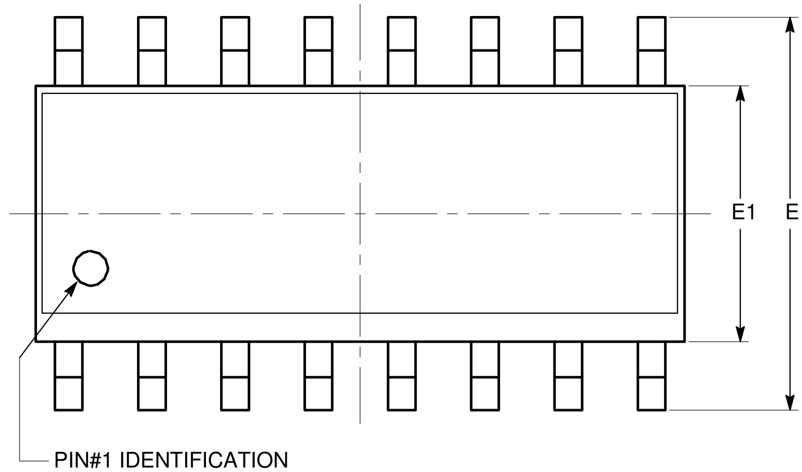


Figure 8. Test Circuits

13. Refer to Test Circuit #2 *Not applicable for (-1, -2, -1H, -2H).

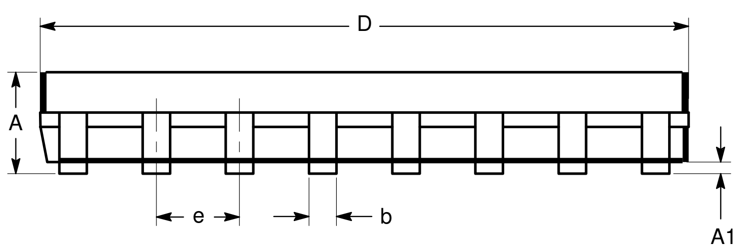
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

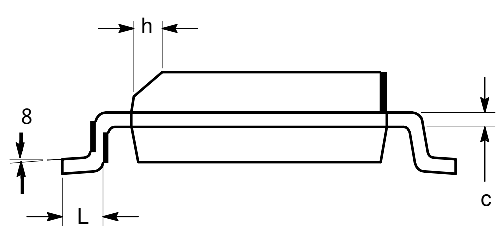


SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º

TOP VIEW



SIDE VIEW

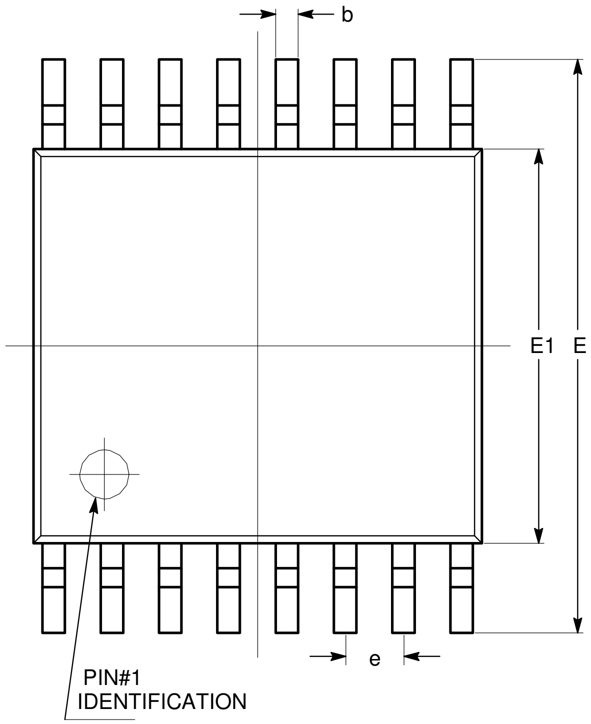


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

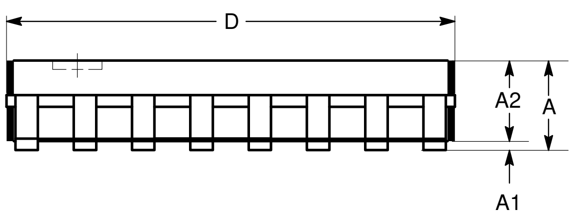
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN−01
ISSUE O

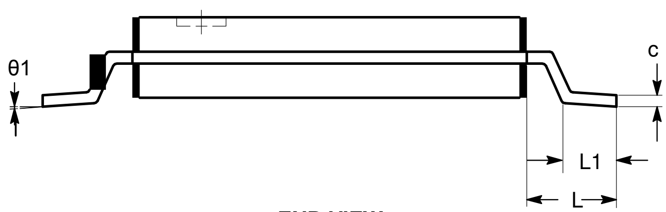


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.45		0.75
θ	0º		8º



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Table 8. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
ASM5P2308AF−1−16−ST	5P2308AF−1	16−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2308AF−1−16−ST	5I2308AF−1	16−pin 150−mil SOIC−TUBE, Pb free	Industrial
ASM5P2308AF−1−16−SR	5P2308AF−1	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5I2308AF−1−16−SR	5I2308AF−1	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5P2308AF−1−16−TT	5P2308AF−1	16−PIN 150−mil TSSOP − TUBE, Pb free	Commercial
ASM5I2308AF−1−16−TT	5I2308AF−1	16−PIN 150−mil TSSOP − TUBE, Pb free	Industrial
ASM5P2308AF−1−16−TR	5P2308AF−1	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Commercial
ASM5I2308AF−1−16−TR	5I2308AF−1	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Industrial
P5P2308AF−1H16ST	5P2308AF−1H	16−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2308AF−1H−16−ST	5I2308AF−1H	16−pin 150−mil SOIC−TUBE, Pb free	Industrial
P5P2308AF−1H16SR	5P2308AF−1H	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5I2308AF−1H−16−SR	5I2308AF−1H	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5P2308AF−1H−16−TT	5P2308AF−1H	16−PIN 150−mil TSSOP − TUBE, Pb free	Commercial
ASM5I2308AF−1H−16−TT	5I2308AF−1H	16−PIN 150−mil TSSOP − TUBE, Pb free	Industrial
P5P2308AF−1H16TR	5P2308AF−1H	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Commercial
ASM5I2308AF−1H−16−TR	5I2308AF−1H	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Industrial
P5P2308AF−2−16ST	5P2308AF−2	16−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2308AF−2−16−ST	5I2308AF−2	16−pin 150−mil SOIC− TUBE, Pb free	Industrial
P5P2308AF−216SR	5P2308AF−2	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5I2308AF−2−16−SR	5I2308AF−2	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5P2308AF−2−16−TT	5P2308AF−2	16−PIN 150−mil TSSOP − TUBE, Pb free	Commercial
P5I2308AF−216TT	5I2308AF−2	16−PIN 150−mil TSSOP − TUBE, Pb free	Industrial
P5P2308AF−216TR	5P2308AF−2	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Commercial
ASM5I2308AF−2−16−TR	5I2308AF−2	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Industrial
ASM5P2308AF−3−16−ST	5P2308AF−3	16−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2308AF−3−16−ST	5I2308AF−3	16−pin 150−mil SOIC− TUBE, Pb free	Industrial
ASM5P2308AF−3−16−SR	5P2308AF−3	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5I2308AF−3−16−SR	5I2308AF−3	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5P2308AF−3−16−TT	5P2308AF−3	16−PIN 150−mil TSSOP − TUBE, Pb free	Commercial
ASM5I2308AF−3−16−TT	5I2308AF−3	16−PIN 150−mil TSSOP − TUBE, Pb free	Industrial
P5P2308AF−3−16TR	5P2308AF−3	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Commercial
ASM5I2308AF−3−16−TR	5I2308AF−3	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Industrial
ASM5P2308AF−4−16−ST	5P2308AF−4	16−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2308AF−4−16−ST	5I2308AF−4	16−pin 150−mil SOIC− TUBE, Pb free	Industrial
ASM5P2308AF−4−16−SR	5P2308AF−4	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5I2308AF−4−16−SR	5I2308AF−4	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5P2308AF−4−16−TT	5P2308AF−4	16−PIN 150−mil TSSOP − TUBE, Pb free	Commercial
ASM5I2308AF−4−16−TT	5I2308AF−4	16−PIN 150−mil TSSOP − TUBE, Pb free	Industrial
ASM5P2308AF−4−16−TR	5P2308AF−4	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Commercial
ASM5I2308AF−4−16−TR	5I2308AF−4	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Industrial
ASM5P2308AF−5H−16−ST	5P2308AF−5H	16−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2308AF−5H−16−ST	5I2308AF−5H	16−pin 150−mil SOIC− TUBE, Pb free	Industrial
ASM5P2308AF−5H−16−SR	5P2308AF−5H	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5I2308AF−5H−16−SR	5I2308AF−5H	16−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5P2308AF−5H−16−TT	5P2308AF−5H	16−PIN 150−mil TSSOP − TUBE, Pb free	Commercial
ASM5I2308AF−5H−16−TT	5I2308AF−5H	16−PIN 150−mil TSSOP − TUBE, Pb free	Industrial
ASM5P2308AF−5H−16−TR	5P2308AF−5H	16−PIN 150−mil TSSOP − TAPE & REEL, Pb free	Commercial
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