RoHS

Ultra-Mobile Platform PMIC

900841

POWER MANAGEMENT

98ASA10841D

11 mm x 11 mm

The 900841 is a high-efficiency, Power Management Integrated Circuit (PMIC), capable of providing all operating voltages for ultra-mobile platforms through its 29 voltage rails. It has nine switching power supplies running at frequencies from 1.0 to 4.0 MHz,17 highly-efficient LDOs and three, 3.3 V power switches. It incorporates a switching mode Li-Ion battery charger, advanced audio path, signaling and backlight LED drivers, 22-channel ADC, real time clock, 8 GPIO, 8 GPO, and 4 GPOSW for specific platform switches control.

The SC900841 is fully configurable and controllable through its SPI and Mini SPI interfaces. Along with companion chip SC900842, it provides an optimized power management solution for ultra-mobile platforms used on Mobile Internet Devices (MID), netbooks, tablets, slates, smart phones and other high-tech portable devices.

Optimum partitioning, high feature integration, and state-of-the-art technology allow Freescale to effectively serve this growing market segment.

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
SC900841JVK/R2	-40°C to 85°C	338-MAPBGA

Features

- Complete system power management, battery charging and audio support integrated in a single chip
- Advanced audio path
- Fully programmable DC/DC switching, low drop-out regulators, and load switches
- Power path management & switching mode Li-Ion/Li-Polymer battery charger
- LCD backlight and system lighting support
- SPI interface (up to 25 MHz operation)
- 22-channel (32 capable) 10-bit ADC for internal and external sensing with touch screen interface
- Real time clock (RTC)
- 8 Interrupt capable GPIOs and 8 GPOs
- 4 GPOs for controlling platform switches
- I/O interrupt and reset controller

Applications

- Mobile Internet Devices (MID)
- Tablet PC
- Netbooks

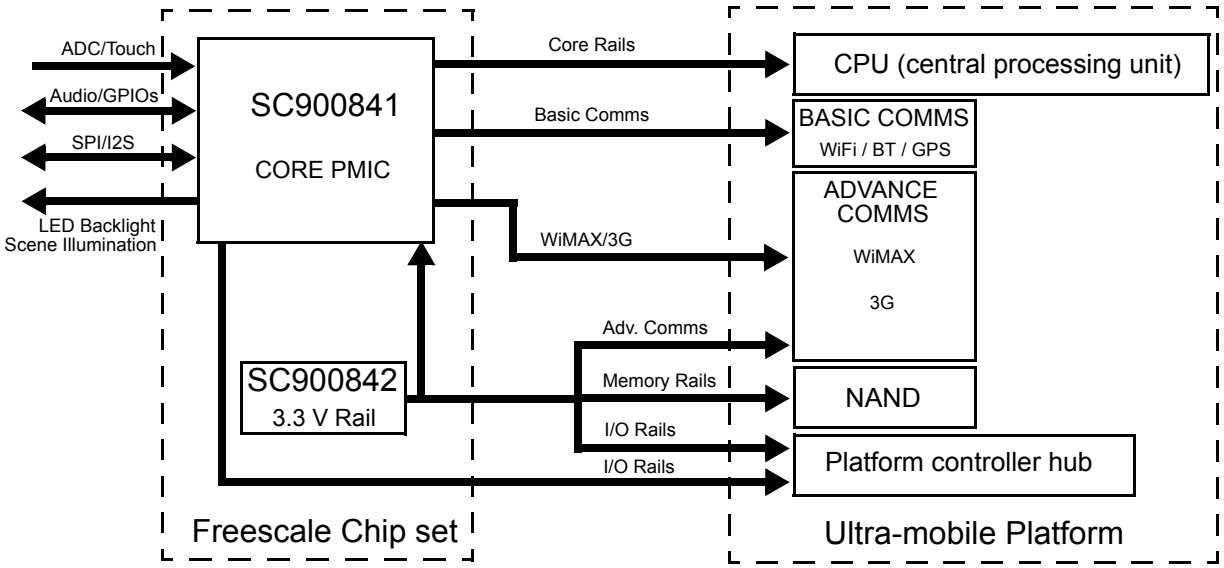

Figure 1. 900841 Simplified Application Diagram

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ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 1. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Charger Input Voltage	-	-0.3 to +20	V
LCD Backlight Circuitry Voltage	-	-0.3 to +28	V
Battery Voltage	-	-0.3 to +4.4	V
Coin Cell Voltage	-	-0.3 to +3.6	V
ESD Rating, All Pins, Human Body Model (HBM)(3)	V_{ESDHBM}	±2000	V
ESD Rating, All Pins, Charge Device Model (CDM) (3), (4)	V_{ESDCDM}	±450	V
THERMAL RATINGS			
Ambient Operating Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-30 to +125	°C
Storage Temperature Range	T_{ST}	-65 to +150	°C
Peak Package Reflow Temperature(1), (2)	T_{PPRT}	260	°C

Notes

1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
2. Freescale's Package Reflow capability meets the Pb-free requirements for JEDEC standard J-STD-020C, for Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL)
3. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).
4. All pins meet 500 V CDM except VCOREREF.

POWER DISSIPATION

During operation, the temperature of the die must not exceed the maximum junction temperature. Depending on the operating ambient temperature and the total internal dissipation this limit can be exceeded.

To optimize the thermal management scheme and avoid overheating, the 900841 provides a thermal management system that protects against overheating. This protection should be considered as a fail-safe mechanism, and the application design should initiate thermal shutdown under normal conditions. Reference Thermal Management for more details.

POWER CONSUMPTION

Table 2 defines the maximum power consumption specifications in the various system and device states. For each entry in the table, the component is assumed to be configured for driving purely capacitive loads, and the voltages listed in each entry are nominal output voltages.

Note that the “Soft Mechanical Off” state is a transitional state. The device will spend less than 150 µs in this state before V15 starts to turn on, upon detection of a valid USB device or valid battery.

Table 2. Power Rating

Condition	Description	Logic	Maximum Power Consumption
Hard Mechanical Off	There is no Valid USB device or valid battery connected to SC900841	USBDET = 0 BATDET = 0	0 mW
Soft Mechanical Off	SC900841 has input power from either a USB device or a battery. All VRs are programmed “OFF”	USBDET = 1 BATDET = 0	50 mW
		USBDET = 0 BATDET = 1	5 mW
Power On	SC900841 has input power from either a USB device or a battery. The cold-boot rails are “ON”. V21 = 2.1 V V15 = 1.5 V VAON = 1.2 V VCCPAOAC = 1.05 V VPMIC = 1.8 V All VR outputs are set in PFM or APS mode driving purely capacitive loads.	USBDET = 0 BATDET = 1	100 mW
		USBDET = 1 BATDET = 0	10 mW

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM CONTROL INTERFACE					
Input Low Voltage	V_{IL}				V
VYMXGPSEN, VYMXPAEN, VYMX3GEN, SDATA, SCK, CS		0	-	$0.3*V_{PMIC}$	
EXITSTBY, VID[6:0]		0	-	$0.3*V_{CCP}$	
THRMTRIPB, VIDEN[1:0]		0	-	$0.3*V_{CCPAOAC}$	
V33STTS, V3GPASTTS		0	-	$0.3*V_{PMIC}$	
Input High Voltage	V_{IH}				V
VYMXGPSEN, VYMXPAEN, VYMX3GEN, SDATA, SCK, CS		$0.7*V_{PMIC}$	-	V_{PMIC}	
EXITSTBY, VID[6:0]		$0.7*V_{CCP}$	-	V_{CCP}	
THRMTRIPB, VIDEN[1:0]		$0.7*V_{CCPAOAC}$	-	$V_{CCPAOAC}$	
V33STTS, V3GPASTTS		$0.7*V_{PMIC}$	-	V_{PMIC}	
Output Low Voltage PMICINT, VRCOMP, RESETB, PWRGD, V33EN, V3GPAEN	V_{OL}	0	-	0.1	V
Output High Voltage PMICINT, VRCOMP, RESETB, PWRGD, V33EN, V3GPAEN	V_{OH}	V_{PMIC} - 0.1	-	V_{PMIC}	V
SPI INTERFACE LOGIC IO					
Operating Voltage Range (SPIVCC Pin)	V_{SPIVCC}	1.74	1.8	3.1	V
Input High SPICSB, MOSI, SPICLK	-	$0.7*V_{SPIVCC}$	-	$V_{SPIVCC}+0.3$	V
Input Low SPICSB, MOSI, SPICLK	-	0	-	$0.3*V_{SPIVCC}$	V
Output Low MISO (Output sink 100 µA)	-	0	-	0.1	V
Output High MISO (Output source 100 µA)	-	V_{SPIVCC} -0.1	-	V_{SPIVCC}	V
OSCILLATOR AND CLOCK OUTPUTS MAIN CHARACTERISTICS					
Operating Voltage	-	1.2	-	1.5	V
RTC OSC Consumption Current (RTC Mode: All blocks disabled, no main battery attached, coin cell is attached to COINCELL)	-	-	1.0	2.0	µA
26 MHz OSC Consumption Current	-	-	-	500	µA
Output Low CLK32K & CLK26M (Output sink 100 µA)	-	0	-	0.1	V
Output High CLK32K & CLK26M (Output source 100 µA)	-	V_{SPIVCC} - 0.1	-	V_{SPIVCC}	V
CLK32K & CLK26M Output Duty Cycle	-	40	50	60	%

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
RTC					
Input Voltage Range	-	1.2	-	1.5	V
Consumption Current	-	-	15	25	µA
Crystal OSC Frequency Tolerance	-	-30	-	+30	ppm
Crystal OSC Peak Temperature Frequency (Turn Over Temperature)	-	20	25	30	°C
Crystal OSC Maximum Series Resistance	-	-	80	-	KΩ
Crystal OSC Maximum Drive Level	-	-	0.5	-	µW
Crystal OSC Operating Drive Level	-	0.25	-	0.5	µW
Crystal OSC Nominal Lead Capacitance	-	-	9.0	-	pF
Crystal OSC Aging	-	-	-	3	ppm/ year
COIN CELL CHARGER					
Coin cell Charge Voltage (Selectable through VCOIN[2:0] bits)	$V_{COINCELL}$	2.5	-	3.3	V
Coin cell Charge Voltage Accuracy	-	-100	-	100	mV
Coin cell Charge Current	I_{COIN}	-	60	-	µA
Coin cell Charge Current Accuracy	-	-15	-	15	%
POWER STATES DETECTION THRESHOLDS					
Input Voltage Rising Detection Threshold	$V_{RAWCHGDET}$	-	-	4.50	V
Input Voltage Rising Detection Threshold Hysteresis	$V_{RAWCHGDETHYS}$	-	100	-	mV
Battery Cutoff Threshold (Depending on Battery Model)	V_{BATOFF}	2.2	-	2.4	V
Coin Cell Disconnect Threshold	$V_{COINOFF}$	1.8	-	2.0	V
Low Battery Threshold	V_{LOWBAT}	3.2	-	-	V
Valid Battery Threshold	V_{TRKL}	-	3.0	-	V
VPWR Rising Under-voltage Threshold	V_{PWRUVR}	-	3.1	-	V
VPWR Falling Under-voltage Threshold	V_{PWRUVF}	-	2.55	-	V
VCC ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Programmability Range Low Power Mode Active Mode	V_{CC}	 0.3 0.65	 - -	 0.7 1.2	V
Output Voltage Programmability Step Size	-	-	12.5	-	mV
Output Voltage Accuracy 0.6 V < V_{CC} < 12 V, 1.5 A < I_{CC} < 3.5 A 0.6 V < V_{CC} < 12 V, I_{CC} < 1.5 A 0.3 V < V_{CC} < 0.6 V	-	 -5.0 -4.0 -7.0	 - - -	 5.0 4.0 7.0	%
Output Voltage Overshoot Maximum overshoot voltage above VID setting voltage. Maximum overshoot time is 10-30 s, output voltage = 0.9 V at 50 mA	V_{OS}	-	-	50	mV

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Continuous Output Load Current					A
Low Power mode	I_{CC}	-	-	0.2	
Active Mode		0.2	-	3.5	
Peak Current Limit	I_{LIMCC}	-	5.0	-	A
Output Current Limit Accuracy	-		±15	-	%
Transient Load Change	ΔI_{CC}				A
Low Power Mode		-	-	0.2	
Active Mode		-	-	1.2	
VNN ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Programmability Range (Set by VID Control Signals)	V_{NN}	0.65	-	1.2	V
Output Voltage Programmability Step Size	-	-	12.5	-	mV
Output Voltage Accuracy	-	-5.0	-	5.0	%
Output Voltage Overshoot Maximum overshoot voltage above VID setting voltage. Maximum overshoot time is 10 s, output voltage = 0.9 V at 50 mA	V_{OS}	-	-	50	mV
Continuous Output Load Current	I_{NN}				A
Low Power Mode		-	-	0.2	
Active Mode		0.2	-	1.6	
Peak Current Limit	I_{LIMNN}	-	2.5	-	A
Output Current Limit Accuracy	-	-	±20	-	%
Transient Load Change	ΔI_{NN}	-	-	0.5	A
VDDQ ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Setting	V_{DDQ}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Continuous Output Load Current	I_{DDQ}	-	-	1.3	A
Peak Current Limit	I_{LIMDDQ}	-	1.78	-	A
Output Current Limit Accuracy	-				%
0.5 A < I_{DDQ} < 1.3 A		-15	-	+15	
I_{DDQ} < 0.5 A		-20	-	+20	
Transient Load Change	I_{DDQ}	-	-	0.5	A
Effective Quiescent Current Consumption (PWM, No Load)	I_{QDDQ}	-	30	-	µA
V21 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Setting	V_{21}	-	2.1	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Continuous Output Load Current	I_{21}	-	-	1.0	A
Peak Current Limit	I_{LIM21}	-	1.42	-	A
Output Current Limit Accuracy	-	-20	-	+20	%
Transient Load Change	I_{21}	-	-	0.5	A
Effective Quiescent Current Consumption (PWM, No Load)	I_{Q21}	-	30	-	µA
V15 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Setting (Also programmable to 1.6 V typical)	V_{15}	-	1.5	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Continuous Output Load Current	I_{15}	0	0.75	1.5	A
Peak Current Limit	I_{LIM15}	-	1.6	-	A
Output Current Limit Accuracy	-	-20	-	+20	%
Transient Load Change	I_{15}	-	-	0.5	A
Effective Quiescent Current Consumption (PWM, No Load)	I_{Q15}	-	30	-	µA
VYMX3G ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Setting YMX 3G (Programmable through Mini-SPI)	V_{YMX3G}	 - 0.6	 1.25 -	 - 1.375	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Output Voltage Ripple (PWM mode)	ΔI_{YMX3G}	-10	-	+10	mV
Continuous Output Load Current	I_{YMX3G}	0	-	0.8	A
Peak Current Limit	$I_{LIMYMX3G}$	-	1.46	-	A
Output Current Limit Accuracy	-	-20	-	+20	%
Transient Load Change	ΔI_{YMX3G}	-	-	0.2	A
Effective Quiescent Current Consumption (PWM, No Load)	I_{QYMX3G}	-	30	-	µA
VYMXPA ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Typical Output Voltage Range	V_{OYMXPA}	(Selectable, see Table 37)			V
Output Accuracy	-	-5.0	-	+5.0	%
Output Voltage Ripple	ΔV_{YMXPA}	-10	-	10	mV
Continuous Output Load Current V_{YMXPA} = 4.2 V V_{YMXPA} = 5.0 V	I_{OYMXPA}	 - -	 - -	 0.70 0.50	A
Under-voltage Protection Threshold	$V_{UVYMXPA}$	-	3.7	-	V
Under-voltage Protection Threshold Hysteresis	$V_{UVYMXPAHYS}$	-	0.2	-	V

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Over-voltage Protection Threshold	$V_{OVYMXPA}$	-	5.75	-	V
Over-voltage Protection Threshold Hysteresis	$V_{OVYMXPAHYS}$	-	0.16	-	V
Over-current limit threshold	$I_{LIMYMXPA}$	-	1.9	-	A
Over-current limit threshold Accuracy	-	-20	-	20	%
Short-circuit Protection Threshold (Measured at the output voltage)	$V_{SCYMXPA}$	-	3.0	-	V
Short-circuit Protection Threshold Accuracy (Measured at the output voltage)	-	-20	-	20	%
Transient Load Change (I_{OYMXPA} from 1.0 to 201 mA)	ΔI_{YMXPA}	-	-	0.2	A
FBYMXPA Leakage Current	$I_{FBYMXPALKG}$	-	0.1	-	µA
YMXPAGTIN Leakage Current	$I_{YMXPAGTINLKG}$	-	-	5.0	µA
YMXPAGT Leakage Current V_{OL}=100 mV, V_{OH}=V_{YMXPA} - 100 mV	$I_{YMXPAGTLKG}$	-25	-	25	µA
Discharge FET Resistance	$R_{DSCHYMXPA}$	-	45	-	Ω
Effective Quiescent Current Consumption (No Load)	I_{QYMXPA}	-	125	-	µA
VOTG ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Typical Output Voltage Range	V_{OTG}	-	5.0	-	V
Output Accuracy	-	-4.0	-	+4.0	%
Continuous Output Load Current	I_{OOTG}	0	-	0.35	A
Under-voltage Protection Threshold	V_{UVOTG}	-	4.5	-	V
Under-voltage Protection Threshold Hysteresis	$V_{UVOTGHYS}$	-	0.2	-	V
Over-voltage Protection Threshold	V_{OVOTG}	-	5.76	-	V
Over-voltage Protection Threshold Hysteresis	$V_{OVOTGHYS}$	-	0.16	-	V
Over-current limit threshold	I_{LIMOTG}	-	1.5	-	A
Over-current limit threshold Accuracy	-	-20	-	20	%
Short-circuit Protection Threshold (Measured at the output voltage)	V_{SCOTG}	-	3.5	-	V
Short-circuit Protection Threshold Accuracy (Measured at the output voltage)	-	-20	-	20	%
Transient Load Change (I_{OOTG} from 1.0 mA to 201 mA)	I_{OTG}	-	-	0.2	A
FBOTG Leakage Current	$I_{FBOTGLKG}$	-	0.1	-	µA
OTGGTIN Leakage Current	$I_{OTGGTINLKG}$	-	-	5.0	µA
OTGGT Leakage Current	$I_{OTGGTLKG}$	-25	-	25	µA
Discharge FET Resistance	$R_{DSCHOTG}$	-	100	-	Ω
Effective Quiescent Current Consumption (No Load)	I_{QOTG}	-	100	-	µA

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VBKLT ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Typical Output Voltage Range LCD Backlight Active Only Camera Scene	V_{BKLT}	 6.0 21	 - 22	 23 23	V
Maximum Output Load Current	$I_{BKLTMAX}$	-	-	120	mA
LED Forward Voltage Range	V_F	-	-	4.0	V
Under-voltage Detection Threshold	V_{UVBKLT}	-	20	-	V
Under-voltage Detection Threshold Hysteresis	$V_{UVBKLTHYS}$	-	1.0	-	V
Over-voltage Protection Threshold	V_{OVBKLT}	-	24	-	V
Over-voltage Protection Threshold Hysteresis	$V_{OVBKLTHYS}$	-	1.0	-	V
Over-current limit threshold	$I_{LIMBKLT}$	-	1.9	-	A
Over-current limit threshold Accuracy	-	-20	-	20	%
Short-circuit Protection Threshold (Measured at the output voltage)	V_{SCBKLT}	-	4.0	-	V
Short-circuit Protection Threshold Accuracy (Measured at the output voltage)	-	-20	-	20	%
LED Current Sink Headroom	-	0.4	0.5	0.6	mV
FBBKLT Leakage Current	$I_{FBBKLTLKG}$	-	0.1	-	µA
WLEDx and LEDSCN Leakage Current (VBKLT is disabled and current sink is OFF)	-	-	-	1.0	µA
Effective Quiescent Current Consumption (No Load)	I_{QBKLT}	-	500	-	µA
VBG ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{DDQ}	1.71	1.80	1.89	V
Output Voltage Setting	V_{BG}	-	1.25	-	V
Output Voltage Accuracy	-	-2.0	-	2.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{BGUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{BGUVH}	-	1.0	-	%
Continuous Output Load Current Active Mode Low Power Mode	I_{BG}	 - -	 - -	 2.0 40	 mA µA
Current Limit	I_{LIMBG}	-	94	-	mA
Transient Load Change	ΔI_{BG}	-	-	1.0	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{BG} = 1.5 mA, V_{DDQ} = 1.8 V)	$PSRR_{BG}$	50	60	-	dB
Effective Quiescent Current Consumption Active Mode Low Power Mode	I_{QBG}	 - -	 - -	 18 10	µA

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VCCA ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{DDQ}	1.71	1.80	1.89	V
Output Voltage Setting	V_{CCA}	-	1.5	-	V
Output Voltage Accuracy	-	-2.0	-	2.0	%
Under Voltage Detection Threshold (With respect to the output voltage)	V_{CCAUV}	-	-12	-	%
Under Voltage Detection Threshold Hysteresis	V_{CCAUVH}	-	1.0	-	%
Continuous Output Load Current	I_{CCA}				
Active Mode		-	-	150	mA
Low Power Mode		-	-	3.0	mA
Current Limit	I_{LIMCCA}	-	225	-	mA
Transient Load Change	ΔI_{CCA}	-	-	50	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CCA} = 112.5 mA, V_{DDQ} = 1.8 V)	$PSRR_{CCA}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QCCA}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VCC180 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{21}	1.995	2.1	2.205	V
Output Voltage Setting	V_{CC180}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{CC180UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{CC180UVH}$	-	1.0	-	%
Continuous Output Load Current	I_{CC180}				
Active Mode		-	-	390	mA
Low Power Mode		-	-	7.8	mA
Current Limit	$I_{LIMCC180}$	-	585	-	mA
Transient Load Change	ΔI_{CC180}	-	-	350	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CC180} = 292.5 mA, V_{21} = 2.1 V)	$PSRR_{CC180}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QCC180}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VPNL18 ELECTRICAL CHARACTERISTICS SPECIFICATION					
Input Voltage Range	V_{21}	1.995	2.1	2.205	V
Output Voltage Setting	V_{PNL18}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{PNL18UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{PNL18UVH}$	-	1.0	-	%

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Continuous Output Load Current					mA
Active Mode	I_{PNL18}	-	-	210	
Low Power Mode		-	-	4.2	
Current Limit	$I_{LIMPNL18}$	-	315	-	mA
Transient Load Change	ΔI_{PNL18}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{PNL18} = 157.5 mA, V_{21} = 2.1 V)	$PSRR_{PNL18}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QPNL18}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VPMIC ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{21}	1.995	2.1	2.205	V
Output Voltage Setting	V_{PMIC}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{PMICUV}	-	-12	-	%
Under Voltage Detection Threshold Hysteresis	$V_{PMICUVH}$	-	1.0	-	%
Continuous Output Load Current	I_{PMIC}				mA
Active Mode		-	-	100	
Low Power Mode		-	-	2.0	
Current Limit	$I_{LIMPMIC}$	-	150	-	mA
Transient Load Change	ΔI_{PMIC}	-	-	20	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{PMIC} = 75 mA, V_{21} = 2.1 V)	$PSRR_{PMIC}$	50	60	-	dB
Effective Quiescent Current Consumption					µA
Active Mode	I_{QPMIC}	-	-	18	
Low Power Mode		-	-	10	
VYMXYFI18 ELECTRICAL CHARACTERISTICS					
Input Voltage Range					V
Supplied by V_{21} DC/DC	V_{21}	1.995	2.1	2.205	
Supplied by V_{PWR}	V_{PWR}	3.0	3.6	4.4	
Output Voltage Setting	$V_{YMXYFI18}$	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{YMXYFI18UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{YMXYFI18UVH}$	-	1.0	-	%
Continuous Output Load Current	$I_{YMXYFI18}$				mA
Active Mode		-	-	200	
Low Power Mode		-	-	4.0	
Current Limit	$I_{LIMYMXYFI18}$	-	300	-	mA
Transient Load Change	$\Delta I_{YMXYFI18}$	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, $I_{YMXYFI18}$ = 150 mA), (V_{21} = 2.1 V or V_{PWR} = 3.6 V)	$PSRR_{YMXYFI18}$	40	-	-	dB

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Output Noise (10 Hz to 100 kHz, $I_{YMXYFI18}$ = 200 mA), (V_{21} = 2.1 V or V_{PWR} = 3.6 V)	$V_{NOISEYMXYFI18}$	-	-	40	μV_{RMS}
Effective Quiescent Current Consumption	$I_{QYMXYFI18}$				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VYMXYFI ELECTRICAL CHARACTERISTICS					
Input Voltage Range					V
Supplied by V_{15} DC/DC (WiFiBT Applications)	V_{15}	1.425	1.5	1.575	
Supplied by V_{33} DC/DC (WiMAX Applications)	V_{33}	3.168	3.3	3.432	
Supplied by V_{PWR} (WiMAX Applications)	V_{PWR}	3.0	3.6	4.4	
Output Voltage Setting	V_{YMXYFI}				V
WiFiBT Applications		-	1.2	-	
WiMAX Applications		-	2.5	-	
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{YMXYFIUV}$	-	-12	-	%
Under Voltage Detection Threshold Hysteresis	$V_{YMXYFIUVH}$	-	1.0	-	%
Continuous Output Load Current	I_{YMXYFI}				mA
Active Mode (WiFiBT Applications)		-	-	60	
Active Mode (WiMAX Applications)		-	-	150	
Low Power Mode		-	-	1.2	
Current Limit	$I_{LIMYMXYFI}$	-	225	-	mA
Transient Load Change	ΔI_{YMXYFI}				mA
WiFiBT Applications		-	-	32	
WiMAX Applications		-	-	130	
Power Supply Rejection Ratio (PSRR) (20 kHz, I_{YMXYFI} = 45 mA), (V_{15} = 1.5) (WiFiBT Applications)	$PSRR_{YMXYFI}$	50	60	-	dB
Power Supply Rejection Ratio (PSRR) (100 kHz, I_{YMXYFI} = 112.5 mA), (V_{33} = 3.3 V or V_{PWR} = 3.6 V) (WiMAX Applications)	$PSRR_{YMXYFI}$	40	-	-	dB
Output Noise (10 Hz to 100 kHz, I_{YMXYFI} = 60 mA), (V_{15} = 1.5 V) (WiFiBT Applications)	$V_{NOISEYMXYFI}$	-	-	40	μV_{RMS}
Output Noise (10 Hz to 100 kHz, I_{YMXYFI} = 150 mA), (V_{33} = 3.3 V or V_{PWR} = 3.6 V) (WiMAX Applications)	$V_{NOISEYMXYFI}$	-	-	40	μV_{RMS}
Effective Quiescent Current Consumption	$I_{QYMXYFI}$				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VYMXGPS ELECTRICAL CHARACTERISTICS					
Input Voltage Range					V
Supplied by V_{15} DC/DC (WiMAX Applications)	V_{15}	1.52	1.6	1.68	
Supplied by V_{21} DC/DC (GPS Applications)	V_{21}	1.995	2.1	2.205	
Supplied by V_{PWR} (GPS Applications)	V_{PWR}	3.0	3.6	4.4	
Output Voltage Setting	V_{YMXGPS}				V
WiMAX Applications		-	1.3	-	
GPS Applications		-	1.8	-	
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{YMXGPSUV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{YMXGPSUVH}$	-	1.0	-	%
Continuous Output Load Current	I_{YMXGPS}				mA
Active Mode (WIMAX Applications)		-	-	350	
Active Mode (GPS Applications)		-	-	170	
Low Power Mode		-	-	3.4	
Current Limit	$I_{LIMYMXGPS}$	-	525	-	mA
Transient Load Change	ΔI_{YMXGPS}				mA
WiMAX Applications		-	-	200	
GPS Applications		-	-	130	
Power Supply Rejection Ratio (PSRR) (20 kHz, I_{YMXGPS} = 262.5 mA), (V_{15} = 1.6 V) (WiMAX Applications)	$PSRR_{YMXGPS}$	50	60	-	dB
Power Supply Rejection Ratio (PSRR), (20 to 100 kHz, I_{YMXGPS} = 127.5 mA), (V_{21} = 2.1 V or V_{PWR} = 3.6 V) (GPS Applications)	$PSRR_{YMXGPS}$	40	-	-	dB
Output Noise (10 Hz to 100 kHz, I_{YMXGPS} = 350 mA), (V_{15} = 1.6 V) (WiMAX Applications)	$V_{NOISEYMXGPS}$	-	-	40	μV_{RMS}
Output Noise (10 Hz to 100 kHz, I_{YMXGPS} = 170 mA), (V_{21} = 2.1 V or V_{PWR} = 3.6 V) (GPS Applications)	$V_{NOISEYMXGPS}$	-	-	40	μV_{RMS}
Effective Quiescent Current Consumption	$I_{QYMXGPS}$				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VCCPAOAC ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	$V_{CCPAOAC}$	-	1.05	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{CCPAOACUV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{CCPAOACUVH}$	-	1.0	-	%
Continuous Output Load Current	$I_{CCPAOAC}$				mA
Active Mode		-	-	155	
Low Power Mode		-	-	3.1	
Current Limit	$I_{LIMCCPAOAC}$	-	232.5	-	mA

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Transient Load Change	$\Delta I_{CCPAOAC}$	-	-	50	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, $I_{CCPAOAC}$ = 116 mA, V_{15} = 1.5 V)	$PSRR_{CCPAOAC}$	50	60	-	dB
Effective Quiescent Current Consumption	$I_{QCCPAOAC}$				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VCCPDDR ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{CCPDDR}	-	1.05	-	V
Output Voltage Accuracy	-	-2.0	-	2.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{CCPDDRUV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{CCPDDRUVH}$	-	1.0	-	%
Continuous Output Load Current	I_{CCPDDR}				mA
Active Mode		-	-	60	
Low Power Mode		-	-	1.2	
Current Limit	$I_{LIMCCPDDR}$	-	90	-	mA
Transient Load Change	ΔI_{CCPDDR}	-	-	10	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CCPDDR} = 45 mA, V_{15} = 1.5 V)	$PSRR_{CCPDDR}$	50	60	-	dB
Effective Quiescent Current Consumption	$I_{QCCPDDR}$				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VAON ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{AON}	-	1.2	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{AONUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{AONUVH}	-	1.0	-	%
Continuous Output Load Current	I_{AON}				mA
Active Mode		-	-	250	
Low Power Mode		-	-	5	
Current Limit	I_{LIMAON}	-	375	-	mA
Transient Load Change	ΔI_{AON}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{AON} = 187.5 mA, V_{15} = 1.5 V)	$PSRR_{AON}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QAON}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VMM ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{MM}	-	1.2	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{MMUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{MMUVH}	-	1.0	-	%
Continuous Output Load Current	I_{MM}				mA
Active Mode		-	-	5.0	
Low Power Mode		-	-	0.1	
Current Limit	I_{LIMMM}	-	25	-	mA
Transient Load Change	ΔI_{MM}	-	-	3.0	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{MM} = 4.0 mA, V_{15} = 1.5 V)	$PSRR_{MM}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QMM}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VCCP ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{CCP}	-	1.05	-	V
Output Voltage Accuracy	-	-5	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{CCPUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{CCPUVH}	-	1.0	-	%
Continuous Output Load Current	I_{CCP}				mA
Active Mode		-	-	445	
Low Power Mode		-	-	8.9	
Current Limit	I_{LIMCCP}	-	667.5	-	mA
Transient Load Change	ΔI_{CCP}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CCP} = 334 mA, V_{15} = 1.5 V)	$PSRR_{CCP}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QCCP}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VIMG25 ELECTRICAL CHARACTERISTICS					
Input Voltage Range					V
Supplied by V_{33} DC/DC	V_{33}	3.168	3.3	3.432	
Supplied by V_{PWR}	V_{PWR}	3.0	3.6	4.4	
Output Voltage Setting	V_{IMG25}	-	2.5	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{IMG25UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{IMG25UVH}$	-	1.0	-	%

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Continuous Output Load Current	I_{IMG25}				mA
Active Mode		-	-	80	
Low Power Mode		-	-	1.6	
Current Limit	$I_{LIMIMG25}$	-	120	-	mA
Transient Load Change	ΔI_{IMG25}	-	-	10	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{IMG25} = 60 mA, V_{33} = 3.3 V)	$PSRR_{IMG25}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QIMG25}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VIMG28 ELECTRICAL CHARACTERISTICS					
Input Voltage Range					V
Supplied by V_{33} DC/DC	V_{33}	3.168	3.3	3.432	
Supplied by V_{PWR}	V_{PWR}	3.0	3.6	4.4	
Output Voltage Setting	V_{IMG28}	(Selectable, see Table 58)			V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{IMG28UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{IMG28UVH}$	-	1.0	-	%
Continuous Output Load Current	I_{IMG28}				mA
Active Mode		-	-	225	
Low Power Mode		-	-	4.5	
Current Limit	$I_{LIMIMG28}$	-	337.5	-	mA
Transient Load Change	ΔI_{IMG28}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{IMG28} = 169 mA, V_{33} = 3.3 V)	$PSRR_{IMG28}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QIMG28}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VVIB ELECTRICAL CHARACTERISTICS					
Input Voltage Range[5]	V_{PWR}	3.0	3.6	4.4	V
Output Voltage Setting	V_{VIB}	(Selectable, see Table 59)			V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{VIBUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{VIBUVH}	-	1	-	%
Continuous Output Load Current	I_{VIB}				mA
Active Mode		-	-	200	
Low Power Mode		-	-	4.0	
Current Limit	I_{LIMVIB}	-	300	-	mA
Transient Load Change	ΔI_{VIB}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{VIB} = 150 mA, V_{PWR} = 3.6 V)	$PSRR_{VIB}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QVIB}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VSDIO ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{33}	3.168	3.3	3.432	V
Output Voltage Setting	V_{SDIO}	(Selectable, see Table 60)			V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{SDIOUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{SDIOUVH}$	-	1.0	-	%
Continuous Output Load Current	I_{SDIO}				mA
Active Mode		-	-	215	
Low Power Mode		-	-	4.3	
Current Limit	$I_{LIMSDIO}$	-	322.5	-	mA
Transient Load Change	ΔI_{SDIO}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{SDIO} = 161 mA, V_{33} = 3.3 V)	$PSRR_{SDIO}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QSDIO}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	

Notes

5. PVINVIB pin has to always be connected to VPWR node, even if the vibrator is not used.

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SWITCHES ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{33}	3.168	3.3	3.432	V
Drop Across Switch with reference to V_{33} VGPS33, VYMXGPS33, and VPNL33	-	-	-	3.0	%
Continuous Output Load Current VPNL33 VGP33 VYMXGPS33	 I_{PNL33} I_{GP33} $I_{YMXGPS33}$	 - - -	 - - -	 100 60 60	mA
LCD BACKLIGHT DRIVERS (WLED) ELECTRICAL CHARACTERISTICS					
Current Sink Capability per string	I_{SINK}	-	-	30	mA
LED Forward Voltage Range	V_F	-	-	4.0	V
LED Current Accuracy (I_{SINK} = 10 mA) T = 25°C	-	-3.0	-	3.0	%
LED Current Matching Accuracy T = 25°C	-	-2.0	-	2.0	%
CAMERA SCENE ILLUMINATION DRIVERS ELECTRICAL CHARACTERISTICS					
Current Sink Capability	I_{SINK}	-	-	30	mA
LED Forward Voltage Range	V_F	-	-	4.0	V
LED Current Accuracy (I_{SINK} = 10 mA) T = 25°C	-	-3.0	-	3.0	%
LED Current Matching Accuracy (When used as backlight 4th string) T = 25°C	-	-2.0	-	2.0	%
SIGNALING/STATUS LED DRIVERS ELECTRICAL CHARACTERISTICS					
LED Absolute Current Tolerance	-	-	0	15	%
LED Current Sink capability (Selectable)	-	0	-	28	mA
LED Current Matching Within Banks (With Respect to Average Current in the Bank, V_{DRIVER} = 400 mV, I_{LED} = 20 mA)	-	-	-	5.0	%
LED Channel Off Current (LED Disabled)	-	-	0	1.0	µA
Quiescent Consumption (Duty Cycle set to 000000, Current Levels set to 00)	-	-	10	-	µA
LED Current Sink Headroom	-	0.3	0.4	-	mV
Driver Pin Voltage Range	-	0	-	6.0	V
POWER PATH MANAGER PLUS LI-ION CHARGER ELECTRICAL CHARACTERISTICS					
Input voltage Range (Normal Operation)	V_{RAWCHG}	4.75	5.00	5.25	V
Input Voltage Rising Detection Threshold	$V_{RAWCHGDET}$	-	-	4.5	V
Input Voltage Rising Detection Threshold Hysteresis	$V_{RAWCHGDETHYS}$	-	100	-	mV
Input Over-voltage Protection Threshold	$V_{RAWCHOVP}$	5.50	5.75	6.00	V
Input Over-voltage Protection Threshold Hysteresis	$V_{RAWCHOVPHYS}$	-	75	-	mV

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
V_{PWR} Output Voltage Range $V_{BAT} < V_{TRKL}$	V_{PWR}	- -	 4.2	 -	V
V_{PWR} Output Voltage Range 100% Duty-cycle mode	V_{PWR}	- -	 -	 4.7	V
Constant Charge Voltage (V_{CHRGCV}) Accuracy Initial Accuracy at 25°C -20°C to 70°C -40°C to 85°C	-	 -0.2 -0.8 -1.0	 - - -	 +0.2 +0.8 +1.0	%
Battery Charge Voltage	V_{CHGCV}	Selectable, CHRGCV Register on Table 79			V
Battery Charge Voltage Over-voltage Threshold (V_{CHGCV} + Setting)	$V_{OVRVOLT}$	Selectable, see CHRGPROT Register on Table 79			mV
Maximum Continuous Input Average Current	-	Selectable, see CHRGPROT Register on Table 79			mA
Maximum Continuous Input Average Current Accuracy	-	-5.0	-	5.0	%
Trickle Charge Threshold Voltage	V_{TRKL}	-	3.0	-	V
Trickle Charge Threshold Accuracy	-	-3.0	-	+3.0	%
Constant Charge Current Range	I_{CHGCC}	Selectable, see CHRGCNTL Register on Table 79			mA
Discharge Current Over-current Threshold	I_{BATOC}	Selectable, see BATOCP Register on Table 67			A
Constant Charge Current Accuracy I_{CC} < 400 mA I_{CC} > 400 mA	-	 -15 -10	 - -	 +15 +10	%
Trickle Charge Current Value	I_{TRKL}	Selectable, see Table 81			mA
Trickle Charge Current Accuracy	-	-30	-	+30	%
EOC Detect Threshold	$I_{CHGCOMP}$	Selectable, see CHRGCNTL Register on Table 79			mA
EOC Detect Threshold Accuracy	-	-12	-	+12	%
Discharge Indication Threshold (Used to turn on M_{CHGBYP})	$V_{BAT} - V_{PWR}$	100	-	-	mV
NTC Bias Voltage	V_{NTC}	-	V_{CORE}	-	V
NTC Low Temperature Threshold (As a ratio of V_{NTC}, 3500 B factor) During Charging (0°C) During Discharging (-10°C)	V_{COLD}	 - -	 0.746 0.825	 - -	 - -
NTC Low Temperature Hysteresis	$V_{COLDHYS}$	-	0.06	-	-
NTC High Temperature Threshold (As a ratio of V_{NTC}, 3500 B factor) During Charging (45°C) During Discharging (60°C)	V_{HOT}	 - -	 0.324 0.227	 - -	 - -
NTC High Temperature Hysteresis	V_{HOTHYS}	-	0.06	-	-

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
ADC ELECTRICAL CHARACTERISTICS					
Conversion Current	-	-	-	1.2	mA
OFF Supply Current	-	-	-	1.0	µA
Converter Reference Voltage	-	-	2.4	-	V
Integral Nonlinearity (Rs = 5.0 kΩ maximum) (6)	-	-	-	±3.0	LSB
Differential Nonlinearity (Rs = 5.0 kΩ maximum) (6)	-	-	-	±1.0	LSB
Zero Scale Error (Offset) (Rs = 5.0 kΩ maximum) (6)	-	-	-	10	LSB
Full Scale Error (Gain) (Rs = 5.0 kΩ maximum) (6), (10)	-	-	-	11	LSB
Drift Over Temperature				±2.0	LSB
Source Impedance					
No Bypass Capacitor at Input	-	-	-	5.0	kΩ
Bypass Capacitor at Input of (10 nF)	-	-	-	30	kΩ
Input Buffer Input Range(7)	-	0.02	-	2.4	V
BATTERY CURRENT READING					
Amplifier (8) Gain	-	19	20	21	-
Amplifier Offset	-	-2.0	-	2.0	mV
Sense Resistor	-	-	20	-	mΩ
BATTERY THERMISTOR INTERFACE TARGET					
Thermistor Input Range	-	2.0	-	100	k
Internal Current Source	-	-	20	-	µA
Absolute Resistance Measurement Inaccuracy Over Temperature	-	-	10	-	%
Battery Removal Detection Threshold (9)	-	-	31/32* V_{NTC}	-	V
COULOMB COUNTER					
Sense Resistor R_{CC}	-	-	20	-	mΩ
Sense Current though R_{CC}	-	+/-1.0	-	+/-3000	mA
Quiescent Current Consumption	-	-	10	20	µA
Resolution (1LSB Increment in CCOUT with ONEC=1)	-	-	366.2	-	µC

Notes
6. Rs represents a possible external series resistor between the voltage source and the ADIN input.
7. Refer to Table 96 for analog valid input range and input buffer range characteristics for each ADC Channel
8. Amplifier bias current accounted for in overall ADC current drain
9. This is equivalent to a 10 kΩ pull-up and a 10 kΩ thermistor at -35°C
10. At room temperature

Table 3. Static Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
GPIOS ELECTRICAL CHARACTERISTICS					
GPIO Voltage Level (This is wired externally though GPIOVCC pin)	$V_{GPIOVCC}$	-	1.8V, 2.5V, 3.3V	-	V
GPOSW Voltage Level (This is wired externally though GPOSWVCC pin)	$V_{GPOSWVCC}$	-	V_{BAT}	-	V
GPO Voltage Level (This is wired externally though GPOVCC pin)	V_{GPOVCC}	-	1.8V, 2.5V, 3.3V	-	V
Accuracy for GPIOVCC, GPOVCC	-	-5.0	-	5.0	%
GPIO Output Drive Capability	-	-	20	-	Ω
GPOSW Typical Drive Capacitance	Look at the Si8407DB PFET as an example for maximum drive capability				
Input Low Voltage	V_{IL}	0	-	$0.3*V_{CC}$	V
Input High Voltage	V_{IH}	$0.7*V_{CC}$	-	V_{CC}	V
Output Low Voltage ($V_{CC} = V_{CC\_MIN}$, I_{OL} = 4.0 mA)	V_{OL}	-	-	0.1	V
Output High Voltage ($V_{CC} = V_{CC\_MIN}$, I_{OH} = -4.0 mA)	V_{OL}	V_{CC}-0.1	-	-	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE TIMING AND LOGIC IO					
Time SPICSB has to be low before the first rising edge of SPICLK	t_{SELSU}	20	-	-	ns
Time SPICSB has to remain low after the last falling edge of SPICLK	t_{SELHLD}	20	-	-	ns
Time SPICSB has to remain high between two transfers	$t_{SELHIGH}$	20	-	-	ns
Clock period of SPICLK (Equivalent to a maximum clock frequency of 25 MHz)	t_{CLKPER}	40	-	-	ns
Part of the clock period where SPICLK has to remain high	$t_{CLKHIGH}$	18	-	-	ns
Part of the clock period where SPICLK has to remain low	t_{CLKLOW}	18	-	-	ns
Time MOSI has to be stable before the next falling edge of SPICLK	t_{WRTSU}	5.0	-	-	ns
Time MOSI has to remain stable after the falling edge of SPICLK	t_{WRTHLD}	5.0	-	-	ns
Time MISO will be stable before the next falling edge of SPICLK	t_{RDSU}	5.0	-	-	ns
Time MISO will remain stable after the falling edge of SPICLK	t_{RDHLD}	5.0	-	-	ns
Time MISO needs to become active after the falling edge of SPICSB	t_{RDEN}	Refer to Figure 5 for more details			
Time MISO needs to become inactive after the rising edge of SPICSB	t_{RDDIS}	5.0	-	-	ns
VIDEN/VID TIMING SPECIFICATION					
VIDEN/VID Debounce time	t_{DB}	100	-	400	ns
VIDEN Invalid State Hold Time	t_{HOLD}	1.0	-	-	µs
OSCILLATOR AND CLOCK OUTPUTS MAIN CHARACTERISTICS					
RTC OSC Startup Time (Upon Application of Power)	-	-	-	500	ms
26 MHz OSC Startup Time	-	-	-	1.0	ms
RTC					
RTC Clock Frequency, Crystal OSC Nominal Frequency	-	-	32.768	-	KHz
VCC ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CC}/t	-	-	1	A/ns
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V (25 mV/s))	t_{SSCC}	-	-	0.06	ms
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{CCOFF}	-	-	1	ms
DAC Slew Rate	-	-	25	-	mV/µs
Switching Frequency	f_{SW}	-	1.0	-	MHz
VNN ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{NN}/t	-	-	1.0	A/ns
Soft Start Time (Enable to output voltage ramp up from 0 V to 1.0 V (25 mV/s))	t_{SSNN}	-	-	0.06	ms
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{NNOFF}	-	-	1.0	ms
DAC Slew Rate	-	-	25	-	mV/µs
Switching Frequency	f_{SW}	-	1.0	-	MHz

Table 4. Dynamic Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VDDQ ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{DDQ}/t	-	-	1.0	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	t_{SSDDQ}	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{DDQOFF}	-	-	1.0	ms
Switching Frequency	f_{SW}	-	4.0	-	MHz
V21 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{21}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 V to 2.1 V)	t_{SS21}	-	-	84	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{21OFF}	-	-	1.0	ms
Switching Frequency	f_{SW}	-	4.0	-	MHz
V15 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{15}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.1 V)	t_{SS15}	-	-	100	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{15OFF}	-	-	1.0	ms
Switching Frequency	f_{SW}	-	4.0	-	MHz
VYMX3G ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{YMX3G}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.1 V)	$t_{SSYMX3G}$	-	-	0.5	ms
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{YMX3GOFF}$	-	-	1.0	ms
Transition Time (3G mode), VOUT delta = ±0.3 V with 100 mA load current	$t_{YMX3GTRAN}$	-	-	100	µs
Switching Frequency	f_{SW}	-	4.0	-	MHz
VYMXPA ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{YMXPA}/t	-	-	0.03	A/µs
Soft Start Time No Load Full Load	$t_{SSYMXPA}$	 - -	 0.5 2.0	 - -	ms
Turn Off Time	$t_{YMXPAOFF}$	-	1.0	-	ms
Switching Frequency	$f_{SWYMXPA}$	-	2.0	-	MHz
VOTG ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{OTG}/t	-	-	0.03	A/µs
Soft Start Time No Load Full Load	t_{SSOTG}	 - -	 0.5 2.0	 - -	ms
Turn Off Time	t_{OTGOFF}	-	1.0	-	ms
Switching Frequency	f_{SWOTG}	-	2.0	-	MHz
VBKLT ELECTRICAL CHARACTERISTICS					
Soft Start Time	t_{SSBKLT}	-	2.0	-	ms
Switching Frequency	f_{SWBKLT}	-	2.0	-	MHz

Table 4. Dynamic Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VBG ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{BG}/t	-	-	0.001	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	t_{SSBG}	-	-	20	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{BGOFF}	-	-	5.0	ms
VCCA ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CCA}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.5 V)	t_{SSCCA}	-	-	30	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{CCAOFF}	-	-	5.0	ms
VCC180 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CC180}/t	-	-	1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	$t_{SSCC180}$	-	-	30	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{CC180OFF}$	-	-	5.0	ms
VPNL18 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{PNL18}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	$t_{SSPNL18}$	-	-	140	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{PNL18OFF}$	-	-	5.0	ms
VPMIC ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{PMIC}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	t_{SSPMIC}	-	-	700	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{PMICOFF}$	-	-	5.0	ms
VYMXYFI18 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	$I_{YMXYFI18}/t$	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	$t_{SSYMXYFI18}$	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{YMXYFI18OFF}$	-	-	5.0	ms
VYMXYFI ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{YMXYFI}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V for WiFiBT applications and 0 to 1.8 V for WiMAX applications) WiFiBT Applications WiMAX Applications	$t_{SSYMXYFI}$	 - -	 - -	 20 35	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{YMXYFIOFF}$	-	-	5.0	ms
VYMXGPS ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{YMXGPS}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V for WiMAX applications and 0 to 1.8 V for GPS applications) WiMAX Applications GPS Applications	$t_{SSYMXGPS}$	 - -	 - -	 15 15	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{YMXYFIGPSOFF}$	-	-	5.0	ms

Table 4. Dynamic Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VCCPAOAC ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	$I_{CCPAOAC}/t$	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	$t_{SSCCPAOAC}$	-	-	30	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{CCPAOACOFF}$	-	-	5.0	ms
VCCPDDR ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CCPDDR}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	$t_{SSCCPDDR}$	-	-	35	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{CCPDDROFF}$	-	-	5.0	ms
VAON ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{AON}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	t_{SSAON}	-	-	25	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{AONOFF}	-	-	5.0	ms
VMM ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{MM}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.2 V)	t_{SSMM}	-	-	125	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{MMOFF}	-	-	5.0	ms
VCCP ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CCP}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	t_{SSCCP}	-	-	26	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{CCPOFF}	-	-	5.0	ms
VIMG25 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{IMG25}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.5 V)	$t_{SSIMG25}$	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{IMG25OFF}$	-	-	5.0	ms
VIMG28 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{IMG28}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.9 V)	$t_{SSIMG28}$	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{IMG28OFF}$	-	-	5.0	ms
VVIB ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{VIB}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.7 V)	t_{SSVIB}	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{VIBOFF}	-	-	5.0	ms
VSDIO ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{SDIO}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	t_{SSSDIO}	-	-	100	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{SDIOOFF}$	-	-	5.0	ms

Table 4. Dynamic Electrical Characteristics

T_A = -40 °C to 85 °C, V_{PWR} = 3.0 to 4.4 V, typical external component values, and full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SWITCHES ELECTRICAL CHARACTERISTICS					
Ramp Up Time	-	-	-	50	µs
LCD BACKLIGHT DRIVERS (WLED) ELECTRICAL CHARACTERISTICS					
PWM Frequency (Register Setting)	f_{PWM}	128	-	8192	Hz
PWM Frequency Accuracy	-	-10	-	10	%
PWM Duty Cycle Resolution	-	-	-	8.0	Bit
Backlight string minimum on time	-	-	2.0	-	s
PWM Duty Cycle Accuracy	-	-0.3	-	0.3	%
CAMERA SCENE ILLUMINATION DRIVERS ELECTRICAL CHARACTERISTICS					
PWM Frequency	f_{PWM}	-	256	-	Hz
PWM Frequency Accuracy	-	-10	-	10	%
PWM Duty Cycle Resolution	-	-	-	3.0	Bit
POWER PATH MANAGER PLUS LI-ION CHARGER ELECTRICAL CHARACTERISTICS					
Input Over-voltage Protection Threshold Response Time (M_{OVPCHG} FET OFF)	t_{OVP}	-	2.0	5.0	µs
Trickle Charge Threshold Filter Time	-	-	32	-	ms
EOC Detect Threshold Filter Time	-	-	1.0	-	ms
ADC ELECTRICAL CHARACTERISTICS					
Conversion Time Per Channel	-	-	-	10	µs
Turn on/off Time				31	µs

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The 900841 is a high efficiency Power Management Integrated Circuit(PMIC), incorporating a Li-Ion battery charger. It is optimized for Ultra-mobile platforms of which Mobile Internet Devices(MID) are representative. Other end-user applications include but are not limited to Netbooks, Tablets, Slates, and Smartphones.

The 900841 PMIC, along with the companion chip 900842, is designed for optimum partitioning, as an integral part of Freescale's power management solution to meet the needs of Ultra-mobile platforms.

Optimum partitioning, high feature integration, and state of the art technology, enable Freescale to support Ultra-mobile platforms that are cost effective, by reducing component count and board area. The Freescale solution also allows ease of system design, resulting in a faster time to market development cycle.

It accepts input from commonly available single-cell Li-Ion (Li+) or Li-Polymer battery, and delivers regulated power to various components (CPU, chip sets, wireless, memory, storage, display, sensors, and others) on Ultra-mobile platforms.

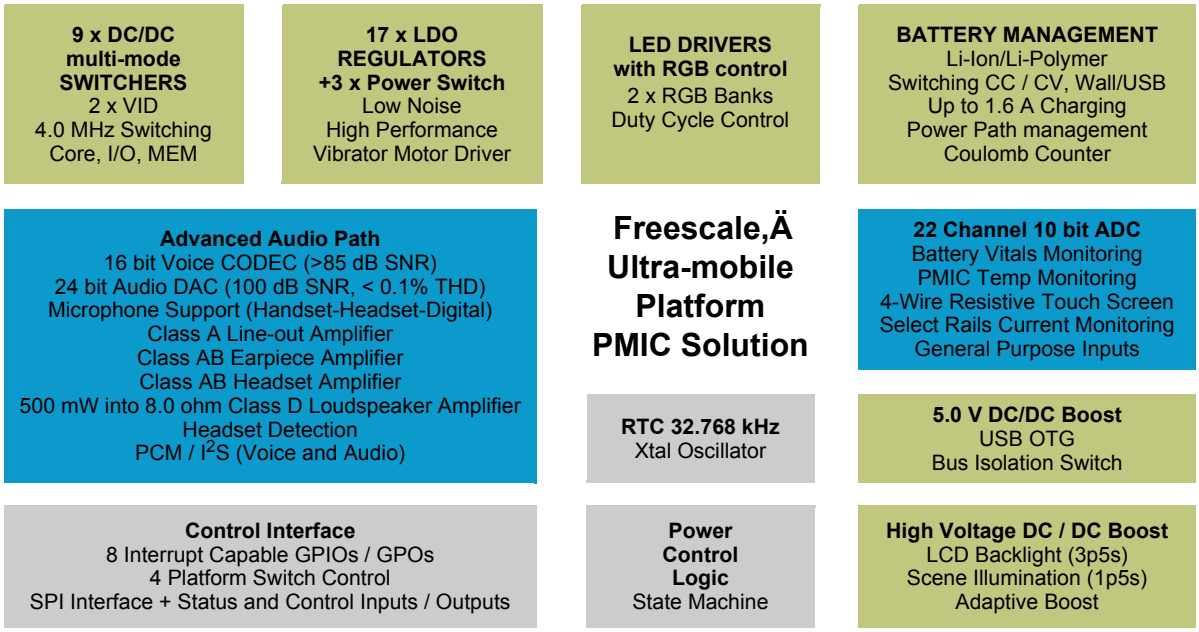

Figure 2. Freescale's Ultra-mobile Platform Power Management Solution High Level Block Diagram

FEATURE LIST

- Complete system power management, battery charging and audio support integrated in a single chip reducing board space and component count
- Ultra-mobile platform Architecture Support
- Audio System Capabilities:
  - PCM / I^2S (Voice & Audio) - All formatting and flexibility including automatic sample rate detection in slave mode
  - 16 bit Voice CODEC (>85 dB SNR)
  - 24 bit Audio DAC (100 dB SNR, <0.1%THD)
  - Microphone Support
    - Handset with bias / Headset with bias and detection / Digital with clock
  - Stereo Line Inputs
  - Single ended outputs Class A Line-Out Amplifier
    - 2.0 V_{PP} into 10 kΩ
  - Battery supplied Class AB Ear piece Amplifier with differential outputs
    - 4.0 V_{PP} into 32 Ω
  - Single ended output Class AB Headset Amplifier with negative charge pump for capacitor less headset coupling
    - 20 mWrms typical per channel
    - Headset insertion/stereo detection circuit

- 500 mW into 8.0 Ω Class-D Loudspeaker Amplifier with differential outputs
- Fully Programmable DC/DC Switching, Low Drop-Out Regulators, and Load Switches
  - Delivers regulated reliable power to various system components
  - High efficiency multi mode power conversion ensuring extended battery life
  - Fully programmable with extensive protection features and complete fault reporting for best in class overall system reliability
  - Internal Compensation
  - 6 Buck DC/DC Regulators
    - 2x VID Controlled with 1.0 MHz switching and external switches for CPU and Graphics core support
    - 4x with 4.0 MHz switching and integrated switches for system support and LDO supply for optimized thermal performance and power efficiency
  - 3 Boost DC/DC Regulators (Non-Synchronous with integrated low side switch)
    - High voltage boost regulator for backlight support
    - 5.0 V boost regulator for RGB LED supply and OTG Host Mode support
    - 4.2 V boost regulator for WiMAX PA supply support
  - 17 Low Drop-Out (LDO) regulators including a vibrator motor regulator
  - 1 configurable LDO/Switch regulator for SDIO card support
  - Three 3.3 V load switches for system support
- Power Path Management & Switching Mode Li-Ion/Li-Polymer Battery Charger
  - Efficient switching Li-Ion battery charger allowing for reduced power dissipation and reduced charge time
  - Power path management that allows power to the system even in the absence of the battery through an external power supply
  - Programmable options for various charging parameters
  - Charger input over-voltage protection
  - Battery vitals monitoring/reporting/protecting
  - Coin Cell Backup battery charger
- LCD Backlight support with up to 15 LEDs (3p5s)
- Camera Scene Illumination support (1p5s)
- 2xRGB banks LED drivers with optimized LED control
- SPI interface supporting Ultra-mobile Platform architecture (up to 25 MHz operation)
- 22-channel (32 capable) 10-bit ADC for internal and external sensing with touch screen interface
- Low power 32.786 kHz XTAL oscillator.
- Real Time Clock (RTC) to provide time reference and alarm functions with wake up control.
- 8 Interrupt capable GPIOs and 8 GPOs
- 4 GPOs for controlling platform switches
- Various control and status reporting I/Os
- Interrupt and Reset controller. All interrupt signals can be masked.
- Overall solution size target of < 900 mm^2 (including clearance and routing)
- Operating temperature of -40°C to +85°C

INTERNAL BLOCK DIAGRAM

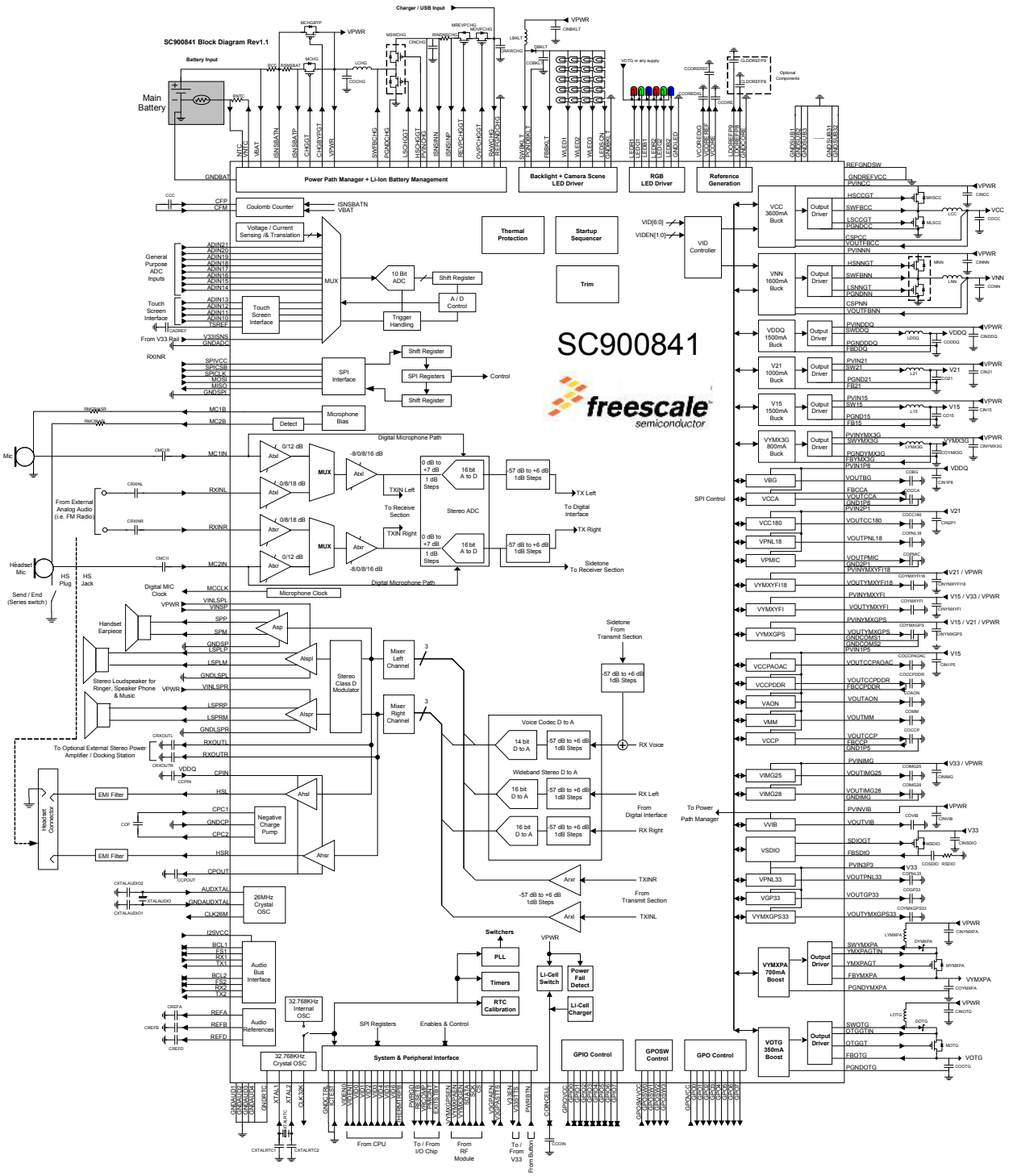

Figure 3. Functional Block Diagram

PIN OUT DESCRIPTION AND BALL MAP

Refer to Pin Description for a detailed list of pins and ball assignments. The ball map of the package is given in Figure 4 as a top view. The BGA footprint on the application PCB will have the same mapping as given in Figure 4.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC1		NC1		PVIN1P5		FBCCP		SDATA		PVIN2P1		VOUT PNL18		SPICLK		REFD		GND LSPR		GND LSPL		HSL		REFB		NC2		NC2
B		NC1		VOUTCC PAOAC		LDO REFP8		CS		VOUT PMIC		VOUT CC180		VCORE		PMICINT		VINLSPR		VYMX3G EN		LSPLP		HSR		REFA		NC2	
C	NC1		VOUT CCA		PVIN1P5		VOUT AON		VOUT CCP		PVIN2P1		VCORE REF		RESETB		LSPRP		VYMXPA EN		VINLSPL		RXINR						NC2
D		VOUTBG		VIDEN0		PVIN1P8								SPICSB				LSPRM		LSPLM								CPC2	
E	VID2		VID0		VIDEN1		FBCCA																		CPOUT		GNDCP		CPC1
F		VID6		VID4																								CPIN	
G	CSPCC		SWFBCC				FBCC PDDR		VOUTCC PDDR		PWRBTN		LDO REFP9		MOSI		THERM TRIPB		VYMX GPSEN		GND AUD4		GND AUD1				AUD XTAL		GNDAUD XTAL
H		LSCCGT		LSCCGT				VID1		GND1P5		SCK		GND CORE		VRCOMP		GNDSUB		RXINL		GNDSUB				CLK26M		RX2	
J	PGNDCC		PGNDCC				VID5		VID3		VOUTMM		VCORE DIG		MISO		EXITSTB Y		GNDSUB		GNDSUB		GNDSUB				FS2		BCL2
K		HSCCGT		HSCCGT				VOUT FBCC														TX1				TX2		BCL1	
L	HSNNGT		PVINNN		PVINCC		PVINCC		PGNDNN		GNDREF VCC		GNDSPI		SPIVCC		GNDSUB		GNDSUB		GND AUD2		RX1		I2SVCC		FS1		SPM
M		LSNNGT		VOUT FBNN		PGND DDQ		PGND DDQ				GND2P1		GNDSUB		PWRGD		GNDSUB				MCCLK						GNDSP	
N	SWDDQ		SWDDQ		PGND DDQ		PGND DDQ		SWFBNN		CSPNN		GND1P8		GNDSUB		GNDSUB		GNDSUB		MC2IN		MC2B				VINSP		SPP
P		SWDDQ		SWDDQ		PVINDDQ		PVINDDQ				GNDSUB		GNDSUB		GNDSUB		GNDSUB				MC1IN				MC1B		RXOUTR	
R	PGND YMX3G		PGND YMX3G		PVINDDQ		PVINDDQ		FBDDQ		GNDSUB		GNDSUB		GNDSUB		GNDSUB		GND AUD3		RXOUTL		ICTEST				LEDB2		GNDLED
T		SWYMX 3G		SWYMX 3G		PVINYMX 3G		PVINYMX 3G				GNDSUB		GNDSUB		GNDSUB		GNDSUB				GNDSUB				LEDG2		LEDR1	
U	PGND21		PGND21		PGND21		REFGND SW		FBYMX 3G		GNDSUB		GNDSUB		GNDSUB		GNDSUB		GNDSUB		OTGGTIN		LEDG1		LEDR2		SWOTG		SWOTG
V		SW21		SW21		SW21		FB21				GNDSUB		GNDIMG		GNDADC		GNDSUB				LEDB1		FBOTG		PGND OTG		PGND OTG	
W	PVIN21		PVIN21		PVIN21		FB15				GND COMS2		FB YMXPA		ADIN20		TSREF		V33STTS		OTGGT		FBBKLT		LEDSCN		SWBKLT		SWBKLT
Y		PGND15		PGND15		PGND15		GPO4														WLED3				PGND BKLT		PGND BKLT	
AA	SW15		SW15		SW15		GND COMS1		GPOSW0		GPIO3		YMXPA GTIN		YMXPA GT		ADIN13		REV PCHGGT		GNDBAT		V3GPA EN		V3GPA STTS		WLED1		WLED2
AB		PVIN15		PVIN15		PVIN15		GPO7		GPIO1		SDIOGT		GND CTRL		ADIN11		GPIO6		V33EN		CFP				VPWR		GND BKLT	
AC	PVIN YMXGPS		VOUT YMXGPS				GPO1		GPOSW VCC		GPIOVCC		FBSDIO		ADIN21		ADIN15		GPIO4		REFGND CHG		NTC		CHGBYP GT		VBAT		COIN CELL
AD		PVIN YMXYFI18		GPO2								PGND YMXPA										PVINCHG				ISNS BATP		CFM	
AE	VOUT YMXYFI18		PVINYMX YFI		GPOVCC						SW YMXPA						ADIN14				OVPCHG GT		ISNSINP		LSCHG GT		CHGGT		VNTC
AF		VOUTYM XYFI		GPO0		GPOSW1						PGND YMXPA						XTAL2		GPIO5		PVINCHG		HSCHG GT		PGND CHG		ISNS BATN	
AG	NC3		GPO3		GPO6		GPIO0		VOUT PNL33		SW YMXPA		PVINVIB		VOUT IMG28		ADIN16		XTAL1		GPIO7		RAW CHG		LSCHG GT		ISNSINN		NC4
AH		NC3		GPO5		GPOSW3		VOUT GP33		VOUTYM XGPS33		PGND YMXPA		VOUT IMG25		ADIN19		ADIN17		ADIN10		CLK32K		HSCHG GT		PGND CHG		NC4	
AJ	NC3		NC3		GPOSW2		GPIO2		PVIN3P3		SW YMXPA		VOUTVIB		PVINIMG		ADIN18		ADIN12		GNDRTC		V33ISNS		SWFB CHG		NC4		NC4

Figure 4. SC900841 Package Ball Map (Top view)

PIN DESCRIPTION

The Type Column indicates the maximum average current through each ball assigned to the different nodes, 500 mA maximum for HIPWR, 300 mA maximum for MDPWR, and 100 mA maximum for LOPWR

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
VCC - (0.65 V-1.2 V) / 3.5 A VID CPU BUCK with External FETs						
PVINCC	HIPWR	-	4.8 V	2	L5, L7	Gate Drivers Power Supply Input
HSCCGT	HIPWR	-	4.8 V	2	K2, K4	High Side FET Gate Drive
LSCCGT	HIPWR	-	4.8 V	2	H2, H4	Low Side FET Gate Drive
PGNDCC	HIPWRGND	-	-	2	J1, J3	Local Ground for Internal Circuitry
VOUTFBCC	SGNL	I	4.8 V	1	K8	Output Voltage Sensing Input and Negative Current Sense Terminal
SWFBCC	SGNL	I	3.6 V	1	G3	Switch Node Feedback
CSPCC	SGNL	I	3.6 V	1	G1	Positive Current Sense Terminal
VNN - (0.65 V-1.2 V) / 1.6 A VID CPU BUCK with External FETs						
PVINNN	HIPWR	-	4.8 V	1	L3	Gate Drivers Power Supply Input
HSNNGT	HIPWR	-	4.8 V	1	L1	High Side FET Gate Drive
LSNNGT	HIPWR	-	4.8 V	1	M2	Low Side FET Gate Drive
PGNDNN	HIPWRGND	-	-	1	L9	Local Ground for Internal Circuitry
VOUTFBNN	SGNL	I	4.8 V	1	M4	Output Voltage Sensing Input and Negative Current Sense Terminal
SWFBNN	SGNL	I	3.6 V	1	N9	Switch Node Feedback
CSPNN	SGNL	I	3.6 V	1	N11	Positive Current Sense Terminal
VDDQ - 1.8 V / 1.3 A BUCK						
PVINDDQ	HIPWR	-	4.8 V	4	P6, P8, R5, R7	Power Supply Input
SWDDQ	HIPWR	-	4.8 V	4	N1, N3, P2, P4	Switch Node
PGNDDDQ	HIPWRGND	-	-	4	M6, M8, N5, N7	Power Ground
FBDDQ	SGNL	I	3.6 V	1	R9	Output Voltage Feedback Input
V21 - 2.1 V / 1.0 A BUCK						
PVIN21	HIPWR	-	4.8 V	3	W1, W3, W5	Power Supply Input
SW21	HIPWR	-	4.8 V	3	V2, V4, V6	Switch Node
PGND21	HIPWRGND	-	-	3	U1, U3, U5	Power Ground
FB21	SGNL	I	3.6 V	1	V8	Output Voltage Feedback Input
V15 - 1.5 V (or 1.6 V) / 1.5 A BUCK						
PVIN15	HIPWR	-	4.8 V	3	AB2, AB4, AB6	Power Supply Input
SW15	HIPWR	-	4.8 V	3	AA1, AA3, AA5	Switch Node
PGND15	HIPWRGND	-	-	3	Y2, Y4, Y6	Power Ground
FB15	SGNL	I	3.6 V	1	W7	Output Voltage Feedback Input
V33 Interface (SC900842)						
V33EN	SGNL	O	2.5 V	1	AB20	V33 Enable output pin
V33STTS	SGNL	I	2.5 V	1	W19	V33 Status input pin. Active low when V33 output is on
V33ISNS	SGNL	I	2.5 V	1	AJ23	Input Interface with the ADC to measure V33 output current

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
VYMX3G - (YMX: 1.25 V or 3G: 0.6 V-1.375 V) / 1.0 A BUCK						
PVINYMX3G	HIPWR	-	4.8 V	2	T6, T8	Power Supply Input
SWYMX3G	HIPWR	-	4.8 V	2	T2, T4	Switch Node
PGNDYMX3G	HIPWRGND	-	-	2	R1, R3	Power Ground
FBYMX3G	SGNL	I	3.6 V	1	U9	Output Voltage Feedback Input
VYMXPA - 4.2 V / 0.7 A Boost						
SWYMXPA	HIPWR	-	5.5 V	3	AE11, AG11, AJ11	Switch Node
PGNDYMXPA	HIPWRGND	-	-	3	AD12, AF12, AH12	Power Ground
FBYMXPA	SGNL	I	5.5 V	1	W13	Output Voltage Feedback Input
YMXPAGTIN	MDPWR	-	5.5 V	1	AA13	Gate Drive Input for VYMXPA isolation FET
YMXPAGT	MDPWR	-	5.5 V	1	AA15	Gate Driver for external switch if output isolation is required
V3GPA Interface (Reserved)						
V3GPAEN	SGNL	O	2.5 V	1	AA23	V3GPA Enable output pin. Reserved
V3GPASTTS	SGNL	I	2.5 V	1	AA25	V3GPA Status input pin. Reserved
VOTG - 5.0 V / 0.35 A Boost						
SWOTG	HIPWR	-	5.5 V	2	U27, U29	Switch Node
PGNDOTG	HIPWRGND	-	-	2	V26, V28	Power Ground
FBOTG	SGNL	I	5.5 V	1	V24	Output Voltage Feedback Input
OTGGTIN	MDPWR	-	5.5 V	1	U21	Gate Drive Input for VOTG Isolation FET
OTGGT	MDPWR	-	5.5 V	1	W21	Gate Driver for external switch if output isolation is required
VBKLT - 5s3p (Backlight) and 5s1p (Camera Scene) / 120 mA Boost						
SWBKLT	HIPWR	-	26 V	2	W27, W29	Switch Node
PGNDBKLT	HIPWRGND	-	-	2	Y26, Y28	Power Ground
FBBKLT	SGNL	I	26 V	1	W23	Output Voltage Feedback Input
VBG - 1.25 V/2 mA LDO VCCA - 1.5 V/150 mA LDO						
PVIN1P8	LOPWR	-	3.6 V	1	D6	Power Supply Input, shared by VBG and VCCA
GND1P8	GND	-	-	1	N13	Ground Reference
VOUTBG	LOPWR	-	2.5 V	1	D2	VBG Output Voltage Node
VOUTCCA	LOPWR	-	2.5 V	1	C3	VCCA Output Voltage Node
FBCCA	SGNL	I	2.5 V	1	E7	VCCA Output Voltage Feedback Input

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
VCC180- 1.8 V/390 mA LDO VPNL18- 1.8 V/225 mA LDO VPMIC - 1.8 V/50 mA LDO						
PVIN2P1	HIPWR	-	3.6 V	2	A11, C11	Power Supply Input, shared by VCC180, VPNL18, and VPMIC
GND2P1	GND	-	-	1	M12	Ground Reference
VOUTCC180	HIPWR	-	2.5 V	1	B12	VCC180 Output Voltage Node
VOUTPNL18	MDPWR	-	2.5 V	1	A13	VPNL18 Output Voltage Node
VOUTPMIC	LOPWR	-	2.5 V	1	B10	VPMIC Output Voltage Node
VYMXYFI18 - (YMX:1.8 V/200 mA - YFI:1.8 V/200 mA) LDO						
PVINYMXYFI18	MDPWR	-	4.8 V	1	AD2	Power Supply Input for VYMXYFI18
VOUTYMXYFI18	MDPWR	-	3.6 V	1	AE1	VYMXYFI18 Output Voltage Node
GNDCOMS1	GND	-	-	1	AA7	Ground Reference
GNDCOMS2	GND	-	-	1	W11	Ground Reference
VYMXYFI - (YMX:2.5 V/150 mA - YFI:1.2 V/60 mA) LDO						
PVINYMXYFI	MDPWR	-	4.8 V	1	AE3	Power Supply Input for VYMXYFI
VOUTYMXYFI	MDPWR	-	3.6 V	1	AF2	VYMXYFI Output Voltage Node
VYMXGPS - (YMX:1.3 V/350 mA - GPS:1.8 V/170 mA) LDO						
PVINYMXGPS	HIPWR	-	4.8 V	1	AC1	Power Supply Input for VYMXGPS
VOUTYMXGPS	HIPWR	-	3.6 V	1	AC3	VYMXGPS Output Voltage Node
VCCPAOAC- 1.05 V/155 mA LDO VCCPDDR - 1.05 V/60 mA LDO VAON - 1.2 V/250 mA LDO VMM- 1.2 V/5 mA LDO VCCP - 1.05 V/445 mA LDO						
PVIN1P5	HIPWR	-	3.6 V	2	A5, C5	Power Supply Input, shared by VCCPAOAC, VCCPDDR, VAON, VMM, and VCCP
GND1P5	GND	-	-	1	H10	Ground Reference
VOUTCCPAOAC	LOPWR	-	2.5 V	1	B4	VCCPAOAC Output Voltage Node
VOUTCCPDDR	LOPWR	-	2.5 V	1	G9	VCCPDDR Output Voltage Node
FBCCPDDR	SGNL	I	2.5 V	1	G7	VCCPDDR Output Voltage Feedback Input
VOUTAON	MDPWR	-	2.5 V	1	C7	VAON Output Voltage Node
VOUTMM	LOPWR	-	2.5 V	1	J11	VMM Output Voltage Node
VOUTCCP	HIPWR	-	2.5 V	1	C9	VCCP Output Voltage Node
FBCCP	SGNL	I	2.5 V	1	A7	VCCP Output Voltage Feedback Input
VIMG25- 2.5 V/80 mA LDO VIMG28- 2.8 V/225 mA LDO						
PVINIMG	MDPWR	-	4.8 V	1	AJ15	Power Supply Input, shared by VIMG25 and VIMG28
GNDIMG	GND	-	-	1	V14	Ground Reference
VOUTIMG25	LOPWR	-	3.6 V	1	AH14	VIMG25 Output Voltage Node
VOUTIMG28	MDPWR	-	3.6 V	1	AG15	VIMG28 Output Voltage Node

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
VVIB - xV/200 mA LDO						
PVINVIB	MDPWR	-	4.8 V	1	AG13	Power Supply Input for VVIB and Reference Generation. This must always be connected to VPWR.
VOUTVIB	MDPWR	-	3.6 V	1	AJ13	VVIB Output Voltage Node
VPNL33 - 3.3 V/100 mA Switch VGP33 - 3.3 V/60 mA Switch VYMXGPS33 - 3.3 V/60 mA Switch						
PVIN3P3	MDPWR	-	3.6 V	1	AJ9	Power Supply Input, shared by VPNL33, VGP33, VYMXGPS33 and VSDIO
VOUTPNL33	LOPWR	-	3.6 V	1	AG9	VPNL33 Output Voltage Node
VOUTGP33	LOPWR	-	3.6 V	1	AH8	VPG33 Output Voltage Node
VOUTYMXGPS33	LOPWR	-	3.6 V	1	AH10	VYMXGPS33 Output Voltage Node
VSDIO - 3.3 V/215 mA Switch OR 1.8 V/215 mA LDO						
SDIOGT	LOPWR	-	3.6 V	1	AB12	Gate Driver Output for VSDIO pass FET
FBSDIO	SGNL	-	3.6 V	1	AC13	Feedback node when VSDIO is in Switch mode; Output voltage node when VSDIO is in LDO mode.
Internal Supplies						
VCORE	LOPWR	-	3.6 V	1	B14	Internal Supply Output Voltage Node
VCOREDIG	LOPWR	-	1.5 V	1	J13	Internal Supply Output Voltage Node
VCOREREF	LOPWR	-	3.6 V	1	C13	Internal BandGap Supply Output Voltage Node
LDOREFP8	LOPWR	-	3.6 V	1	B6	Internal Divided Down BandGap Supply Output Voltage Node dedicated for LDOs
LDOREFP9	LOPWR	-	3.6 V	1	G13	Internal Divided Down BandGap Supply Output Voltage Node dedicated for LDOs
GNDCORE	LOPWRGND	-	-	1	H14	Ground for Internal Supplies
Audio Bus						
I2SVCC	LOPWR	-	3.6 V	1	L25	Supply Voltage to the I2S Bus
BCL1	SGNL	I/O	3.6 V	1	K28	Bit clock for audio bus 1. Input in slave mode, output in master mode
FS1	SGNL	I/O	3.6 V	1	L27	Frame synchronization clock for audio bus 1. Input in slave mode, output in master mode.
RX1	SGNL	I	3.6 V	1	L23	Receive Data for audio bus 1
TX1	SGNL	O	3.6 V	1	K22	Transmit data for audio bus 1
BCL2	SGNL	I/O	3.6 V	1	J29	Bit clock for audio bus 2. Input in slave mode, output in master mode
FS2	SGNL	I/O	3.6 V	1	J27	Frame synchronization clock for audio bus 2. Input in slave mode, output in master mode.
RX2	SGNL	I	3.6 V	1	H28	Receive Data for audio bus 2
TX2	SGNL	O	3.6 V	1	K26	Transmit data for audio bus 2

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
Audio Transmit						
MC1B	LOPWR	-	3.6 V	1	P26	Handset primary/right and secondary/left microphone bias supply
MC2B	LOPWR	-	3.6 V	1	N23	Headset microphone bias supply with integrated bias resistor and headset microphone detect
MC1IN	SGNL	I	3.6 V	1	P22	Handset primary or right microphone amplifier input. Requires external DC blocking capacitor
MC2IN	SGNL	I	3.6 V	1	N21	Headset microphone input. Requires external DC blocking capacitor
MCCLK	SGNL	O	3.6 V	1	M22	Digital MIC Clock output
RXINR	LOPWR	-	3.6 V	1	C23	Analog Audio Input R
RXINL	LOPWR	-	3.6 V	1	H20	Analog Audio Input L
Audio Receive						
VINLSPR	MDPWR	-	5.5 V	1	B18	Handset speaker-phone or alert differential power amplifier supply input, Right Channel
VINLSPL	MDPWR	-	5.5 V	1	C21	Handset speaker-phone or alert differential power amplifier supply input, Left Channel
LSPRP	MDPWR	-	5.5 V	1	C17	Handset speaker-phone or alert differential power amplifier positive terminal, Right Channel
LSPRM	MDPWR	-	5.5 V	1	D18	Handset speaker-phone or alert differential power amplifier minus terminal, Right Channel
LSPLP	MDPWR	-	5.5 V	1	B22	Handset speaker-phone or alert differential power amplifier positive terminal, Left Channel
LSPLM	MDPWR	-	5.5 V	1	D20	Handset speaker-phone or alert differential power amplifier minus terminal, Left Channel
VINSP	LOPWR	-	5.5 V	1	N27	Handset ear piece supply input
SPP	LOPWR	-	5.5 V	1	N29	Handset ear piece speaker differential amplifier output positive terminal
SPM	LOPWR	-	5.5 V	1	L29	Handset ear piece speaker differential power amplifier output minus terminal
GNDSP	LOPWRGND	-	-	1	M28	Ground Handset ear piece speaker
GNDLSPR	MDPWRGND	-	-	1	A19	Ground for Handset speaker-phone or alert differential power amplifier, Right Channel
GNDLSPL	MDPWRGND	-	-	1	A21	Ground for Handset speaker-phone or alert differential power amplifier, Left Channel
RXOUTL	LOPWR	-	4.8 V	1	R21	Analog Line Out, Left Channel
RXOUTR	LOPWR	-	4.8 V	1	P28	Analog Line Out, Right Channel
HSL	LOPWR	-	2.5 V	1	A23	Headset output to left channel ear piece
HSR	LOPWR	-	2.5 V	1	B24	Headset output to right channel ear piece
CPIN	LOPWR	-	3.6 V	1	F28	Negative Charge Pump Supply input and supply input to headset amplifier
CPC1	LOPWR	-	5.5 V	1	E29	Negative Charge Pump Capacitor Connection 1
CPC2	LOPWR	-	4.8 V	1	D28	Negative Charge Pump Capacitor Connection 2

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
CPOUT	LOPWR	-	6.6 V	1	E25	Negative Charge Pump Output
GNDCP	LOPWRGND	-	-	1	E27	Ground for negative charge pump
Audio 26 MHz Clock						
AUDXTAL	SGNL	I/O	2.5 V	1	G27	26 MHz Oscillator crystal connection 1
GNDAUDXTAL	GND	-	-	1	G29	26 MHz Oscillator crystal connection 2
CLK26M	SGNL	O	2.5 V	1	H26	26 MHz Oscillator clock output
Audio Other						
REFA	LOPWR	-	1.5 V	1	B26	Reference for audio amplifiers
REFB	LOPWR	-	1.5 V	1	A25	Reference for low noise audio bandgap
REFD	LOPWR	-	1.5 V	1	A17	Reference for stereo DAC
GNDAUD1	GND	-	-	1	G23	Ground for audio circuitry 1 (analog)
GNDAUD2	GND	-	-	1	L21	Ground for audio circuitry 2 (analog)
GNDAUD3	GND	-	-	1	R19	Ground for audio circuitry 3 (analog)
GNDAUD4	GND	-	-	1	G21	Ground for audio circuitry 4 (analog)
Lighting System						
WLED1	LOPWR	-	26 V	1	AA27	Backlight String #1 Current Feedback Input
WLED2	LOPWR	-	26 V	1	AA29	Backlight String #2 Current Feedback Input
WLED3	LOPWR	-	26 V	1	Y22	Backlight String #3 Current Feedback Input
LEDSCN	LOPWR	-	26 V	1	W25	Camera Scene Illumination LED driver output 1
GNDBKLT	GND	-	-	1	AB28	Ground for Backlight and Camera Scene LED drivers
LEDR1	LOPWR	-	5.5 V	1	T28	Tricolor red LED driver output 1
LEDG1	LOPWR	-	5.5 V	1	U23	Tricolor green LED driver output 1
LEDB1	LOPWR	-	5.5 V	1	V22	Tricolor blue LED driver output 1
LEDR2	LOPWR	-	5.5 V	1	U25	Tricolor red LED driver output 2
LEDG2	LOPWR	-	5.5 V	1	T26	Tricolor green LED driver output 2
LEDB2	LOPWR	-	5.5 V	1	R27	Tricolor blue LED driver output 2
GNDLED	GND	-	-	1	R29	Ground for RGB LED drivers
Switching Charger						
RAWCHG	MDPWR	-	20 V	1	AG23	Charger Input Voltage Detection Node
OVPCHGGT	MDPWR	-	20 V	1	AE21	Charger Input Over-voltage Protection FET Gate Drive
REVPCHGGT	MDPWR	-	20 V	1	AA19	Charger Input Reverse Current Protection FET Gate Drive
ISNSINP	SGNL	I	5.5 V	1	AE23	Charger Input Current Sensing Positive Terminal
ISNSINN	SGNL	I	5.5 V	1	AG27	Charger Input Current Sensing Negative Terminal
PVINCHG	HIPWR	-	5.5 V	2	AD22, AF22	Charger Buck Stage Input Voltage Node
HSCHGGT	HIPWR	-	5.5 V	2	AF24, AH24	Charger Buck High Side FET Gate Drive
SWFBCHG	SGNL	I	5.5 V	1	AJ25	Charger Buck Switch Node Feedback

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
LSCHGGT	HIPWR	-	5.5 V	2	AE25, AG25	Charger Buck Low Side FET Gate Drive
PGNDCHG	HIPWRGND	-	-	2	AF26, AH26	Charger Buck Stage Power Ground
VPWR	MDPWR	-	4.8 V	1	AB26	Charger Buck Output Voltage Sense Node and Main Input for System Supplies.
CHGGT	MDPWR	-	4.8 V	1	AE27	Charger FET Gate Drive
CHGBYPGT	MDPWR	-	4.8 V	1	AC25	Charger Bypass FET Gate Drive
ISNSBATP	SGNL	I	4.8 V	1	AD26	Battery/Charging Current Sensing Input Point 1
ISNSBATN	SGNL	I	4.8 V	1	AF28	Battery/Charging Current Sensing Input Point 2, Coulomb Counter Sensing Input Point 1
CFP	LOPWR	-	4.8 V	1	AB22	Accumulated Current Filter Capacitor Plus Terminal
CFM	LOPWR	-	4.8 V	1	AD28	Accumulated Current Filter Capacitor Minus Terminal
VBAT	LOPWR	-	4.8 V	1	AC27	Battery Voltage Sensing Input, Coulomb Counter Sensing Input Point 2
GNDBAT	LOPWRGND	-	-	1	AA21	Kelvin Sensing Connection To The Battery Ground
VNTC	LOPWR	-	3.6 V	1	AE29	Bias voltage for NTC resistor stack
NTC	SGNL	I	3.6 V	1	AC23	NTC connection node
Coin Cell Charger						
COINCELL	LOPWR	-	3.6 V	1	AC29	Coin cell Supply Input, Coin cell Charger Output
ADC + TS I/F						
ADIN10	SGNL	I	4.8 V	1	AH20	ADC Generic Input 1, Used as Touchscreen Input X1, TSX1
ADIN11	SGNL	I	4.8 V	1	AB16	ADC Generic Input 2, Used as Touchscreen Input X2, TSX2
ADIN12	SGNL	I	4.8 V	1	AJ19	ADC Generic Input 3, Used as Touchscreen Input Y1, TSY1
ADIN13	SGNL	I	4.8 V	1	AA17	ADC Generic Input 4, Used as Touchscreen Input Y2, TSY2
ADIN14	SGNL	I	4.8 V	1	AE17	ADC Generic Input 5
ADIN15	SGNL	I	4.8 V	1	AC17	ADC Generic Input 6
ADIN16	SGNL	I	4.8 V	1	AG17	ADC Generic Input 7
ADIN17	SGNL	I	4.8 V	1	AH18	ADC Generic Input 8
ADIN18	SGNL	I	4.8 V	1	AJ17	ADC Generic Input 9
ADIN19	SGNL	I	4.8 V	1	AH16	ADC Generic Input 10
ADIN20	SGNL	I	4.8 V	1	W15	ADC Generic Input 11
ADIN21	SGNL	I	4.8 V	1	AC15	ADC Generic Input 12
TSREF	LOPWR	-	3.6 V	1	W17	Reference for Touchscreen interface
GNDADC	LOPWRGND	-	-	1	V16	Ground Reference for ADC
Oscillator and Real Time Clock - RTC						
XTAL1	SGNL	I	2.5 V	1	AG19	32.768 kHz Oscillator crystal connection 1
XTAL2	SGNL	O	2.5 V	1	AF18	32.768 kHz Oscillator crystal connection 2
CLK32K	SGNL	O	3.6 V	1	AH22	32 kHz Clock output
GNDRTC	GND	-	-	1	AJ21	Ground for the RTC block

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
Ultra-mobile Platform Architecture Sideband Signals						
PMICINT	SGNL	O	2.5 V	1	B16	PMIC Interrupt. Asserted by PMIC to wake Platform controller hub and begin communications. Level-sensitive, read to clear.
VRCOMP	SGNL	O	2.5 V	1	H16	Voltage Regulator Complete. Asserted high by the PMIC when a SPI voltage regulation request has been decoded. The signal is de-asserted on completion of the request (i.e. the rail is in regulation).
RESETB	SGNL	O	2.5 V	1	C15	Active low hard reset for Platform controller hub. When asserted, Platform controller hub should return to its initial default state.
PWRGD	SGNL	O	2.5 V	1	M16	POWER GOOD: SC900841 asserts this signal to indicate that all power rails to Platform controller hub are good. Assertion of PWRGD also means that VCCA_OSC has been valid for at least 30 microseconds. The Platform Controller Hub will remain “off” until this signal is asserted.
EXITSTBY	SGNL	I	2.5 V	1	J17	EXIT Standby. When asserted, SC900841 exits the AOAC Standby settings for regulating the platform supplies. When asserted SC900841 switches VRs on which are defined in registers 0x09 through 0x0D. This is a low latency VR context switch.
THERMTRIPB	SGNL	I	1.5 V	1	G17	Thermal trip. Asserted by the CPU to indicate a catastrophic thermal event.
VIDEN0	SGNL	I	1.5 V	1	D4	Driven by the CPU to indicate which VR the VID bus is addressed to (VCC or VNN). Debounced inside SC900841 for 150 ns. The CPU will hold the value for at least 300 ns.
VIDEN1	SGNL	I	1.5 V	1	E5	
VID0	SGNL	I	1.5 V	1	E3	Driven by the CPU to indicate the output voltage setting for the VCC and VNN rails. Debounced inside SC900841 for 150 ns. The CPU will hold the value for at least 300 ns.
VID1	SGNL	I	1.5 V	1	H8	
VID2	SGNL	I	1.5 V	1	E1	
VID3	SGNL	I	1.5 V	1	J9	
VID4	SGNL	I	1.5 V	1	F4	
VID5	SGNL	I	1.5 V	1	J7	
VID6	SGNL	I	1.5 V	1	F2	
VYMXGPSEN	SGNL	I	2.5 V	1	G19	Enable Input signal for the VYMXGPS rail. Asserted by the communications subsystem to enable a supply voltage with minimal latency.
VYMXPAEN	SGNL	I	2.5 V	1	C19	Enable Input signal for the VYMXPA rail. Asserted by the communications subsystem to enable a supply voltage with minimal latency.
VYMX3GEN	SGNL	I	2.5 V	1	B20	Enable Input signal for the VYMX3G rail. Asserted by the communications subsystem to turn on/off a supply voltage with minimal latency.
GNDCTRL	GND	-	-	1	AB14	Logic Control Ground

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
SPI Interface						
SPIVCC	LOPWR	-	3.6 V	1	L15	Supply for SPI Bus and Audio Bus
SPICLK	SGNL	I	3.6 V	1	A15	SPI Clock Input
MOSI	SGNL	I	3.6 V	1	G15	SPI Write Input
MISO	SGNL	O	3.6 V	1	J15	SPI Read Output
SPICSB	SGNL	I	3.6 V	1	D14	SPI Chip Select Input
GNDSPI	GND	-	-	1	L13	Ground for SPI Interface
Mini SPI Interface						
SDATA	SGNL	I	3.6 V	1	A9	Mini SPI Bus Data In
SCK	SGNL	I	3.6 V	1	H12	Mini SPI Bus Clock
CS	SGNL	I	3.6 V	1	B8	Mini SPI Bus Chip Select
GPIOs & GPOSWs & GPOs & Power Button						
GPIOVCC	LOPWR	-	3.6 V	1	AC11	GPIO Power
GPIO0	SGNL	I/O	3.6 V	1	AG7	Fully Configurable GPIO inputs/outputs for general purpose sensing and platform control
GPIO1	SGNL	I/O	3.6 V	1	AB10	
GPIO2	SGNL	I/O	3.6 V	1	AJ7	
GPIO3	SGNL	I/O	3.6 V	1	AA11	
GPIO4	SGNL	I/O	3.6 V	1	AC19	
GPIO5	SGNL	I/O	3.6 V	1	AF20	
GPIO6	SGNL	I/O	3.6 V	1	AB18	
GPIO7	SGNL	I/O	3.6 V	1	AG21	
GPOSWVCC	MDPWR	-	5.5 V	1	AC9	GPOSW Power
GPOSW0	MDPWR	-	5.5 V	1	AA9	Gating Signals for Discrete Platform VR Switches
GPOSW1	MDPWR	-	5.5 V	1	AF6	
GPOSW2	MDPWR	-	5.5 V	1	AJ5	
GPOSW3	MDPWR	-	5.5 V	1	AH6	
GPOVCC	LOPWR	-	3.6 V	1	AE5	GPO Power
GPO0	SGNL	O	3.6 V	1	AF4	General Purpose Outputs
GPO1	SGNL	O	3.6 V	1	AC7	
GPO2	SGNL	O	3.6 V	1	AD4	
GPO3	SGNL	O	3.6 V	1	AG3	
GPO4	SGNL	O	3.6 V	1	Y8	
GPO5	SGNL	O	3.6 V	1	AH4	
GPO6	SGNL	O	3.6 V	1	AG5	
GPO7	SGNL	O	3.6 V	1	AB8	
PWRBTN	SGNL	I	5.5 V	1	G11	PMIC Hardware On/Off Button

Table 5. SC900841 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
Test Pin						
ICTEST	SGNL	I	7.5 V	1	R23	IC Test Mode enable input
Substrate Ground						
REFGNDCHG	GND	-	-	1	AC21	Dedicated Reference Ground for the Switching Charger
REFGNDSW	GND	-	-	1	U7	Dedicated Reference Ground for the Switching Regulators
GNDREFVCC	GND	-	-	1	L11	Dedicated Reference Ground for VCC regulator
GNDSUB	GND	-	-	32	H18, H22, J19, J21, J23, L17, L19, M14, M18, N15, N17, N19, P12, P14, P16, P18, R11, R13, R15, R17, T12, T14, T16, T18, T22, U11, U13, U15, U17, U19, V12, V18	Substrate Ground

Notes
11. The Type Column indicates the maximum average current through each ball assigned to the different nodes. 500 mA maximum for HIPWR, 300 mA maximum for MDPWR, and 100 mA maximum for LOPWR

FUNCTIONAL DEVICE OPERATION

SYSTEM CONTROL INTERFACE

OVERVIEW

This section addresses the various interfaces and I/Os between the PMIC solution and the rest of the system.

System control interface includes the following:

- SPI interface: This is the serial communications interface between the 900841and the System Control Unit (SCU) in the platform controller hub.
- Communications (COMMs) Module Interface: This is the interface between the various basic and advanced communication modules, and the PMIC solution. It consists of two components:
  - A Serial Communications port (Mini-SPI): This port goes to the 900841 PMIC, which houses the digital core supply of the COMMs module.
  - Dedicated I/O signals for direct COMMs control of the PMIC solution.
- Interrupt controller
- Sideband signals: These are I/O signals between the 900841 and the Ultra-mobile Platform architecture for control and status reporting.
- I^2S Bus Interface for Audio/Voice
- Freescale chip set communications signals: This includes control and status reporting signal between the 900841 and the companion chip, 900842 in Freescale's power management solution.
- Special registers

SPI INTERFACE

The 900841 contains a SPI interface port, which allows a host controller to access the register set. Using these registers, 900841 resources can be controlled. The registers provide information on the PMIC status, as well as information on external signals.

The addressable register map spans 1024 registers of 8 data bits each. The map is not fully populated. A detailed structure of the register set along with bit names, positions, and basic descriptions, are given in Table 116. Expanded bit descriptions are included in the individual functional sections for application guidance.

Note that not all bits are truly writable. Refer to the individual sub-circuit descriptions and the Table 116 to determine the read/write capability of each bit.

Table 6. SPI Interface Pin Functionality

Pin Name	SPI Functionality
SPICLK	SPI Clock Input (up to 25 MHz)
MOSI	Master Out / Slave In (Serial Data In)
MISO	Master In / Slave Out (Serial Data Out)
SPICSB	Chip Select (Active Low)
SPIVCC	SPI Bus Supply - 1.8 V typical

The Platform controller hub is the master, while the PMIC is the slave. The SPI interface operates at a typical frequency of 12.5 MHz, and at a maximum frequency of 25 MHz, with lower speeds supported.

The SPI interface is configured in mode 1: clock polarity is active high (CPOL = 0), and data is latched on the falling edge of clock (CPHA = 1). The chip select signal, SPICSB, is active low. The SPICSB line must remain active during the entire SPI transfer. The MISO line will be tri-stated while SPICSB is high.

The SPI frame consists of 24 bits: a Read/Write bit, a 10-bit address code (MSB first), 5 "dead" bits and 8 data bits (also MSB first). The Read/Write bit selects whether the SPI transaction is a read or a write: for a write operation, the R/W bit must be a one; for a read operation, it must be a zero.

For a read transaction, any data on the MOSI pin after the address bits is ignored. The MISO pin will output the data field pointed to by the 10-bit address loaded at the beginning of the SPI sequence. SPI read backs of the address field and unused bits are returned as zero. For read operations, the PMIC supports address auto-increment.

For a write operation, once all the data bits are written, the data is transferred into the registers on the falling edge of the 24th clock cycle. All unused SPI bits in each register must be written to a zero.

To start a new SPI transfer, the SPICSB line must go inactive and then active again. After the LSB of data is sent, if the SPICSB line is held low, up to seven additional address/data packets may be sent as writes to the PMIC. Refer to the VRCOMP Pin section.

The following diagrams illustrate the SPI Write Protocol, SPI Read Protocol, and SPI Timing.

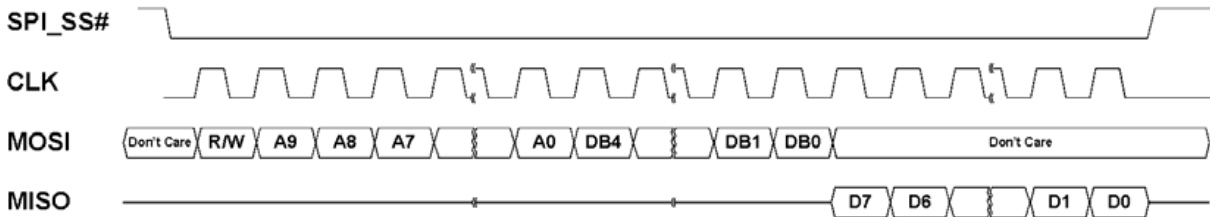

Figure 5. SPI Read from PMIC Diagram (One Address/Data Packet shown)

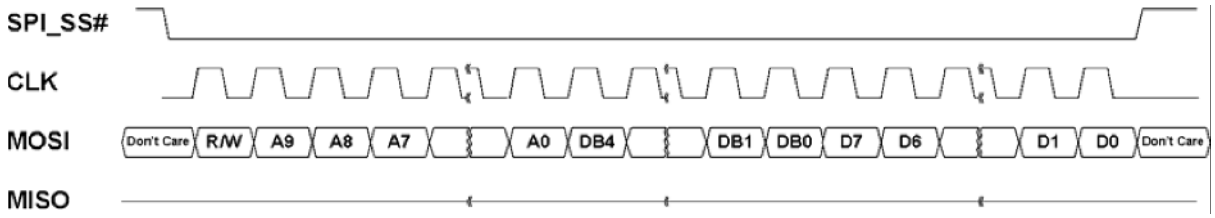

Figure 6. SPI Write to PMIC Diagram (One address/Data Packet Shown)

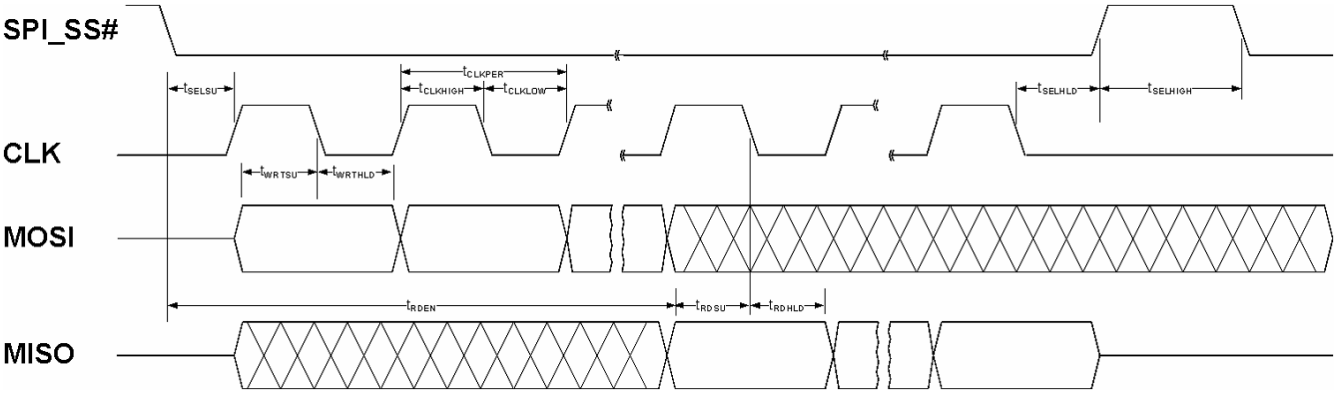

Figure 7. SPI Interface Timing Diagram (Processor Input capacitance is 3.0 pF)

COMMS MODULE INTERFACE

The 900841 supports the following communication modules:

1. Basic COMMs: WiFi, Bluetooth (BT), and GPS. The basic COMMs subsystem is present on all Ultra-mobile Platforms.
2. Advanced COMMs: WiMax and 3G options.

The 900841 provides a set of pins to enable/disable the voltage rails that support the Advanced COMMs module(s): VYMXGPS, VYMXPA, and VYMX3G.

Table 7. COMMs Modules Interface Pin Functionality

Pin Name	Pin Functionality
VYMXGPSEN	Enable Input signal for the VYMXGPS rail. Only applicable when the VYMXGPS rail is set to the 1.3 V option.
VYMXPAEN	Enable Input signal for the VYMXPA rail. Only applicable when the VYMXPA rail is set to the 4.2V option.
VYMX3GEN	Enable Input signal for the VYMX3G rail

The Advanced COMMs rails can be controlled either by hardware or software. If a software control is desired, the enable input signal must always be active, and the internal SPI register is used to turn on/off the output voltage. If hardware control is desired, the internal SPI register must be configured to turn on the voltage rail, and the ENABLE pin is used to enable/disable the voltage rail.

Table 8 shows the control logic of the Advanced COMMs rails. For a voltage rail to be active, both the SPI register setting and the ENABLE pin must be active.

Table 8. COMMs Modules Interface Pins vs. Control Registers

Signal	Register Setting	Rail Output
OFF (Low)	OFF	OFF
OFF (Low)	ON	OFF
ON (High)	OFF	OFF
ON (High)	ON	ON

Each enable pin includes an internal pull-down resistor. If the pin is left open, the enable signal will be asserted low by the internal pull-down, and the voltage rail will be inactive.

The enable signals follow the DC signaling specifications in Table 3 with a reference of 1.8 V (VPMIC).

Advanced COMMs Serial Interface

The advanced COMMs module interfaces with the 900841 through a simple serial interface, referred to as the “Mini-SPI” in this document. This interface is used to control the output voltage levels of the Advanced COMMs rails and has the following characteristics:

- SPI maximum clock speed is 10 MHz
- SPI interface consists of 16-bit word
- MSB Bit 15 is sent first followed by MSB-1 and so forth.
- SPI configured with rising-edge clock where data is sampled on the rising edge of clock
- CS (Chip Select) indicates when the master starts SPI data exchange. It is also used to reset the SPI slave so that

it is ready to receive the next word. This improves the noise immunity of the system.

- Next five bits, SDATA[15:11] are dedicated to core voltage levels
- Following five bits, SDATA[10:6] are reserved
- Last six bits, SDATA[5:0] are unused. These bits are read as zeroes
- Changes to core supply voltage levels are applied only after receiving all 16-bits of data

The VYMX3G output voltage is determined by bits 11 through 15 as follows:

- **VYMX3G** =0.6V+ 0.025*{2^4*SDATA[15] + 2^3*SDATA[14] + 2^2*SDATA[13] + 2^1*SDATA[12] + SDATA[11]}

Table 9. Advanced COMMs Mini-SPI Pin Functionality

Pin Name	Pin Functionality
SDATA	Advanced COMMs SPI Bus Data In
SCK	Advanced COMMs SPI Bus Clock Input
CS	Advanced COMMs SPI Bus Chip Select Input

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Figure 8. Mini-SPI Architecture and Simplified Timing Diagram

INTERRUPT CONTROLLER

Control

The PMIC informs the system of important events using interrupts. Unmasked interrupt events are signaled to the host by driving the PMICINT pin high.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. If a new interrupt occurs while the controller clears an existing interrupt bit, the interrupt line will remain high.

Each interrupt can be masked by setting the corresponding mask bit to a ‘1’. As a result, when a masked interrupt bit goes high, the interrupt line will not go high. A masked interrupt can still be read from the register. If a masked interrupt bit was already high, the interrupt line will go high after unmasking.

The following is the interrupt handling mechanism which has inherent latency that the clients must expect:

1. PMIC interrupts SCU, if both the 1st and 2nd level bits are not masked.
2. SCU reads PMIC master, 1st level, interrupt event register.
3. SCU then traverses all the branches of the interrupt tree where events are indicated.
4. SCU will service events in leaf node registers.

When an unmasked interrupt event happens:

- The 2nd level bit is set.
- The 1st level bit is set by a rising edge sent from the 2nd level register, and the PMICINT signal goes from low to high
- When the system controller, the SCU, reads the 1st level register the 2nd level registers that were set, remain set. Any unset registers are free to accept an interrupt event.
- When the 1st level register is read, any 1st level register bits that were set at the point the SPI read strobe shifts the register value into the SPI transmit shift register, that bit will be cleared by the SPI self clear signal immediately following the read strobe. This allows new interrupts to be recorded without being lost. If all unmasked 1st level bits get cleared by the read, the PIMCINT pin will de-assert. If a new unmasked 1st level interrupt event happens, just after the read of the 1st level register, the PIMCINT pin interrupt pin will remain asserted. The SCU reads each 2nd level register and these are cleared on read.

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- When the 2nd level register is read, any 2nd level register bits that were set at the point the SPI read strobe sweeps, the register value into the SPI transmit shift register, that bit will be cleared by the SPI self clear signal immediately following the read strobe. This allows new interrupts to be recorded without being lost. If a new unmasked 2nd level interrupt event happens just after the read of the 2nd level register, the PMICINT pin will assert if the 1st level bit is not masked.

Table 10. Interrupt Registers Summary

Block	Address	Register Name	RW	D7	D6	D5	D4	D3	D2	D1	D0	Initial
IRQ	0x04	INTERRUPT	R	EXT	AUX	VRFAULT	GPIO	RTC	CHR	ADC	PWRBTN	0x00
IRQ	0x05	INTMASK	R/W	MEXT	MAUX	MVRFAULT	MGPIO	MRTC	MCHR	MADC	MPWRBTN	0xFA
RTC	0x1C	RTCC	R	IRQF	PF (=0)	AF	UF	RSVD	RSVD	RSVD	RSVD	0x00
POWER	0x30	VRFAULTINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	VRFAIL	BATOCP	THRM	0x00
POWER	0x31	MVRFAULTINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MVRFAIL	MBATOCP	MTHRM	0x03
ADC	0x5F	ADCINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	OVERFLOW	PENDET	RND	0x00
ADC	0x60	MADCINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MOVERFLOW	MPENDET	MRND	0x00
CHARGER	0xD0	CHRGINT	R	USBOVP	DCLMT	BATDET	USBDET	COMP	TEMP	BATOVP	RSVD	0x00
CHARGER	0xD1	MCHRGINT	R/W	MUSBOVP	MDCLMT	MBATDET	MUSBDET	MCOMP	MTEMP	MBATOVP	RSVD	0x00
GPIO	0xE8	GPIOINT	R	GPIINT7	GPIINT6	GPIINT5	GPIINT4	GPIINT3	GPIINT2	GPIINT1	GPIINT0	0x00
AUDIO	0X197	AUD24	R	RSVD	RSVD	RSVD	RSVD	HSDET	HPDET	SWMPINT	SWLPINT	0X00
AUDIO	0X198	AUD25	RW	RSVD	RSVD	RSVD	RSVD	MHSDET	MHPDET	MSWMPINT	MSWLPINT	0X0F

Notes

12. Because of the design of the clear on read logic, any interrupt event is allowed to happen at any time. If the interrupt event happens close to when a read of the interrupt register happens, if the SPI read captures that interrupt bit as being set, then that bit will get cleared. If the read does not capture the bit as being set, it will not be cleared. In this way no interrupt events are lost.
13. The 2nd level interrupts that get "Ored" together to set the 1st level interrupt bits can block other 2nd level interrupts from setting the 1st level interrupt register. This is because if any of the 2nd level interrupts is high, the output of the OR will remain high, blocking the other 2nd level interrupt's rising edge. This should not be a problem. because when the 2nd level register is read, the SCU will see all the bits that are active when it is read. The software will decide which one to service first, just as it needs to do when more than one 1st level interrupt bits are set when that register is read.
14. Masking has no affect on interrupt bits being set or cleared. Masking just prevents the interrupt event from asserting the interrupt pin. If an interrupt bit is set, but is masked, the interrupt pin does not assert. If the mask bit is cleared while the bit is still set, the interrupt pin will assert. Most interrupt registers have 1st and 2nd level mask bits. Both mask bits must be in the unmasked state to generate an interrupt to the SCU.
15. Some 2nd level interrupt registers are level sensitive. If the level that sets these interrupts registers is active when the register is read, it will clear during the active time of the clear on read signal and then reassert. This will reassert the 1st level interrupt bit.
16. The GPIO interrupts do not have interrupt masking bits, they have interrupt prevention bits. This is controlled by bits 5:4 of the GPIO control register. See GPIOs for more details on using the GPIO as interrupt inputs.
17. Interrupts generated by external events are de-bounced. Therefore, the event needs to be stable throughout the de-bounce period before an interrupt is generated. Nominal de-bounce periods for each event are documented in Table 11. Due to the asynchronous nature of the de-bounce timer, the effective de-bounce time can vary slightly.

Interrupt Bit Summary

The following table summarizes all 1st and 2nd level interrupt bits associated with the Interrupt Controller. For more detailed behavioral descriptions, refer to the related sections.

Table 11. Interrupt Bit Summary

1st Level		2nd Level		Interrupt Event Condition	Detect	Debounce time
Name	Bit	Name	Bit			
PWRBTN	D0	-	-	PWRBTN falling edge detection	Falling	10 ms
ADC	D1	RND	D0	ADC Round Robin Cycle Complete	Hi Level	-
		PENDET	D1	Touch Screen Wake-up	Rising	-
		OVERFLOW	D2	Coulomb Counter is > 50% of its full value	Hi level	-
		RSVD	D7:D3	-	-	-
CHR	D2	RSVD	D0	-	-	-
		BATOVP	D1	Battery Over-voltage	Rising/Falling	see note (19)
		TEMP	D2	Battery Temperature Outside Valid Window	Hi Level	1.0 ms
		COMP	D3	Battery Charger Cycle Completion	Rising	1.0 ms
		USBDET	D4	USB Connect/Disconnect	Rising/Falling	10 ms
		BATDET	D5	Battery Connect/Disconnect	Hi Level	0.5 sec
		DCLMT	D6	Input Current Limit Reached	Hi Level	32 ms
		USBOVP	D7	Input Over-voltage Reached	Hi level	10 ms
RTC	D3	RSVD	D3:D0	-	-	-
		UF	D4	Update Cycle	Hi Level	-
		AF	D5	Current Time = Alarm Time	Hi Level	-
		RSVD	D6	-	-	-
		IRQF	D7	IRQF=UIE*UF + AIE*AF	Hi Level	-
GPIO	D4	GPINT0	D0	Edge Detect	Rising/Falling/Both	GPIDBNC0
		GPINT1	D1	Edge Detect	Rising/Falling/Both	GPIDBNC1
		GPINT2	D2	Edge Detect	Rising/Falling/Both	GPIDBNC2
		GPINT3	D3	Edge Detect	Rising/Falling/Both	GPIDBNC3
		GPINT4	D4	Edge Detect	Rising/Falling/Both	GPIDBNC4
		GPINT5	D5	Edge Detect	Rising/Falling/Both	GPIDBNC5
		GPINT6	D6	Edge Detect	Rising/Falling/Both	GPIDBNC6
		GPINT7	D7	Edge Detect	Rising/Falling/Both	GPIDBNC7
VRFAULT	D5	THRM	D0	Junction Temperature > Thermal Warning Threshold	Hi Level	10 ms
		BATOCP	D1	Battery Current > BATOCPSET	Hi Level	BATOCPT
		VRFAIL	D2	Regulator Fault Present	Hi Level	see note (18)
		RSVD	D7:D3	-	-	-
AUX	D6	SWLPINT	D0	Long Button Press Interrupt	Rising	80 ms
		SWMPINT	D1	Momentary Button Press Interrupt	Rising	80 ms
		HPDET	D2	Stereo Headphone Connect/Disconnect	Rising/Falling	30 ms
		HSDET	D3	Stereo Headset Connect/Disconnect	Rising/Falling	30 ms
		RSVD	D7:D4	-	-	-
EXT	D7	Not supported				

Notes

18. Varies by regulator. Normally it is 1.5 times the regulator turn on time.
19. 32 ms rising and 120 μs falling

SIDEBAND SIGNALS

The following pins are included as part of the Sideband signals:

Table 12. Sidebands Pin Functionality

Pin Name	I/O	Pin Functionality
PMICINT	O	Active high PMIC Interrupt Output pin
VRCOMP	O	Active high Voltage Regulator Complete signal
RESETB	O	Active low hard reset for Platform controller hub
PWRGD	O	Active high Power Good Output signal
EXITSTBY	I	Active high Exit Standby signal
THRMTRIPB	I	Active low Thermal Trip Assertion Input signal
VIDEN[1:0]	I	Active high Input signals driven by the CPU, to indicate if the VID bus is addressing VCC or VNN.
VID[6:0]	I	Active high input signals driven by the CPU, to indicate the output voltage setting for the VCC and VNN rails.

PMCINT Pin

The PMICINT pin interrupts the Platform controller hub by rising from low to high when an unmasked interrupt event occurs. It is a level sensitive pin and it is cleared when the Platform controller hub reads the Interrupt registers. Reference Interrupt Controller for a more detailed explanation of the Interrupt mechanism.

The PMICINT pin follows the DC Signaling specifications in Table 3 with a reference of 1.8 V (VPMIC).

VRCOMP Pin

This is an active high voltage regulator complete signal. It is asserted low by the PMIC when a SPI voltage regulation request, or other write request has been decoded. The signal is de-asserted on completion of the request (i.e. the rail is in regulation). This signal is relevant to the SPI initiated writes and EXITSTBY assertion.

The VRCOMP pin follows the DC Signaling specifications in Table 3 with a reference of 1.8 V (VPMIC).

Figure 9 illustrates the Voltage Regulators register write cycles and VRCOMP functionality. The rising edge on the SPICSB pin indicates the end of the block of Voltage Regulators configurations, at which point the VRCOMP pin is driven low. As an address/data block is written, the PMIC can start to ramp those rails (DC-DC, LDO, or switch). Once all of the rails are in regulation, the PMIC drives the VRCOMP pin high, indicating to the Platform controller hub that the voltage regulator configuration request is completed, and the PMIC is ready for subsequent transactions. The maximum number of voltage regulator change packets (address/data combinations) is 8. The voltage regulators should ramp at the rate defined in the regulators tables. Due to the relatively long turn-off time of the voltage regulators, the VRCOMP signal is to be gated-off after a 500 ns minimum (30 ms max.) low time.

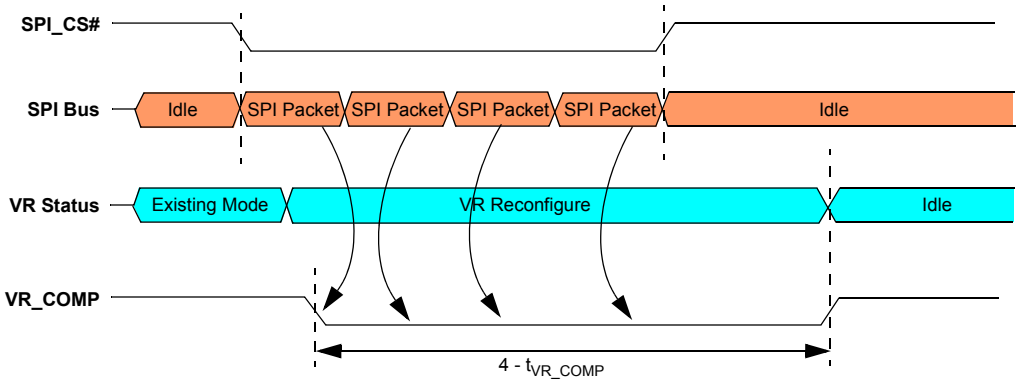

Figure 9. VRCOMP Functionality in a SPI Voltage Regulators Configuration

$\overline{\text{RESET}}$ Pin

This is an active low, hard reset for the Platform controller hub. When this pin is asserted, the Platform controller hub returns to its initial default state. This signal can be asserted when a cold or warm reset is initiated, depending on the settings in the CHIPCNTL register.

The $\overline{\text{RESET}}$ pin follows the DC Signaling specifications in Table 3 with a VCC of 1.8 V (VPMIC)

PWRGD Pin

This is a Power Good Output Signal from the 900841 to the Platform controller hub. Assertion of PWRGD means that the VCCPAOAC, VAON, and VPMIC rails have been valid for at least 100 microseconds. The Platform Controller Hub will remain off until this signal is asserted. This signal is only de-asserted if VCCPAOAC, VAON, or VPMIC is out of regulation, or a cold reset is initiated by the firmware.

The PWRGD pin follows the DC Signaling specifications in Table 3 with a reference of 1.8 V (VPMIC)

WARM and COLD RESET

The $\overline{\text{RESET}}$ and PWRGD signals have two functions which are initiated through the register file. Together they define a warm reset or cold reset to the Platform controller hub. The sequencing shown in Figure 10 and is controlled from the register CHIPCNTRL through bits WARMRST and COLDRST. The pulse should be held low for 5s < t < 31s.|

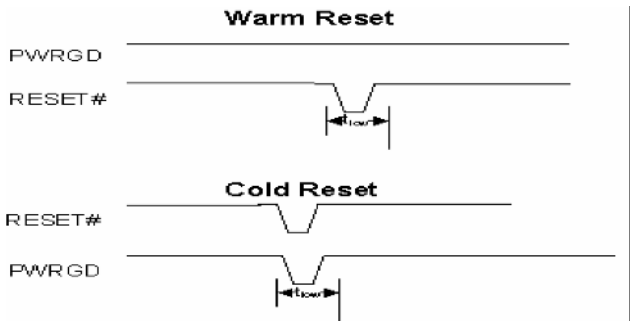

Figure 10. Warm/Cold Reset Functionality

Table 13. CHIPCNTL Register Structure and Bit Description

Name	Bits	Description
CHIPCNTL (ADDR 0x 06 - R/W - Default Value: 0x00)		
COLDRST	0	Cold Reset Function Enable x0 = No Change x1 = Pulse $\overline{\text{RESET}}$ and PWRGD Low
WARMRST	1	Warm Reset Function Enable x0 = No Change x1 = Pulse $\overline{\text{RESET}}$ Low
Reserved	7:2	Reserved

EXITSTBY Pin

When the EXITSTBY pin is asserted high, the 900841 exits the AOAC standby settings for regulating the platform supplies. When asserted, the PMIC switches the voltage regulators, as defined in the voltage regulator registers from the CTL Bits to the AOACTL Bits. This is a low latency voltage regulators context switch.

EXITSTBY pin follows the DC signaling specifications in Table 3 with a reference of 1.05 V (VCCP)

AOAC Exit Standby

When the EXITSTBY signal is asserted high from the Platform controller hub, the VRCOMP signal should be driven low. On the rising edge of the EXITSTBY signal, the AOACTL bits should be copied to the CTL bits in the different voltage regulator control registers, unless Bit 5 is '0'. If Bit 5 is '0', then the CTL bits are not modified. The VRCOMP signal is de-asserted at this point. Next the rails defined in the new CTL registers should be ramped up together or remain in the same state, as if the AOACTL settings were the same as the previous CTL setting. Once all of the rails are in regulation, the VRCOMP signal should be driven high.

Figure 11 shows the timing diagram of the EXITSTBY signal. There is a special case (Optimized Case) when the EXITSTBY signal is asserted with the VCCP, VCCPDDR, VCCA, and VCC180 rails. If some combination of these four rails turn on with the assertion of the EXITSTBY signal, the entire time for the re-configuration should take no longer than 30 ms. See Figure 12.

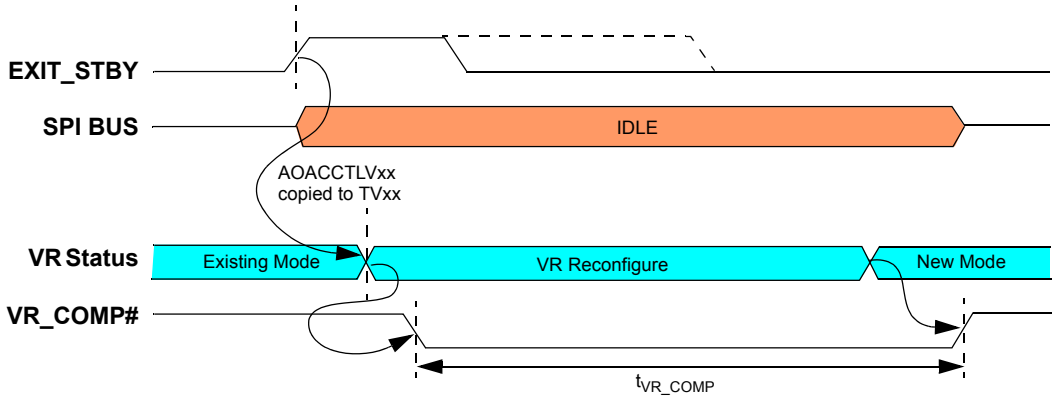

Figure 11. General Exit Standby Diagram

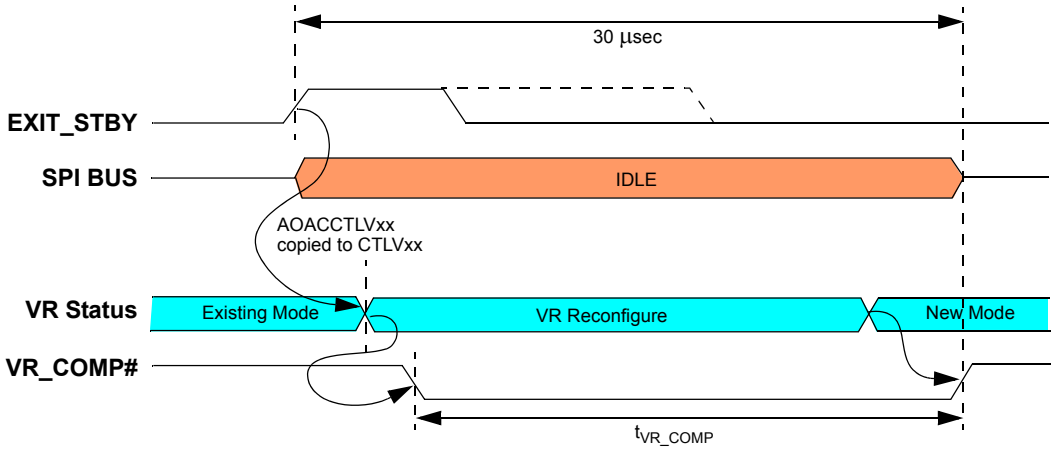

Figure 12. Optimized Exit Standby Diagram

The power-on default AOACCTLVxx register setting for the VCCP, VCCPDDR, VCCA, and VCC180 rails are to be turned on by the assertion of the EXITSTBY signal. However, every regulator has an AOACCTLVxx register setting, and can be configured to turn on, turn off, or have no change. The power-on default AOACCTLVxx register setting for all other regulators is set to no change. Note that the VDDQ regulator has to be enabled in order for the VCCA regulator to turn on.

THERMTRIPB Pin

THERMTRIPB is an active low Thermal Trip input signal. It is asserted by the CPU to indicate a catastrophic thermal event. On the falling edge of THERMTRIPB, the PMIC has 500 ms to sequence off all rails from the highest to lowest. The PMIC will turn on automatically upon detecting a turn on event, at which point the cold boot flow should be followed as shown in Turn on Events.

The PMIC provides a weak (50 -100 kΩ) pull-up to VCCPAOAC. The PMIC only responds to a THERMTRIPB signal if the VCCP regulator is on. The Platform controller hub output driver is 55 Ω nominal.

The THERMTRIPB pin follows the DC Signaling specifications in Table 3 with a reference of 1.05 V (VCCPAOAC).

VIDEN[1:0] & VID[6:0] Pins

Both VCC and VNN regulators are variable in the CPU and supply two different sub-systems. The CPU implements a VID mechanism that minimizes the number of required pins. The VID for VNN and VCC are multiplexed on to the same set of pins and a separate 2-bit enable/ID is defined to specify to which sub-system the driven VID corresponds. One of the combinations is used to notify that the VID is invalid. This is used when the CPU is in C6/Standby, to tri-state the VID pins to save power.

Table 14. VIDEN Selections

VIDEN[1:0] Bits		Selection
0	0	Invalid
0	1	VCC
1	0	VNN
1	1	Unused

Both VCC and VNN have initial boot voltage (VCC VBOOT = 1.1 V; VNN VBOOT = 0.9 V) settings that the Platform controller hub sets to the VNN and VCC regulators by a SPI write to the VNNLATCH and VCCLATCH registers. Once all of the platform voltage rails are up, the CPU will drive the VID and VIDEN signals to set the VNN and VCC output voltage to the appropriate level. The VID and VIDEN signals will go through the sequence INVALID >> VNN >> INVALID >> VCC.

VID[6:0] and VIDEN[1:0] will transition together and the PMIC must de-bounce the VID[6:0] and VIDEN[1:0] for 100 to 400 ns. The CPU will hold these signals valid for at least 500 ns. VID signals are disabled from controlling VCC/VNN unless the VCCP regulator is enabled

Both regulators support dynamic VID transitioning during normal runtime operation. For the VNN regulator, dynamic VIDs require the CPU to change the VIDEN signals to INVALID each time to change the VNN output voltage. The VCC regulator is different in that it does not require the VIDEN signals to change to change the VCC output voltage. If the VIDEN signals are set for VCC (01) the VID signals can change and the VCC regulator will respond by changing the output voltage accordingly.

Figure 13 shows how the VCC output voltage can change during normal runtime operation when the VIDEN signals are set to VCC (01). If the VIDEN signals are set to VCC (01), the VCC regulator must monitor the VID signals, latch any changes, and change the output voltage setting accordingly. During normal operation, when the CPU is dynamically changing the VID setting for the VCC regulator, it will only change the VID combination by 1 step, which corresponds to a voltage step of ±12.5 mV. During these changes, the VCC regulator must follow the 25 mV/ms slew rate specification.

The VNN regulator differs from the VCC regulator, in that dynamic changes to the VNN regulator output voltage require the VIDEN signals to change to INVALID each time. Figure 14 shows how the VNN output voltage can change during normal runtime operation.

The VIDEN[1:0] pins are active high signals driven by the CPU to indicate if the VID bus is addressing VCC or VNN. They follow the DC Signaling specifications in Table 3 with a reference of 1.05 V (VCCPAOAC)

The VID[6:0] pins are active high signals driven by the CPU to indicate the output voltage setting for the VCC and VNN rails. They follow the DC Signaling specifications in Table 3 with a reference of 1.05 V (VCCP)

The VID output buffer driver is of the CMOS type. The Platform controller hub output driver Impedance is a pull-up (55 Ω+20%/-55%) and pull-down (55 Ω+20%/-55%). Motherboard Impedance is 55 Ω±15%. Under extreme conditions, there could be ringing that cross the 70/30% threshold, hence the de-bounce requirements. Maximum leakage current on the VID pins is 100 mA.

VID[6:0] for each of the VCC and VNN rails will be latched in an internal register that will be updated with every VID[6:0] pin signaling

Table 15. VCC and VNN Latch Register Structure and Bit Description

Name	Bits	Description
FSLVCCLATCH (ADDR 0x1C9 - R - Default Value: 0x7F)		
VCCVID	6:0	This register latches an Image of the last VID[6:0] signals for VCC
Reserved	7	Reserved
FSLVNNLATCH (ADDR 0x1CA - R - Default Value: 0x7F)		
VNNVID	6:0	This register latches an Image of the last VID[6:0] signals for VNN
Reserved	7	Reserved

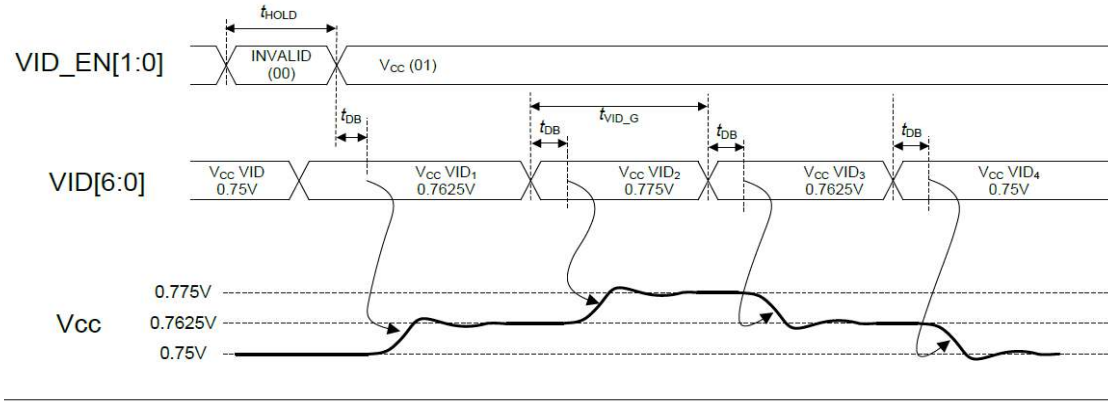

Figure 13. Dynamic VCC Timing Diagram

900841

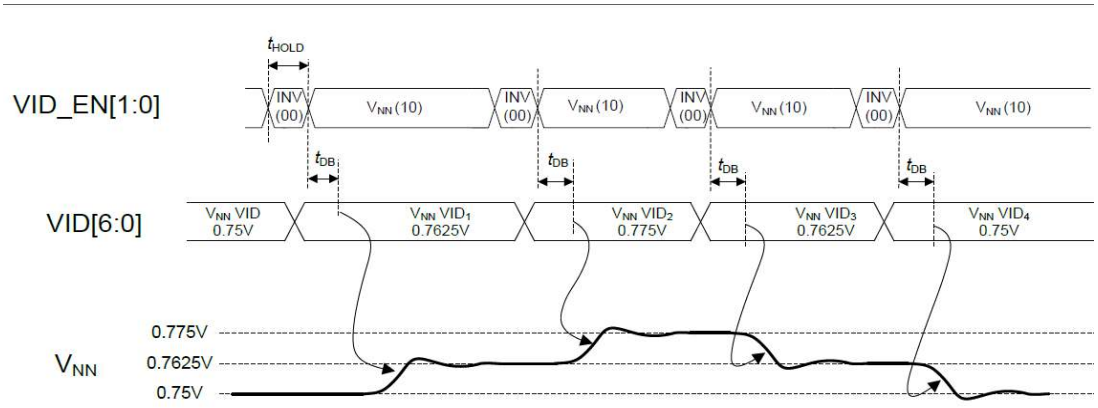

Figure 14. Dynamic VNN Timing Diagram

Figure 15 shows the 7-bit VID codes vs. the output voltage of VCC and VNN.

VID 6	5	4	3	2	1	0	VID (V)	VID 6	5	4	3	2	1	0	VID (V)	VID 6	5	4	3	2	1	0	VID (V)	VID 6	5	4	3	2	1	0	VID (V)
0	0	0	0	0	0	0	1.2000	0	1	0	0	0	0	0	1.1000	1	0	0	0	0	0	0	0.7000	1	1	0	0	0	0	0	0.3000
0	0	0	0	0	0	1	1.2000	0	1	0	0	0	0	1	1.0875	1	0	0	0	0	0	1	0.6875	1	1	0	0	0	0	1	OFF
0	0	0	0	0	1	0	1.2000	0	1	0	0	0	1	0	1.0750	1	0	0	0	0	1	0	0.6750	1	1	0	0	0	1	0	OFF
0	0	0	0	0	1	1	1.2000	0	1	0	0	0	1	1	1.0625	1	0	0	0	0	1	1	0.6625	1	1	0	0	0	1	1	OFF
0	0	0	0	1	0	0	1.2000	0	1	0	0	1	0	0	1.0500	1	0	0	0	1	0	0	0.6500	1	1	0	0	1	0	0	OFF
0	0	0	0	1	0	1	1.2000	0	1	0	0	1	0	1	1.0375	1	0	0	0	1	0	1	0.6375	1	1	0	0	1	0	1	OFF
0	0	0	0	1	1	0	1.2000	0	1	0	0	1	1	0	1.0250	1	0	0	0	1	1	0	0.6250	1	1	0	0	1	1	0	OFF
0	0	0	0	1	1	1	1.2000	0	1	0	0	1	1	1	1.0125	1	0	0	0	1	1	1	0.6125	1	1	0	0	1	1	1	OFF
0	0	0	1	0	0	0	1.2000	0	1	0	1	0	0	0	1.0000	1	0	0	1	0	0	0	0.6000	1	1	0	1	0	0	0	OFF
0	0	0	1	0	0	1	1.2000	0	1	0	1	0	0	1	0.9875	1	0	0	1	0	0	1	0.5875	1	1	0	1	0	0	1	OFF
0	0	0	1	0	1	0	1.2000	0	1	0	1	0	1	0	0.9750	1	0	0	1	0	1	0	0.5750	1	1	0	1	0	1	0	OFF
0	0	0	1	0	1	1	1.2000	0	1	0	1	0	1	1	0.9625	1	0	0	1	0	1	1	0.5625	1	1	0	1	0	1	1	OFF
0	0	0	1	1	0	0	1.2000	0	1	0	1	1	0	0	0.9500	1	0	0	1	1	0	0	0.5500	1	1	0	1	1	0	0	OFF
0	0	0	1	1	0	1	1.2000	0	1	0	1	1	0	1	0.9375	1	0	0	1	1	0	1	0.5375	1	1	0	1	1	0	1	OFF
0	0	0	1	1	1	0	1.2000	0	1	0	1	1	1	0	0.9250	1	0	0	1	1	1	0	0.5250	1	1	0	1	1	1	0	OFF
0	0	0	1	1	1	1	1.2000	0	1	0	1	1	1	1	0.9125	1	0	0	1	1	1	1	0.5125	1	1	0	1	1	1	1	OFF
0	0	1	0	0	0	0	1.2000	0	1	1	0	0	0	0	0.9000	1	0	1	0	0	0	0	0.5000	1	1	1	0	0	0	0	OFF
0	0	1	0	0	0	1	1.2000	0	1	1	0	0	0	1	0.8875	1	0	1	0	0	0	1	0.4875	1	1	1	0	0	0	1	OFF
0	0	1	0	0	1	0	1.2000	0	1	1	0	0	1	0	0.8750	1	0	1	0	0	1	0	0.4750	1	1	1	0	0	1	0	OFF
0	0	1	0	0	1	1	1.2000	0	1	1	0	0	1	1	0.8625	1	0	1	0	0	1	1	0.4625	1	1	1	0	0	1	1	OFF
0	0	1	0	1	0	0	1.2000	0	1	1	0	1	0	0	0.8500	1	0	1	0	1	0	0	0.4500	1	1	1	0	1	0	0	OFF
0	0	1	0	1	0	1	1.2000	0	1	1	0	1	0	1	0.8375	1	0	1	0	1	0	1	0.4375	1	1	1	0	1	0	1	OFF
0	0	1	0	1	1	0	1.2000	0	1	1	0	1	1	0	0.8250	1	0	1	0	1	1	0	0.4250	1	1	1	0	1	1	0	OFF
0	0	1	0	1	1	1	1.2000	0	1	1	0	1	1	1	0.8125	1	0	1	0	1	1	1	0.4125	1	1	1	0	1	1	1	OFF
0	0	1	1	0	0	0	1.2000	0	1	1	1	0	0	0	0.8000	1	0	1	1	0	0	0	0.4000	1	1	1	1	0	0	0	OFF
0	0	1	1	0	0	1	1.1875	0	1	1	1	0	0	1	0.7875	1	0	1	1	0	0	1	0.3875	1	1	1	1	0	0	1	OFF
0	0	1	1	0	1	0	1.1750	0	1	1	1	0	1	0	0.7750	1	0	1	1	0	1	0	0.3750	1	1	1	1	0	1	0	OFF
0	0	1	1	0	1	1	1.1625	0	1	1	1	0	1	1	0.7625	1	0	1	1	0	1	1	0.3625	1	1	1	1	0	1	1	OFF
0	0	1	1	1	0	0	1.1500	0	1	1	1	1	0	0	0.7500	1	0	1	1	1	0	0	0.3500	1	1	1	1	1	0	0	OFF
0	0	1	1	1	0	1	1.1375	0	1	1	1	1	0	1	0.7375	1	0	1	1	1	0	1	0.3375	1	1	1	1	1	0	1	OFF
0	0	1	1	1	1	0	1.1250	0	1	1	1	1	1	0	0.7250	1	0	1	1	1	1	0	0.3250	1	1	1	1	1	1	0	OFF
0	0	1	1	1	1	1	1.1125	0	1	1	1	1	1	1	0.7125	1	0	1	1	1	1	1	0.3125	1	1	1	1	1	1	1	OFF

Figure 15. 7-Bit VID Code vs. VCC/VNN Output Voltage

As explained previously, the output voltage setting for the VCC and VNN regulators can be set via the VID/VIDEN pins from the CPU, or by programming the VNNLATCH and VCCLATCH registers through the SPI interface via the Platform controller hub. Figure 16 shows the relationship between the VID/VIDEN signals, the DVPxVRD bit in the Latch registers, and the VRCOMP output signal. The figure shows VCC as an example, but is also applicable to VNN

The DVPxVRD bit in the VNNLATCH and VCCLATCH registers controls the select input to the multiplexer. If the DVPxVRD bit is set to a '0', the regulator uses the VID/VIDEN

pins from the CPU, and if the DVPxVRD bit is set to a '1', the regulator uses the VNNLATCH and VCCLATCH registers to set the output voltage.

When the DVPxVRD bit is set to a '0', any changes to the VNNLATCH and VCCLATCH registers should be ignored. When the DVPxVRD bit is set to a '1', any changes on the VID/VIDEN pins from the CPU should be ignored.

As soon as the DVPxVRD bit is set to a '1', the regulator switches from using the VID/VIDEN pins to using the VCCLATCH register, and the output voltage of the regulator changes to what the VCCLATCH register is set.

Figure 16 also shows how the PMIC controls the VRCOMP signal. The PMIC toggles the VRCOMP signal any time the DVPxVRD bit is set to a '1' and the output voltage of the VNN or the VCC regulator changes. If the output voltage of the VCC/VNN regulator changes and the DVPxVRD bit is set to a '0', the VRCOMP signal should not toggle. In other words, VRCOMP only toggles for changes to VCC and VNN through the SPI registers.

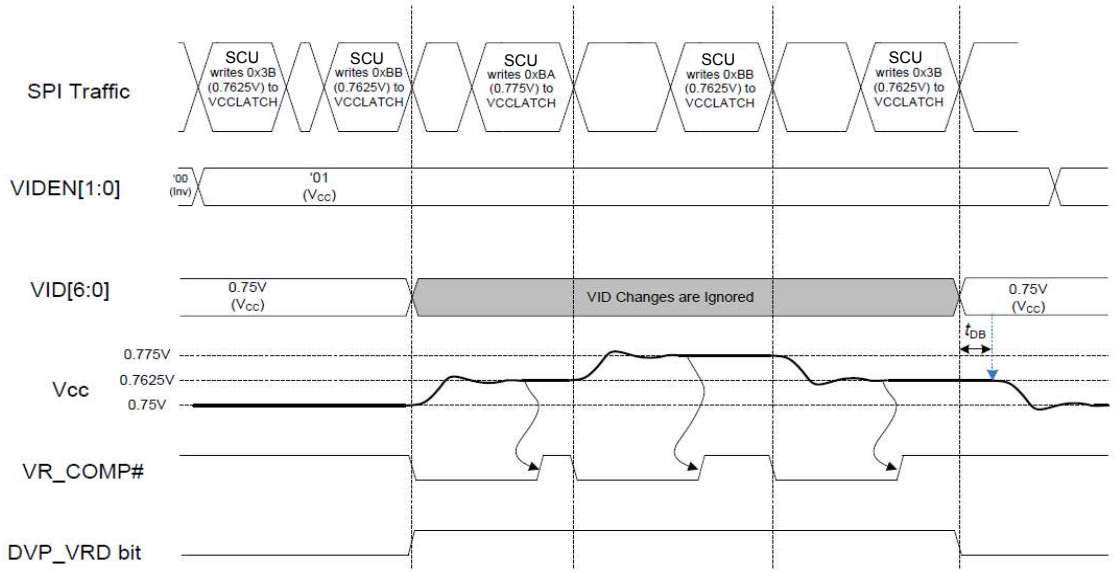

Figure 16. Relationship Between the VID/VIDEN Pins, the DPV1VRD Bit, and VRCOMP Signal

I2S/PCM INTERFACE

A detailed description of the I2S interface is provided in Audio.

FREESCALE CHIP SET COMMUNICATION SIGNALS

This includes the control and status reporting signal between the 900841 and the companion chip, 900842, in Freescale's power management solution.

Table 16. Freescale Chipset Communication Signals Pin Functionality

Pin Name	I/O	Pin Functionality
V33EN	O	V33 Enable output pin
V33STTS	I	V33 Status input pin. Active low when V33 output is on
V33ISNS	I	Input Interface with the ADC to measure V33 output current
V3GPAEN	O	Reserved
V3GPASTTS	I	Reserved

As explained in General Description, Freescale's power management solution consists of two chips. The 900842 supplies the 3.3 V rail (V33).

The 900841 interfaces with the 900842 using the signals outlined above for control and status reporting functions.

The Platform controller hub has full control over the V33 chip, by setting the desired voltage regulator control setting in the 900841 register space. The 900841 in turn uses the V33EN pin to enable or disable the V33 chip. This transaction is seamless to the Platform controller hub.

If the 900841 is going through a forced shutdown event, like THERMTRIPB assertion, it can also use the V33EN pin to turn off the V33 rail. In turn, the V33 rail communicates back to the 900841 its output voltage status, through the V33STTS pin, so the 900841 has full visibility on the health of the 3.3 V rail and can report back to the Platform controller hub through the VRFAULT Interrupt if V33 has shutdown, due to a local problem, such as over-temperature.

V33 also sends its output current information to the 900841 for sampling by the ADC through the V33ISNS pin.

SPECIAL REGISTERS

Vendor ID and Version ID

The Vendor ID and other version details can be read via the Identification bits. These are hard-wired on the chip.

Table 17. Vendor ID Registers Structure and Bits Description

Name	Bits	Description
ID1 (ADDR 0x00 - R - Default Value: 0x28)		
VENDID1	2:0	Chip1 Vendor ID
REV1	5:3	Chip1 Revision ID
Reserved	7:6	Reserved
ID2 (ADDR 0x01 - R - Default Value: 0x00)		
VENDID2	2:0	Chip2 Vendor ID
REV2	5:3	Chip2 Revision ID
Reserved	7:6	Reserved
ID3 (ADDR 0x02 - R - Default Value: 0x00)		
Reserved	7:0	Reserved
ID4 (ADDR 0x03 - R - Default Value: 0x00)		
Reserved	7:0	Reserved

Embedded Memory

There are 24 register banks of general purpose embedded memory, accessible by the processor to store critical data during power down. The data written to these registers is maintained by the coin cell when the main battery is deeply discharged or removed, and is part of the RTC block. The content of the embedded memory is reset by RTCPORB. The banks can be used for any system need, for bit retention with coin cell backup.

X is from 1 to 8 in Table 18.

Table 18. General Purpose Memory MEMx Register Structure and Bits Description

Register	Name	Bits	Description
MEMx	-	7:0	General Purpose Memory Register x

The rest of the 24 registers reside in the Freescale dedicated register space.

X is from 1 to 16 in the following table

Table 19. General Purpose Memory FSLMEMx Register Structure and Bits Description

Register	Name	Bits	Description
FSLMEMx	-	7:0	General Purpose Memory Register x

Output Driver Control

Select output pins output drive capability can be programmed for 4 different settings as shows in the following tables. All of the following outputs follow the settings as shown.

Table 20. Output Driver Control Selection

Slope Select		Rise Time (ns)	Fall Time (ns)
0	0	8.4	7.0
0	1	6.2	6.2
1	0	Hi-Z	Hi-Z
1	1	22.3	21.3

Table 21. Output Driver Register Structure and Bit Description

Name	Bits	Description
FSLOUTDRVCNTL1 (ADDR 0x1BF - R/W - Default Value: 0x00)		
PWRGDDRV	1:0	PWRGD Output Pin Driver Capability
VRCOMPBDRV	3:2	VRCOMP Output Pin Driver Capability
PMICINTDRV	5:4	PMICINT Output Pin Driver Capability
RESETBDRV	7:6	RESETB Output Pin Driver Capability
FSLOUTDRVCNTL2 (ADDR 0x1C0 - R/W - Default Value: 0x04)		
CLK26KDRV	1:0	CLK26K Output Pin Driver Capability
CLK26MDRV	3:2	CLK26M Output Pin Driver Capability
V3GPAENDRV	5:4	V3GPAEN Output Pin Driver Capability
V33ENDRV	7:6	V33EN Output Pin Driver Capability
FSLOUTDRVCNTL3 (ADDR 0x1C1 - R/W - Default Value: 0x01)		
SPISDODRV	1:0	MISO Output Pin Driver Capability
RSVD	7:2	Reserved

PLL Control

The following register controls the PLL and the different divider values for different output frequencies.

Table 22. PLL Control Register Structure and Bit Description

Name	Bits	Description
FSLPLLCNTL (ADDR 0x1E4 - R/W - Default Value: 0x1B)		
PLLDIVIDE	2:0	PLL Divide Ratio and Effective VCO Frequency Settings x0 = 112, 3.670 MHz x1 = 116, 3.801 MHz x2 = 120, 3.932 MHz x3 = 124, 4.063 MHz x4 = 128, 4.194 MHz x5 = 132, 4.325 MHz x6 = 136, 4.456 MHz x7 = 140, 4.588 MHz
PLL16MEN	3	16 MHz frequency enable x0 = 16 MHz clock disabled x1 = 16 MHz clock enabled and PLL enabled
PLLEN	4	PLL Enable, even if there is no block requesting a clock x0 = PLL enabled based on device enables only x1 = PLL enabled
Reserved	7:5	Reserved

TEST MODES

Test Mode Configuration

During evaluation and testing, the IC can be configured for normal operation or test mode via the ICTEST pin and other register configurations. Details of Test mode programmability are not documented herein, but should be referenced from other Design for Test documentation.

Test modes are for Freescale use only, and must not be accessed in applications. In test modes, signals are multiplexed on existing functional pins. The ICTEST pin must therefore be tied to ground (for normal operation) at the board level, in product applications

Test mode also disables the thermal protection for high temperature op life testing. A proprietary protocol is included for scan chain test configurations, which reuses the SPI pins.

In-package Trimming

During IC final test, several parameters are trimmed in the package, such as the main bandgap, and other precision analog functions. Trim registers are for Freescale use only and must not be accessed in product applications. Fuse programming circuitry will be blocked during normal and test mode operation.

CLOCK GENERATION AND REAL TIME CLOCK (RTC)

CLOCK GENERATION

A system clock is generated for internal digital circuitry, as well as for external applications utilizing the clock output pins. A crystal oscillator is used for the 32.768 kHz time base and generation of related derivative clocks. If the crystal oscillator is not running (for example, if the crystal is not present), an internal 32 kHz oscillator will be used instead.

In addition, another crystal oscillator is used to generate a 26 MHz clock for Audio usage. This clock is also routed to the companion chip, 900842, through the CLK26M pin.

Clocking Scheme

The internal 32 kHz oscillator is an integrated backup for the crystal oscillator and provides a 32.768 kHz nominal frequency at 50% accuracy, if running. The internal oscillator only runs if a valid supply is available at the charger input, battery, or coin cell, and would not be used as long as the crystal oscillator is active. The crystal oscillator continues running, supplied from one of the sources as described previously, until all power is depleted or removed. All control functions will run off the crystal derived frequency, occasionally referred to as the "32 kHz".

At system startup, the 32 kHz clock is driven to the CLK32K output pin, which is SPIVCC referenced. CLK32K is provided as a peripheral clock reference. The driver is enabled by the startup sequencer. Additionally, a SPI bit M32KCLK bit is provided for direct SPI control. The M32KCLK bit defaults to 0 to enable the driver and resets on the RTCPORB to ensure the buffer is activated at the first power up and configured as desired, for subsequent power ups.

The drive strength of the output drivers is programmable with CLK32KDRV[1:0] (master control bits that affect the drive strength of CLK32K), see FSLOUTDRVCNTL2 Register in Table 21.

If a switchover occurs between the two clock sources (such as when the crystal oscillator is starting up), it will occur during the active low phase of both clocks, to avoid clocking glitches. A status bit, OSCSTP, is available to indicate to the processor which clock is currently selected: OSCSTP=1 when the internal RC is used, and OSCSTP=0 if the XTAL source is used.

The 26 MHz XTAL is necessary to provide a low jitter clock operation for the Audio block of 900841. The 26 MHz signal is needed internally for Audio operation, but is also provided to the companion chip, 900842, via the CLK26M output pin when the V33 voltage rail is enabled..

The drive strength of the output drivers is programmable with CLK26MDRV[1:0] (master control bits that affect the drive strength of CLK26M), see the FSLOUTDRVCNTL2 Register in Table 21.

Oscillator Specifications

The 32 kHz crystal oscillator has been optimized for use in conjunction with the Abracon™ ABS07-32.768KHZ-T or equivalent, and is capable of handling its parametric variations.

The 26 MHz is targeting for use in conjunction with the NDK™ NX2016AB-26MHZ SB1 or equivalent, and is capable of handling its parametric variations.

The electrical characteristics of the 32 kHz and 26 MHz Crystal oscillators are given in the Oscillator section on Table 3 and Table 4, taking into account the crystal characteristics noted previously. The oscillator accuracy depends largely on the temperature characteristics of the used crystal. Application circuits can be optimized for required accuracy by adapting the external crystal oscillator network (via component accuracy and/or tuning). Additionally, a clock calibration system is provided to adjust the 32.768 cycle counter that generates the 1.0 Hz timer and RTC registers; see Real Time Clock (RTC) for more detail.

REAL TIME CLOCK (RTC)

The RTC block provides a real-time clock with time-of-day, year, month, and date, as well as daily alarm capabilities. The real-time clock will use the 32.768 kHz oscillator as its input clock. The real-time clock will be powered by the coin cell backup battery as a last resort, if no other power source is available (Battery or USB/Wall plug). The register set is compatible with the Motorola™ MC146818 RTC device.

Overview

The RTC module uses a 15-bit counter to generate a 1.0 Hz clock for timekeeping. The seven time and calendar registers keep track of seconds, minutes, hours, day-of-week, day-of-month, month, and year. The three seconds, minutes, and hours alarm registers can be used to generate time-of-day alarm interrupts.

The RTC time, alarm, and calendar values can be represented in 8-bit binary or BCD format. The hours and hours alarm values can be represented in 24 hour or 12 hour format, with AM/PM in the 12 hour mode. RTC control register B allows for software configurable clock formatting and interrupt masking. Control registers A, C, and D, report software testable RTC status, including interrupt flags, update-in-progress, and valid-RAM-time.

The RTC resets when the RTCPORB signal is driven low. The clock and calendar registers will be initialized to 00:00:00, Sunday, January 1, 2000.

Features

The RTC module includes the following features:

- Counts seconds, minutes, and hours of the day
- Counts days of the week, date, month, and year
- Binary or BCD representation of time, calendar, and alarm
- 12 or 24 hour clock with AM and PM in 12 hour mode
- Automatic leap year compensation
- Automatic end of month recognition
- 15 bytes of clock, calendar, RTC control, and coin cell registers
- Two interrupts are separately software maskable and testable
- Time-of-day Alarm
- End-of-clock update cycle interrupt
- 15-bit counter to generate 1.0 Hz RTC clock
- Software testable Valid-ram-and-time status bit indicates data integrity

Modes of Operation

NORMAL MODE

In Normal mode, the RTC module updates time and calendar registers using the internal 1.0 Hz RTC clock. Once per second, the alarm registers are compared to the current time, and if enabled, an alarm interrupt will occur when the alarm time matches the current time. During normal operation, all 14 bytes of RTC and coin cell battery registers can be read through the SPI interface. Control register B may be updated to enable End-of-clock Update interrupts, alarm interrupts, or to put the RTC in Set mode.

The coin cell charger register is available for R/W in normal mode.

Coin Cell mode

When the application is powered down, the RTC will continue to keep track of time using power provided by the coin cell battery.

Since the system SPI will be powered down during this time, there is no read or write access to the RTC registers in Coin Cell mode.

Set mode

In Set mode, the clock and calendar updates are suspended, and the software may update the time, calendar, and alarm registers. The time and calendar formats must match the formats specified by the DM and 12/24 format bits in RTC register B. When the format bits are modified, all 14 time, calendar, and alarm registers must be updated in the specified format.

Scan/Test mode

Internal Test mode not available for the end application.

Setting the Time, Calendar, and Alarm

Before initializing the internal registers, the Set bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. Select the data format by writing the appropriate values to the DM and 24/12 bits in Register B.

Next, the program should initialize all 10 time, calendar, and alarm locations in the format specified by Register B (binary or BCD, 12 or 24 hour). All 10 time, calendar, and

alarm bytes must use the same data mode, either binary or BCD. Both the alarm hours, and the hours bytes must use the same hours format, either 12 or 24.

The Set bit may now be cleared to allow updates. Once initialized, the real-time clock makes all updates in the selected data mode. The data mode (DM) cannot be changed without re-initializing the 10 data bytes.

The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. When the 12 hour format is selected the high order bit of the hour bytes represents PM when it is a "1". The 24/12 bit cannot be changed without re-initializing the hour and alarm-hour locations.

Table 23 shows the binary and BCD formats of the 10 time, calendar, and alarm locations.

Table 23. Time, Calendar, and Alarm Data Modes

Address location	Function	Decimal Range	Range		Example [20]	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0x10	Seconds	0-59	$00-$3B	$00-$59	15	21
0x11	Seconds Alarm	0-59	$00-$3B	$00-$59	15	21
0x12	Minutes	0-59	$00-$3B	$00-$59	3A	58
0x13	Minutes Alarm	0-59	$00-$3B	$00-$59	3A	58
0x14	Hours (12 Hour Mode) (24 Hour Mode)	 1-12 0-23	 $01-$0C(AM) / $81-$92(PM) $00-$17	 $01-$12(AM) / $81-$92(PM) $00-$23	0B	11
0x15	Hours Alarm (12 Hour Mode) (24 Hour Mode)	 1-12 0-23	 $01-$0C(AM) / $81-$92(PM) $00-$17	 $01-$12(AM) / $81-$92(PM) $00-$23	0B	11
0x16	Day of the Week Sunday=1	1-7	$01-$07	$01-$07	05	05
0x17	Date of the Month	1-31	$01-$1F	$01-$31	0F	15
0x18	Month	1-12	$01-$0C	$01-$12	02	02
0x19	Year	0-99	$00-$63	$00-$99	08	08

Notes
20. Example: 11:58:21 Thursday 15 February 2008 (time is AM)

Reading the Time, Calendar, and Alarm

Under normal operation, the current time and date may be read by accessing the RTC registers through the system SPI. Since the alarm is only updated by a SPI write instruction, the three alarm registers may be read at any time and will always be defined.

The 900841 SPI will run at a minimum of 12.5 MHz. Each individual SPI read transaction requires 25 cycles (less for burst-read). The RTC contains seven timekeeping registers to keep track of seconds, minutes, hours, day-of-week, day-of-month, month, and year. If the SPI is clocked at the slowest frequency, and the RTC is read using individual (not burst) SPI read commands, the following equation gives the maximum amount of time it takes the processor to read a complete date and time (assuming the reads are done sequentially, and uninterrupted): (25 * 7) / (12.5 MHz) = 14 μs.

This equation shows that a program which randomly accesses the time and date information will find the data in transition statistically 14 times per million attempts. If a clock update occurs during the time it takes to read all seven timekeeping registers, the values read may be inconsistent. In other words, if the program starts to read the seven date/time registers and an RTC update occurs, the data collected may be in transition. In this event, it is possible to read transition data in one of the registers, resulting in undefined output. It is more likely that the registers read after the update would be incremented (by one second), and the registers read before the update would not.

The time, calendar, and alarm bytes are always accessible by the processor program. Once per second the seven bytes are advanced by one second and checked for an alarm condition. If any of the seven bytes are read at this time, the data outputs should be considered undefined. Similarly, all seven bytes should be read between updates to get a consistent time and date. Reading some of the bytes before an update and some after, may result in an erroneous output. The Update Cycle section explains how to accommodate the update cycle in the processor program.

Update Cycle

The RTC module executes an update cycle once per second, assuming one of the proper time bases is in place and

the SET bit in Register B is clear. The SET bit in the “1” state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the Seconds byte, check for overflow, increment the Minutes byte when appropriate, and so forth, up through the month and year bytes. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match is present in all three positions.

Two methods of avoiding undefined output during updates are usable by the program. In discussing the two methods, it is assumed that at random points, user programs are able to call a subroutine to obtain the time of day.

The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle, which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A, to determine if the update cycle is in progress. The UIP bit will pulse once per second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 3,640 attempts. After the UIP bit goes high, the update cycle begins 244.1 μs later. Therefore, if a low is read on the UIP bit, the user has at least 244.1 μs before the time/calendar data will be changed. If a “1” is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines which would cause the time needed to read valid time/calendar data to exceed 244.1 μs.

The RTC uses seven synchronous counters to increment the time and calendar values. All seven timekeeping registers are clocked by the same internal 1.0 Hz clock, so updates occur simultaneously, even during rollover. After the counters are incremented, the current time is compared to the time-of-day alarm registers 30.5 μs later, and if they match, the AF bit in register C will be set.

The Update-cycle begins when the clock and calendar registers are incremented, and ends when the alarm comparison is complete. During this 30.5 μs update cycle, the time, calendar, and alarm bytes are fully accessible by the processor program. If the processor reads these locations during an update, the transitional output may be undefined. The update in progress (UIP) status bit is set 244.1 μs before this interval, and is cleared when the update cycle completes.

Interrupts

The RTC includes two separate, fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at a rate of once per day. The update-ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Two bits in Register B enable the two interrupts. Writing a “1” to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A “0” in the interrupt-enable bit, prohibits the IRQF bit from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the IRQF bit is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a “1” in Register C. Each of the two interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The interrupt flag bit becomes a status bit, which the software interrogates when it wishes. When the software detects the flag is set, it is an indication to the software an interrupt event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C, so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One or two flag bits may be found to be set when Register C is used. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the IRQF bit is asserted high. IRQF is asserted as long as at least one of the two interrupt sources has its flag and enable bits both set.

The processor program can determine that the RTC initiated the interrupt by reading Register C. A “1” in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt mask bits set and service each interrupt which is set. Again, more than one interrupt flag bit may be set.

ALARM INTERRUPT

The three alarm bytes may be used to generate a daily alarm interrupt. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day, if the alarm enable bit is high.

Update-Ended Interrupt

If enabled, an interrupt occurs after every update cycle which indicates that there is over 999 ms available to read valid time and date information.

RTC Timer Calibration

By default, the calibration circuit is off and clock accuracy is limited to the performance of the 32.768 kHz crystal input. For clock accuracy beyond the limits of the crystal oscillator, a calibration circuit is included. The processor can use a high-frequency clock to sample the 32.768 kHz output to determine if it is fast or slow, and calculate an adjustment value. The adjustment algorithm has a resolution of ±477 nanoseconds-per-second average adjustment, which equates to a time accuracy of approximately 1.2 seconds per month.

Calibration can be turned on by setting the RTC ADJ bit of the ADJ register. A "0" in the ADJ bit turns calibration off. The Sign bit in the Trim register determines if periodic adjustments are made to speed up or slow down the clock.

When calibration is enabled, the Trim register is used to grow or shrink the average 1.0 Hz clock period. By default, one second is defined as 32,768 periods of the CLK32K input pin. Each period of the input clock is approximately 30.5 μs. By occasionally adding (or subtracting) one extra cycle per second, the average second can be adjusted. If SIGN is high (subtract one), occasional seconds will be trimmed to 32,767 cycles. If SIGN is low (add one), occasional seconds will be trimmed to 32,769 cycles.

The 6-bit TRIMVAL in the Trim register represents the number of seconds to adjust out of every 64 seconds, and can range from 0-63. For example, TRIMVAL = 0x08 then 8 seconds out of every 64 will be adjusted up or down, according to the SIGN bit.

CLOCK GENERATION AND REAL TIME CLOCK (RTC) REGISTERS AND BITS DESCRIPTION

Table 24. RTC Date/Time Configuration Register Structure and Bits Description

Name	Bits	Description
RTCS (ADDR 0x10 - R/W - Default Value: 0x00)		
SEC	6:0	Seconds Counter Register
Reserved	7	Reserved
RTCSA (ADDR 0x11 - R/W - Default Value: 0x00)		
SECALARM	6:0	Seconds Alarm Setting Register
Reserved	7	Reserved
RTCM1 (ADDR 0x12 -R/W - Default Value: 0x00)		
MIN	6:0	Minutes Counter Register
Reserved	7	Reserved
RTCMA (ADDR 0x13 - R/W - Default Value: 0x00)		
MINALARM	6:0	Minutes Alarm Setting Register
Reserved	7	Reserved
RTCH (ADDR 0x14 - R/W - Default Value: 0x00)		
HRS	5:0	Hours Counter Register
Reserved	6	Fixed to 0
PA-H	7	AM/PM Indication, Only active during 12 Hr mode x0 = AM x1 = PM
RTCHA (ADDR 0x15 - R/W - Default value: 0x00)		
HRSALARM	5:0	Hours Alarm Setting Register
Reserved	6	Fixed to 0
PA-HA	7	AM/PM Alarm Setting, Only active during 12 Hr mode x0 = AM x1 = PM

Table 24. RTC Date/Time Configuration Register Structure and Bits Description

RTCDW (ADDR 0x16 - R/W - Default Value: 0x01)		
DOW	2:0	Day of Week counter register : 1= Sunday ... 7= Saturday
Reserved	7:3	Reserved
RTCDM (ADDR 0x17 - R/W - Default Value: 0x01)		
DOM	5:0	Day Of Month Counter Register
Reserved	7:6	Reserved
RTCM2 (ADDR 0x18 - R/W - Default Value: 0x01)		
MONTH	4:0	Months Counter Register
Reserved	6:5	Reserved
19/20	7	THIS BIT IS NOT SUPPORTED Always Reads 0 (treated as a reserved bit)
RTCY (ADDR 0x19 - R/W - Default Value: 0x00)		
YEAR	7:0	Year Counter Register. Note: Values range from 0 to 99

Table 25. RTC Control Registers Structure and Bit Description

Name	Bits	Description
RTCA (ADDR 0x1A - R - Default Value: 0x20)		
Reserved	6:0	Fixed to 010000
UIP	7	This is the Update In Progress (UIP) bit used as a status flag x0 = Update cycle not in progress x1 = Update cycle is in progress or will begin soon
RTCB (ADDR 0x1B - R/W - Default Value: 0x02)		
Reserved	0	Fixed to 0
HRMODE	1	Hour Format Control x0 = 12 Hour Mode x1 = 24 Hour Mode
DM	2	Data Mode for Time and Calendar Updates x0 = Binary-Coded-Decimal (BCD) x1 = Binary
Reserved	3	Fixed to 0
UIE	4	Update-Ended Interrupt Enable x0 = Update-End (UF) bit in Register C is not permitted to assert the interrupt request flag (IRQF) in Register C x1 = Update-End (UF) bit in Register C is permitted to assert the interrupt request flag (IRQF) in Register C
AIE	5	Alarm Interrupt Enable x0 = Alarm flag (AF) bit in Register C is not permitted to assert the interrupt request flag (IRQF) in Register C x1 = Alarm flag (AF) bit in Register C is permitted to assert the interrupt request flag (IRQF) in Register C
Reserved	6	Fixed to 0
SET	7	Set mode enable bit for the program to initialize the time and calendar bytes x0 = The update cycle functions normally by advancing the counts once-per-second. x1 = Any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing.

Table 25. RTC Control Registers Structure and Bit Description

RTCC (ADDR 0x1C - R - Default Value: 0x00)		
Reserved	3:0	Reserved
UF	4	Update-Ended Interrupt Flag. Set after each update cycle. X0 = UIE bit will not effect IRQF state x1 = When UIE bit goes high, the IRQF bit goes high
AF	5	Alarm Interrupt Flag. Indicates that the current time has matched the alarm time. X0 = AIE bit will not effect IRQF state x1 = When AIE bit goes high, the IRQF bit goes high
Reserved	6	Fixed to 0
IRQF	7	Interrupt Request Flag. IRQF = (AF&AIE) + (UF&UIE) The interrupt request flag (IRQF) is set to a “1” when one or more of the following are true: AF = AIE = “1” UF = UIE = “1” x0 = Above Equation is not true x1 = Above Equation is true
RTCD (ADDR 0x1D - R - Default Value: 0x00)		
Reserved	6:0	Fixed to 000000
VRT	7	The Valid RAM and Time (VRT) bit indicates the condition of the contents of the RTC time and calendar registers . A “0” appears in the VRT bit when the RTC registers have been reset. The processor program should set the VRT bit after the time and calendar are initialized to indicate that the time and calendar are valid. The VRT bit can only be set by reading register D.
RTCE (ADDR 0x1E - R/W - Default Value: 0x05)		
OSCSTP	0	Oscillator (32 kHz) Clock Stop Flag x0 = XTAL Oscillator x1 = Internal RC Oscillator
BKDET	1	Coin Cell Backup Voltage Status x0 = No change x1 = Coin Cell below “low-voltage” threshold When this bit is set to 1, the SW takes corresponding action for a coin cell well below the operating voltage, and clear the BKDET in order to get ready for the next event.
POR	2	RTC Reset Flag x0 = No reset was detected x1 = POR occurred
SCRATCH	7:3	These bits shall not exert any control over the operation of the RTC, and are intended to be used as scratch pad registers by the system controller. Their contents are erased on RTCPORB.
ADJ (ADDR 0x1F - R/W - Default Value: 0x00)		
ADJ	0	RTC Trim Enable Signal x0 = Do Not Trim x1 = Trim
Reserved	7:1	Fixed to 0000000
TRIM (ADDR 0x20 - R/W - Default Value: 0x00)		
TRIMVAL	5:0	6-Bit Trim Control This is a number from 0 to 63 that represents the number of seconds to adjust out of every 64 seconds
SIGN	6	RTC Calibration Sign Bit x0 = Add x1 = Subtract

Table 25. RTC Control Registers Structure and Bit Description

Reserved	7	Fixed to 0
CLKOUT (ADDR 0x21 - R/W - Default Value: 0x00)		
M32KCLK	0	32 kHz clock output mask x0 = 32 kHz clock output enabled x1 = 32 kHz clock output masked (disabled)
Reserved	7:1	Fixed to 0000000

POWER STATES AND CONTROL

OVERVIEW

The following section discusses the different Power States of the 900841 PMIC, what causes the 900841 to be in each of them, and how the SCU is involved.

In Ultra-mobile platforms, the SCU is required to be alive as long as a valid battery or a valid charger input (a USB source or a wall plug) exists. If any of the previous two power sources are present, the 900841 powers up the SCU part of Platform controller hub, with a minimum set of power supplies, and the SCU takes over the system.

The previous paragraph simplifies the operation modes and power states of the 900841 solution, and essentially limits the power states to 3 different states, that is discussed at length later:

1. No Power: Depleted or no coin cell battery, main battery, and charger input
2. RTC State: 900841 has enough power to support the RTC operation and keep registers alive, but not to power the SCU
3. Active State: 900841 has enough power to supply the SCU

INTERNAL SUPPLIES POWER TREE

Before going into the Power State of 900841 solution as a system and how it interacts with Platform controller hub to support the needs of the platform, first examine how the 900841 powers itself up and its internal power tree.

Figure 17 is a block diagram of the 900841 internal power tree.

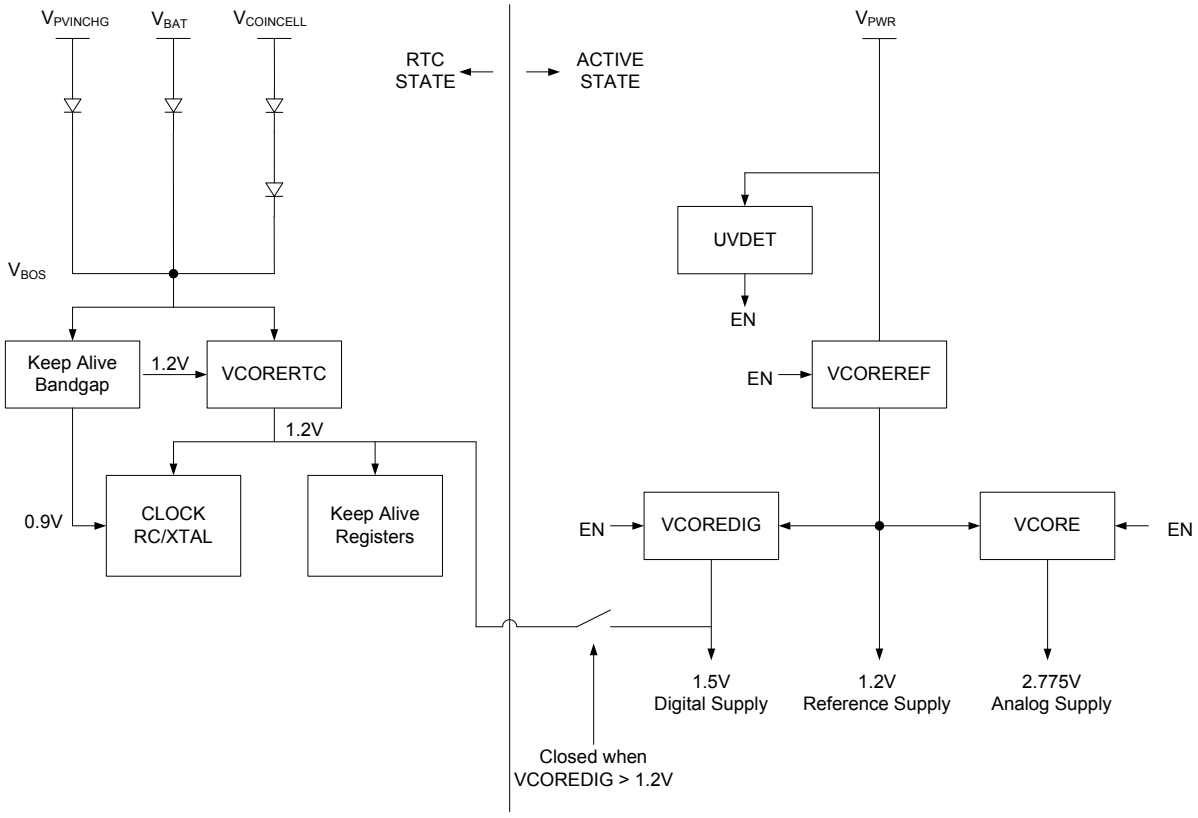

Figure 17. 900841 Internal Power Tree Block Diagram

It is important to note that the VPWR node is the main supply to the loads and the rest of the system (see Battery Interface and Power Path Management). The availability of V_{PWR} determines what power state the 900841 IC is in. Availability of V_{PWR} is discussed later. The next subject is the effect of V_{PWR} voltage on how the 900841 is internally powered.

$V_{PWR} < V_{PWRUVF}$

If V_{PWR} is less than the under-voltage falling threshold of 2.65 V, then the system cannot power up, and the RTC circuitry and clock, and the keep alive registers, receive their supply from a node, called the Best of Supply node (V_{BOS}), see Figure 17. These ensure that power to these critical circuits is maintained for maximum life.

V_{BOS} represents the highest of the following voltages:

1. $V_{PVINCHG}$: This is the charger input voltage after the protection circuitry, reference Battery Interface and Power Path Management for more information
2. V_{BAT}: This is the main battery voltage
3. $V_{COINCELL}$: This is the coin cell battery voltage, backup battery

$V_{PWR} > V_{PWRUVR}$

If V_{PWR} is available and valid (V_{PWR} > 3.0 V), then the main internal supplies that provide power to the rest of the circuitry can power up:

1. $V_{COREREF}$: This is the main bandgap and reference voltage for all internal circuitries.
2. V_{CORE}: This is the supply for the 900841 analog circuitry.
3. $V_{COREDIG}$: This is the supply for the 900841 digital circuitry.

Notice that when $V_{COREDIG}$ is > 1.2 V, a switch is closed, and the circuitry that was powered from V_{BOS} is now powered from $V_{COREDIG}$.

The following table summarizes the voltage references on the 900841.

Table 26. 900841 Internal Power Supply Summary

Reference	Parameter	Target
VCOREREF (Bandgap & Regulators Reference)	Output Voltage	1.2 V
	Bypass Capacitor	100 nF typ.
VCOREDIG (Digital Core Supply)	Output Voltage	1.5 V
	Bypass Capacitor	2.2 μF typ.
VCORE (Analog Core Supply)	Output Voltage	2.775 V
	Bypass Capacitor	2.2 μF typ.

POWER STATES

Figure 18 shows the flow of power, the different power states, and the conditions necessary to transition between the different states. This diagram serves as the basis for the description in the remainder of this section.

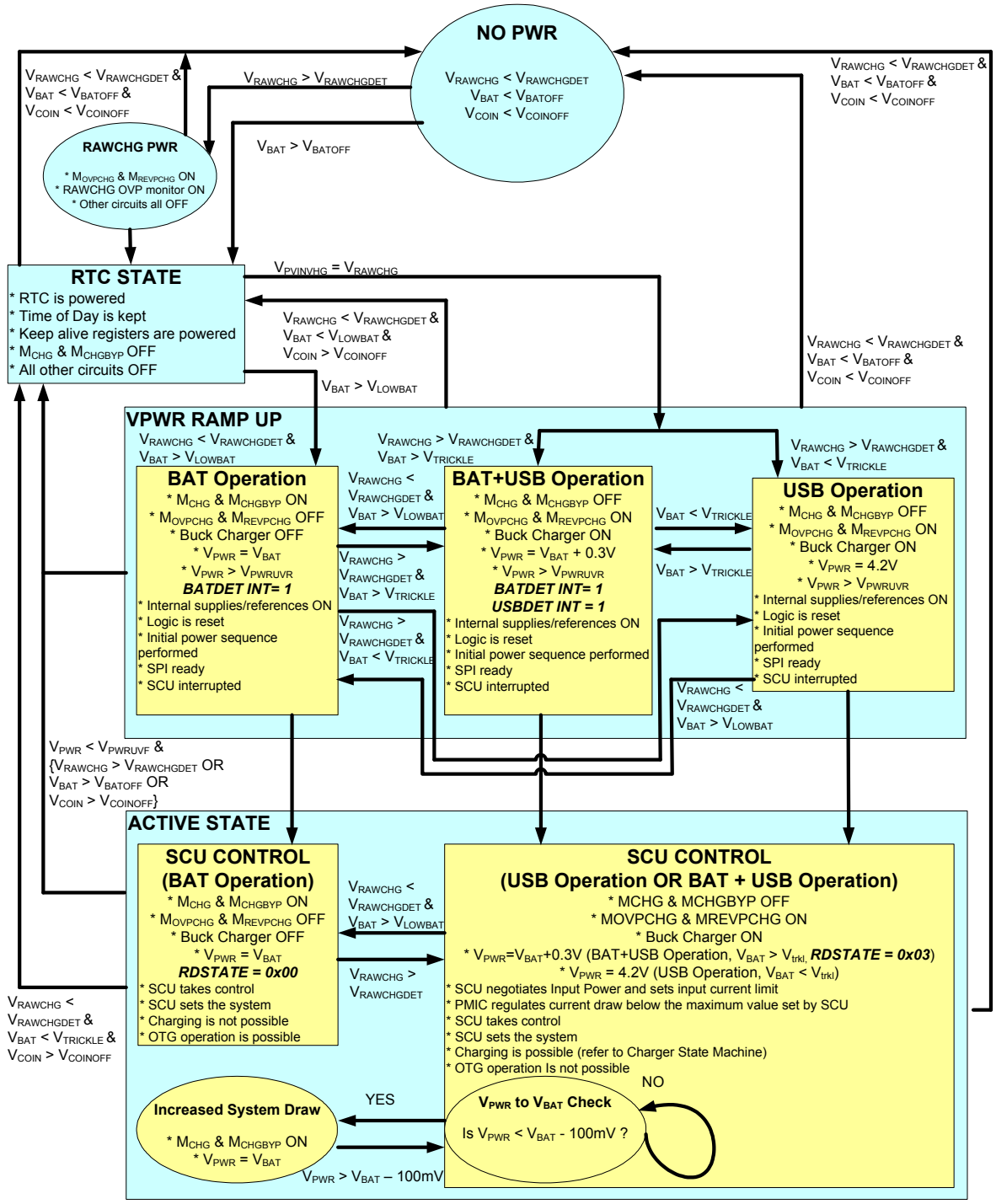

Figure 18. 900841 Power States

No Power State

In this state, every source of power has been removed or is fully depleted:

- $V_{RAWCHG} < V_{RAWCHGDET}$: The charger input is not available or is below the detection threshold
- $V_{BAT} < V_{BATOFF}$: The main battery has been removed or has been isolated by its own protection circuitry to stop it from depleting even further
- $V_{COIN} < V_{COINOFF}$: The coin cell backup battery has been removed or has been isolated by the 900841 coin cell discharge prevention circuitry (see Coin Cell Battery Backup/Charger)

The 900841 has lost any source of power to maintain the RTC and its keep alive registers, and all circuitry will power down and time of day cannot be kept.

RTC State

If one of the following two conditions is satisfied, then SC900841 goes from the No Power State to the RTC State:

1. $V_{RAWCHG} > V_{RAWCHGDET}$: A charger input is valid and has been detected.
2. $V_{BAT} > V_{BATOFF}$: A main battery has been inserted with a valid voltage range.

If either of the previous two conditions occur, the V_{BOS} is available and will route the power to the $V_{CORERTC}$ and the Keep Alive bandgap. As a result, the RTC is powered, Time of day is initialized to a factory set value, see Real Time Clock (RTC), and all keep alive registers are maintained.

During this mode the main battery is isolated and all other circuits are off. SCU cannot be powered up.

In order to route the power from the RAWCHG node to the PVINCHG node, which is one of the supplies to the Best of Supply circuitry, MOVPCHG and MREVPCHG have to turn on upon valid charger input voltage detection. See Battery Interface and Power Path Management for more information.

During this mode no turn on is accepted. The only blocks operational are:

- The charger interface (monitoring of the charger input voltage)
- RTC module
- Keep alive registers

No specific power control timer is running in this mode. All main and external supplies are off. The Platform controller hub will also be off by virtue of the loss of its supply source.

The 900841 stays in this state as long as the previous two conditions are satisfied, and V_{PWR} is below its rising threshold V_{PWRUVR}

Active State

In this state the 900841 internal circuits are fully powered, the Platform controller hub SCU and I/Os are powered, and SPI communication is available. All features of the 900841 are either operating or can be enabled, which is under the control of the Platform controller hub.

The key to entering the active state is a valid V_{PWR} voltage. The following examines how the 900841 ramps up V_{PWR} depending on the available power source:.

V_{PWR} RAMP UP

One of the following two conditions causes a VPWR ramp up sequence:

1. $V_{RAWCHG} > V_{RAWCHGDET}$: A charger input is valid and has been detected. Note that this is the same condition for an RTC state. This means that if this condition occurs, the device goes through the RTC state, then directly into a VPWR ramp up sequence to try and get to the active state (see Figure 18 for more details).
2. $V_{BAT} > V_{LOWBAT}$: The main battery voltage is above the V_{LOWBAT} threshold of 3.2 V.

For number 1, the Buck Charger turns on and regulates V_{PWR} to a voltage that depends on the state of the battery:

- If $V_{BAT} < V_{TRICKLE}$, then $V_{PWR} = 4.2$ V
- If $V_{BAT} > V_{TRICKLE}$, then $V_{PWR} = V_{BAT} + 0.3$ V

For number 2, the Buck charger stays off, and the MCHG and MCHGBYP FETs turn on to short the battery voltage with the V_{PWR} node. Note that number 2 implies that the charger input is not present or is not valid.

After V_{PWR} crosses the under-voltage rising detection threshold (V_{PWRUVR}) of 3.0 V, the internal supplies power on, the logic is reset, initial power sequence is performed, SPI communication is ready, and the Platform controller hub is interrupted. The system is now completely under SCU control. Now it is in the active state.

In the active state, the following types of operations are possible. Note that for simplicity, a valid charger input operation is called the USB Operation:

1. Battery Operation
   - $V_{BAT} > V_{LOWBAT}$ and $V_{RAWCHG} < V_{RAWCHGDET}$.
   - $V_{PWR} = V_{BAT}$
   - MCHG and MCHGBYP are ON, shorting the battery with the VPWR node
   - MOVPCHG and MREVPCHG are OFF, isolating the charging input from the battery
   - Charging is not possible
   - OTG host mode operation is possible
   - Note: If OTG host mode operation is enabled, the USBDET Interrupt flag is ignored.
2. USB Operation
   - $V_{RAWCHG} > V_{RAWCHGDET}$ and $V_{BAT} < V_{TRICKLE}$.
   - $V_{PWR} = 4.2$ V
   - MCHG and MCHGBYP are OFF, isolating the battery
   - MOVPCHG and MREVPCHG are ON
   - Charging is possible
   - OTG host mode operation is not possible
3. USB + Battery Operation
   - $V_{RAWCHG} > V_{RAWCHGDET}$ and $V_{BAT} > V_{TRICKLE}$.
   - $V_{PWR} = V_{BAT} + 0.3$ V
   - MCHG and MCHGBYP are OFF, isolating the battery

- MOVPCHG and MREVPCHG are ON
- Charging is possible
- OTG host mode operation is not possible

During 2 and 3, if at any time $V_{PWR} < V_{BAT} - 100$ mV, MCHG and MCHGBYP turn on fully to support the system power requirements.

Reference Figure 18 and Battery Interface and Power Path Management.

Table 27 summarizes the power selection, V_{PWR} value, and the operation mode of the 900841, depending on the state of battery and charger input.

Table 27. Power Selection Summary

Detection		Register Setting			Mode of Operation					Comment
USBDET	BATDET	CHRENB	CHR	OTGB	Buck Charger	MOVPCHG & MREVPCHG	MCHG	MCHGBYP	VPWR	
0	0	X	X	X	OFF	OFF	OFF	OFF	Floating	System not in operation
0	1	X	0	X	OFF	OFF	ON	ON	VBAT	System can turn on - No OTG Host mode
		X	1	0	OFF	ON	ON	ON	VBAT	System Can turn on & OTG Host mode ON (VOTG = 5.0 V)
		X	1	1	OFF	OFF	ON	ON	VBAT	System can turn on - No OTG Host mode
1	0	0	X	X	ON	ON	ON	OFF	4.2 V	Charging
		1	X	X	ON	ON	OFF	OFF	4.2 V	USB Supplies System - No Battery Operation - No Charging
1	1	0	X	X	ON	ON	ON	OFF	VBAT+0.3 V	Charging
		1	X	X	ON	ON	OFF	OFF	VBAT+0.3 V	USB Supplies System - No Battery Operation - No Charging

TURN ON EVENTS

If the 900841 is in the RTC State, full operation as outlined previously to reach to the active state, can be obtained via a turn on event. The turn on events are listed by the following. To indicate to the SC, which turn on event caused the system to power on, a corresponding interrupt status bit is set, allowing the system controller to retrieve when it is up.

- $V_{RAWCHG} > V_{RAWCHGDET}$: Valid Charger Input present. USBDET Interrupt bit is set
- $V_{BAT} > V_{LOWBAT}$: Valid Battery for system turn on present. The BATDET Interrupt bit is set

Reference Interrupt Controller for more information on the various system interrupts.

These are the only 2 turn on events. Otherwise, the 900841 is in the RTC State or the No Power State.

Initial Power Up Sequence

The following diagram shows the initial power up sequence the 900841 performs when a turn on event is detected:

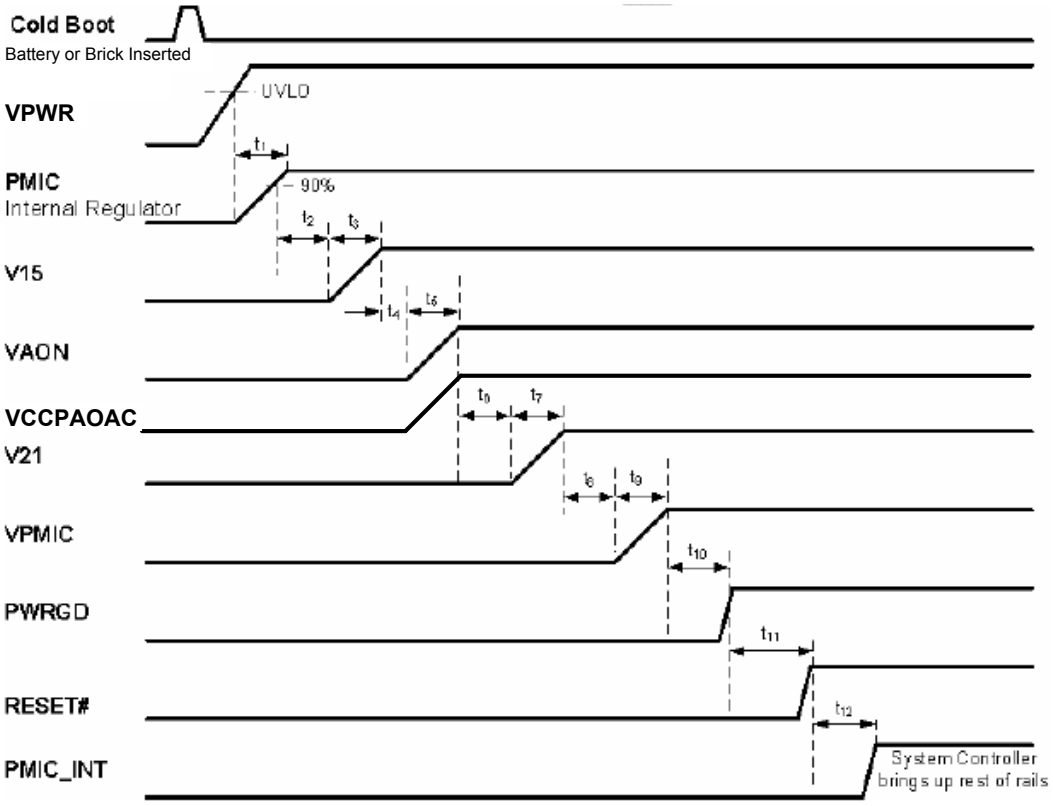

Figure 19. 900841 Initial Power Up Sequence

1. A turn on event as outlined above is detected
2. V_{PWR} ramps up
3. The 900841 internal circuits are powered
4. The 900841 turns on a minimal set of voltage rails as outlined in Figure 19
5. SPI communication is ready
6. PMICINT pin is asserted
7. The system controller reads the 900841 interrupt flag register (over SPI) to see why the 900841 interrupted the Platform controller hub.
8. SC decides whether to boot the rest of the system, or just run SC code to manage charger or other functions.
9. If SC decides to power up system, then CPU (central processing unit) drives VNN VID, VIDEN[1:0] = 10 to the 900841 and BSEL to the Platform controller hub.
10. The 900841 drives CPU selected voltage for VNN
11. There will be no explicit signaling from the 900841 that indicates that the VNN ramp has been complete.
12. VIDEN[1:0] is driven to 00 to avoid it switching from 10 to 01 directly.
13. NC drives the VCC boot VID on the VID pins. The VIDEN[1:0] = 1 enables, only after HPLL has locked.
14. X86 Instruction Executions starts.

Table 28. SC900841 Initial Power Up Timing

Parameter	Description	Min	Typ	Max
t_1	PMIC internal regulator Ramp-up	-	-	100 µs
t_2	V15 turn on delay	0 µs	-	31 µs
t_3	V15 Ramp-up	-	-	10 µs
t_4	VAON/VCCPAOAC turn on delay	0 µs	-	31 µs
t_5	VAON/VCCPAOAC ramp-up	-	-	700 µs
t_6	V21 turn on delay	0 µs	-	31 µs
t_7	V21 ramp-up	-	-	100 µs
t_8	VPMIC turn on delay	0 µs	-	31 µs
t_9	VPMIC ramp-up	-	-	700 µs
t_{10}	PWRGD delay	70 ms	-	90 ms
t_{11}	RESET delay	1.0 µs	-	31 µs
t_{12}	PMICINT delay	31 µs	-	124 µs

TURN OFF EVENTS

Once in the active state, the following causes the 900841 to power off the system, including the SCU. The 900841 internal circuitry and logic is still active:

- PWRBTN pressed for more than 5 seconds. See Power Button Functionality (PWRBTN).

- The 900841 junction temperature is above the thermal shutdown threshold. See Thermal Management for more details.
- A THERMTRIPB assertion. See THERMTRIPB Pin for more details.
- A BATOCP detection. See BATOCP.

The following causes the 900841 to power the entire system, including its internal circuitry if $V_{PWR} < V_{PWRUVF}$ occurs.

Power Button Functionality (PWRBTN)

The Power button is pulled up internally through a 132 k resistor to the $V_{COREDIG}$ output voltage node. See Figure 20 for more details. This guarantees the functionality of the button when either power source available.

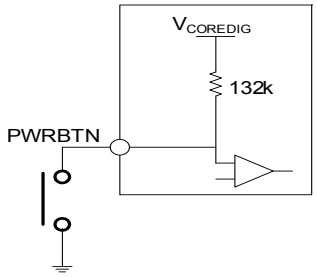

Figure 20. PWRBTN Circuit Diagram

Figure 21 describes the functionality of the PWRBTN:

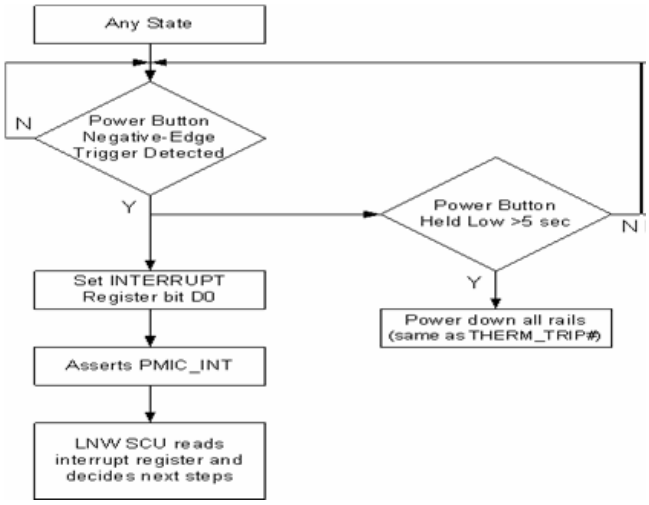

Figure 21. PWRBTN Function Flow Diagram

DETECTION THRESHOLDS

Table 29 summarizes the various detection thresholds between the different states:

Table 29. Power States Detection Thresholds

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Rising Detection Threshold	$V_{RAWCHGDET}$	-	-	4.50	V
Input Voltage Rising Detection Threshold Hysteresis	$V_{RAWCHGDETHYS}$	-	100	-	mV
Battery Cutoff Threshold (Depending on Battery Model)	V_{BATOFF}	2.2	-	2.4	V
Coin Cell Disconnect Threshold	$V_{COINOFF}$	1.8	-	2.0	V
Low Battery Threshold	V_{LOWBAT}	3.2	-	-	V
Valid Battery Threshold	V_{TRKL}	-	3.0	-	V
VPWR Rising Under-voltage Threshold	V_{PWRUVR}	-	3.1	-	V
VPWR Falling Under-voltage Threshold	V_{PWRUVF}	-	2.55	-	V

POWER SUPPLIES

POWER MAP

Figure 22 is a power map of Freescale's power management solution for Ultra-mobile platforms:

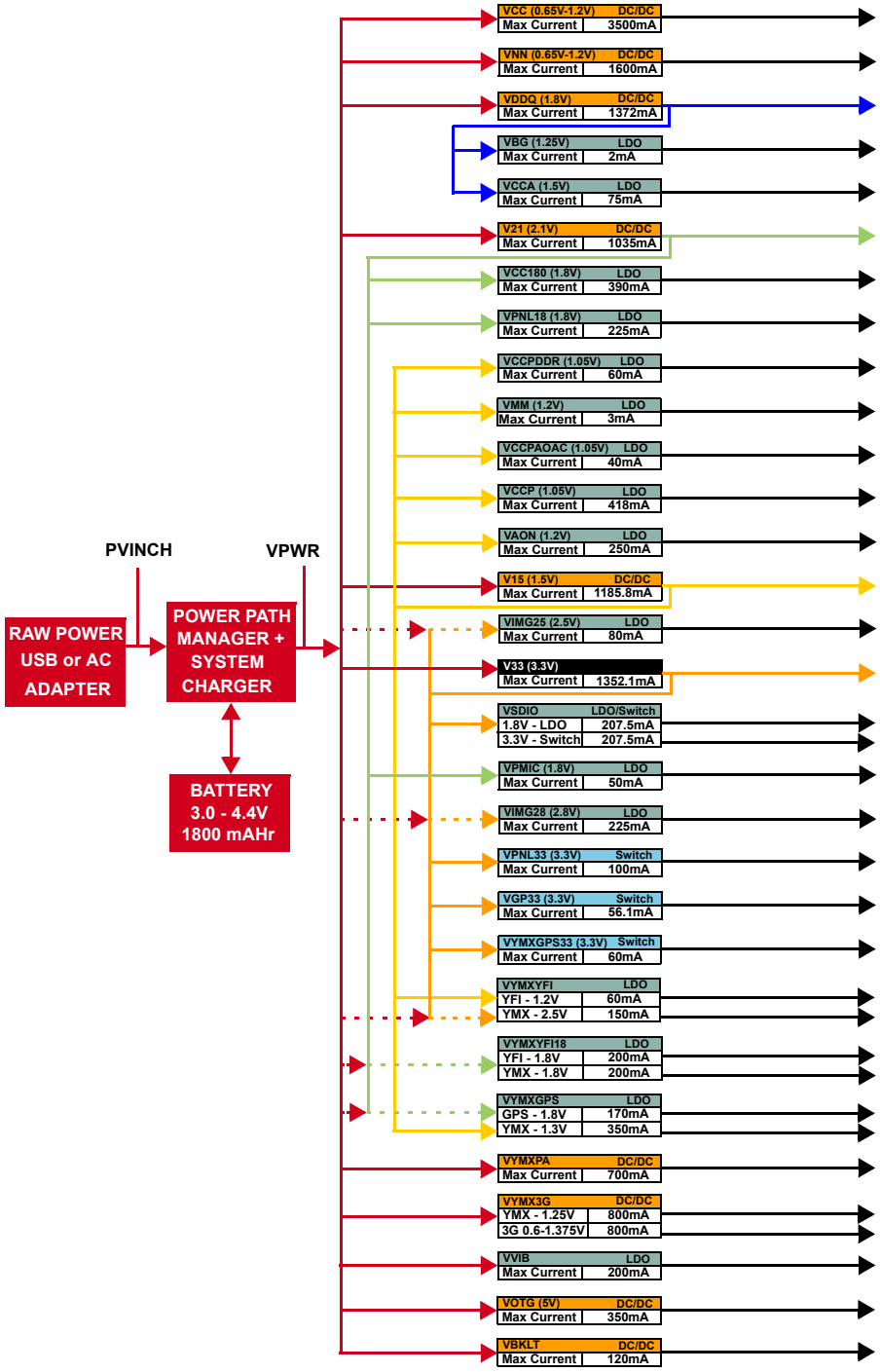

Figure 22. SC900841 Power Map

DC/DC POWER SUPPLIES

Freescale's power management solution for the Ultra-mobile platform for MID includes 10 DC/DC switching regulators, nine are included in the 900841 PMIC, and one is implemented in the companion chip, 900842. Six out of the nine regulators are Buck converters, and the remaining three are Boost converters, and these can be set to work in the following operation modes:

Buck converters Operation Modes Selections (VCC, VNN, VDDQ, V21, V15, VYMX3G)

- OFF - The regulator is switched off and the output voltage is discharged.
- PFM - The regulator is switched on and set to PFM mode operation. In this mode, the regulator is always running in PFM mode. Useful at light loads for optimized efficiency.
- Automatic Pulse Skip - The regulator is switched on and set to Automatic Pulse Skipping. In this mode, the regulator moves automatically between pulse skipping and full PWM mode depending on load conditions.
- PWM - The regulator is switched on and set to PWM mode. In this mode, the regulator is always in full PWM mode operation regardless of load conditions.
- TEST/TRIM - This is not a functional mode, thus requiring certain steps to prevent unintentional activation of this mode. During this mode, the device performs measurements and trimming.

Boost Converters Operation Modes Selections (VYMXPA, VOTG, VBKLT)

- OFF - The regulator is switched off
- ON
  - The regulator is switched on and the output is at the programmed level
  - Maximum load current allowed
- TEST/TRIM
  - This is not a functional mode, thus requiring certain steps to prevent unintentional activation of this mode
  - During this mode, the device performs measurements and trimming

DC-DC Power Supply Summary Table

Table 30 provides a summary of all DC/DC regulators on the 900841.

Table 30. SC900841 DC-DC power supplies.

Regulator	Typ. Voltage	Max Continuous Current	Description
VCC	0.3 - 1.2 V	3.5 A	1.0 MHz synchronous Buck converter with external switching MOSFETs. Internally compensated. VID is controlled using a shared 7-bit bus for voltage coding and 2 VID enable signals for VCC or VNN selection.
VNN	0.3 - 1.2 V	1.6 A	1.0 MHz synchronous Buck converter with external switching MOSFETs. Internally compensated. VID is controlled using a shared 7-bit bus for voltage coding and 2 VID enable signals for VCC or VNN selection.
VDDQ	1.8 V	1.3 A	4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.
V21	2.1 V	1.0 A	4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.
V15	1.5 V	1.5 A	4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.
VYMX3G	1.25 V 0.6-1.375 V	1.0 A	4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.
VYMXPA	4.2 V 5.0 V	0.7 A 0.5 A	2.0 MHz non-synchronous Boost PWM current mode control DC/DC regulator with internal low side FET.
VOTG	5.0 V	0.35 A	2.0 MHz non-synchronous Boost PWM current mode control DC/DC regulator with internal low side FET to support host mode in USB On-The-Go systems.
VBKLT	6.0 - 23.0 V	120 mA	2.0 MHz non-synchronous Boost PWM current mode control DC/DC regulator with internal low side FET to support LED backlighting system.

Note that all of the DC/DC regulators specify an extended input voltage range beyond the 3.0 to 4.4 V applications range. Under this extended range, functionality is maintained, but parametric performance might be compromised.

VCC

This is a VID controlled single-phase 1.0 MHz 2-switch synchronous Buck PWM voltage mode control DC/DC regulator, designed to power high performance CPUs. VCC uses external MOSFETs, P-Ch high side and N-Ch low side.

VCC includes support for VID active voltage positioning requirements. A 7-bit DAC reads the VID input signals and sets the output voltage level. The output voltage has a range of 0.3 to 1.2 V. The programming step size is 12.5 mV. Values will be read in real time and will be stored in internal registers not accessible to the system host. Reference VIDEN[1:0] & VID[6:0] Pins for more details.

The same VID input signals are shared between VCC and VNN, where a latch signal for each regulator decides which regulator takes control of the VID input signals.

The DAC value represents the output voltage value. The output voltage node is connected directly to the inverting input of the error amplifier that uses the DAC output as its reference, unity gain configuration. Using this configuration with internal compensation eliminates the need for the feedback and compensation network, which saves board space and cost. The DAC/output voltage slew rate is internally set 25 mV/µs to minimize transient currents and audible noise.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The above selection is optimized to maximum battery life based on load conditions.

VCC will be discharged every time the regulator is shutting down.

The output current will be sensed using an intelligent implementation of the DCR sensing method using internal sensing circuitry, which eliminates the need for an external RC filter network in parallel with the output inductor and its winding resistance.

DCR sensing theory is that if the impedance of the two filters are matching by insuring that $R*C = L/R_W$, then the voltage across the capacitor is equal to the value of the voltage across the winding resistance R_W, $V_{CAP} = I_{LOAD}*R_W$. Based on this, the voltage across the capacitor is measured, and with a known R_W value, the load current can be extracted. The measured current value will be digitized by the ADC and stored in a register for the processor to access. The method used on the 900841 measures the voltage across R_W in a similar fashion, while using internal sensing circuitry.

The sensed output current value will also be used for over-current protection. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation, and alert the system through the VCCFAULT signal, which will in turn assert the VRFAULT Interrupt signal.

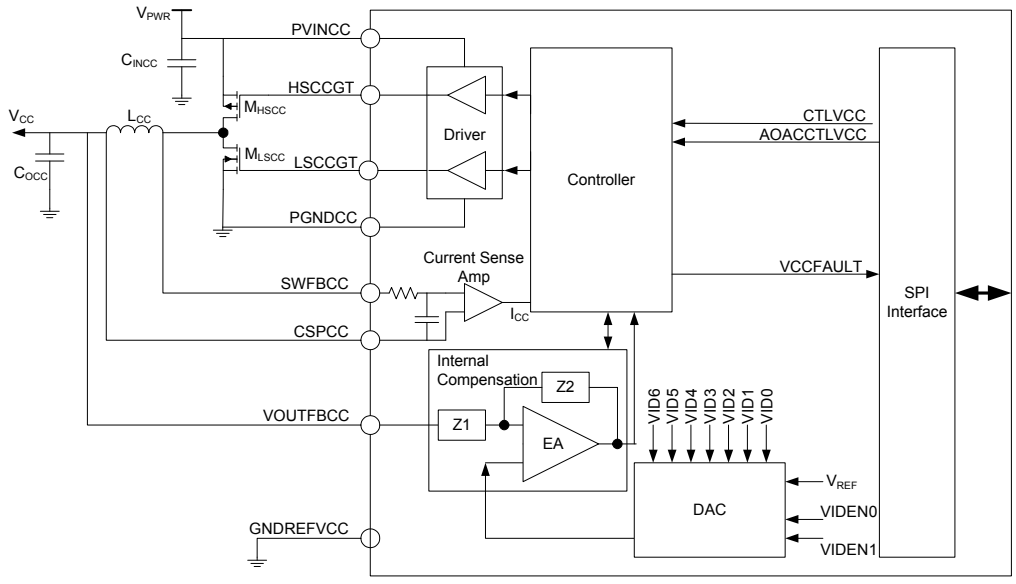

Figure 23. VCC Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used to provide power to the CPU Core.
- Single-Phase Solution with Integrated Drivers and external MOSFETs
- VID Controlled for dynamic voltage scaling requirements of high performance processors
- 1.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.

900841

- Loss-Less Output Current Sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

The efficiency curves in Figure 24 are calculated under PWM mode, based on the recommended external component values and typical output voltage of 1.2 V. 3.0 V ≤ VPWR ≤ 4.4 V.

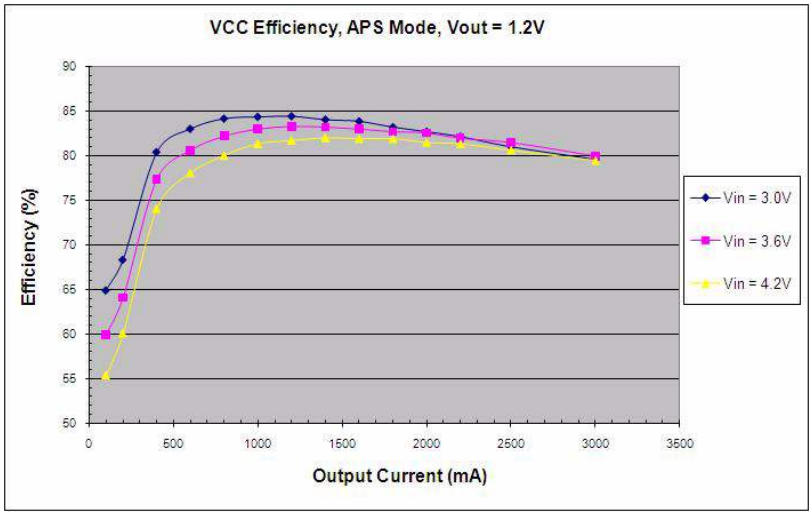

Figure 24. VCC Efficiency Curve

VCC Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 31. VCC Status Registers Structure and Bits Description

Name	Bits	Description	
VCCCNT (ADDR 0x35 - R/W - Default Value: 0x24)			
CTLVCC	2:0	VCC State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLVCC	5:3	VCC State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	
VCCLATCH (ADDR 0X32 - R/W - Default value: 0x7F)			
VIDVCC	6:0	VID VCC Control Through SPI. Signal codes are identical to the VID signal codes. Reference Figures 15 for more details	
DVP1VRD	7	VCC Register override enable bit. X0 = VCC VID control follows the external pins x1 = VCC VID control follows the VIDVCC control register bits	

VNN

This is a VID controlled single-phase 1.0 MHz 2-switch synchronous Buck PWM voltage mode control DC/DC regulator, designed to power high performance CPUs. VNN uses external MOSFETs, P-ch high side and N-ch low side.

VNN includes support for VID active voltage positioning requirements. A 7-bit DAC reads the VID input signals and sets the output voltage level. The output voltage has a range of 0.3 to 1.2 V. The programming step size is 12.5 mV. Values will be read in real time and will be stored in internal registers not accessible to the system host. Reference VIDEN[1:0] & VID[6:0] Pins.

The same VID input signals are shared between VNN and VNN, where a latch signal for each regulator decides which regulator takes control of the VID input signals.

The DAC value represents the output voltage value. The output voltage node is connected directly to the inverting input of the error amplifier that uses the DAC output as its reference, unity gain configuration. Using this configuration with internal compensation eliminates the need for the feedback and compensation network, which saves board space and cost. The DAC/output voltage slew rate is internally set 25 mV/µs to minimize transient currents and audible noise.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The previous selection is optimized to maximum battery life based on load conditions.

VNN will be discharged every time the regulator is shutting down.

The output current is sense in the same way as it is done on VCC regulator. (See VCC)

The sensed output current value will also be used for over-current protection. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation and alert the system through the VNNFAULT signal, which will in turn assert the VRFAULT Interrupt signal.

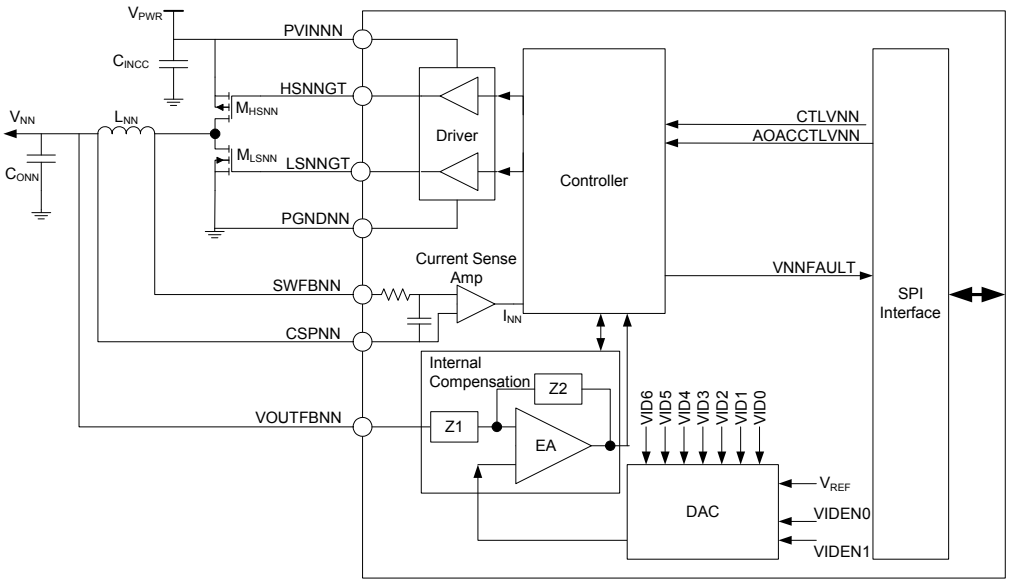

Figure 25. VNN Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used to provide power to the Graphics Core.
- Single-Phase Solution with Integrated Drivers and external MOSFETs
- VID Controlled for dynamic voltage scaling requirements of high performance processors
- 1.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Loss-Less Output Current Sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

The following efficiency curves are calculated under PWM mode based on the recommended external component values and typical output voltage of 1.2. 3.0 V ≤ VPWR ≤ 4.4 V.

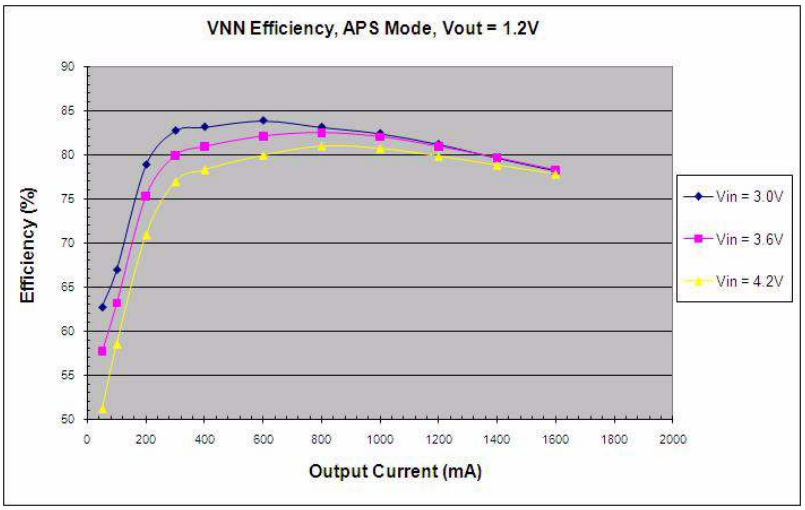

Figure 26. VNN Efficiency Curve

VNN Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers

Table 32. VNN Status and Control Registers Structure and Bits Description

Name	Bits	Description	
VNNCNT (ADDR 0x36 - R/W - Default value: 0x04)			
CTLVNN	2:0	VNN State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLVNN	5:3	VNN State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	
VNNLATCH (ADDR 0x33 - R/W - Default value: 0x7F)			
VIDVNN	6:0	VID VNN Control Through SPI. Signal codes are identical to the VID signal codes. Reference Figure 15 for more details	
DVP1VRD	7	VNN Register override enable bit. X0 = VNN VID control follows the external pins x1 = VNN VID control follows the VIDVNN control register bits	

VDDQ

This is a 4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage-mode control DC/DC regulator.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode.

VDDQ will be discharged every time the regulator is shutting down.

The output current is measured internally, digitized by the ADC, and stored in a register for the processor to access. The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through a cycle by cycle operation and alert the system through the VDDQFAULT signal, which will in turn assert the VRFAULT Interrupt signal.

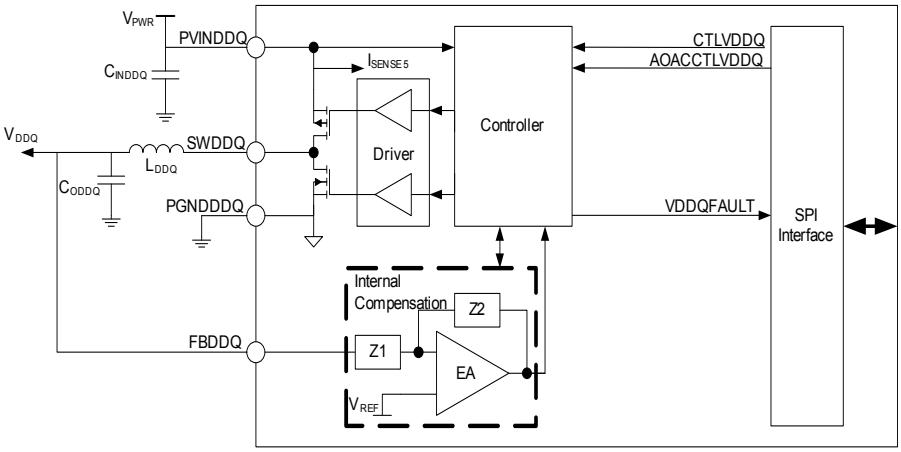

Figure 27. VDDQ Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used as a pre-regulator to many LDO rails, for enhanced efficiency and reduced thermal dissipation. It also supplies power to rails in the CPU (central processing unit), Platform controller hub, and the platform
- Uses Integrated MOSFETs
- 4.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Peak current sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

The following efficiency curves are calculated under PWM mode, based on the recommended external component values and typical output voltage of 1.8 V. 3.0 V ≤ VPWR ≤ 4.4 V.

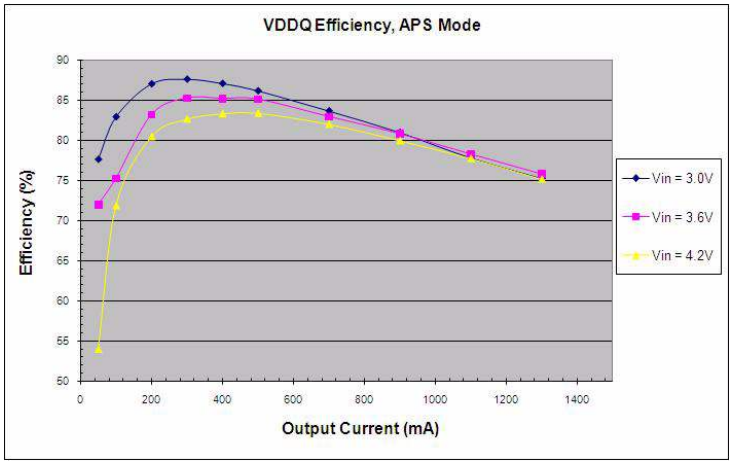

Figure 28. VDDQ Efficiency Curves

VDDQ Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 33. VDDQ Status and Control Register Structure and Bits Description

Name	Bits	Description	
VDDQCNT (ADDR 0x37 - R/W - Default Value: 0x04)			
CTLVDDQ	2:0	VDDQ State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLVDDQ	5:3	VDDQ State Control during AOAC Exit (when EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	

V21

This is a 4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage-mode control DC/DC regulator.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The previous selection is optimized to maximum battery life based on load conditions.

V21 will be discharged every time the regulator is shutting down.

The output current is measured internally, digitized by the ADC, and stored in a register for the processor to access.

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation and alert the system through the V21FAULT signal, which will in turn assert the VRFAULT Interrupt signal.

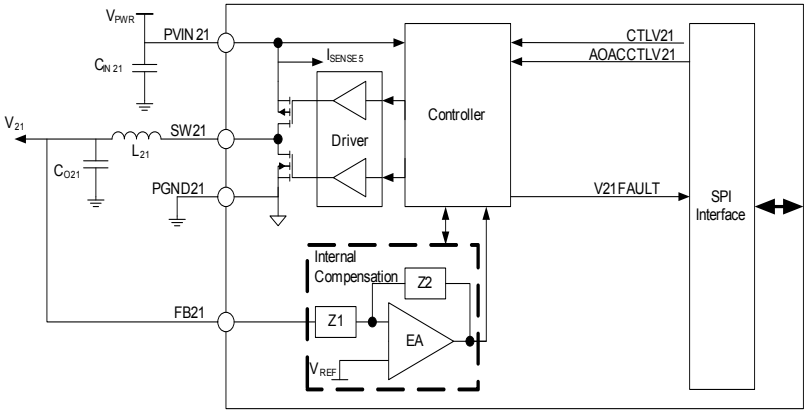

Figure 29. V21 Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used as a pre-regulator to many LDO rails, for enhanced efficiency and reduced thermal dissipation.
- Uses Integrated MOSFETs
- 4.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Peak current sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

The following efficiency curves are calculated under PWM mode, based on the recommended external component values and typical output voltage of 2.1 V. 3.0 V ≤ VPW ≤ 4.4 V.

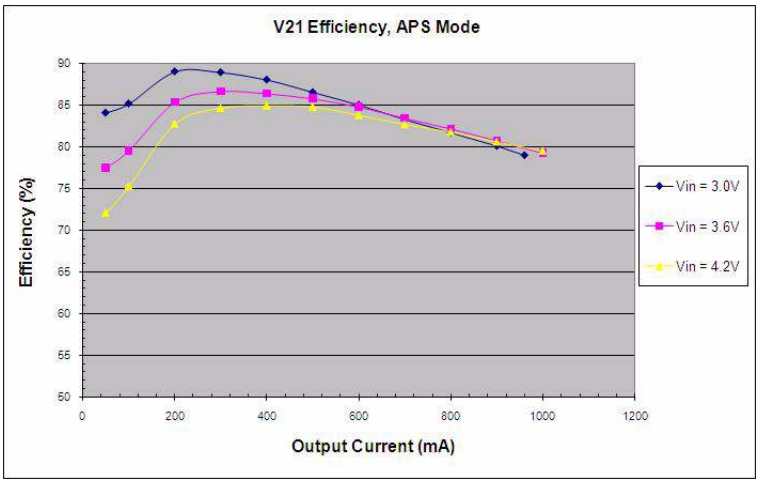

Figure 30. V21 Efficiency Waveforms

V21 Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 34. V21 Status/Control Registers Structure and Bits Description

Name	Bits	Description	
V21CNT (ADDR 0x38 - R/W - Default value: 0x07)			
CTLV21	2:0	V21 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLV21	5:3	V21 State Control during AOAC Exit (when EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	

V15

This is a 4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage-mode control DC/DC regulator.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The above selection is optimized to maximum battery life based on load conditions.

V15 will be discharged every time the regulator is shutting down.

The output current is measured internally, digitized by the ADC, and stored in a register for the processor to access.

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation and alert the system through the V15FAULT signal, which will in turn assert the VRFAULT Interrupt signal.

Please note that when VYMXGPS is set at 1.3 V, V15 is automatically set at 1.6 V to maintain voltage headroom for the operation of 1.3 V VYMXGPS, reference VYMXGPS for more details.

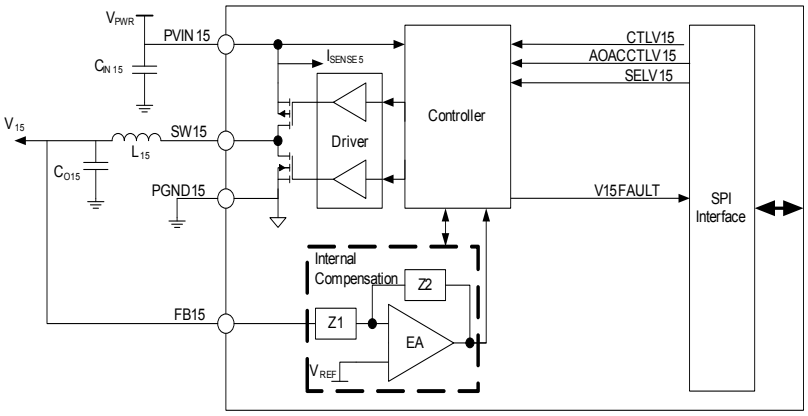

Figure 31. V15 Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used as a pre-regulator to many LDO rails, for enhanced efficiency and reduced thermal dissipation. It also supplies power to rails in the Platform controller hub
- Uses Integrated MOSFETs
- 4.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Peak current sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

The following efficiency curves are calculated under PWM mode, based on the recommended external component values and typical output voltage of 1.5 V. 3.0 V ≤ VPWR ≤ 4.4 V.

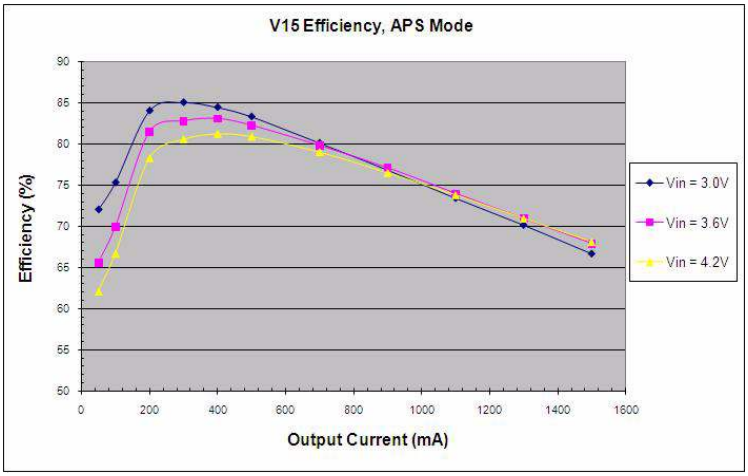

Figure 32. V15 Efficiency Curves

V15 Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 35. V15CNT Register Structure and Bits Description

Name	Bits	Description	
V15CNT (ADDR 0x39 - R/W - Default value: 0x07)			
CTLV15	2:0	V15 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLV15	5:3	V15 State Control during AOAC Exit (when EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
SELV15	7:6	V15 Output Voltage Selection (FSL Usage Only) X0 = 1.5 V x1 = 1.6 V x2, x3 = Reserved	

VYMX3G

This is a 4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage-mode control DC/DC regulator.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The above selection is optimized to maximum battery life based on load conditions.

VYMX3G will be discharged every time the regulator is shutting down.

The output current is measured internally, digitized by the ADC, and stored in a register for the processor to access.

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation and alert the system through the VYMX3GFAULT signal, which will in turn assert the VRFAULT Interrupt signal.

This regulator is used as the advanced communications modules digital core supply and has to different output voltage settings depending on the application. For WiMAX applications the output voltage is set to 1.25 V. For 3G applications the output voltage can be varied between 0.6 to 1.375 V through the Mini-SPI interface. See Advanced COMMs Serial Interface for more details.

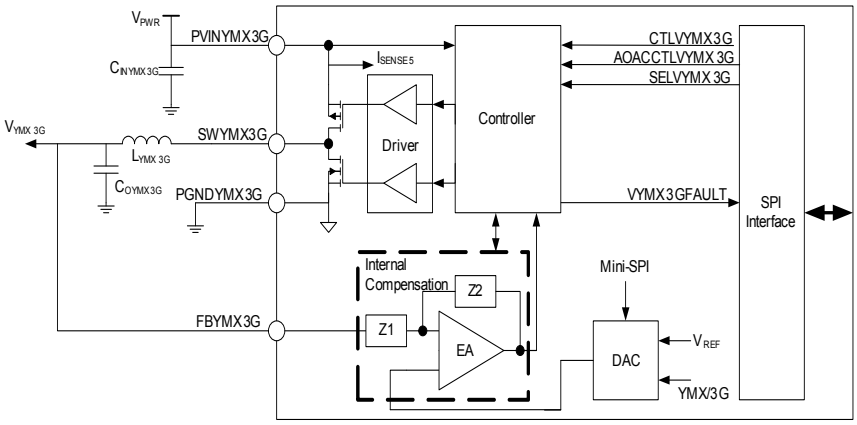

Figure 33. VYMX3G Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- Used as the advanced communications module digital core supply
- Uses Integrated MOSFETs
- 4.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch
- Output current sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

The following efficiency curves are calculated under PWM mode based on the recommended external component values and typical output voltage of 1.2 V. 3.0 V ≤ VPWR ≤ 4.4 V.

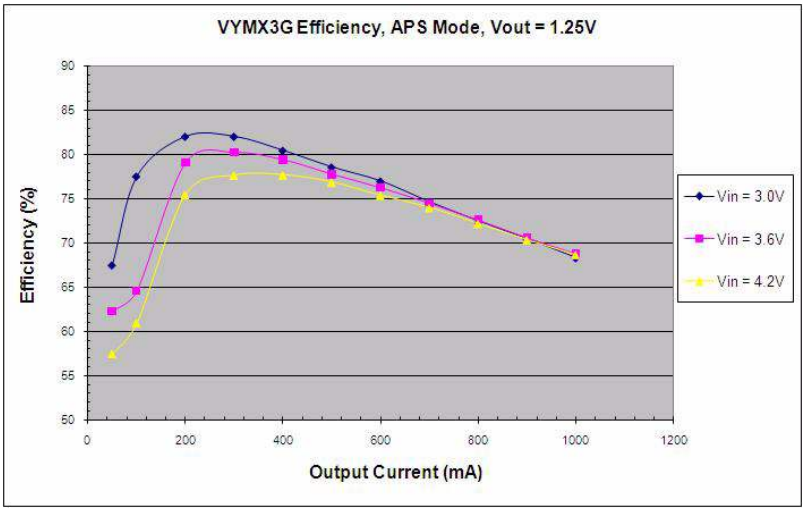

Figure 34. VYMX3G Efficiency Curves

VYMX3G Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 36. VYMX3G Control Register Structure and Bits Description

Name	Bits	Description	
VYMX3GCNT (ADDR 0x3C - R/W - Default Value: 0x24)			
CTLVYMX3G	2:0	VYMX3G State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLVYMX3G	5:3	VYMX3G State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
SELVYMX3G	7:6	VYMX3G Output Voltage Selection. X0 = 1.25 V (WiMAX Operation) x1 = 1.0 V (Default 3G Operation Mini-SPI controls output voltage) x2, x3 = Reserved	

VYMXPA

This is a 2.0 MHz non-synchronous Boost PWM current-mode control DC/DC regulator with internal low side FET.

VYMXPA is designed to supply the Power Amplifier for the WiMAX module, it provides a fixed 4.2V output voltage, and capability to supply up to 700 mA of drive current. It can also be used to support many applications that need a 5.0 V supply voltage, as in motor drives and high current OTG Buses. If used as a 5.0 V supply then the current capability is limited to a 500 mA maximum.

Since the output of VYMXPA is close to the maximum battery voltage, at very high battery input voltage conditions, the output will track the battery voltage minus a diode forward voltage drop (output is directly connected to the input through the inductor and an external diode).

Due to the possible need to isolate the output of VYMXPA boost from the actual load, an external PMOS switch (M_{YMXPA}) will be used to switch in VYMXPA output to the load, as shown in Figure 13. M_{YMXPA} is always enabled and if it is not needed, then do not populate the switch and ground the YMXPAGTIN and YMXPAGT pins.

When M_{YMXPA} is used, then users can either connect the feedback node after or before the switch. Accuracy is maintained where the feedback node is connected. The output capacitor C_{OYMXPA} can also connect to either node but is recommended to follow the feedback node connection.

VYMXPA can be discharged only if M_{YMXPA} is used and the feedback node is taken after the switch. The discharge FET is connected internally to the FBYMXPA pin. If M_{YMXPA} is not used, then the discharge FET should be disabled by setting the VYMXPADISDSCH bit, since VYMXPA cannot be discharged due to the lack of an isolation FET (the output is directly connected to the input through the inductor and an external diode).

Since VYMXPA is supplying the power amplifier of a WiMAX module, it can be presented with a high load transient current, so close attention to the VYMXPA transient response is in order here to account for these possible load changes.

VYMXPA includes under-voltage, over-voltage, over-current, and short-circuit protection.

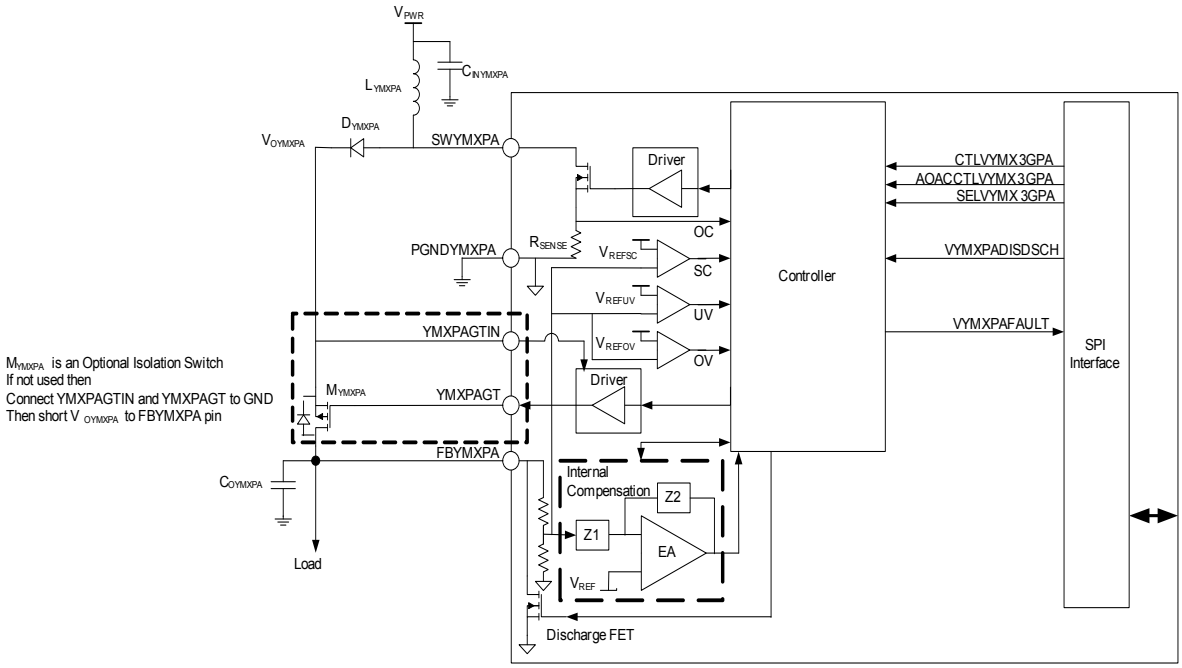

Figure 35. VYMXPA Detailed Internal Block Diagram

Under-voltage Detection

VYMXPA features an output under-voltage detection comparator that serves as an output ready signal, along with the absence of faults. When VYMXPA is turned on, a VYMXPAFAULT is asserted, the under-voltage comparator is turned on, and V_{OYMXPA} starts ramping up. When V_{OYMXPA} (measured at FBYMXPA) reaches a steady state, VYMXPAFAULT is de-asserted to indicate the VYMXPA output readiness to start. During operation, if the output voltage is decreased below the under-voltage threshold, an under-voltage condition is detected, and VYMXPAFAULT is asserted. If the output voltage rises above the under-voltage threshold plus hysteresis, the VYMXPAFAULT signal is cleared, assuming no other faults are occurring.

Over-current Protection

VYMXPA limits the peak inductor current by sensing the switch MOSFET current. The over-current threshold value is set higher than the worst peak inductor current value. If an over-current is detected, the switch MOSFET turns off, the VYMXPAFAULT flag is asserted, and the regulator goes into a cycle by cycle current limiting until the fault is serviced. If the

output current falls below the over-current threshold, normal operation is regained and the VYMXPAFAULT is cleared, assuming no other faults are occurring.

Short-circuit Protection

VYMXPA protects the internal MOSFET from excessive currents, in case of an output short, by detecting the voltage on the feedback pin FBYMXPA. If the FBYMXPA voltage falls below a set threshold, VYMXPA detects a short-circuit, turns off VYMXPA, turns off the isolation switch, and asserts the VYMXPAFAULT flag. There is no automatic restart after this event, and VYMXPA has to be re-enabled in order to clear the VYMXPAFAULT flag.

Short-circuit protection is disabled during soft start, to prevent false or premature detection of a short-circuit condition, as the block will be subjected to an inrush current possibly higher than the trip threshold. If a short were already present when starting up, soft start would end after about 4.0 ms, SC is detected, and the boost is disabled as described.

Over-voltage Protection

VYMXPA features an output over-voltage protection comparator that senses the output voltage through an internal resistor divider connected at FBYMXPA pin, compares it to an internal reference, and shuts down the regulator, in the case an excessive voltage occurs for any reason, and asserts the VYMXPAFAULT flag. The over-voltage threshold is fixed at a 5.77 V typical. There is no automatic restart after this event. VYMXPA has to be re-enabled in order to clear the VYMXPAFAULT flag.

Main Features

- Supplies the power amplifier of a WiMAX module.
- Uses the V_{PWR} rail as its power supply
- Supports up to 700 mA (500 mA) of output current at 4.2 V (5.0 V) fixed output voltage
- 2.0 MHz switching frequency
- Uses internal compensation
- Soft Start feature to minimize inrush currents at power up
- Uses internal low side switch MOSFET
- Gate drive circuits are supplied directly from V_{PWR}
- Output over-voltage, under-voltage, over-current, and short-circuit protection
- External switch control for output isolation when needed

Efficiency Curves

The following efficiency curves are calculated based on the recommended external component values and typical output voltage. 3.0 V ≤ VPWR ≤ 4.4 V. Curves below do not take in account the switch drop across $M_{YMXPA.}$

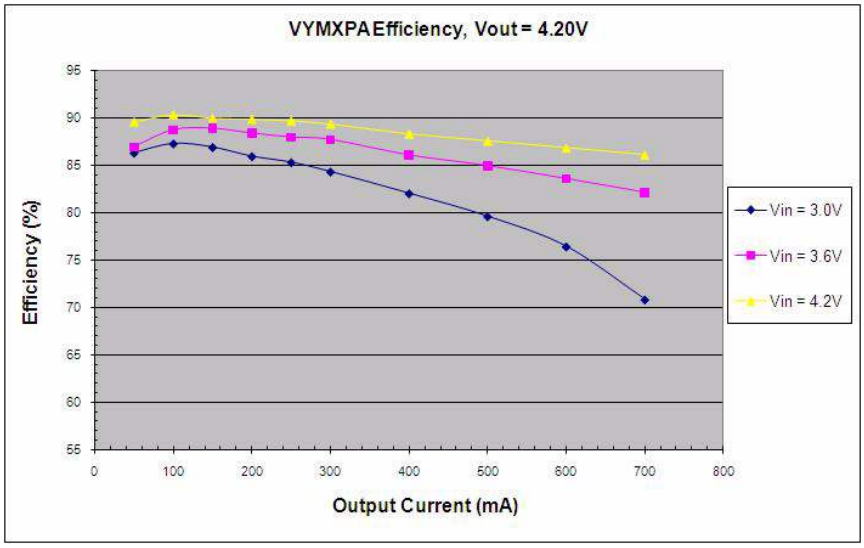

Figure 36. VYMXPA Efficiency Curves (V_{OYMXPA} = 4.2 V)

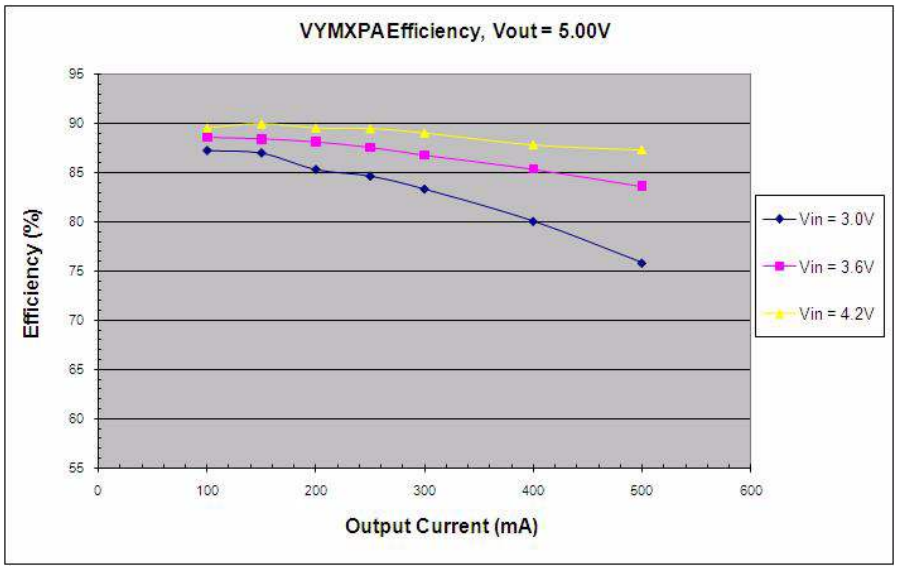

Figure 37. VYMXPA Efficiency Curves (V_{OYMXPA} = 5.0 V)

VYMXPA Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 37. VYMX3GPA Control Register Structure and Bits Description

Name	Bits	Description	
VYMX3GPACNTL (ADDR 0x3B - R/W - Default value: 0x24)			
CTLVYMX3GPA	2:0	VYMX3GPA State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = Output is OFF x5 = Not Used x6 = Not Used x7 = Output is ON
AOACCTLVYMX3GPA	5:3	VYMX3GPA State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Don't Copy x1 = Don't Copy x2 = Don't Copy x3 = Don't Copy	x4 = Output is OFF x5 = Not Used x6 = Not Used x7 = Output is ON
SELVYMX3GPA	7:6	VYMX3GPA Output Voltage Settings x0 = 4.2 V (WiMAX application) x1 = Reserved x2 = 5.0 V (General use applications) x3 = Not Used	

VYMXPA Status/Control Registers and Bits Description (Freescale Defined)

Reference the register map for read/write conditions and default state for each of these registers

Table 38. FSLVYMXPACNTL Register Structure and Bits Description

Name	Bits	Description
FSLVYMXPACNTL (ADDR 0x1C7 - R/W - 0x01)		
VYMXPADISDSCH	0	VYMXPA Discharge FET Disable Signal x0 = Discharged enabled x1 = Discharged disabled
Reserved	7:1	Reserved

VOTG

This is a 2.0 MHz non-synchronous Boost PWM current-mode control DC/DC regulator with internal low side FET. VOTG provides a fixed 5.0 V output voltage and capability to supply up to 350 mA of drive current. It can be used separately to support many applications that need a 5.0 V supply voltage, as in motor drives. The following are the typical loads for VOTG in SC900841 application

- Signaling/Status LED Drivers, See Lighting System.
- USB Bus (VBUS) while 900841 is operating in host mode as part of an UBS On-The-Go (OTG) System.

VOTG allows the 900841 the capability to support host mode in USB-OTG systems. It offers the capability of up to 100 mA to supply to the USB Bus (VBUS). Due to the need to isolate the USB Bus from the rest of the system when not in use, an external PMOS switch (M_{OTG}) will be used to switch in a VOTG output to VBUS, as shown in Figure 16.

M_{OTG} enable is controlled through the CHRG and OTGB bits in the CHRGCNTL register. Reference Active State for more details into when the OTG host mode is enabled and M_{OTG} is enabled. OTG host mode is only possible when under battery operation and no input power is connected. When OTG host mode is enabled, the USBDET interrupt flag is ignored.

If OTG support is not needed, this switch does not need to be populated, reducing the overall system cost, while the OTGGTIN and OTGGT pins are grounded

The rest of the VOTG load consists of a total of 6 LED drivers at 30 mA maximum each. These LED drivers may turn on one at a time, at different drive values, or they may all turn on together at the maximum driver value for each. Close attention to VOTG transient response is in order here, to account for these possible load changes.

If OTG host mode is not used, M_{OTG} can still be used as an isolation switch. When M_{OTG} is used, then users can either connect the feedback node after or before the switch. Accuracy is maintained where the feedback node is connected. The output capacitor C_{OOTG} can also connect to either node, but is recommended to follow the feedback node connection.

VOTG can be discharged only if M_{OTG} is used and the feedback node is taken after the switch. The discharge FET is connected internally to the FBOTG pin. If M_{OTG} is not used, then the discharge FET should be disabled by setting the VOTGDISDSCH bit, since VOTG cannot be discharged due to the lack of an isolation FET (the output is directly connected to the input through the inductor and an external diode).

VOTG includes under-voltage, over-voltage, over-current, and short-circuit protection.

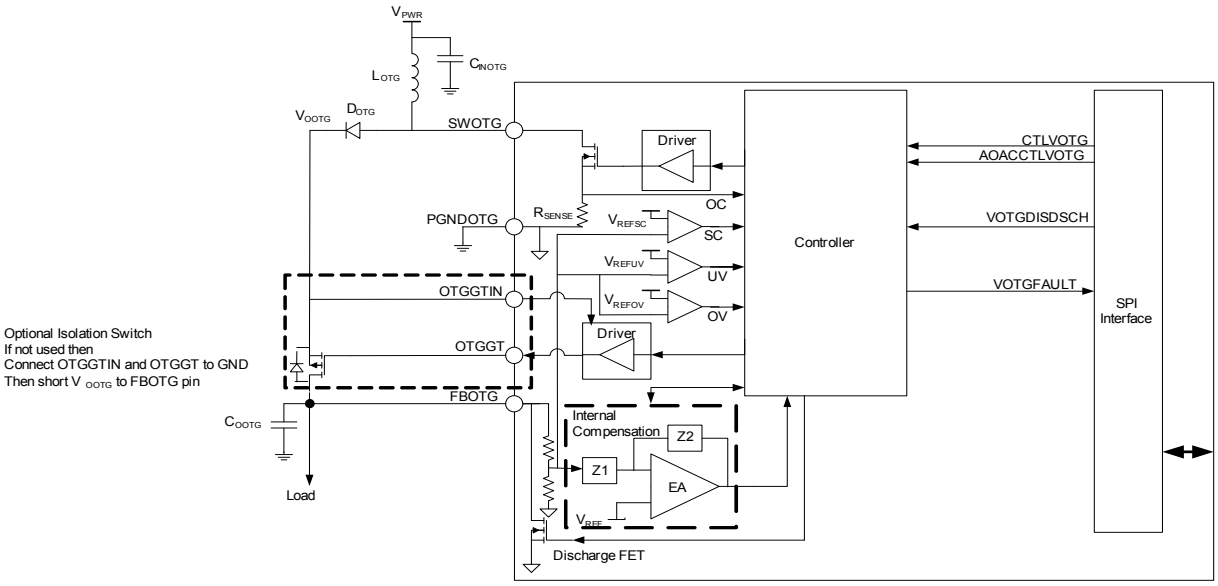

Figure 38. VOTG Detailed Internal Block Diagram (Using OTG Host Mode)

VOTG Operation

VOTG on/off control is based on a combination of signals, FSLVOTGCNTL2 bits (Table 40), and CHRG and OTGB bits in the CHRGCNTL register. Table 39 summarizes VOTG response to the signals.

The CHRG bit will direct if the OTG Host mode is allowed, and the OTGB bit will control if the OTG Boost voltage is fed to the connector. In other words, if CHRG=0, then the isolation FET is OFF, regardless of the status of OTGB and CTLVOTG, and the boost is controlled directly via the CTLVOTG.

If CHRG=1, then the isolation FET is controlled via the OTGB signal. If OTGB=0, then the boost is on and the isolation FET is on. If OTGB=1, then the boost is controlled via CTLVOTG.

Remember that the VOTG can handle two different loads, before the switch (LEDs) and after the switch (OTG Host). This is why it is extremely important to separate the operation of the Boost output and the isolation FET. See Table 39 for a truth table of the discussion.

Table 39. VOTG On/Off Control

CHRG	OTGB	CTLVOTG	VOTG	Isolation FET	SC900841	Comments
0	0	OFF	OFF	OFF	Since CHRG=0, then SC900841 the system intends for the charger to work in the buck mode, so no OTG host mode is required. The isolation FET should stay OFF	This does not mean that we cannot use VOTG (the node before the isolation switch) to supply other loads like RGB LEDs. This is why the VOTG output is controlled directly by the CTLVOTG. Notice if CHRG=0, OTGB does not play a role, and software should plan for that
0	0	ON	ON	OFF		
0	1	OFF	OFF	OFF		
0	1	ON	ON	OFF		
1	0	OFF	ON	ON	Since CHRG=1, then the system intends the charger to work in the boost mode, so the OTG host mode is allowed. The isolation FET can be turned off/on to supply OTG voltage to the connector	OTG mode is allowed, now supplying the voltage to the connector, which is controlled via the OTGB bit, directly turning the isolation FET on/off. If OTGB=0, then the OTG voltage is supplied to the connector (VOTG and isolation FET are on). If OTGB=1, then the isolation FET is OFF and the VOTG voltage is controlled directly through the CTLVOTG bits to supply another load if desired
1	0	ON	ON	ON		
1	1	OFF	OFF	OFF		
1	1	ON	ON	OFF		

Under-voltage Detection

VOTG features an output under-voltage detection comparator that serves as an output ready signal along with the absence of faults. When VOTG is turned on, VOTGFAULT is asserted, the under-voltage comparator is turned on, and V_{OOTG} starts ramping up. When V_{OOTG} (measured at FBOTG) reaches a steady state, VOTGFAULT is de-asserted to indicate the VOTG output readiness to start. During operation, if the output voltage decreased below the under-voltage threshold, an under-voltage condition is detected and VOTGFAULT is asserted. If the output voltage rises above the under-voltage threshold plus hysteresis, the VOTGFAULT signal is cleared, assuming no other fault are occurring.

Over-current Protection

VOTG limits the peak inductor current by sensing the switch MOSFET current. The over-current threshold value is set higher than the worst peak inductor current value. If an over-current is detected, the switch MOSFET turns off, the VOTGFAULT flag is asserted, and the regulator goes into a cycle by cycle current limiting until the fault is serviced. If the output current falls below the over-current threshold, normal operation is regained and the VOTGFAULT is cleared, assuming no other faults are occurring.

automatic restart after this event, and VOTG has to be re-

Short-circuit Protection

VOTG protects the internal MOSFET from excessive currents, in case of an output short, by detecting the voltage on the FBOTG feedback pin. If the FBOTG voltage falls below a set threshold, VOTG detects a short-circuit, turns off VOTG, turns off the isolation switch, and asserts the VOTGFAULT flag. There is no automatic restart after this event, and VOTG has to be re-enabled in order to clear the VOTGFAULT flag.

Short-circuit protection is disabled during soft start to prevent false or premature detection of a short-circuit condition, as the block will be subjected to an inrush current, possibly higher than the trip threshold. If a short were already present when starting up, soft start would end after about 4.0 ms and then, SC is detected and the boost is disabled as described.

Over-voltage Protection

VOTG features an output over-voltage protection comparator that senses the output voltage through an internal resistor divider connected at the FBOTG pin. It compares it to an internal reference, shuts down the regulator, in the case that an excessive voltage occurs for any reason. It then asserts the VOTGFAULT flag. The over-voltage threshold is fixed at 5.77V, typical. There is no

enabled in order to clear the VOTGFAULT flag.

Main Features

- Supplies signaling/status LEDs and USB OTG
- Uses the V_{PWR} rail as its power supply
- Supports up to 350 mA of output current at a 5.0 V fixed output voltage
- 2.0 MHz switching frequency
- Uses internal compensation
- Soft start feature to minimize inrush currents at power up
- Uses an internal low side switch MOSFET
- Gate drive circuits are supplied directly from V_{PWR}
- Output over-voltage, over-current, and short-circuit protection
- External switch control for output isolation when needed

Efficiency Curves

The following efficiency curves are calculated, based on the recommended external component values and typical output voltage. 3.0 V ≤ VPWR ≤ 4.4 V. The following curves do not take in account the switch drop across M_{OTG}.

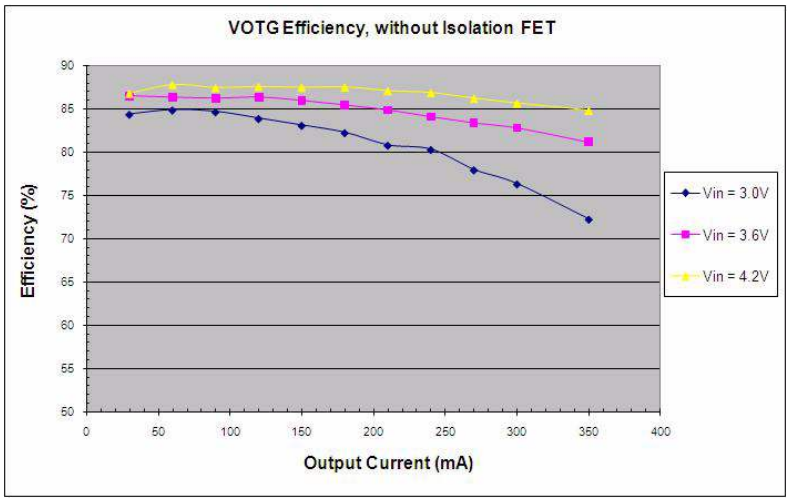

Figure 39. VOTG Efficiency Curves

VOTG Status/Control Registers and Bits Description

The following registers are defined by Freescale in order to provide extended functionality to the VOTG regulator.

Table 40. VOTG Status and Control Registers Structure and Bits Description

Name	Bits	Description	
FSLVOTGCNTL2 (ADDR 0x1C6 - R/W - Default Value: 0x24)			
CTLVOTG	2:0	VOTG State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = VOTG is OFF x5 = Not Used x6 = Not Used x7 = VOTG is ON
AOACCTLVOTG	5:3	VOTG State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Don't Copy x1 = Don't Copy x2 = Don't Copy x3 = Don't Copy	x4 = VOTG is OFF x5 = Not Used x6 = Not Used x7 = VOTG is ON
Reserved	7:6	Reserved	

Table 40. VOTG Status and Control Registers Structure and Bits Description

FSLVOTGCNTL1 (ADDR 0x1C5 - R/W - Default Value: 0x01)		
VOTGDISDSCH	0	VOTG Discharge FET Disable Signal x0 = Discharged enabled x1 = Discharged disabled
Reserved	7:1	Reserved

VBKLT

This is a 2.0 MHz non-synchronous Boost PWM current mode control DC/DC regulator with an internal low side FET.

VBKLT supplies two different loads (see Lighting System) as part of the 900841 LED support:

- 3 strings at up to 5 LEDs per string (3P5S) for LCD backlights. Each string is capable of up to 30 mA.
- 1 string of up to 5 LEDs (1P5S) capable of up to 30 mA for camera scene illumination support.

The Camera Scene Illumination string can be used to expand the backlight support to 4 strings of up to 5 LEDs each (4P5S).

The 900841 can also support an independent zone backlighting option, each supported by two strings. Both backlight displays are completely independent

VBKLT is dedicated to support the prior two loads and cannot be operated with any other load, i.e. VBKLT is enabled only when one or both of the prior two loads is enabled.

It contains adaptive boost control when backlight LEDs are running, to minimize the voltage headroom across the backlight LED current sinks, which in turn reduces power dissipation and saves on overall efficiency. When only operating the camera scene illumination LEDs, the VBKLT output voltage is set to a fixed 22 V output. If the Camera scene string is selected as part of backlight operation, then it can also be selected as part of the adaptive boost control.

PWM signals for the backlight strings are staggered to reduce the amount of transient current on the output of VBKLT and inrush current from the battery.

VBKLT includes under-voltage detection, over-voltage protection, open LED protection, short-circuit and over-current protection

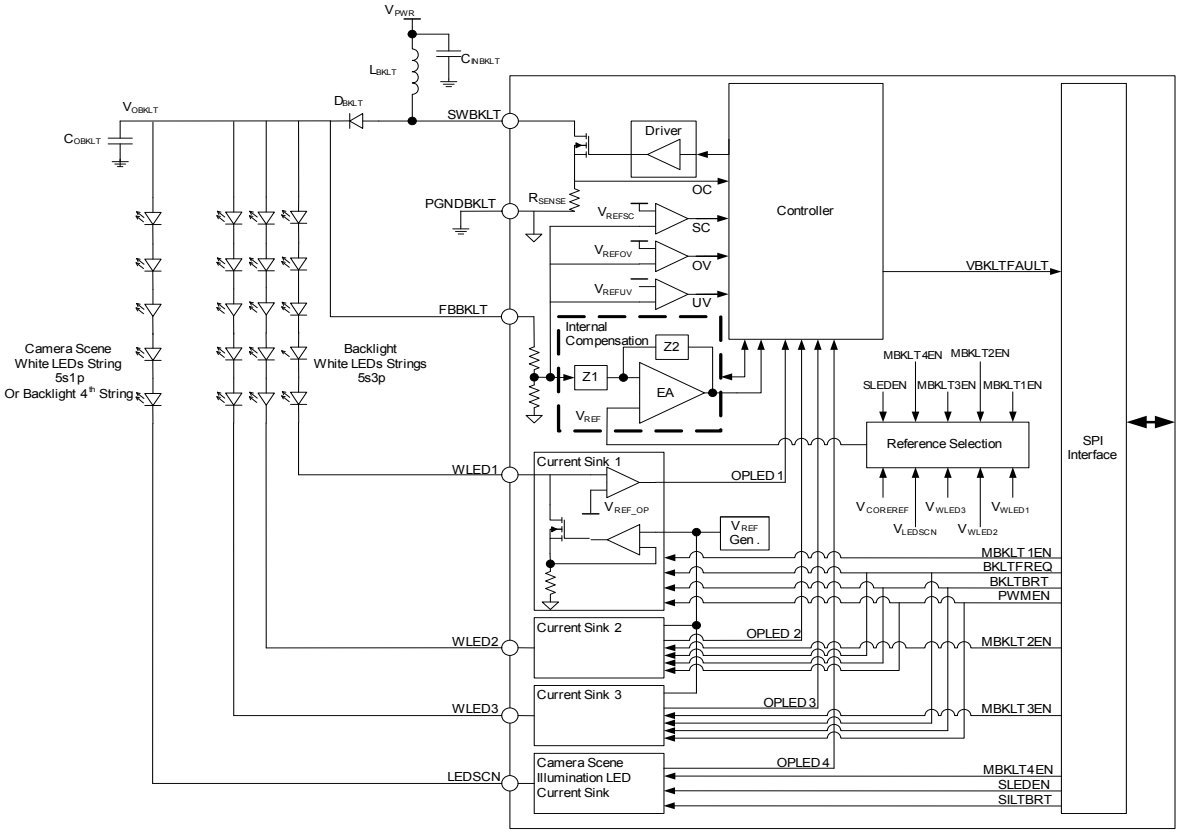

Figure 40. VBKLT Detailed Internal Block Diagram

Operation

VBKLT is not independent and cannot be operated with another load, however the backlight LEDs can be operated without VBKLT.

When supplying only the LCD backlight or both loads, VBKLT uses the lowest voltage of WLED1, WLED2, WLED3, or LEDSCN (if used for backlight support and/or S4ADAPT bit in register FSLVBKLTADAPT is set) as its reference voltage for output voltage regulation. This method assures the string with the highest drop (lowest voltage) has enough voltage headroom to operate, and the minimum output voltage (maximum forward voltage drop across LED strings + voltage headroom necessary to operate the current sinks) is set at the minimum value necessary to drive all LED strings, which reduces power dissipation. If the 4th string is used for camera scene illumination application, then it does not control the output voltage VBKLT.

When supplying only the camera scene illumination string, the output voltage of VBKLT is fixed to 22 V, and uses a fixed reference voltage.

By setting the TWOPTWO bit in the FSLVBKLTCNTL, the 900841 can support an independent zone backlighting option, where strings 1 and 2 support one display backlight, and strings 3 and 4 (Camera scene) support another display. Both string groups are completely independent in terms of frequency and duty cycle control. They are both still supplied from the VBKLT rail.

This reference voltage selection is controlled by the MLED1EN, MLED2EN, MLED3EN, MLED4EN, and SLEDEN bits as shown in Table 41.

Table 41. VBKLT Reference Selection

MLED1EN	MLED2EN	MLED3EN	MLED4EN	SLEDEN	S4ADAPT	VBKLT Voltage Reference
0	0	0	0	0	0	OFF
0	0	0	0	1	0	Fixed
0	0	0	0	1	1	Adaptive
0	0	0	1	0	x	Invalid
x	x	x	1	1	x	Adaptive
1	x	x	x	x	x	Adaptive
x	1	x	x	x	x	Adaptive
x	x	1	x	x	x	Adaptive

The LED current sinks, WLED1-3, can be used as PWM outputs by providing a pull-up to a supply, such as 3.3 V. These PWM outputs can be used to drive an "Integrated Display" with local power supply. In this case, and in the event camera scene illumination is not needed either, then VBKLT is not used and the current sinks are enabled by the PWMEN signal. This signal only enables the current sinks and not VBKLT

VBKLT cannot drive LED(s) with a total minimum forward voltage drop of less than the maximum battery voltage.

VBKLT cannot be discharged due to the lack of an isolation FET (the output is directly connected to the input through the inductor and the external diode). VBKLT however limits the LED leakage current in the off state through the internal current sinks.

VBKLT can support higher number of LEDs in series, with an applications work-around. Reference the Freescale's Evaluation Board KITINTMIDPMMEVBE schematics or discuss with your Freescale representative for more details.

VBKLT Enable Control

Table 42 outlines different cases for VBKLT operation, depending on the display type used and the loads being supplied.

Note that the 4th string cannot be operated for backlighting unless the camera scene enable bit (SLEDEN) is asserted. Also, in order for the 4th string to have the ability to turn on VBKLT, SLEDEN has to be asserted.

In summary, in order for MLED4EN to have any effect, SLEDEN has to also be asserted. This holds true in all of the cases in Table 42.

Table 42 outlines the relation between the different enable bits, the status of VBKLT, and the application mode supported. An “x” in the MLEDxEN column refers to strings 1, 2, and 3.

Table 42. Backlight and Camera Scene LED Enable Bits Control

PWMEN	MLEDxEN	TWOPTWO	SLEDEN	MLED4EN	VBKLT	String 1-3	String 4
0	0	x	0	x	OFF	OFF	OFF
0	0	0	1	0	ON	OFF	Camera Scene

Table 42. Backlight and Camera Scene LED Enable Bits Control

0	0	0	1	1	ON	OFF	Backlight - BKLT1
0	0	1	1	x	ON	OFF	Backlight - BKLT2
0	1	0	0	x	ON	S1-3 Backlight - BKLT1	OFF
0	1	0	1	0	ON	S1-3 Backlight - BKLT1	Camera Scene
0	1	0	1	1	ON	S1-3 Backlight - BKLT1	Backlight - BKLT1
0	1	1	0	x	ON	S1-2 Backlight - BKLT1 S3 Backlight - BKLT2	OFF
0	1	1	1	x	ON	S1-2 Backlight - BKLT1 S3 Backilight - BKLT2	Backlight - BKLT2
1	0	0	0	x	OFF	S1-3 PWM - BKLT1	OFF
1	0	0	1	0	ON	S1-3 PWM - BKLT1	Camera Scene
1	0	0	1	1	ON	S1-3 PWM - BKLT1	Backlight - BKLT1
1	0	1	0	x	OFF	S1-2 PWM - BKLT1 S3 PWM - BKLT2	OFF
1	0	1	1	x	ON	S1-2 PWM - BKLT1 S3 PWM - BKLT2	Backlight - BKLT2
1	1	x	x	x	**Invalid:** PWM mode can't be set at the same time than Backlight for strings 1-3		

Under-voltage Detection

VBKLT features an output under-voltage detection comparator that serves as an output ready signal along with the absence of faults. When VBKLT is turned on, VBKLTFAULT is asserted, the under-voltage comparator is turned on, and VOBKLT starts ramping up. When VBKLT reaches a steady state, VBKLTFAULT is de-asserted, to indicate the VBKLT output readiness to start PWMing the LED sinks.

If VBKLT is supplying the backlight LEDs, the under-voltage comparator is turned off, since the output voltage will not be regulated and is moving, depending on the LED current level and forward voltage drop. If VBKLT is only supplying the camera scene illumination, the under-voltage comparator can stay on, as it is set as a fixed output voltage of 22 V.

Table 43. VBKLT Under-voltage Comparator Status

MLEDxEN	SLEDEN	Under-voltage Comparator
0	0	OFF
0	1	Stays On After VBKLT Ready
1	0	Turns OFF After VBKLT Ready
1	1	Turns OFF After VBKLT Ready

During operation if the output voltage decreased below the undervoltage threshold, an undervoltage condition is detected, VBKLTFAULT is asserted. If the output voltage rises above the under-voltage threshold plus hysteresis, then the VBKLTFAULT signal is cleared, assuming no other faults are occurring.

Over-voltage Protection

VBKLT features an output over-voltage protection comparator that senses the output voltage through an internal resistor divider connected at the FBBKLT pin. It compares the output voltage to an internal reference and shuts down the regulator, in the case an excessive voltage occurs, due to an open LED or other reason, and asserts the VBKLTFAULT flag. The over-voltage threshold is fixed at 24 V, typical. The output is re-enabled, the VBKLTFAULT is cleared (assuming no other faults are occurring), and normal operation is resumed when the voltage drops below the over-voltage threshold, minus hysteresis.

Any current sinks being supplied from VBKLT are also turned off.

The output voltage can also be clamped by connecting a Zener diode from the output to ground. The Zener breakdown must be at least 3.0 V higher than the output voltage setting.

Over-current Protection

VBKLT also limits the peak inductor current by sensing the switch MOSFET current. The over-current threshold value is set higher than the worst peak inductor current value. If an over-current is detected, the switch MOSFET turns off, the VBKLTFAULT flag is asserted, and the regulator goes into a cycle by cycle current limiting until the fault is serviced. If the output current falls below the over-current threshold, normal operation is regained, and the VBKLTFAULT is cleared (assuming no other faults are occurring).

Short-circuit Protection

VBKLT protects the internal MOSFET from excessive currents, in case of an output short, by detecting the voltage on the FBBKLT feedback pin. If the FBBKLT voltage falls below a set threshold, VBKLT detects a short-circuit, turns off VBKLT, and asserts the VBKLTFAULT flag. There is no automatic restart after this event, and VBKLT has to be re-enabled in order to clear the VBKLTFAULT flag.

Short-circuit protection is disabled during soft-start to prevent false or premature detection of a short-circuit condition. The block will be subjected to an inrush current, possibly higher than the trip threshold. If a short were already present when starting up, the soft-start would end after about 4.0 ms. SC is detected, and the boost is disabled as described.

Open LED Protection

VBKLT monitors the LED status at the 3 main backlight channels. If an LED fails open, the voltage at the WLEDx pin for the effected string falls close to ground. When this event is detected, the affected string is taken out of the VBKLT control loop, and the output voltage (V_{BKLT}) is determined by the other two strings. Normal operation can be resumed while the affected string is disabled. If this open LED event caused the output voltage to rise, the output voltage will be clamped to 22 V.

Leakage Current Limiting

The LED leakage current is limited to 1.0 µA at room temperature when the current sinks are disabled.

Main Features

- Supplies the LCD backlight and camera scene illumination LEDs
- Drives up to 4 parallel strings of up to 5 LED(s) each at 30 mA maximum current
- Uses the V_{PWR} rail as its power supply
- 120 mA maximum continuous output current for full voltage capabilities.
- 2.0 MHz switching frequency
- Uses internal compensation
- Soft-start feature to minimize inrush currents at power up
- Uses an internal 26 V low side switch MOSFET
- Output under-voltage detection and output over-voltage, short-circuit, and over-current protection
- Open LED protection
- Minimum Leakage current in the off state

Efficiency Curves

The efficiency curves in Figure 41 are calculated based on the recommended external component values and typical output voltage. 3.0 V ≤ VPWR ≤ 4.4 V

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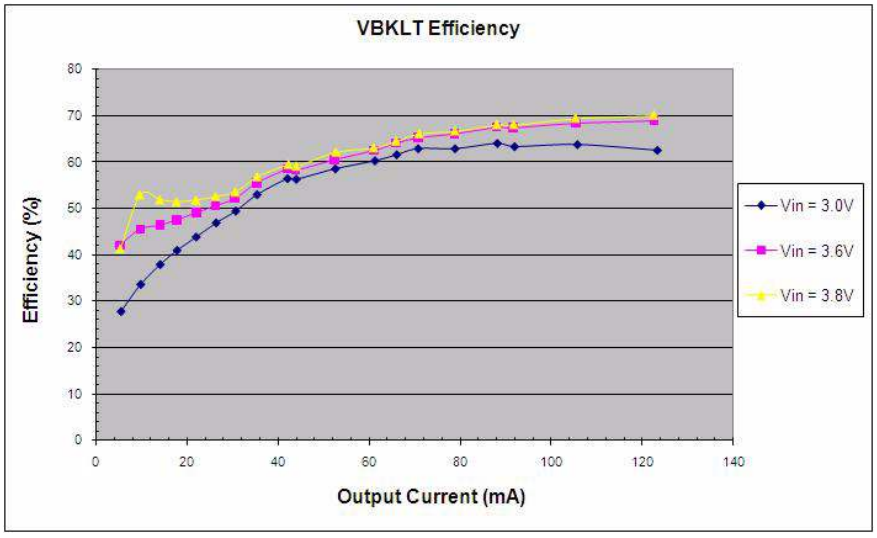

Figure 41. VBKLT Efficiency Curves

VBKLT Status/Control Registers and Bits Description

LED Drivers registers will be detailed in Lighting System.
There are no dedicated registers for VBKLT.

LDO POWER SUPPLIES

Freescale's power management solution for the Ultra-mobile platform for MID includes 17 LDO regulators, all of which are housed in the 900841 PMIC.

LDO OPERATION MODES SELECTIONS

- OFF - The regulator is switched off
- Active
  - The regulator is switched on and the output is at the programmed level
  - Maximum load current allowed
- Low Power
  - The regulator is switched on and the output is at the programmed level
  - load current is limited
- TEST/TRIM
  - This is not a functional mode, thus requiring certain steps to prevent unintentional activation of this mode
  - During this mode, the device performs measurements and trimming

All LDOS are able to work in a low power mode, in which the bias current is reduced. The output drive capability and performance are limited in this mode. This mode occurs automatically when the load current decreases below the low power mode limit, except on VBG and VMM, in which this mode can only be set through SPI programming. All other LDOS can set the low power mode through SPI programming.

Note: If low power mode is set through the SPI at a load current higher than the maximum allowed, the performance of the LDO is not guaranteed.

Table 44 is a summary of LDO characteristics

Table 44. SC900841 LDO Power Supplies Summary

Regulator	Typ. Voltage	Max Continuous Current	Description
VBG	1.25 V	2.0 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCCA	1.5 V	150 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCC180	1.8 V	390 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VPNL18	1.8 V	225 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VPMIC	1.8 V	50 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VYMXYFI18	1.8 V	200 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VYMXYFI	1.2 V	60 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VYMXGPS	1.3 V	350 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VYMXYFI	2.5 V	150 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VYMXGPS	1.8 V	170 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCCPAOAC	1.05 V	155 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCCPDDR	1.05 V	60 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VAON	1.2 V	250 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VMM	1.2 V	5.0 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.

Table 44. SC900841 LDO Power Supplies Summary

Regulator	Typ. Voltage	Max Continuous Current	Description
VCCP	1.05 V	445 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VIMG25	2.5 V	80 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VIMG28	1.5 - 2.9 V	225 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VVIB	1.3 - 2.7 V	200 mA	Low Drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response. It is used to drive the vibrator motor for alert functions
VSDIO	1.8 or 3.3 V	215 mA	VSDIO is a combo Low Drop-out (LDO) and power switch. It uses an external P-CH Pass FET. VSDIO serves as an LDO when its output voltage is set to 1.8 V, and as a switch when its output voltage is set to 3.3 V.

VBG

VBG is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VBG is actively discharged during shutdown.

VBG shares an input voltage pin (PVIN1P8) and a reference ground pin (GND1P8) with the VCCA regulator, yet each has independent control. PVIN1P8 is supplied from the VDDQ voltage.

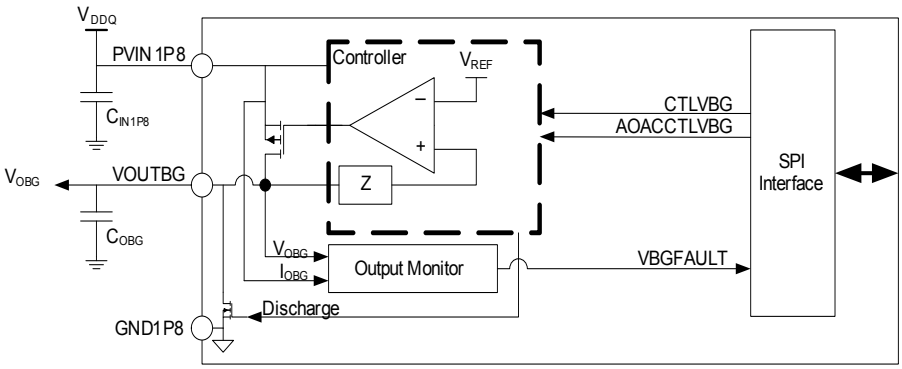

Figure 42. VBG Detailed Internal Block Diagram

Main Features

- Uses VDDQ as the main power supply
- 2.0 mA maximum continuous output current
- Optimized for a 1.0 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VBG Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 45. VBG Control Register Structure and Bits Description

Name	Bits	Description	
VLBGCNT (ADDR 0x3F - R/W - Default Value: 0x24)			
CTLVBG	2:0	VBG State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVBG	5:3	VBG State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCCA

VCCA is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCA is actively discharged during shutdown.

VCCA shares an input voltage pin (PVIN1P8) and a reference ground pin (GND1P8) with VBG regulator, yet each has independent control. PVIN1P8 is supplied from the VDDQ voltage.

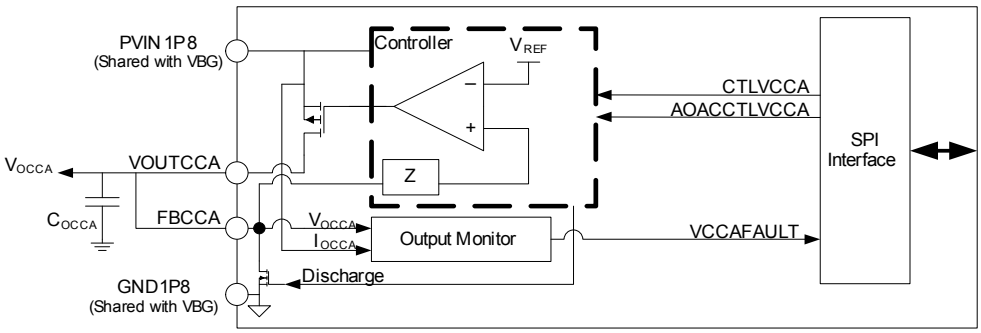

Figure 43. VCCA Detailed Internal Block Diagram

Main Features

- Uses VDDQ as the main power supply
- 150 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VCCA Status/Control Registers and Bits Description

Table 46. VCCA Control Register Structure and Bits Description

Name	Bits	Description	
VCCACNT (ADDR 0x40 - R/W - Default Value: 0x3C)			
CTLVCCA	2:0	VCCA State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active

Table 46. VCCA Control Register Structure and Bits Description

AOACCTLVCCA	5:3	VCCA State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCC180

VCC180 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCC180 is actively discharged during shutdown.

VCC180 shares an input voltage pin (PVIN2P1) and a reference ground pin (GND2P1) with VPNL18 and VPMIC regulators, yet each has independent control. PVIN2P1 is supplied from the V21 voltage.

The output current for VCC180 is measured and reported through the ADC. Reference ADC Subsystem for more information.

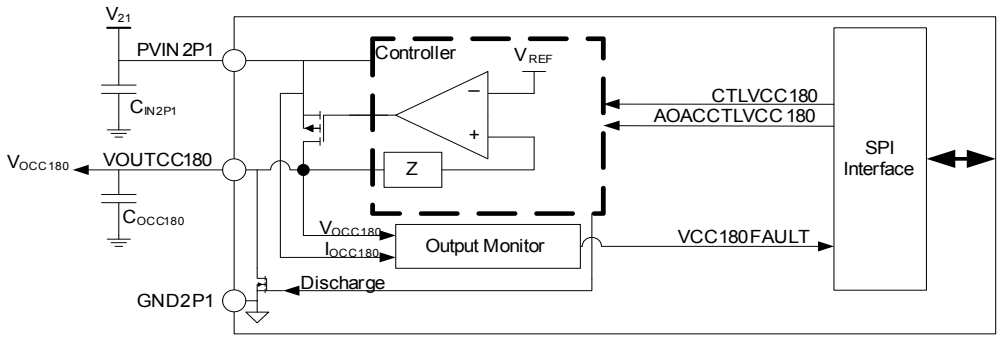

Figure 44. VCC180 Detailed Internal Block Diagram

Main Features

- Uses V21 as the main power supply
- 390mA maximum continuous output current
- Optimized for a 2.2µF external filter capacitor with a maximum of 10mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VCC180 Status/Control Registers and Bits Description

Table 47. VCC180CNT Register Structure and Bits Description

Name	Bits	Description	
VCC180CNT (ADDR 0x43 - R/W - 0x3C)			
CTLVCC180	2:0	VCC180 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active

Table 47. VCC180CNT Register Structure and Bits Description

AOACCTLVCC180	5:3	VCC180 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VPNL18

VPNL18 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VPNL18 is actively discharged during shutdown.

VPNL18 shares an input voltage pin (PVIN2P1) and a reference ground pin (GND2P1) with VCC180 and VPMIC regulators, yet each has independent control. PVIN2P1 is supplied from the V21 voltage.

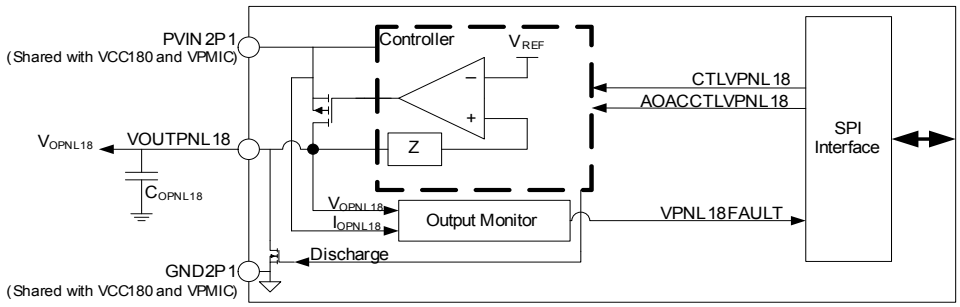

Figure 45. VPNL18 Detailed Internal Block Diagram

Main Features

- Uses V21 as the main power supply
- 225 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VPNL18 Status/Control Registers and Bits Description

Table 48. VPNL18 Control Register Structure and Bits Description

Name	Bits	Description	
VPANEL18CNT (ADDR 0x46 - R/W - Default value: 0x24)			
CTLVPANEL18	2:0	VPNL18 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVPANEL18	5:3	VPNL18 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VPMIC

VPMIC is a low drop-out (LDO) fully integrated regulator with a P-CH pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VPMIC is actively discharged during shutdown.

VPMIC shares an input voltage pin (PVIN2P1) and a reference ground pin (GND2P1) with VCC180 and VPNL18 regulators, yet each has independent control. PVIN2P1 is supplied from the V21 voltage.

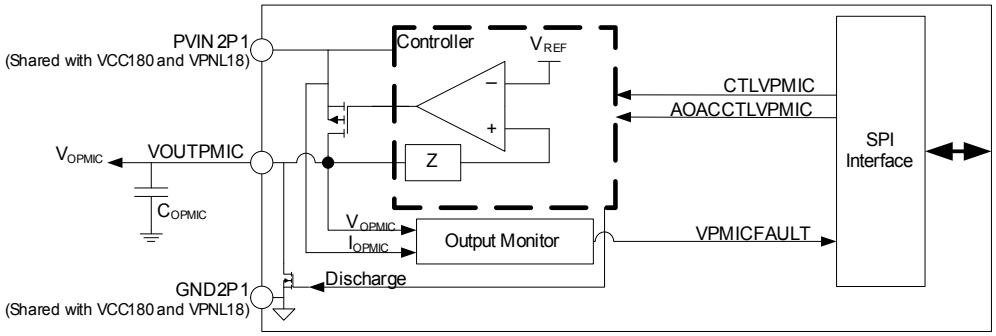

Figure 46. VPMIC Detailed Internal Block Diagram

Main Features

- Uses V21 as the main power supply
- 100 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VPMIC Status/Control Registers and Bits Description

Table 49. VPMIC Register Structure and Bits Description

Name	Bits	Description	
VPMICCNT (ADDR 0x41 - R/W - Default Value: 0x07)			
CTLVPMIC	2:0	VPMIC State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVPMIC	5:3	VPMIC State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VYMXYFI18

VYMXYFI18 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VYMXYFI18 is actively discharged during shutdown.

VYMXYFI18 supplies a 1.8 V output voltage to the communications modules in the system for WiMAX and WiFiBT applications

VYMXYFI18 can be supplied by either the V21 output voltage (V21) or directly from the VPWR node. Using V21 as the input voltage supply offers enhanced thermal performance and higher efficiency. Using the VPWR node can offer enhanced performance against noise coupling from an output of a DC/DC regulator. Users are encouraged to take the resulting thermal dissipation in account when supplying VYMXYFI18 directly from VPWR. For more information about package thermal capabilities, reference Thermal Management.

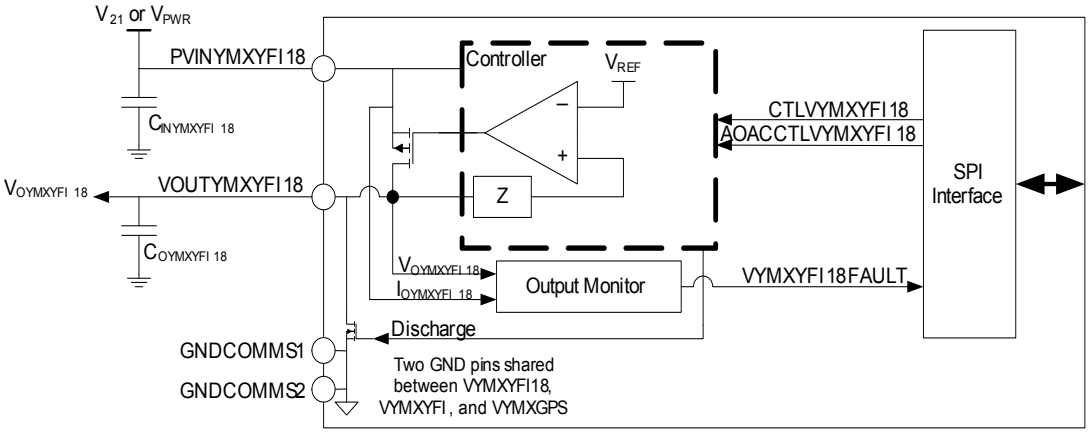

Figure 47. VYMXYFI18 Detailed Internal Block Diagram

Main Features

- Uses V21 or VPWR as the main power supply
- 200 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VYMXYFI18 Status/Control Registers and Bits Description

Table 50. VYMXYFI18 Register Structure and Bits Description

Name	Bits	Description	
VWYMXARFCNT (ADDR 0x4C - R/W - Default Value: 0x24)			
CTLVWYMXARF	2:0	VYMXYFI18 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVWYMXARF	5:3	VYMXYFI18 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VYMXYFI

VYMXYFI is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VYMXYFI is actively discharged during shutdown.

VYMXYFI supplies two different voltages, depending on the communications module used, 1.2 V for WiFiBT applications, and 2.5 V for WiMAX applications.

If set at 1.2 V, VYMXYFI is supplied by the V15 DC/DC regulator. When set at 2.5 V, VYMXYFI can be supplied by either the V33 DC/DC output voltage (V33), or directly from the VPWR node. Using V33 as the input voltage supply offers enhanced thermal performance and higher efficiency. Using the VPWR node can offer enhanced performance against noise coupling from an output of a DC/DC regulator. Users are encouraged to take the resulting thermal dissipation in account when supplying VYMXYFI directly from VPWR. For more information about package thermal capabilities, reference Thermal Management.

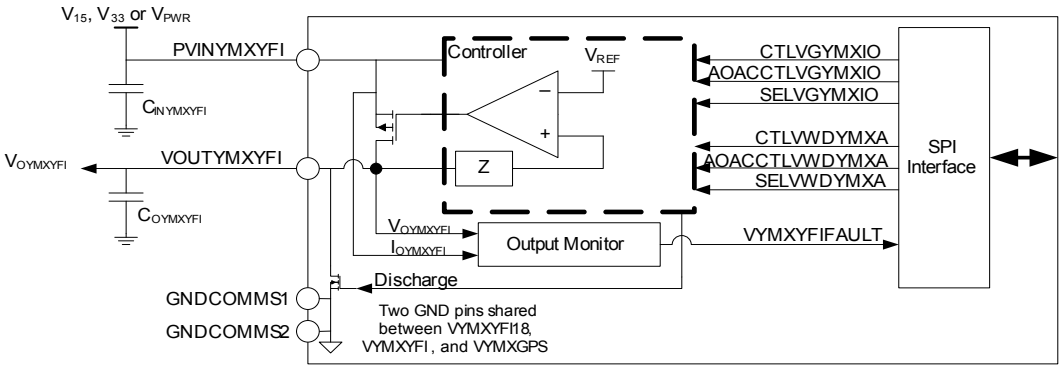

Figure 48. VYMXYFI Detailed Internal Block Diagram

Main Features

- Uses V15, V33, or VPWR as the main power supply
- 60 mA maximum continuous output current for the 1.2 V setting
- 150 mA maximum continuous output current for the 2.5 V setting
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events
- The Status and Control registers of VYMXFYI will be discussed along with status/control registers for the VYMXGPS LDO in the following section VYMXGPS

VYMXGPS

VYMXGPS is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VYMXGPS is actively discharged during shutdown.

VYMXGPS supplies two different voltages, depending on the communications module used, 1.8 V for GPS applications, and 1.3 V for WiMAX applications.

If set at 1.8 V, VYMXGPS can be supplied by either V21 DC/DC output voltage (V21), or directly from the VPWR node. When set at 1.3 V, VYMXGPS is supplied from the V15 DC/DC output voltage (V15). Using V21 as the input voltage supply offers enhanced thermal performance and higher efficiency. Using the VPWR node can offer enhanced performance against noise coupling from an output of a DC/DC regulator. Users are encouraged to take the resulting thermal dissipation in account when supplying VYMXGPS directly from VPWR. For more information about package thermal capabilities, reference Thermal Management.

Note that when VYMXGPS is set at 1.3 V, V15 is automatically set at 1.6 V, to maintain voltage headroom for the operation of 1.3V VYMXGPS. Reference V15 for more details.

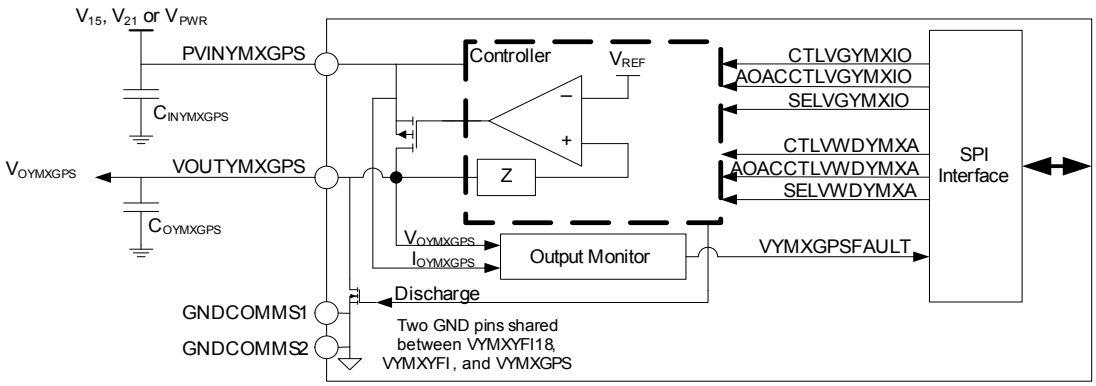

Figure 49. VYMXGPS Detailed Internal Block Diagram

Main Features

- Uses V15, V21, or VPWR as the main power supply
- 170 mA maximum continuous output current for the 1.8 V setting
- 350 mA maximum continuous output current for the 1.3 V setting
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VYMXYFI/VYMXGPS Status/Control Registers and Bits Description

In order to minimize conductive loses in the Advance communication voltage rails, the Freescale Chipset uses the VYMXYFI and VYMXGP rails to supply VWDYMXA and VGYMXIO on the Ultra-mobile platform. Figure 50 shows the voltage mapping for these signals.

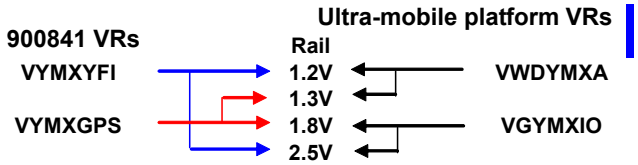

Figure 50. Freescale vs. Customer LDO Mapping for Communication Modules

When the software programs a certain voltage rail, Freescale will turn on that voltage rail using the right LDO, see Table 51.

Table 51. VYMXYFI and VYMXGPS Control Register Structure and Bits Description

Name	Bits	Description	
VGYMXIOCNT (ADDR 0x4A - R/W - Default Value: 0x24)			
CTLVGYMXIO	2:0	VGYMXIO State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVGYMXIO	5:3	VGYMXIO State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
SELVGYMXIO	7:6	VGYMXIO output voltage selection bits	
		X0 = 1.8 V x1 = 2.5 V	x2 = Reserved x3 = Reserved

Table 51. VYMXYFI and VYMXGPS Control Register Structure and Bits Description

VWDYMXACNT (ADDR 0x4B - R/W - Default Value: 0x24)			
CTLVWDYMXA	2:0	VWDYMXA State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVWDYMXA	5:3	VWDYMXA State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
SELVWDYMXA	7:6	VWDYMXA output voltage selection bits	
		X0 = 1.2 V x1 = 1.3 V	x2 = Reserved x3 = Reserved

Freescale's control of these 4 application voltage rails depend on the SEL bits setting of VGYMXIO and VDWYMXA:

- When SELVGYMXIO is set to 1.8 V:
  - The VGYMXIO register is now controlling VYMXGPS.
  - VYMXGPS is set at 1.8 V
- When SELVGYMXIO is set to 2.5 V:
  - The VGYMXIO register is now controlling VYMXYFI.
  - VYMXYFI is set at 2.5 V
- When SELVDWYMXA is set to 1.2 V:
  - The VDWYMXA register is now controlling VYMXYFI.
  - VYMXYFI is set at 1.2 V
- When SELVDWYMXA is set to 1.3 V:
  - The VDWYMXA register is now controlling VYMXGPS.
  - VYMXGPS is set at 1.3 V

It is the responsibility of the user (firmware) to guarantee that no conflict will occur. For example, it is not permissible to set VGYMXIO for a 1.8 V output, and also to set VDWYMXA for a 1.3 V output.

VCCPAOAC

VCCPAOAC is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCPAOAC is actively discharged during shutdown.

VCCPAOAC shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with VCCPDDR, VAON, VMM, and the VCCP regulator. Each has independent control. PVIN1P5 is supplied from the V15 voltage.

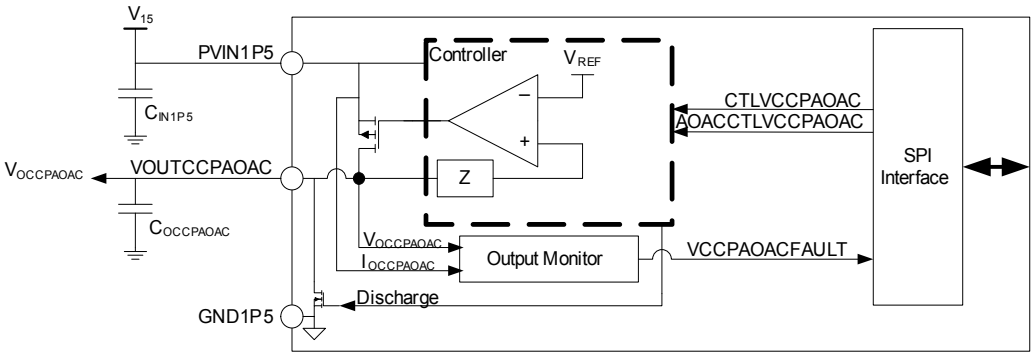

Figure 51. VCCPAOAC Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply.
- 155 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VCCPAOAC Status/Control Registers and Bits Description

Table 52. VCCPAOACCNT Register Structure and Bits Description

Name	Bits	Description	
VCCPAOACCNT (ADDR 0x3D - R/W - Default Value: 0x07)			
CTLVCCPAOAC	2:0	VCCPAOAC State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVCCPAOAC	5:3	VCCPAOAC State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCCPDDR

VCCPDDR is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCPDDR is actively discharged during shutdown.

VCCPDDR shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VAON, VMM, and VCCP regulators, yet each has independent control. PVIN1P5 is supplied from the V15 voltage.

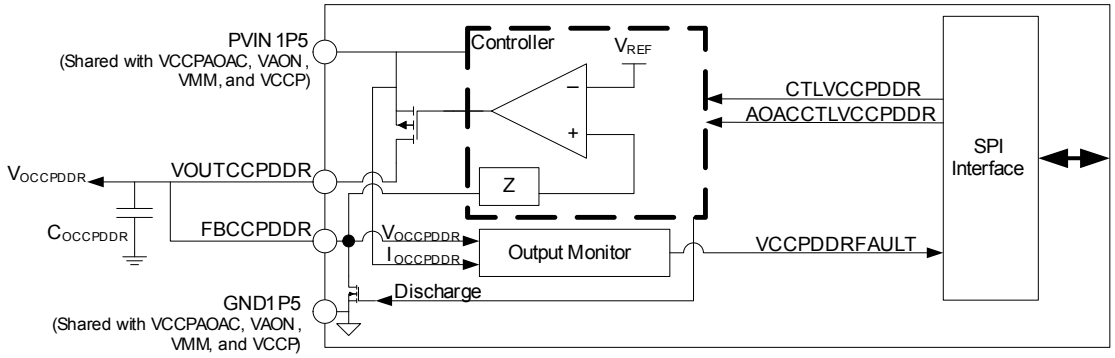

Figure 52. VCCPDDR Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 60 mA maximum continuous output current
- Optimized for a 1.0 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VCCPDDR Status/Control Registers and Bits Description

Table 53. VCCPDDR Control Register Structure and Bits Description

Name	Bits	Description	
VCCPDDRCNT (ADDR 0x3E - R/W - Default value: 0x3C)			
CTLVCCPDDR	2:0	VCCPDDR State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active

900841

Table 53. VCCPDDR Control Register Structure and Bits Description

AOACCTLVCCPDDR	5:3	VCCPDDR State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VAON

VAON is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VAON is actively discharged during shutdown.

VAON shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VCCPDDR, VMM, and VCCP regulators, yet each has independent control. PVIN1P5 is supplied from the V15 voltage.

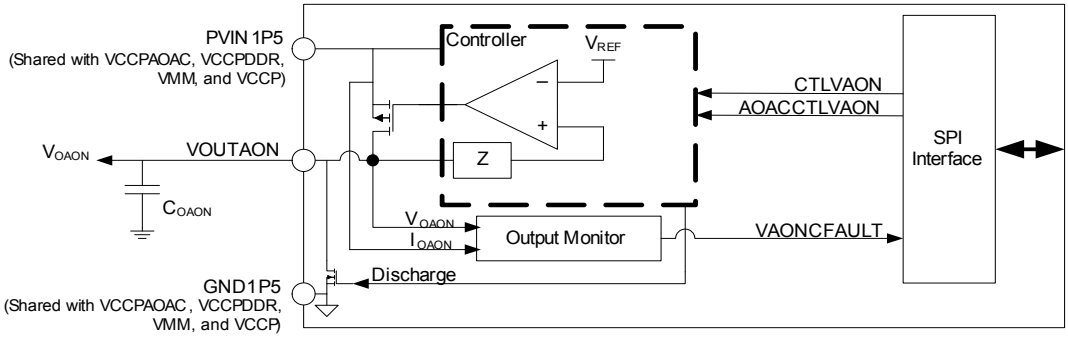

Figure 53. VAON Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 250 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VAON Status/Control Registers and Bits Description

Table 54. VAON Control Register Structure and Bits Description

Name	Bits	Description	
VAONCNT (ADDR 0x45 - R/W - Default Value: 0x07)			
CTLVAON	2:0	VAON State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVAON	5:3	VAON State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VMM

VMM is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VMM will be actively discharged during shutdown.

VMM shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VCCPDDR, VAON, and VCCP regulators, yet each has independent control. PVIN1P5 is supplied from V15 voltage.

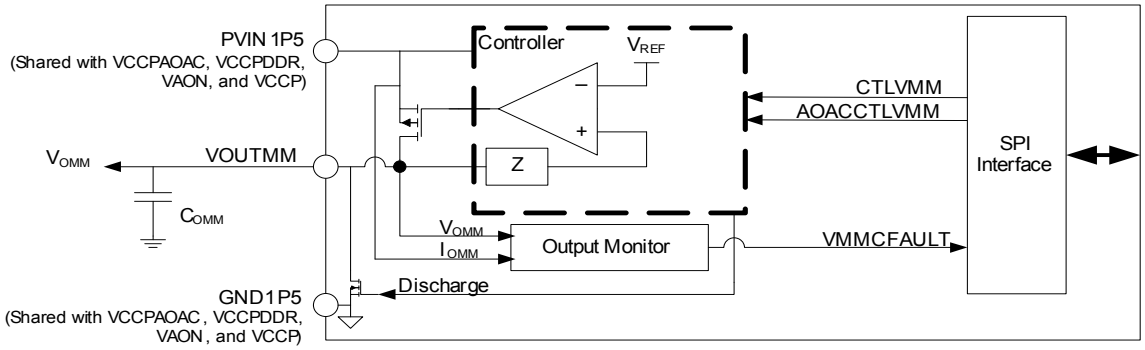

Figure 54. VMM Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 5.0 mA maximum continuous output current
- Optimized for a 1.0 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VMM Status/Control Registers and Bits Description

Table 55. VMM control Register Structure and Bits Description

Name	Bits	Description	
VMMCNT (ADDR 0x47 - R/W - Default Value: 0x24)			
CTLVMM	2:0	VMM State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVMM	5:3	VMM State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCCP

VCCP is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCP is actively discharged during shutdown.

VCCP shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VCCPDDR, VAON, and VMM regulators, yet each has independent control. PVIN1P5 is supplied from V15 voltage.

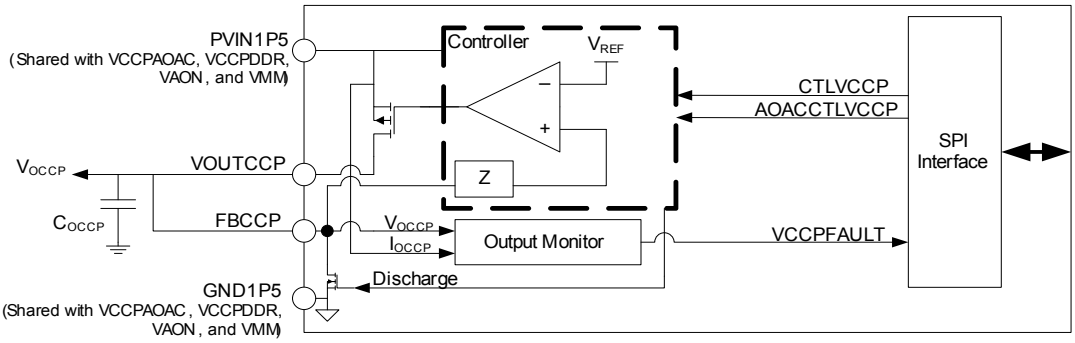

Figure 55. VCCP Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 445 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VCCP Status/Control Registers and Bits Description

Table 56. VCCP Control Register Structure and Bits Description

Name	Bits	Description	
VCCPCNT (ADDR 0x44 - R/W - Default Value: 0x3C)			
CTLVCCP	2:0	VCCP State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVCCP	5:3	VCCP State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VIMG25

VIMG25 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VIMG25 is actively discharged during shutdown.

VIMG25 shares an input voltage pin (PVINIMG) and a reference ground pin (GNDIMG) with the VIMG28 regulator, yet each has independent control. Both can be supplied by either the V33 output voltage (V33) or directly from the VPWR node, depending on the output voltage selection of LDO VIMG28.

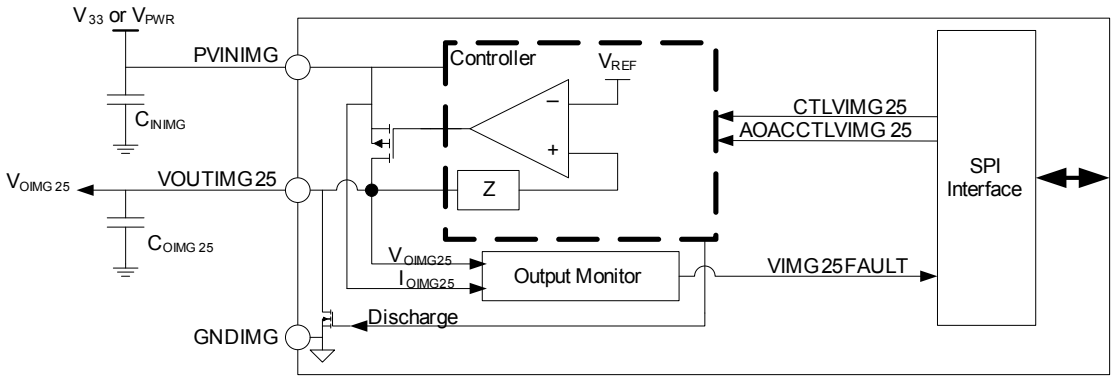

Figure 56. VIMG25 Detailed Internal Block Diagram

Main Features

- Uses V33 or VPWR as the main power supply
- 80 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VIMG25 Status/Control Registers and Bits Description

Table 57. VIMG25 Register Structure and Bits Description

Name	Bits	Description	
VIMG25CNT (ADDR 0x42 - R/W - Default Value: 0x04)			
CTLVIMG25	2:0	VIMG25 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVIMG25	5:3	VIMG25 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VIMG28

VIMG28 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VIMG28 is actively discharged during shutdown.

VIMG28 shares an input voltage pin (PVINIMG) and a reference ground pin (GNDIMG) with the VIMG25 regulator, yet each has independent control. Both can be supplied by either the V33 output voltage or directly from the V_{PWR} node, depending on its output voltage selections. It is recommended to supply VIMG28 from V33 at all times, regardless of the VIMG28 output voltage setting. This LDO is optimized to work with 300 mV headroom, which leaves enough margin between the input and the highest output of this LDO. If it is desired to supply these LDO directly from VPWR, two notes are worth mentioning:

- Users are encouraged to take the resulting thermal dissipation into account when supplying VIMG28 (and VIMG25) directly from VPWR. For more information about package thermal capabilities, reference Thermal Management.
- At high VIMG28 output voltage selections, the output will start tracking the battery voltage when V_{BAT} decreases below V_{OIMG28} + 300 mV.

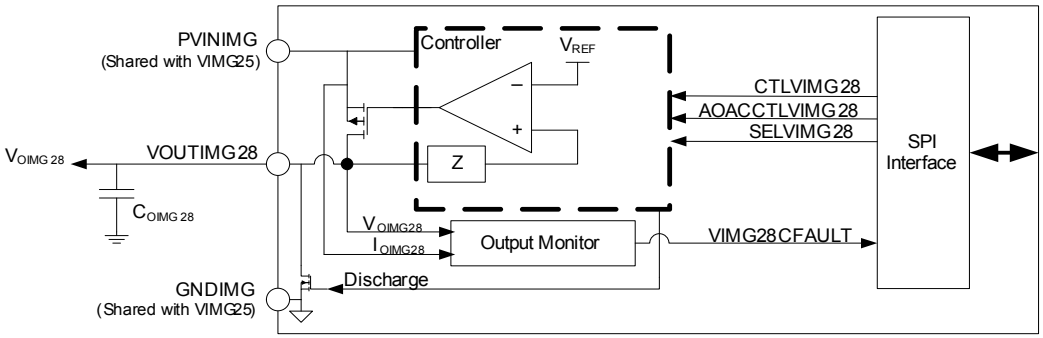

Figure 57. VIMG28 Detailed Internal Block Diagram

Main Features

- Uses V33 or VPWR as the main power supply
- 225 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VIMG28 Status/Control Registers and Bits Description

Table 58. VIMG28 Control Register Structure and Bits Description

Name	Bits	Description	
VIMGACNT (ADDR 0x0x48 - R/W - Default Value: 0x24)			
CTLVIMGA	2:0	VIMG28 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVIMGA	5:3	VIMG28 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
SELVIMGA	7:6	VIMG28 output voltage selections:	
		X0 = 1.5 V x1 = 2.7 V x2 = 2.8 V x3 = 2.9 V	

VVIB

VVIB is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VVIB is actively discharged during shutdown.

It is used to drive the vibrator motor for alert functions, and it takes its input voltage directly from the VPWR node.

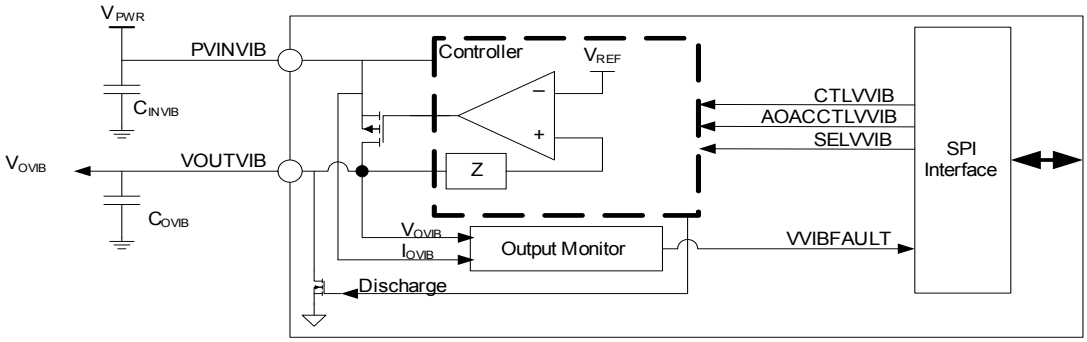

Figure 58. VVIB Detailed Internal Block Diagram

Main Features

- Uses VPWR as the main power supply
- 200 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output is monitored for over-current conditions and under-voltage events

VVIB Status/Control Registers and Bits Description

Table 59. VIB Control Register Structure and Bits Description

Name	Bits	Description	
VIBCNT (ADDR 0x49 - R/W - Default Value: 0x24)			
CTLVVIB	2:0	VVIB State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVVIB	5:3	VVIB State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
SELVVIB	7:6	VVIB output voltage selections:	
		X0 = 1.3 V x1 = 1.5 V x2 = 2.5 V x3 = 2.7 V	

VSDIO

VSDIO is a combo low drop-out (LDO) and power switch. It uses an external P-CH pass FET in Switch mode, and internal pass FET on LDO mode.

VSDIO serves as an LDO when its output voltage is set to 1.8 V, and as a switch when its output voltage is set to 3.3 V. It takes its input voltage directly from the V33 output voltage node (V33).

VSDIO supplies the SDIO card module. The card is initially powered up to 3.3 V. If the card is detected to be a low voltage card, then the rail will be shutdown, configured as 1.8 V, and then turned on.

VSDIO will be actively discharged during shutdown.

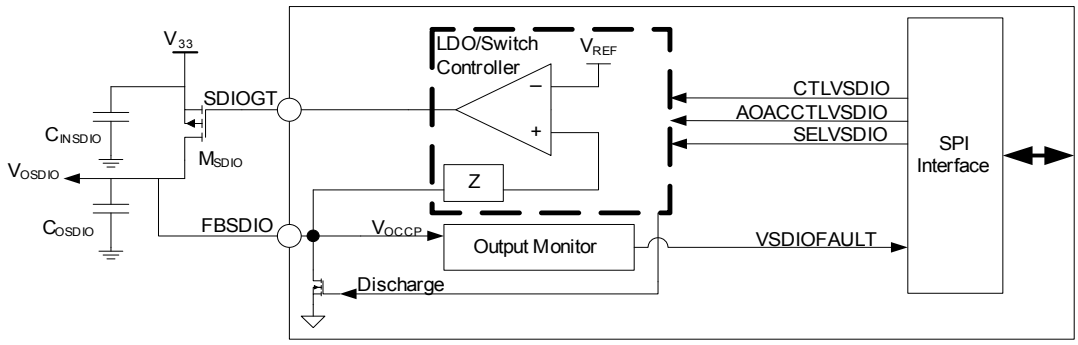

Figure 59. VSDIO Detailed Internal Block Diagram

MAIN FEATURES

- Uses V33 as the main power supply
- 215 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET on LDO mode, and external pass FET on Switch mode.
- The output is monitored for under-voltage and overcurrent conditions in LDO mode.

VSDIO Status/Control Registers and Bits Description

Table 60. VSDIO Control Register Structure and Bits Description

Name	Bits	Description	
VSDIOCNT (ADDR 0x4D - R/W - Default Value: 0x64)			
CTLVSDIO	2:0	VSDIO State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVSDIO	5:3	VSDIO State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
SELVSDIO	7:6	VSDIO output voltage selections:	
		X0 = 1.8 V x1 = 3.3 V x2 = Reserved x3 = Reserved	

POWER SWITCHES

Freescale's power management solution for the Ultra-mobile platform for MID includes 3 dedicated power switches, all of which are housed in the 900841 PMIC. Table 61 lists all Power switches and its power characteristics.

Table 61. SC900841 Power Switches summary

Switch	Typ. Voltage	Max Current	Description
VPNL33	3.3 V	100 mA	Power Switch with integrated MOSFET and less than 1% voltage drop.
VGP33	3.3 V	60 mA	Power Switch with integrated MOSFET and less than 1% voltage drop.
VYMXGPS33	3.3 V	60 mA	Power Switch with integrated MOSFET and less than 1% voltage drop.

All of the switches in Table 61 use an internal switch and are supplied from the V33 output voltage node.

Power Switches Status/Control Registers and Bits Description

Table 62. Power Switches Control Registers Structure and Bits Description

Name	Bits	Description	
VPANEL33CNT (ADDR 0x4F - R/W - Default Value: 0x24)			
CTLVPANEL33	2:0	VPNL33 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVPANEL33	5:3	VPNL33 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	
VGP33CNT (ADDR 0x50 - R/W - Default Value: 0x24)			
CTLVGP33	2:0	VGP33 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVGP33	5:3	VGP33 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	
GYMX33CNT (ADDR 0x4E - R/W - Default Value: 0x24)			
CTLVGYMX33	2:0	VYMXGPS33 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active

Table 62. Power Switches Control Registers Structure and Bits Description

AOACCTLVGYMX33	5:3	VYMXGPS33 State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

STAND ALONE VOLTAGE SUPPLIES.

V33

This is a 1.625 MHz fully integrated 4-switch synchronous Buck-boost PWM voltage mode control DC/DC regulator.

This rail is implemented through an external standalone chip. See General Description.

A separate specification is provided for this rail in the 900842 datasheet.

Reference Freescale Chip set Communication Signals for more details about how the 900841 communicates to this standalone chip for complete system operation.

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used as a pre-regulator to many LDO and Switch rails for enhanced efficiency and reduced thermal dissipation. It also supplies power to rails in Platform controller hub and the platform
- Uses Integrated MOSFETs
- 1.625 MHz switching frequency
- Output can be discharged
- Output Current Sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

V33 Status/Control Registers and Bits Description

Table 63. V33 Control Register Structure and Bits Description

Name	Bits	Description	
V33CNT (ADDR 0x3A - R/W - Default Value: 0x24)			
CTLV33	2:0	V33 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low power x6 = PWM x7 = PWM
AOACCTLV33	5:3	V33 State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low power x6 = PWM x7 = PWM
Reserved	7:6	Reserved	

POWER SUPPLY REGISTER MASK

Mask writes to the power supply registers, in order to avoid the need for the system controller to do read-modify-write cycles. The mask register is shown in Table 64.

Table 64. Mask Register

Register name	ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	initial
PWRMASK	0x34	R/W	M7	M6	M5	M4	M3	M2	M1	M0	0x00

Figure 60 shows an example of the operation of the PWRMASK register.

	D7	D6	D5	D4	D3	D2	D1	D0
Power Supply Register Before Write	1	0	1	0	1	0	1	0
PWRMASK Register Settings	1	1	1	1	0	0	0	0
Example SPI Write to Power Supply	1	1	1	1	1	1	1	1
Power Supply Register After Write	1	0	1	0	1	1	1	1

Figure 60. PWRMASK Register Implementation Example

POWER SUPPLY PROGRAMMABLE RAMP RATE

Turn on time of all buck regulators can be programmed through the SPI, reference Table 65

Table 65. Ramp Rate Control Registers (Freescale Defined)

Name	Bits	Description
FSLTONTCNTL1 (ADDR 0x1C8 - R/W - Default Value: 0xAA)		
VCCTONT	1:0	Turn On Time Settings for VCC Regulator x0 = 180 µs x1 = 90 µs x2 = 45 µs x3 = 22 µs
VNNTONT	3:2	Turn On Time Settings for VNN Regulator x0 = 180 µs x1 = 90 µs x2 = 45 µs x3 = 22 µs
VDDQTONT	5:4	Turn On Time Settings for VDDQ Regulator x0 = 240 µs x1 = 120 µs x2 = 60 µs x3 = 30 µs
VYMX3GTONT	7:6	Turn On Time Settings for VYMX3G Regulator x0 = 160 µs x1 = 80 µs x2 = 40 µs x3 = 20 µs
FSLTONTCNTL2 (ADDR 0x1CB - R/W - Default Value: 0xAA)		
V21TONT	1:0	Turn On Time Settings for V21 Regulator x0 = 320 µs x1 = 160 µs x2 = 80 µs x3 = 40 µs
V15TONT	3:2	Turn On Time Settings for V15 Regulator x0 = 200 µs x1 = 100 µs x2 = 50 µs x3 = 25 µs
Reserved	7:4	Reserved

POWER SUPPLIES FAULT MANAGEMENT

The following section discusses faults related to, or caused by power supplies (directly or indirectly) operating outside their specified boundaries.

Reference Interrupt Controller for more information on the various interrupt signals, and the interrupt mechanism used to communicate to the system controller.

THERMAL MANAGEMENT

The thermal protection is based on a circuit with a voltage output that is proportional to the absolute temperature. This voltage can be read out via the ADC for precise temperature readouts. See ADC Subsystem.

This voltage is monitored by an integrated comparator. Interrupt THRM will be generated, if not masked, when crossing the thermal warning threshold TWARN, and sets the VRFAULT 1st level interrupt that causes the PMICINT pin to assert, notifying the system controller of a system event.

In addition to the previous, the 900841 includes integrated thermal protection that shuts down and powers off the system, in cases of over dissipation, if the junction temperature exceeds the TSHUTDOWN threshold. This thermal protection will act above the maximum junction temperature, to avoid any unwanted power downs. The protection is de-bounced by one period of the 32 kHz clock in order to suppress any (thermal) noise. This protection should be considered as a fail-safe mechanism. Therefore, the application design should execute a thermal shutdown under normal conditions.

Once the thermal event is cleared and the temperature is back to its normal range, the SC900841 restarts automatically, by following the steps outlined in Initial Power Up Sequence

Table 66. Thermal Warning/Shutdown Thresholds

Parameter	Min	Typ	Max	Unit
Thermal Warning Threshold	115	120	125	°C
Thermal Warning Hysteresis	2	-	4	°C
Thermal Shutdown Threshold	130	140	150	°C

BATOCP

When the battery is being discharged, the current out of the battery is monitored. BATOCSET sets the maximum battery discharge current value. If the battery discharge current is greater than the value set by BATOCSET for more than a time set by BATOCPT, the BATOCP interrupt is set to interrupt the system. If the over-discharge current condition continues for another BATOCPT period, the 900841 initiates a system shutdown similar to the thermal shutdown event.

The BATOCP comparator can be shutdown when the battery is not being discharged.

Table 67. BATOCP Control Register Structure and Bits Description

Name	Bits	Description
CHRGPROT2 (ADDR 0xD8 - R/W - Default Value: 0x60)		
BATOCPSET	1:0	Battery Discharge Current Limit x0 = 2.0 A x1 = 3.0 A x2 = 4.0 A x3 = 5.0 A
Reserved	4:2	Reserved
TOCP	7:5	Battery Discharge Current Limit Filter Timer x0 = 1.0 ms x1 = 5.0 ms x2 = 10 ms x3 = 15 ms x4 = 20 ms x5 = 40 ms x6 = 80 ms x7 = 160 ms

VRFAULT

Every supply is equipped with a fault reporting signal called xxxFAULT, where xxx is the name of the power supply. This FAULT signal is an OR function of all of the following possible faults, or just a subset of them depending on the power supply:

- Output under-voltage
- Output over-voltage
- Over-current
- Short-circuit

Reference each power supply's section for more information on what faults are included, and how the supply protects itself and the load in response to the fault.

All of the xxxFAULT signals from all power supplies are ORed together into the BATOCP interrupt signal, which in turn if unmasked, sets the VRFAULT 1st level interrupt that causes the PMICINT pin to assert, notifying the SC of a system event. The SC can service the VRFAULT register and access the FAULTx registers for more information on which supply caused the fault. The SC can then take different measures, depending on the supply in question.

The xxxFAULT signals are stored in the Freescale defined registers section (Addr 0x180 - 0x1FF), which is meant for extended functionality.

Table 68. Fault Status Registers Structure and Bits Description

Name	Bits	Description
FSLFAULT1 (ADDR 0x1CC - R/W - Default Value: 0x00)		
VCCFAULT	0	VCC Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VNNFAULT	1	VNN Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VDDQFAULT	2	VDDQ Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
V21FAULT	3	V21 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
V15FAULT	4	V15 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
V33FAULT	5	V33 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VYMX3GFAULT	6	VYMX3G Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
V3GPAFAULT	7	Reserved
FSLFAULT2 (ADDR 0x1CD - R/W - Default Value: 0x00)		
VYMXPAFAULT	0	VYMXPA Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VOTGFAULT	1	VOTG Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VBKLTFAULT	2	VBKLT Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists

Table 68. Fault Status Registers Structure and Bits Description

VBGFAULT	3	VBG Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCCAFAULT	4	VCCA Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCC180FAULT	5	VCC180 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VPNL18FAULT	6	VPNL18 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VPMICFAULT	7	VPMIC Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
FSLFAULT3 (ADDR 0x1CE - R/W - Default Value: 0x00)		
VYMXYFI18FAULT	0	VYMXYFI18 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VYMXYFIFAULT	1	VYMXYFI Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VYMXGPSFAULT	2	VYMXGPS Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCCPAOACFAULT	3	VCCPAOAC Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCCPDDRFAULT	4	VCCPDDR Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VAONFAULT	5	VAON Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VMMFAULT	6	VMM Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCCPFAULT	7	VCCP Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
FSLFAULT4 (ADDR 0x1CF - R/W - Default Value: 0x00)		
VIMG25FAULT	0	VIMG25 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists

Table 68. Fault Status Registers Structure and Bits Description

VIMG28FAULT	1	VIMG28 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VVIBFAULT	2	VVIB Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VSDIOFAULT	3	VSDIO Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
Reserved	7:4	Reserved

Power Supplies Fault Management Interrupt/Mask Registers.

Table 69. Fault Management Status and Control Register Structure and Bits Description

Name	Bits	Description
VRFAULTINT (ADDR 0X30 - R - Default Value: 0x00)		
THRM	0	PMIC Thermal Warning Flag x0 = PMIC temperature below warning threshold x1 = PMIC temperature above warning threshold
BATOCP	1	Regulator fault present flag or battery discharge over current x0 = No fault x1 = Fault Exists
VRFAIL	2	Regulator fault present flag or battery discharge over current x0 = No fault x1 = Fault Exists
Reserved	7:3	Reserved
MVRFAULTINT (ADDR 0x31 - R/W - Default Value: 0x03)		
MTHRM	0	PMIC Thermal Warning Flag Mask x0 = Flag unmasked x1 = Flag masked
MBATOCP	1	Regulator fault present flag or battery discharge over current Mask x0 = Flag unmasked x1 = Flag masked
VRFAIL	2	Regulator fault present flag or battery discharge over current Mask x0 = Flag unmasked x1 = Flag masked
Reserved	7:3	Reserved

LIGHTING SYSTEM

The lighting system of the 900841 is comprised of LCD Backlight LED drivers, a Camera Scene Illumination LED driver, and general purpose LED drivers.

LCD BACKLIGHT DRIVERS

900841 supports up to four parallel strings with up to 5-6 LEDs each for LCD backlighting. The strings are powered from the VBKLT DC/DC boost regulator. The brightness control is done through 8-bit PWM duty cycle control and 3-bit PWM frequency control.

Note: The minimum on time of the backlight LEDs should be limited to 2.0 ms

The backlight control resolution is needed to support DPST power savings architecture. The duty cycle change from the previous value will be typically <1%. Dynamic display duty cycle changes are made as frequently as every 100 ms, or 6 frames. The new duty cycle takes effect at the start of the next PWM cycle change. Refer to Figure 40 for a block diagram of how the backlight LED current sinks interface with VBKLT.

Each one of the Backlight current sinks could be used with a pull-up resistor as a PWM output signal to drive an "Integrated Display".

Table 70. LCD Backlight Drivers Brightness Control PWM Duty Cycle Selections

REG M								M# of N*256 clocks	Duty cycle
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
0	0	0	0	0	0	0	0	1	0.39%
0	0	0	0	0	0	0	1	2	0.78%
0	0	0	0	0	0	1	0	3	1.17%
0	0	0	0	0	0	1	1	4	1.56%
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	1	256	100.00%

Table 71. LCD Backlight Drivers Brightness Control PWM Frequency Selections

Reg N							
Bit2	Bit1	Bit0	32.768 kHz divided by	PWM Freq [reg N] (Hz)	Period (s)	Min on time (s) Duty cycle [reg M=0]	Min on time (µs)
0	0	0	256	128	0.007813	3.06 e-05	30.64
0	0	1	128	256	0.003906	1.53 e-05	15.32
0	1	0	64	512	0.001953	7.66 e-06	7.66
0	1	1	32	1024	0.000977	3.83 e-06	3.83
1	0	0	16	2048	0.000488	1.91 e-06	1.91
1	0	1	8	4096	0.000244	9.57 e-07	0.96
1	1	0	4	8192	0.000122	4.79 e-07	0.48
1	1	1	RSVD				

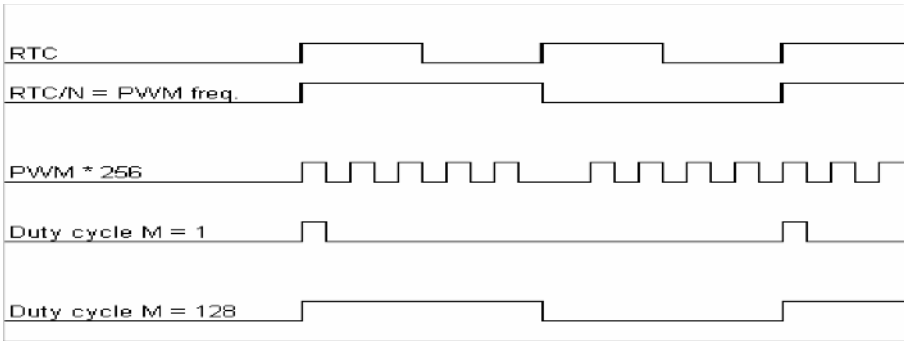

Figure 61. PWM and Duty Cycle Functionality for Backlight Current Sinks

LCD Backlight Status/Control Registers and Bits Description

Table 72. Backlight Control Registers Structure and Bits Description

Name	Bits	Description
BKLTCNT (ADDR 0x28 - R/W - Default Value: 0x00)		
BKLTSS	1:0	No Supported, Reserved
Reserved	4:2	Reserved
MBKLT1EN	5	LCD Backlight String 1 Enable Bit to operate with VBKLT x0 = Disable x1 = Enable
MBKLT2EN	6	LCD Backlight String 2 Enable Bit to operate with VBKLT x0 = Disable x1 = Enable
MBKLT3EN	7	LCD Backlight String 3 Enable Bit to operate with VBKLT x0 = Disable x1 = Enable
BKLTFREQ (ADDR 0x29 - R/W - Default Value: 0x00)		
BKLTFREQ	2:0	LCD Backlight PWM Frequency Settings For Strings 1-3 in single backlight configuration or for Strings 1-2 for independent zone backlighting configuration. See Table 71 for Frequency settings
Reserved	5:3	Reserved
PWMEN	6	LCD Backlight Drivers Enable Bit as PWM outputs, not operating with VBKLT x0 = Disable x1 = Enable
Reserved	7	Reserved
BKLTBRTL (ADDR 0x2A - R/W - Default Value: 0x00)		
BKLTBRTL	7:0	LCD Backlight PWM Duty Cycle Settings For Strings 1-3 in single backlight configuration or for Strings 1-2 for independent zone backlighting configuration. See Table 70 for Duty Cycle Settings

LCD Backlight Status/Control Registers and Bits Description

Table 73. Extended Backlight Control Registers Structure and Bits Description

Name	Bits	Description	
FSLVBKLTCNTL (ADDR 0x1D3 - R/W - Default Value: 0x07)			
BKLTLED	2:0	LCD Backlight LED Maximum Current Settings	
		x0 = 0 mA x1 = 4.3 mA x2 = 8.6 mA x3 = 12.9 mA	x4 = 17.2 mA x5 = 21.5 mA x6 = 25.8 mA x7 = 30 mA
MLED4EN	3	Enable camera scene string to be used as LCD Backlight String 4 x0 = 4th string cannot be used for backlight applications (Default) x1 = 4th string can be used for backlight applications	
BKLTFREQ2	6:4	LCD Backlight PWM Frequency settings for string 4 in single backlight configuration or for strings 3-4 for independent zone backlighting configuration. See Table 71 for Frequency settings	

Table 73. Extended Backlight Control Registers Structure and Bits Description

TWOPTWO	7	Independent Zone (Backlight) Configuration Enable x0 = Independent Zone Backlighting Option is disabled (Default) x1 = Independent Zone Backlighting Option is Enabled	
FSL4STRING (ADDR 0x1D4 - R/W - Default Value: 0x00)			
BKLTBRTL2	7:0	LCD Backlight PWM Duty Cycle Settings for string 4 in single backlight configuration or for Strings 3-4 for independent zone backlight configuration. See Table 70 for Duty Cycle Settings	
FSLVBKLTADAPT (ADDR 0x1D5 - R/W - Default Value: 0x00)			
S4ADAPT	0	Enable String 4 to be part of the adaptive boost control x0 = Disable (Default) x1 = Enable	
Reserved	7:1	Reserved	

CAMERA SCENE ILLUMINATION CURRENT DRIVER

The 900841 supports one string of up to 5-6 LEDs for Camera Scene Illumination. The string is powered from the VBKLT boost regulator. The brightness control is done through a 3-bit PWM duty cycle control with fixed PWM frequency.

This string can also be used as an additional string for backlight support, see VBKLT, in which case it is controlled like the other LCD backlight strings, see LCD Backlight Drivers.

Camera Scene Illumination Drivers Status/Control Registers and Bits Description

Table 74. Camera String Illumination Control Register Structure and Bits Description

Name	Bits	Description	
SSTRING (ADDR 0x2B - R/W - Default Value: 0x00)			
SLEDEN	0	Camera Scene Illumination Drivers Enable Bit	
		x0 = Disable x1 = Enable	
SILTBRT	3:1	Camera Scene Illumination PWM Duty Cycle Settings	
		x0 = 12.5% x1 = 25% x2 = 37.5% x3 = 50%	x4 = 62.5% x5 = 75% x6 = 87.5% x7 = 100%
Reserved	7:4	Reserved	

SIGNALING/STATUS LED DRIVERS

The 900841 contains signaling/status LED drivers in the form of two banks of RGB LED drivers. The signaling LED drivers LEDR1, LEDG1, LEDB1, LEDR2, LEDG2, and LEDB2 are independent current sink channels. Each driver channel features programmable current levels via LEDxBRT[1:0] as well as programmable PWM duty cycle settings with LEDxDC[5:0]. By a combination of level and PWM settings, each channel provides flexible LED intensity control. By driving LEDs of different colors, color mixing can be achieved. The default duty cycle, when a blink period is set, not continuous, is 0.5 s on time.

Blue LEDs or bright green LEDs require more headroom than red and normal green signal LEDs. In the application, a 5.0 V or equivalent supply rail is therefore required. This is provided by the integrated 5.0 V boost converter VOTG.

Battery voltage can also be used to supply the RGB banks directly via VPWR, if enough headroom is possible, by using low forward voltage LEDs. Furthermore, each one of these drivers can be supplied from a different source, as they are completely independent. The PWM waveforms are staggered from each other by one cycle of 32 kHz to minimize sudden load changes on the LED supply.

The signaling LED drivers include ramp up and ramp down patterns implemented in hardware. Ramp patterns for each of the drivers are accessed with the corresponding LEDxRAMP bit. The ramp itself is generated by increasing or decreasing the PWM duty cycle with a 1/32 step every 1/64 seconds. The ramp time is therefore a function of the initial set PWM cycle and the final PWM cycle. As an example, starting from 0/32 and going to 32/32 will take 500 ms, while going to from 8/32 to 16/32 takes 125 ms. Note that the ramp function is executed upon every change in PWM cycle

setting. If a PWM change is programmed via the SPI when the LEDxRAMP=0, then the change is immediate rather than spread out over a PWM sweep.

For color mixing and in order to guarantee a constant color, the color mixing should be obtained by the current level setting so that the intensity is set through the PWM duty cycle. In addition, programmable blink rates are provided. Blinking is obtained by lowering the PWM repetition rate of each of the drivers through LEDxBLNK[1:0] while the on period is determined by the duty cycle setting, default is 0.5 s ON time. To avoid high frequency spur coupling in the application, the switching edges of the output drivers are softened. During blinking, so LEDxBLNK[1:0] is not "00", ramping and dimming patterns cannot be applied.

Apart from using the signal/status LED drivers for driving LEDs they can also be used as general purpose open drain outputs for logic signaling or as generic PWM generator outputs. For the maximum voltage ratings see Maximum Ratings.

Signaling/Status LED Drivers Status/Control Registers and Bits Description

Table 75. Signaling /Status LED Driver Register and Bit Description

Name	Bits	Description
LEDBRT0 (ADDR 0x25 - R/W - Default Value: 0x00)		
LED0BRT	1:0	LEDR1 Driver Current Settings x0 = 0 mA x1 = 8.0 mA x2 = 20 mA x3 = 28 mA
LED0BLNK	3:2	LEDR1 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s
LED1BRT	5:4	LEDG1 Driver Current Settings x0 = 0 mA x1 = 8.0 mA x2 = 20 mA x3 = 28 mA
LED1BLNK	7:6	LEDG1 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s
LEDBRT1 (ADDR 0x26 - R/W - Default Value: 0x00)		
LED2BRT	1:0	LEDB1 Driver Current Settings x0 = 0 mA x1 = 8.0 mA x2 = 20 mA x3 = 28 mA
LED2BLNK	3:2	LEDB1 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s
LED3BRT	5:4	LEDR2 Driver Current Settings x0 = 0 mA x1 = 8.0 mA x2 = 20 mA x3 = 28 mA

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Table 75. Signaling /Status LED Driver Register and Bit Description

LED3BLNK	7:6	LEDR2 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s
LEDBRT2 (ADDR 0x27 - R/W - Default Value: 0x00)		
LED4BRT	1:0	LEDG2 Driver Current Settings x0 = 0 mA x1 = 8.0 mA x2 = 20 mA x3 = 28 mA
LED4BLNK	3:2	LEDG2 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s
LED5BRT	5:4	LEDB2 Driver Current Settings x0 = 0 mA x1 = 8.0 mA x2 = 20 mA x3 = 28 mA
LED5BLNK	7:6	LEDB2 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s

Signaling/Status LED Drivers Status/Control Registers and Bits Description

FSL control registers are completely optional, but if the application wants to have an adjustable duty cycle and/or duty cycle ramping (“advance control”), the FSL registers are activated by setting the LEDxBLNK fields to 00 = no blink. The default duty cycle in advance mode is set to 100%. After enabling the FSL register control, if the user wishes to revert back to “normal control” with 0.5 sec ON time, just write something different than 00 to the LEDxBLNK fields.

Table 76. RGB LED Control Register Structure and Bits Description

Name	Bits	Description			
FSLLEDR1CNT (ADDR 0x1D6 - R/W - Default Value: 0xFC)					
LEDR1BLNK	1:0	LEDR1 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s			
LEDR1DC	7:2	LEDR1 Driver PWM Duty Cycle Settings			
		x00=0/32 x01=1/32 x02=2/32 x03=3/32 x04=4/32 x05=5/32 x06=6/32 x07=7/32	x08=8/32 x09=9/32 x0A=10/32 x0B=11/32 x0C=12/32 x0D=13/32 x0E=14/32 x0F=15/32	x10=16/32 x11=17/32 x12=18/32 x13=19/32 x14=20/32 x15=21/32 x16=22/32 x17=23/32	x18=24/32 x19=25/32 x1A=26/32 x1B=27/32 x1C=28/32 x1D=29/32 x1E=30/32 x1F=31/32 x20=32/32 (Continuous ON) x21-x3F=Don't Care
FSLLEDG1CNT (ADDR 0x1D7 - R/W - Default Value: 0xFC)					
LEDG1BLNK	1:0	LEDG1 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s			
LEDG1DC	7:2	LEDG1 Driver PWM Duty Cycle Settings			
		x00=0/32 x01=1/32 x02=2/32 x03=3/32 x04=4/32 x05=5/32 x06=6/32 x07=7/32	x08=8/32 x09=9/32 x0A=10/32 x0B=11/32 x0C=12/32 x0D=13/32 x0E=14/32 x0F=15/32	x10=16/32 x11=17/32 x12=18/32 x13=19/32 x14=20/32 x15=21/32 x16=22/32 x17=23/32	x18=24/32 x19=25/32 x1A=26/32 x1B=27/32 x1C=28/32 x1D=29/32 x1E=30/32 x1F=31/32 x20=32/32 (Continuous ON) x21-x3F=Don't Care

Table 76. RGB LED Control Register Structure and Bits Description

FSLLEDB1CNT (ADDR 0x1D8 - R/W - Default Value: 0xFC)					
LEDB1BLNK	1:0	LEDB1 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s			
LEDB1DC	7:2	LEDB1 Driver PWM Duty Cycle Settings			
		x00=0/32 x01=1/32 x02=2/32 x03=3/32 x04=4/32 x05=5/32 x06=6/32 x07=7/32	x08=8/32 x09=9/32 x0A=10/32 x0B=11/32 x0C=12/32 x0D=13/32 x0E=14/32 x0F=15/32	x10=16/32 x11=17/32 x12=18/32 x13=19/32 x14=20/32 x15=21/32 x16=22/32 x17=23/32	x18=24/32 x19=25/32 x1A=26/32 x1B=27/32 x1C=28/32 x1D=29/32 x1E=30/32 x1F=31/32 x20=32/32 (Continuous ON) x21-x3F=Don't Care
FSLLEDR2CNT (ADDR 0x1D9 - R/W - Default Value: 0xFC)					
LEDR2BLNK	1:0	LEDR2 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0s x2 = 4.0 s x3 = 8.0 s			
LEDR2DC	7:2	LEDR2 Driver PWM Duty Cycle Settings			
		x00=0/32 x01=1/32 x02=2/32 x03=3/32 x04=4/32 x05=5/32 x06=6/32 x07=7/32	x08=8/32 x09=9/32 x0A=10/32 x0B=11/32 x0C=12/32 x0D=13/32 x0E=14/32 x0F=15/32	x10=16/32 x11=17/32 x12=18/32 x13=19/32 x14=20/32 x15=21/32 x16=22/32 x17=23/32	x18=24/32 x19=25/32 x1A=26/32 x1B=27/32 x1C=28/32 x1D=29/32 x1E=30/32 x1F=31/32 x20=32/32 (Continuous ON) x21-x3F=Don't Care

Table 76. RGB LED Control Register Structure and Bits Description

FSLLEDG2CNT (ADDR 0x1DA - R/W - Default Value: 0xFC)					
LEDG2BLNK	1:0	LEDG2 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s			
LEDG2DC	7:2	LEDG2 Driver PWM Duty Cycle Settings			
		x00=0/32 x01=1/32 x02=2/32 x03=3/32 x04=4/32 x05=5/32 x06=6/32 x07=7/32	x08=8/32 x09=9/32 x0A=10/32 x0B=11/32 x0C=12/32 x0D=13/32 x0E=14/32 x0F=15/32	x10=16/32 x11=17/32 x12=18/32 x13=19/32 x14=20/32 x15=21/32 x16=22/32 x17=23/32	x18=24/32 x19=25/32 x1A=26/32 x1B=27/32 x1C=28/32 x1D=29/32 x1E=30/32 x1F=31/32 x20=32/32 (Continuous ON) x21-x3F=Don't Care
FSLLEDB2CNT (ADDR 0x1DB - R/W - Default Value: 0xFC)					
LEDB2BLNK	1:0	LEDB2 Blink Setting, with a default on time of 0.5 s x0 = No Blink x1 = 1.0 s x2 = 4.0 s x3 = 8.0 s			
LEDB2DC	7:2	LEDB2 Driver PWM Duty Cycle Settings			
		x00=0/32 x01=1/32 x02=2/32 x03=3/32 x04=4/32 x05=5/32 x06=6/32 x07=7/32	x08=8/32 x09=9/32 x0A=10/32 x0B=11/32 x0C=12/32 x0D=13/32 x0E=14/32 x0F=15/32	x10=16/32 x11=17/32 x12=18/32 x13=19/32 x14=20/32 x15=21/32 x16=22/32 x17=23/32	x18=24/32 x19=25/32 x1A=26/32 x1B=27/32 x1C=28/32 x1D=29/32 x1E=30/32 x1F=31/32 x20=32/32 (Continuous ON) x21-x3F=Don't Care

Table 77. FSLLEDRAMPCNT Register Structure and Bits Description

Name	Bits	Description
FSLLEDRAMPCNTL (ADDR 0x1DC - R/W - Default Value: 0x00)		
LEDR1RAMP	0	LEDR1 Driver Ramp Up – Ramp Down Patterns Enable Bit x0 = Disable x1 = Enable
LEDG1RAMP	1	LEDR1 Driver Ramp Up – Ramp Down Patterns Enable Bit x0 = Disable x1 = Enable
LEDB1RAMP	2	LEDR1 Driver Ramp Up – Ramp Down Patterns Enable Bit x0 = Disable x1 = Enable

Table 77. FSLLEDRAMPCNT Register Structure and Bits Description

LEDR2RAMP	3	LEDR1 Driver Ramp Up – Ramp Down Patterns Enable Bit x0 = Disable x1 = Enable
LEDG2RAMP	4	LEDR1 Driver Ramp Up – Ramp Down Patterns Enable Bit x0 = Disable x1 = Enable
LEDB2RAMP	5	LEDR1 Driver Ramp Up – Ramp Down Patterns Enable Bit x0 = Disable x1 = Enable
Reserved	7:6	Reserved

BATTERY INTERFACE AND POWER PATH MANAGEMENT

POWER PATH MANAGER

The 900841 IC sources power to the platform loads through an intelligent power path that consists of the following two components listed in order of priority. Reference Figure 62 for more details:

- Input power source through a mini-USB connector that can be either an AC wall charger or a USB host adaptor. The system host is responsible for notifying the 900841 of what type of input source it is connected to, by setting the maximum current the charger can draw from the input source (for example: 0.5 A USB or 1.8 A power source device).
- A bi-directional source in the form of a rechargeable single cell Li-Ion or Li-Polymer Battery.

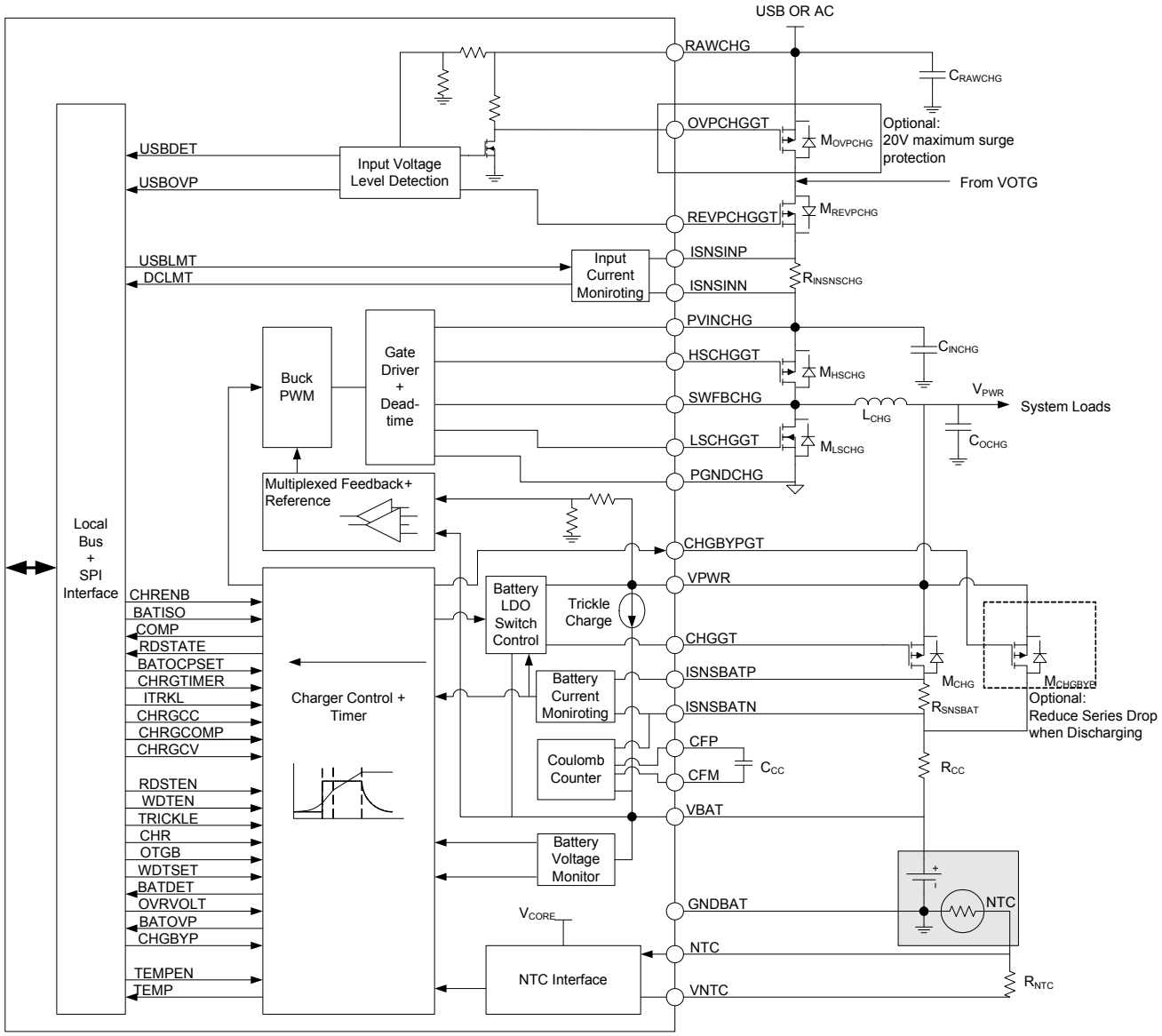

Figure 62. Power Path Manager + Li-Ion Charger Block Diagram

The multiplexed power output is made available at the VPWR node where all on-chip regulators draw their power from at a typical operating range of 3.0 to 4.4 V. See Figure 62. When a power source is detected at the RAWCHG pin, the respective input voltage is converted to a variable output voltage at the VPWR node through a buck switching DC/DC regulator, Charger buck.

CHARGER BUCK OPERATION

Charger buck takes its feedback from two sources, depending on the state of the battery:

- For batteries with a voltage less than the trickle charge threshold, V_{PWR} is set at a constant voltage of 4.2 V to supply the system loads. The feedback is taken from a conventional internal resistor divider connected at the VPWR pin. This supports dead battery operation and allows the system to operate if the battery does not exist, or is being trickle charged through a separate path.
- For batteries within normal operation of 3.0 to 4.4 V, V_{PWR} tracks the battery voltage level V_{BAT}. To keep power dissipation low during charging, VPWR is normally adjusted to be 300 mV above V_{BAT}, subject to a maximum of 4.7 V.

The buck regulator core implements PWM and auto-PFM modes. The charger buck needs to be able to support 100% duty operation for cases when the input falls close to the output voltage. In this mode, M_{HSCHG} is switched fully on, and M_{LSCHG} is disabled. The regulator will stay in 100% (or close to it) duty-cycle mode until either V_{PWR} rises above 4.7V, under which case V_{PWR} is clamped to a maximum of 4.7V, or the loop feedback demands a lower duty cycle. While

in 100% Duty Cycle mode, the output current limit is still operational.

The charger buck monitors the input current draw by sensing the voltage across $R_{INSNSCHG}$ which will allow the charger system to regulate the power draw out of the input adaptor to fit the needs of the system. During charging, if an input source is connected and the selected charging current plus load current exceeds the current limit set by the USBLMT[1:0] bits and detected across $R_{INSNSCHG}$, the charger buck will behave like a constant current source, supplying the current limit. The V_{PWR} voltage will droop, and the DCLMT interrupt signal is asserted. As the V_{PWR} voltage approaches the V_{BAT} voltage, the charger pass transistor, M_{CHG}, will switch itself fully on as the charger control tries to maintain the programmed charge current. At some point, the charge current will start to decrease, as this current starts to get limited by the $R_{ds(on)}$ of M_{CHG}. The V_{PWR} voltage will stabilize at a point where the charge current equates to the difference between the input current limit set by USBLMT[1:0] and the total system load current. If the load current by itself exceeds the input current limit, the V_{PWR} voltage will fall more below the V_{BAT} voltage, and the excess current will come from the battery through M_{CHG}, which is still fully switched on in this instance. The USBLMT settings are maximum numbers and will not be exceeded, so a lower value should be targeted as a typical and ±5% accuracy is desired

In the previous case, where the battery is being discharged, M_{CHGBYP} provides an optional feature to reduce the series resistance between V_{BAT} and V_{PWR}, saving on overall system efficiency and battery life. The system can activate this function by asserting the CHGBYP bit high. So if CHGBYP is “1”, and whenever V_{PWR} falls below V_{BAT} by 100 mV, the 900841 turns on MCHGBYP. If CHGBYP is “0”, this function is deactivated. If MCHGBYP is not used, the CHGBYPGT pin must be connected to ground.

To prevent an over-voltage condition to the system, the charger buck monitors the voltage at the RAWCHG pin. If V_{RAWCHG} rises above 5.75 V, an over-voltage condition is detected, the over-voltage protection FET M_{OVPCHG} is disabled, the charger buck is disabled, and the USBOVP interrupt signal is asserted and the RDSTATE register is updated to state 0x02 (AC Adaptor OVP). Such over-voltage condition can occur due to a faulty USB/AC adapter design or a voltage spike during the insertion of the adapter to the system. Input over-voltage protection is an optional feature, as there are other methods to prevent an over-voltage condition. Such methods, like a Zener clamp, can limit the input voltage to a 6.0 V maximum, under which case M_{OVPCHG} is not needed and can be removed. Using a high performance or well designed adaptor that can guarantee a maximum input voltage of 5.5 V, will eliminate the need for M_{OVPCHG}. If any of these other methods fail, damage will occur to the IC. Without the presence of M_{OVPCHG}, a maximum voltage will be exceeded for many parts of the IC.

Whenever the charger buck is disabled, the battery will supply power to the VPWR node through the charger pass transistor element M_{CHG}, and also through M_{CHGBYP} if used. In that case, $M_{REVPCHG}$ switch is disabled to electrically isolate the input power connector from the battery and prevent reverse current draw from battery to connector. For lower power inputs, like a dedicated USB source, $M_{REVPCHG}$, can be replaced by a low forward voltage drop Schottky Diode, pointing the same direction as the $M_{REVPCHG}$ body diode. In this case, REVPCHGGT should be grounded. No specific Schottky diode is recommended. Any 2.0 A/30 V capable diode with low forward voltage drop can use used.

The system can assert the BATISO bit to turn off M_{CHG}, and M_{CHGBYP} if used, to isolate the battery from the system. In this case, V_{PWR} has to be higher than V_{BAT} and set, depending on the value of the battery, as explained in the first paragraph. Reference Power States and Control for more information.

LI-ION BATTERY CHARGER

FEATURES

- Complete charger for single-cell Li-Ion batteries with an external PFET pass element
- Programmable constant charge current limit (I_{CHGCC})
- Programmable End-of-Charge (EOC) detection current ($I_{CHGCOMP}$)
- Programmable trickle charge current (I_{TRKL})
- Intelligent EOC detection to prevent false indication
- Programmable battery float voltage (V_{CHGCV})
- Programmable battery over-voltage ($V_{OVRVOLT}$)
- Optional battery temperature monitoring NTC thermistor interface for charge qualification with two different temperature ranges for charging and discharging
- Ability for trickle mode only charging
- Programmable smart timer for charge termination and detection of fault conditions (t_{CHG})
- Programmable battery over-voltage protection
- Intelligent Interrupt and State reporting capabilities

Charger Operation

The charger provides the traditional Constant Current/ Constant Voltage (CC/CV) charging output with the preconditioning function (trickle charge) for deeply discharged batteries. Multiple parameters can be programmed through the SPI registers.

The charger is a Constant Current Regulator with V_{PWR} as its input and V_{BAT} as its output, with constant voltage headroom of 300 mV across it, $V_{PWR} – V_{BAT}$. It regulates the maximum charging current flowing into the battery (I_{CHGCC}) to the value set by SPI programming of the CHRGCC[2:0] bits. The 300 mV headroom includes the voltage drop across R_{SNSBAT} and R_{CC}.

The loop will regulate the voltage drop over the sense resistor R_{SNSBAT} by controlling M_{CHG} to a value resulting in a maximum constant current equal to I_{CHGCC}. Therefore, the value of R_{SNSBAT} influences the charge current, and its

accuracy directly effects the accuracy of I_{CHGCC} and $I_{CHGCOMP}$. A value of 100 m ±1% is recommended.

Charger Parameter Programming

Multiple charge parameters are programmable through the SPI interface:

- Battery float voltage (V_{CHGCV})
- Constant charge current (I_{CHGCC})
- End-of-Charge current ($I_{CHGCOMP}$)
- Trickle charge current (I_{TRKL})
- Battery over-voltage ($V_{OVRVOLT}$)
- Charge time monitor timer (t_{CHG})

Charge Starts and Charge Ends

A charging cycle cannot start until a valid voltage is detected at RAWCHG, CHRENB bit is set to 0, and no faults exist. A valid RAWCHG voltage is when V_{RAWCHG} is > 4.75 V. The USB interrupt signal is asserted when V_{RAWCHG} > 4.75 V. During a charging cycle, if the charger system experiences any fault, it stops charging and asserts the appropriate interrupt signal. When a charge cycle completes, the COMP interrupt signal is asserted indicating a normal completion of a charge cycle. What constitutes a charge cycle completion is examined later in this section.

CHARGER STATE MACHINE

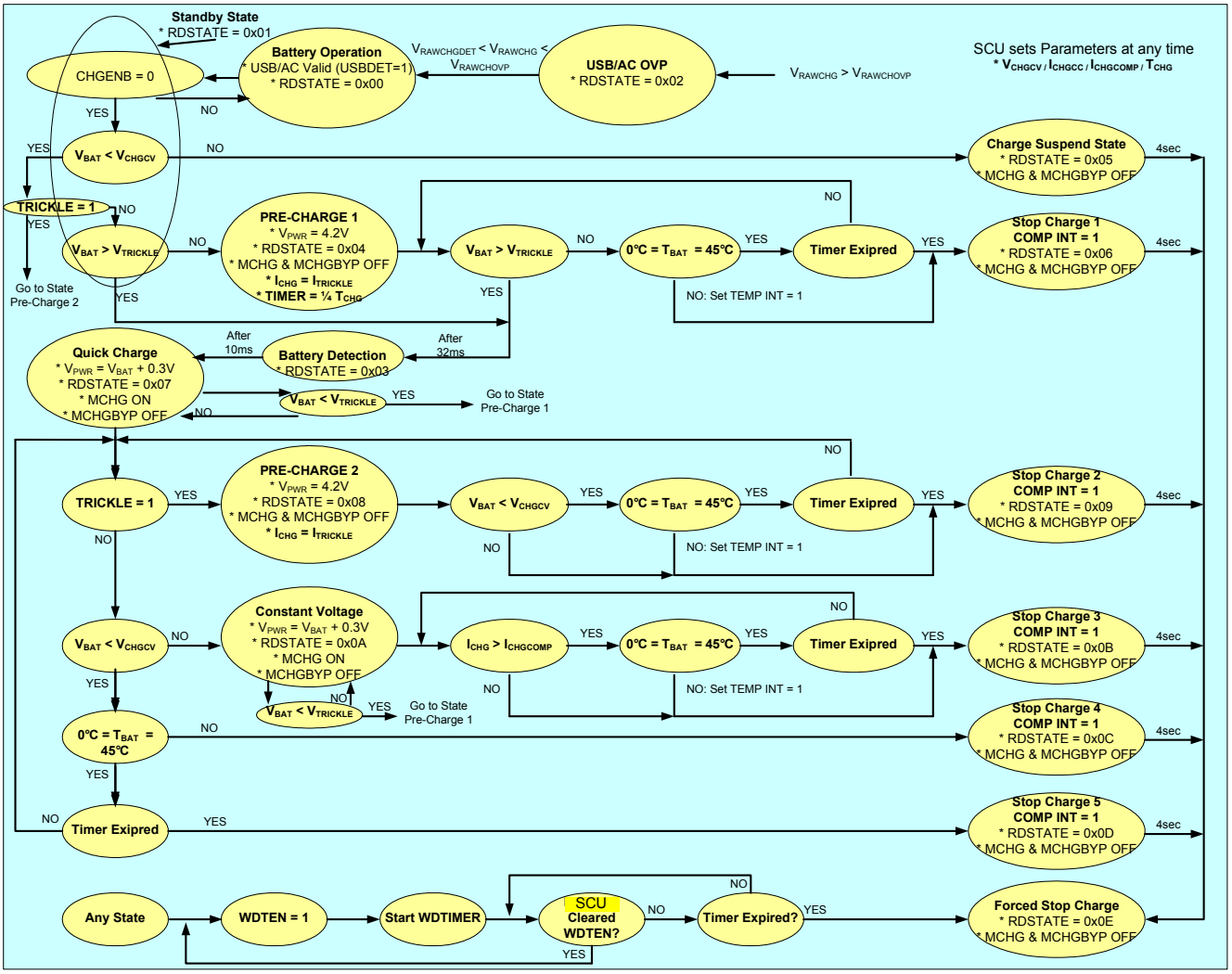

Figure 63. Li-Ion Charger State Machine

TRICKLE CHARGE

Once the charger is enabled and if $V_{BAT} < V_{TRKL}$, the trickle charge starts. The trickle charge current $I_{CHGTRKL}$ is selectable with a default current of 40 mA, and is provided by an internal current source between V_{PWR} and V_{BAT}, as can be seen in Figure 63. The trickle charge function consists of a simple comparator that monitors the battery voltage. The charger stays in the trickle mode as long as the battery voltage is below the trickle charge threshold (V_{TRKL}) of 3.0 V

and the total trickle charge time has not expired. If the trickle charge time expires before V_{BAT} exceeding V_{TRKL}, the charger is turned off and the appropriate state is set. If V_{BAT} rises above V_{TRKL} before the trickle charge time expires, we enter in the Quick Charge stage and I_{CHGCC} is used for charging. At any time during trickle charging, if a fault occurs, the charger turns off and an interrupt is asserted, according to the type of fault. The trickle charge time is always set to 1/4 of the set t_{CHG} timer. The t_{CHG} timer is reset when entering the trickle charge mode. V_{TRKL} detection is equipped with a 32 ms filter to debounce the transition between Trickle and Quick Charge modes. Regardless of the timer state, if V_{BAT} rises above V_{TRKL}, then the BATDET interrupt signal is asserted.

Trickle charging can be forced as well, by setting the bit TRICKLE = 1. In this case, the full t_{CHG} timer is used during trickle charge. In this mode, charging stops if the timer expires or V_{BAT} exceeds V_{CHGCV} triggers the EOC on forced trickle mode.

QUICK CHARGE

The fast charge includes the CC mode and the CV mode. A soft transition between the trickle mode and the CC mode is required to minimize the transient behavior at the input during the transition. The Constant Current value (I_{CHGCC}) can be set by SPI programming the CHRGCC[2:0] bits, and is regulated as explained previously. Once entering the CV mode, the battery voltage is held at the battery float voltage threshold V_{CHGCV}, which can be set by SPI programming the CHRGCV[3:0] bits. The charge current reduces gradually until the end of charge event EOC. The total charge time for the quick charge is limited by t_{CHG}.

The t_{CHG} timer is reset when entering the fast charge mode.

If the battery voltage V_{BAT} exceeds the over-voltage threshold set by SPI programming the OVRVOLT[1:0] bits, the buck charger is turned off and the BATOVP interrupt signal is asserted.

END-OF-CHARGE (EOC)

For a charge cycle to be completed (EOC), two conditions are required to be simultaneously met: the battery voltage must be above the recharge threshold V_{RCHG}, and the charge current must fall below the EOC current $I_{CHGCOMP}$. $I_{CHGCOMP}$ can be set by SPI programming the CHRGCOMP[2:0] bits. A 1.0 ms filter is required to prevent fast transient current, triggering the EOC current threshold.

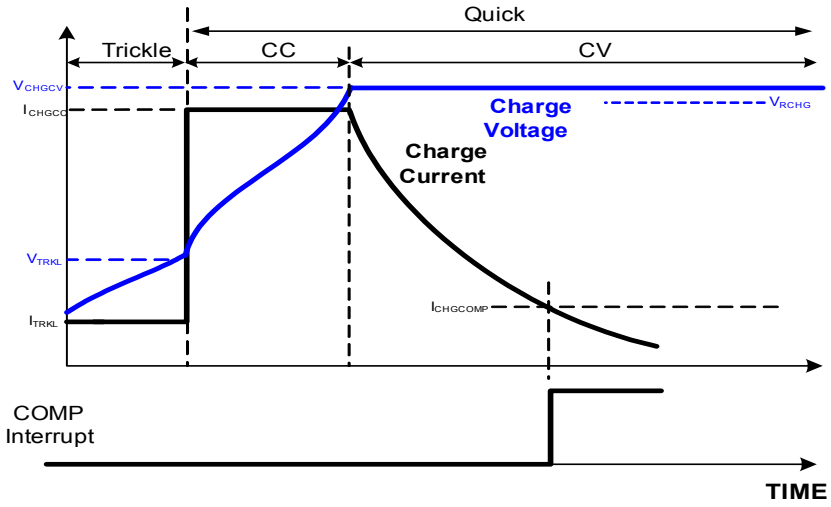

Figure 64. EOC Behavior

WATCHDOG TIMER

The charger is equipped with a watchdog timer that the Platform controller hub can enable and set for different times. Setups and responses are highlighted in Figure 63.

NTC INTERFACE

A battery pack may be equipped with a thermistor which value decreases over temperature (NTC). The NTC interface allows an external NTC thermistor to monitor the battery temperature and disable the charger when the temperature is outside of a specific window. The relationship between temperature T (in Kelvin) and the thermistor value (RT) is well characterized, and can be described as $R_T=R_0*e^{(B*(1/T - 1/T_0)}$, with T_0 being room temperature, R_0 the thermistor value at T_0, and B being the so called B-factor which indicates the slope of the thermistor over temperature. The NTC interface can handle several standard B factors such as 3200, 3500, and 3900.

To read out the thermistor value, it is biased through a pull-up resistor R_{NTC} from the VNTC pin, which switches the V_{CORE} voltage to bias the chain. This switch, along with the NTC comparators, is controlled through the TEMPEN bit.

During charging, the NTC comparators and the switch are turned on automatically for battery temperature monitoring,

and the temperature range is set at 0°C to 45°C. NTC circuitry cannot be disabled during charging.

During discharging, the user has an option to turn the NTC block off through the TEMPEN bit. Whenever an NTC ADC reading is desired or to keep battery temperature monitor on, this bit must be asserted. Turning this block off and disconnecting the switch saves on quiescent current and enhances battery life. During discharging, the battery temperature monitoring range is set at -10°C to 60°C.

The window thresholds are specified as a ratio of the V_{NTC} voltage. The battery thermistor check circuit compares the fraction of V_{NTC} at NTC pin, with two preset thresholds which correspond to one of the previous ranges, depending if the IC is charging or discharging the battery.

During charging, if the battery temperature is not within range, charging is stopped and the TEMP interrupt signal is asserted, to indicate a battery temperature fault. During discharging if the battery temperature is not within range, the TEMP interrupt signal is asserted.

The tolerance should include the resistive divider error, as well as the comparator offset error. Other applications may not require an NTC interface. In that case, the NTC resistor is not populated and this feature is disabled.

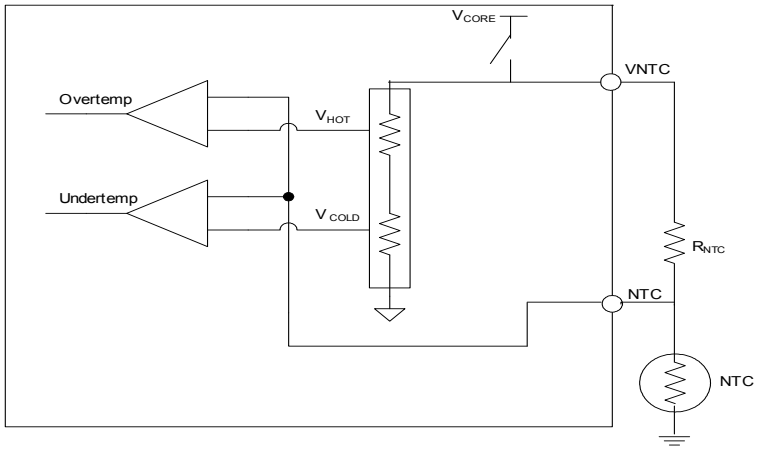

Figure 65. NTC Thermistor Interface

COIN CELL BATTERY BACKUP/ CHARGER

The COIN CELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged or removed, and in the absence of a USB/Wall input source, the RTC system and coin cell maintained logic, will switch over to the COIN CELL for backup power. A small capacitor should be placed from the COIN CELL pin to ground under all circumstances.

The coin cell charger circuit will function as a current limited voltage source, resulting in the CC/CV taper characteristic, typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHGEN bit. which is enabled by default. The output voltage (V_{COIN}) is programmable through the VCOIN[2:0] bits. The coin cell charger voltage is programmable in the active state, where the charge current is fixed at I_{COINHI}. The coin cell charging will be stopped when V_{PWR} goes below V_{PWRUVF}. Reference Power Path Manager SPI Registers for a more detailed description of the coin cell related bits.

A large capacitor, electrolytic or super cap, can also be used instead of a lithium based coin cell. To avoid discharge by leakage currents from external components or by the 900841, the COINCHGEN bit should always remain set.

Coin cell charge is equipped with a disconnect circuitry that isolates the coin cell from any loads, if V_{COIN} goes below 2.0 V, to prevent the coin cell from being deeply discharged and damaged. This will also cause the ADC reading of the coin cell voltage to yield zero.

POWER PATH MANAGER SPI REGISTERS

POWER PATH MANAGER PLUS LI-ION CHARGER REGISTERS AND BITS DESCRIPTION

Table 78. Charger Interrupt/Mask Registers Structure and Bits Description

Name	Bits	Description
CHRGINT (ADDR 0xD0 - R - Default Value: 0x00)		
Reserved	0	Reserved
BATOVP	1	Battery over-voltage Interrupt Signal (V_{BAT} > V_{CHGCV} + $V_{OVRVOLT}$) x0 = No over-voltage condition x1 = Over-voltage condition
TEMP	2	Battery over/under-temperature Interrupt Signal (Battery temperature is out of valid window) x0 = No over/under-temperature condition x1 = Over/under-temperature condition
COMP	3	Battery Charge Cycle Completion Interrupt Signal This signal is set any time a charging cycle is complete or the RDSTATE bits change. The RDSTEN bit controls how often this interrupt signal is asserted. If RDSTEN is 0 the following conditions must be true for the COMP interrupt to be set: VBAT > CHRGCV setting (V_{CHRGCV}) & I_{CHG} < CHRGCOMP setting (IEOC) x0 = Charge Cycle Not Complete x1 = Charge Cycle Complete If RDSTEN is 1 Then the following is true for the COMP interrupt x0 = Charge Cycle Not Complete x1 = RDSTATE register bits change
USBDET	4	USB VBUS Detection Interrupt Signal. This is a dual edge interrupt signal that is set any time a valid USB device (V_{RAWCHG} > $V_{RAWCHGDET}$) is connected or disconnected x0 = No interrupts pending x1 = USB VBUS is connected/disconnected (refer to the SCHRGINT register)
BATDET	5	Battery Detection Interrupt Signal This is a dual edge interrupt signal that is set any time a valid battery (VBAT > VTRKL) is connected or disconnected x0 = No interrupts pending x1 = battery is connected/disconnected (refer to the SCHRGINT register)
DCLMT	6	Charge Input Current Limit Detection Interrupt Signal x0 = No Input Current Limit Detected x1 = Input Current Limit Detected
USBOVP	7	Charge Input over-voltage Detection Interrupt Signal (V_{RAWCHG} > $V_{RAWCHGOVP}$) x0 = No Input over-voltage Detected x1 = Input over-voltage Detected
MCHRGINT (ADDR 0xD1 - R/W - Default Value: 0x00)		
Reserved	0	Reserved
MBATOVP	1	Battery over-voltage Interrupt Signal Mask x0 = Unmask x1 = Mask

Table 78. Charger Interrupt/Mask Registers Structure and Bits Description

MTEMP	2	Battery Over/Under-temperature Interrupt Signal Mask x0 = Unmask x1 = Mask
MCOMP	3	Battery Charge Cycle Completion Interrupt Signal Mask x0 = Unmask x1 = Mask
MUSBDET	4	USB V_{BUS} Detection Interrupt Signal Mask x0 = Unmask x1 = Mask
MBATDET	5	Battery Detection Interrupt Signal Mask x0 = Unmask x1 = Mask
MDCLMT	6	Charge Input Current Limit Detection Interrupt Signal Mask x0 = Unmask x1 = Mask
MUSBOVP	7	Charge Input Over-voltage Detection Interrupt Signal Mask x0 = Unmask x1 = Mask
SCHRGINT (ADDR 0xD2 - R - Default Value: 0x00)		
Reserved	0	Reserved
SBATOVP	1	Battery Over-voltage Status x0 = Battery voltage is lower than the limit (< V_{CHGCV} + $V_{OVRVOLT}$) x1 = Battery voltage is higher than the limit (> V_{CHGCV} + $V_{OVRVOLT}$)
STEMP	2	Battery temperature Status x0 = Battery temperature is within valid window x1 = Battery temperature is out of valid window
SCOMP	3	Battery Charge Cycle Completion Status x0 = Charge cycle not complete (RDSTEN = 0), state not changed (RDSTEN = 1) x1 = charge cycle complete (RDSTEN = 0), state changed (RDSTEN = 1)
SUSBDET	4	Charger Input Voltage Status Signal x0 = Charger input voltage not present (V_{RAWCHG} < $V_{RAWCHGDET}$) x1 = Charger input voltage present (V_{RAWCHG} > $V_{RAWCHGDET}$)
SBATDET	5	Battery Present Status Signal x0 = Battery not present (VBAT < VTRKL) x1 = Battery present (VBAT > VTRKL)
SDCLMT	6	Charge Input Current Limit Status x0 = Charger input current is lower than the limit (< I_{USBLMT}) x1 = Charger input current is higher than the limit (> I_{USBLMT})
SUSBOVP	7	Charger Input Over-voltage Status x0 = Charger input voltage is lower than the limit (< $V_{RAWCHGOVP}$) x1 = Charger input voltage is higher than the limit (> $V_{RAWCHGOVP}$)

Table 79. Charger Status And Control Registers Structure and Bits Description

Name	Bits	Description	
CHRGSTATE (ADDR 0xD3 - R - Default Value: 0x00)			
RDSTATE	3:0	Charger State Register	
		x00 = Battery Operation x01 = Standby Mode x02 = AC Adaptor OVP x03 = Battery Detect x04 = Pre-charge 1 x05 = Charge Suspend x06 = Stop-Charge 1 x07 = Quick Charge	x08 = Pre-charge 2 x09 = Stop-charge 2 x0A = Constant Voltage Mode x0B = Stop-Charge 3 x0C = Stop-Charge 4 x0D = Stop-Charge 5 x0E = Forced Stop Charge x0F = Reserved
Reserved	7:4	Reserved	
CHRGCNTL (ADDR 0xD4 - R/W - Default Value: 0xA1)			
CHRENB	0	Battery Charger Enable Signal, Active low x0 = Enable Charger x1 = Disable Charger	
TRICKLE	1	Trickle Charge Enable Signal x0 = Automatic Trickle Charge x1 = Forced Trickle Charge	
WDTEN	2	Watch Dog Timer Enable Signal x0 = Disable Watchdog Timer x1 = Enable Watchdog Timer	
RDSTEN	3	State Register Update Control x0 = Set the interrupt bit only when a charge cycle has completed. x1 = Set the interrupt bit every time the charger change state.	
USBDETHEN	4	Not Supported, Reserved	
CHR	5	Don't Care for the charger Will be used in combination with OTGB bit to control OTG Host operation	
BATISO	6	Isolate the Battery from the System, FET Control x0 = FET(s) allowed to turn on (M_{CHG} and M_{CHGBYP}) x1 = FET(s) OFF (M_{CHG} and M_{CHGBYP})	
OTGB	7	Don't Care for the charger Will be used in combination with CHR bit to control OTG Host operation	
CHRGCRNT (ADDR 0xD5 - R/W - Default Value: 0x00)			
CHRGCC	3:0	Constant Current Charge Value I_{CHGCC}	
		x0 = 200 mA x1 = 300 mA x2 = 400 mA x3 = 500 mA x4 = 600 mA x5 = 700 mA x6 = 800 mA x7 = 900 mA	x8 = 1000 mA x9 = 1100 mA xA = 1200 mA xB = 1300 mA xC = 1400 mA xD = 1500 mA xE = 1600 mA xF = 1700 mA

Table 79. Charger Status And Control Registers Structure and Bits Description

CHRGCOMP	6:4	Charge Complete Current Value	
		x0 = 40 mA x1 = 80 mA x2 = 120 mA x3 = 160 mA	x4 = 200 mA x5 = 240 mA x6 = 280 mA x7 = 320 mA
Reserved	7	Reserved	
CHRVOLT (ADDR 0xD6 - R/W - Default Value: 0x07)			
CHRGCV	3:0	Maximum Charge Battery Voltage V_{CHGCV}	
		x0 = 4.025 V x1 = 4.050 V x2 = 4.075 V x3 = 4.100 V x4 = 4.125 V x5 = 4.150 V x6 = 4.175 V x7 = 4.200 V	x8 = 4.225 V x9 = 4.250 V xA = 4.275 V xB = 4.300 V xC = 4.325 V xD = 4.350 V xE = 4.375 V xF = 4.400 V
VDSSET	5:4	Not Supported, Reserved	
Reserved	7:6	Reserved	
CHRGPROT (ADDR 0xD7 - R/W - Default Value: 0x3C)			
Reserved	1:0	Reserved	
WDTSET	3:2	Watchdog Timer Settings x0 = 20 sec x1 = 40 sec x2 = 80 sec x3 = 160 sec	
OVRVOLT	5:4	Maximum Charge (Battery) Over-voltage Threshold (Over V_{CHRGCV}) x0 = 75 mV x1 = 100 mV x2 = 150 mV x3 = 200 mV	
USBLMT	7:6	Charger Buck Input Over-current Limit x0 = 100 mA x1 = 500 mA x2 = 1000 mA x3 = 1800 mA	
CHRGTIMER (ADDR 0xDB - R/W - Default Value: 0x03)			
CHRGTIMER	3:0	Charger Timer Settings	
		x0 = 1.0 hr x1 = 2.0 hr x2 = 3.0 hr x3 = 4.0 hr x4 = 5.0 hr x5 = 6.0 hr x6 = 7.0 hr x7 = 8.0 hr	x8 = 9.0 hr x9 = 10 hr xA = 11 hr xB = 12 hr xC = 13 hr xD = 14 hr xE = 15 hr xF = 16 hr

Table 79. Charger Status And Control Registers Structure and Bits Description

Reserved	7:4	Reserved
DISCHRG (ADDR 0xDC - R/W - Default Value: 0x04)		
BATOCPEN	0	Not Supported, Reserved
BATOVPEN	1	Not Supported, Reserved
TEMPEN	2	NTC Block Enable Control x0 = NTC Disabled x1 = NTC Enabled
Reserved	4:3	Reserved
BATDETEN	5	Not Supported, Reserved
Reserved	7:6	Reserved

For a CHRGPROT2 register Description, reference BATOCP.

Table 80. Charger Protection Registers for Future Use

Name	Bits	Description
PROTCMD (ADDR 0xD9 - W - Default Value: 0x00)		
*	0	Not Supported, Reserved
*	1	Not Supported, Reserved
*	2	Not Supported, Reserved
*	3	Not Supported, Reserved
*	4	Not Supported, Reserved
*	5	Not Supported, Reserved
*	6	Not Supported, Reserved
*	7	Not Supported, Reserved

Table 80. Charger Protection Registers for Future Use

WDRCLR (ADDR 0xDA - W - Default Value: 0x03)		
*	0	Not Supported, Reserved
*	1	Not Supported, Reserved
*	2	Not Supported, Reserved
*	3	Not Supported, Reserved
*	4	Not Supported, Reserved
*	5	Not Supported, Reserved
*	6	Not Supported, Reserved
*	7	Not Supported, Reserved

POWER PATH MANAGER PLUS LI-ION CHARGER REGISTERS AND BITS DESCRIPTION

Table 81. FSL Charger Control Register Structure and Bits Description

Name	Bits	Description
FSLCHRGCNTL (ADDR 0x1D1 - R/W - Default Value: 0x13)		
CHGBYP	0	M_{CHGBYP} FET Control is Activated x0 = M_{CHGBYP} is not used (Default) x1 = M_{CHGBYP} is used and can be controlled
COINCHEN	1	Coin cell Charger Enable/Disable x0 = Disable x1 = Enable (Default)

Table 81. FSL Charger Control Register Structure and Bits Description

VCOIN	4:2	Coin cell Charger Output Voltage Setting x0 = 2.5 V x1 = 2.7 V x2 = 2.8 V x3 = 2.9 V x4 = 3.0 V (Default) x5 = 3.1 V x6 = 3.2 V x7 = 3.3 V
ITRKL	5	Trickle Charge Current Setting x0 = 40 mA (Default) x1 = 80 mA
BUCKDIS	6	Enable Control for the Charger Buck: x0 = Charger Buck Enabled (default) x1 = Charger Buck Disabled
Reserved	7	Reserved

AUDIO

FEATURES

The following is a list of the main features of the Audio Solution:

INTERFACE

- Two Interfaces: one Voice and one Audio
- Includes automatic sample rate detection in slave mode
- Uses high frequency 24/26 MHz clock
- Supported word length: 16 bit and 32 bit only
- See also ADC/DAC section

ADC/DAC

- Voice ADC/DAC
  - Sampling frequencies - 8/16 kHz
  - ADC
    - •THD+N: -60 dB (0.1%) max
    - •Idle channel noise: -87 dBp typ
  - DAC
    - •THD+N: -65 dBA (0.06%) max
    - •Idle channel noise: -96 dBA typ
- Stereo ADC/DAC
  - Sampling frequencies
    - •8/11.025/12/16/22.05/24/26/32/44.1/48 kHz
  - ADC
    - •THD+N: -80 dBA (0.01%) max
    - •SNR: 90 dBA typ
    - •Dynamic Range: 90 dBA typ
  - DAC
    - •THD+N: -80 dBA (0.01%) max
    - •SNR: 100 dBA typ
    - •Dynamic Range: 96 dBA typ

TRANSMIT PATH

- Transmit Line-up
  - Analog PGA -8.0 dB to +23 dB in 1.0 dB steps
  - Selectable preamplifier 0/12 dB
- Microphone Support
  - Two electret handset microphones with bias
  - One digital handset microphones with clock
  - Headset microphone with bias and detection
  - Line in for car kit microphone
- Stereo Line Inputs
  - Selectable preamplifier -8/0/8/16 dB
  - Routing to stereo ADC and to receive path

RECEIVE PATH

- Receive Line-up
  - Digital RX PGA for CDC and STDAC -57 dB to +6.0 dB in 1.0 dB steps
  - Analog RX PGA for line in -57 dB to +6.0 dB in 1.0 dB steps
  - Mixer and Mono Adder
- Stereo Loudspeaker Amplifiers
  - Battery supplied Class D with differential outputs
  - Gain internally set to 12 dB (differential)
  - Output power per channel: 500 mW_{RMS} into 8.0 Ω @ V_{BAT}=3.4 V, 1.0 W_{RMS} into 4.0 Ω
  - THD @ 500 mW_{RMS}: -50 dB(0.3%) max
  - Input referred noise: 50 mV_{RMS}A max
- Ear piece amplifier
  - Battery supplied Class AB with differential output
  - Differential output swing into 32 Ω: 4.0 V_{PP}
  - THD: -60 dB (0.1%) max
  - Gain internally set to 10 dB (differential)

- Input referred noise: 8.0 $mV_{RMS}A$
- Headset amplifier
  - Class AB with Negative charge pump
  - Capacitor less headset coupling (referenced to ground)
  - Single ended output swing: 2.0 V_{PP}
  - Output load: 32 Ω
  - Output power per channel: 20 mW_{RMS} typ
  - THD: -60 dBA(0.1%) max
  - Input referred noise: 8.0 $mV_{RMS}A$
  - Gain: 0 dB +/- 0.5 dB
  - Headset detection circuit through microphone bias
- Line-Out amplifier
  - Class A single ended stereo outputs
  - Single ended output swing: 2.0 V_{PP} into 10 kΩ
  - Output load: 10 kΩ min
  - THD: -60 dBA (0.1%) max
  - Input referred noise: 10 $mV_{RMS}A$
  - Gain: 0 dB +/- 0.5 dB

DIGITAL AUDIO BUS

The digital audio interface consists of two busses; one dedicated to voice operation (PCM1) and the other dedicated to stereo audio (PCM2). Each bus consists of a bit clock, frame sync, receive data, and transmit data signal lines. Both busses can be configured independently and be active at the same time. The drive strength for the outputs is controlled by the SLOPESEL[1:0] bits

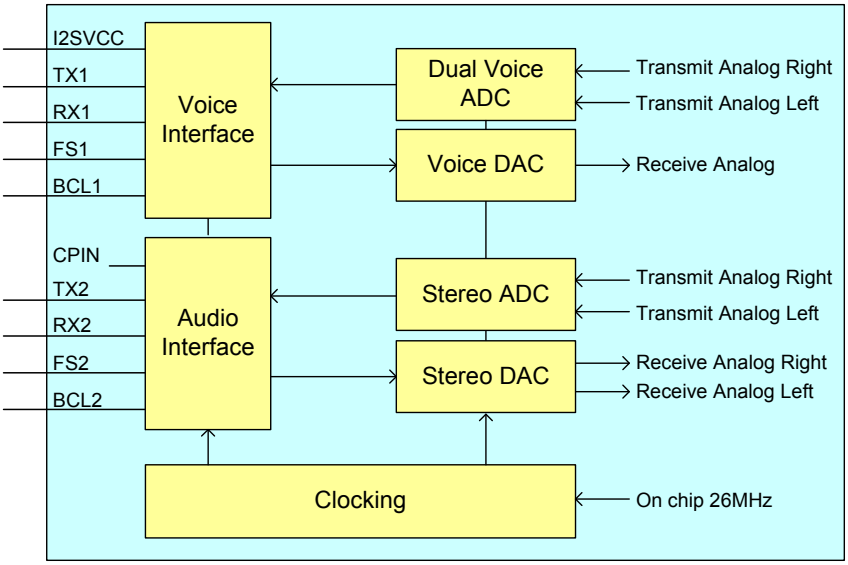

Figure 66. Digital Audio Bus Interface

Table 82. Interface Driver Characteristics

Parameter	Condition	Minimum	Typical	Maximum	Units
I2SVCC Supply Range	Nominal Voltages	1.8		3.3	V
Input High BCL1, FS1, RX1		0.7*I2SVCC		I2SVCC	V
Input Low BCL1, FS1, RX1		0		0.3* I2SVCC	V
Output Low BCL1, FS1, TX1	Output sink 100 μA	0		0.2	V
Output High BCL1, FS1, TX1	Output source 100 μA	I2SVCC -0.2		I2SVCC	V
CPIN Supply	Nominal Voltage		1.8		V
Input High BCL2, FS2, RX2		0.7*CPIN		CPIN	V
Input Low BCL2, FS2, RX2		0		0.3* CPIN	V
Output Low BCL2, FS2, TX2	Output sink 100 μA	0		0.2	V
Output High BCL2, FS2, TX2	Output source 100 μA	CPIN -0.2		CPIN	V
TX1, TX2 Rise and Fall Time	CL=50 pF, IO=1.8 V				

Table 82. Interface Driver Characteristics

BCL1, BCL2, FS1, FS2 Rise and Fall Time if in Master mode	SSIDRV[1:0]=00 (default)		11		ns
	SSIDRV[1:0]=01		6		ns
	SSIDRV[1:0]=10		High Z		ns
	SSIDRV[1:0]=11		22		ns

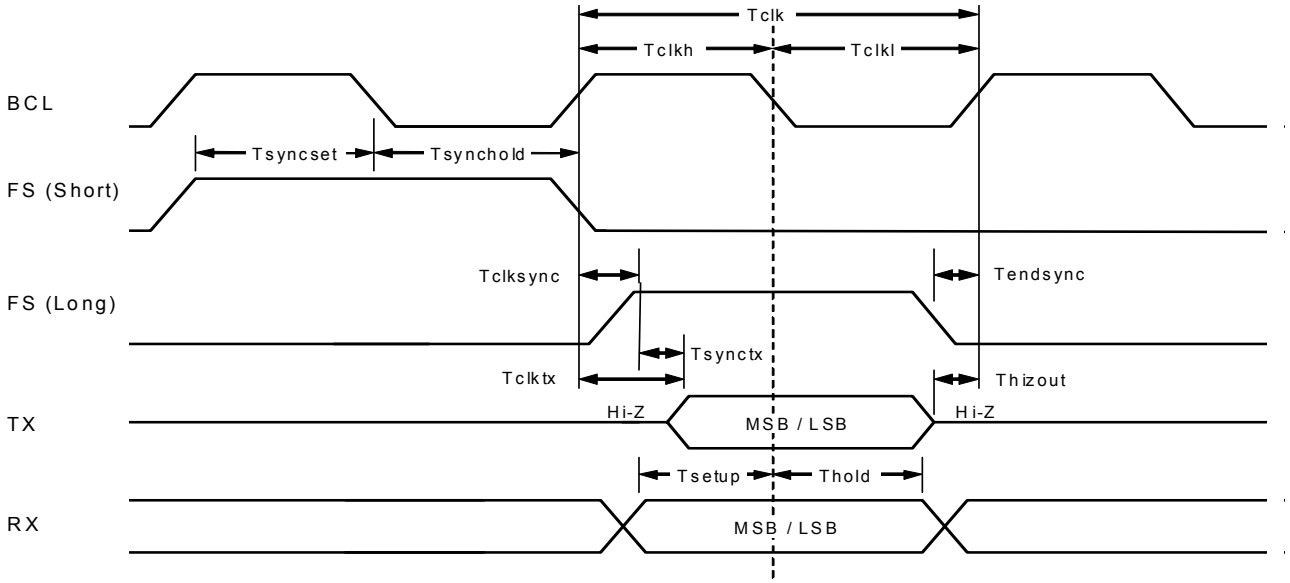

Figure 67. Interface Timing Diagram

Table 83. Interface Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{CLK}	BCL clock frequency	128	-	2048	kHz
t_{CLKH}	BCL clock high	220	-	-	ns
t_{CLKL}	BCL clock low	220	-	-	ns
$t_{SYNCSET}$	Sync setup time for short sync (master mode)	200	-	-	ns
	Sync setup time for short sync (slave mode)	20	-	-	ns
$t_{SYNCHOLD}$	Sync hold time for short sync (master mode)	200	-	-	ns
	Sync hold time for short sync (slave mode)	20	-	-	ns
$t_{CLKSYNC}$	Delay time from clock to long sync	-	-	15	ns
t_{SYNCTX}	Delay time from long sync to TX (slave mode)	-	-	20	ns
t_{CLKTX}	Delay time from clock edge to TX for short sync	-	-	20	ns
$t_{ENDSYNC}$	Delay time from BCL to long sync low after LSB	20	-	-	ns
t_{HIZOUT}	Delay time from LSB of TX to Hi-Z state	20	-	-	ns
t_{SETUP}	Set-up time for RX	20	-	-	ns
t_{HOLD}	Hold time for RX	20	-	-	ns

VOICE CODEC PROTOCOL

The serial interface protocol for the voice codec supports both single word per frame and multiple words per frame time-division multiplexed (TDM) modes, and can be used in either master or slave mode. Master mode is selected by setting the VCEMASTEN bit. In master mode, the voice codec generates the bit clock and frame sync signals, as long as the VCECLKEN bit is set. The data is transmitted and received in a two's complement format, MSB first, and can be clocked on the positive or negative edge of the bit clock. The active edge of the bit clock can be selected by the VCEBCLINV bit. The interface can operate with a short (bit

length) or a long (word length) frame sync, which is selected by the VCELONGFS bit. The frame sync can also be inverted by setting the VCEFSINV bit.

The interface supports 1, 2, or 4 time slots per frame for Tx and Rx. The active slots used by the voice CODEC are controlled by the VCETXSLOT[1:0] and VCERXSLOT [1:0] bits. The short frame sync occurs 1 bit clock cycle before the data MSB, whereas the long frame sync is aligned with the MSB. For multiple time slots, an optional turn around time delay of 1 bit clock cycle can be added in between the slots by setting the VCETRNARND bit. Outside of the assigned time slot, the transmit data line is tri-stated. The tri-state enable can be controlled by the VCETSB bit. The word length is controlled by the VCEWORDLEN[2:0] bits and the bit clock frequency is set with the VCECLKFRQ[2:0] bits.

In practice, only certain modes, defined as modes 1-3 and modes 5-6 will be used for the voice codec. The timing diagrams for these modes are given in Figure 68 and Figure 69. Note that where the TX1 line is shown at Hi-Z, the TX1 driver of the voice codec port is tri-stated and the TX1 line itself may be driven by another device in the application.

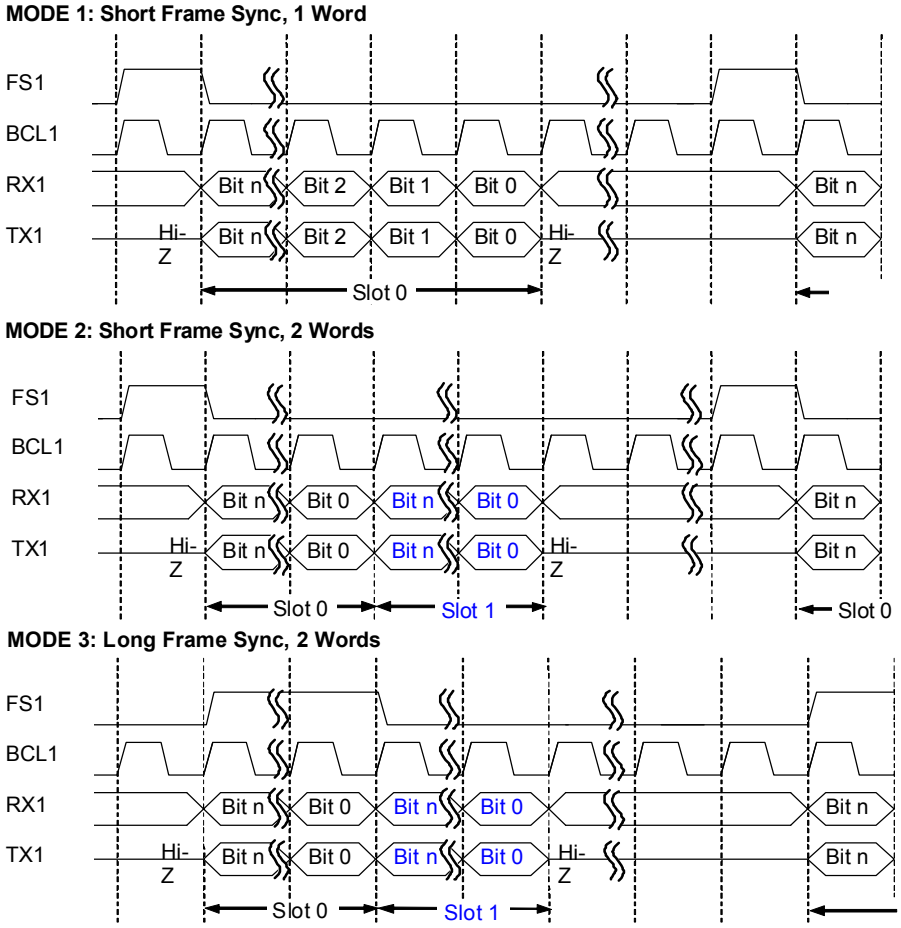

Figure 68. Voice CODEC Serial Interface Timing Diagram Modes 1-3

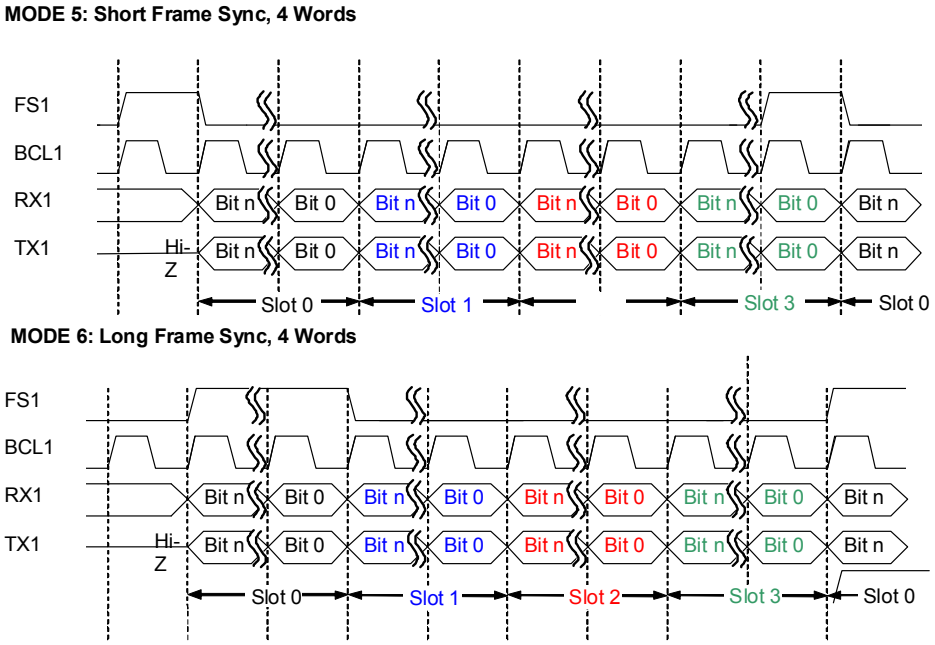

Figure 69. Voice CODEC Serial Interface Timing Diagram Modes 5-6

STEREO DAC AND ADC PROTOCOL

The serial interface protocol for the audio data uses either the I^2S standard, Left-Justified or EIAJ Right-justified formats, and can be used in either master or slave mode. Master mode is selected by setting the STRMASTEN bit. In master mode, the stereo codec generates the bit clock and frame sync signals, as long as the STRCLKEN bit is set. The data is transmitted and received in a two's complement format, MSB first, and can be clocked on the positive or negative edge of the bit clock. The active edge of the bit clock can be selected by the STRBCLINV bit.

The interface operates with a long (word-length) frame sync, which also identifies left vs. right stereo channel words. In I^2S mode, the frame sync leads the data MSB by 1 bit clock cycle, while in Left-justified mode the frame sync is aligned with the MSB of the data, and in Right-justified mode the frame sync is aligned with the LSB of the data. The mode is selected with the STRMODESEL bits. Note that in all modes, the left channel word is sent in the first half of the frame and the right channel word is sent in the second half of the frame. Supported word lengths are 16 to 32 bits. The word length is set with the STRWORDLEN[2:0] bits and the bit clock frequency is set with the STRCLKFRQ[2:0] bits. The frame sync can also be inverted by setting the STRFSINV bit. The tri-state enable can be controlled by the STRTSB bit.

The timing diagrams for these modes are given in Figure 70.

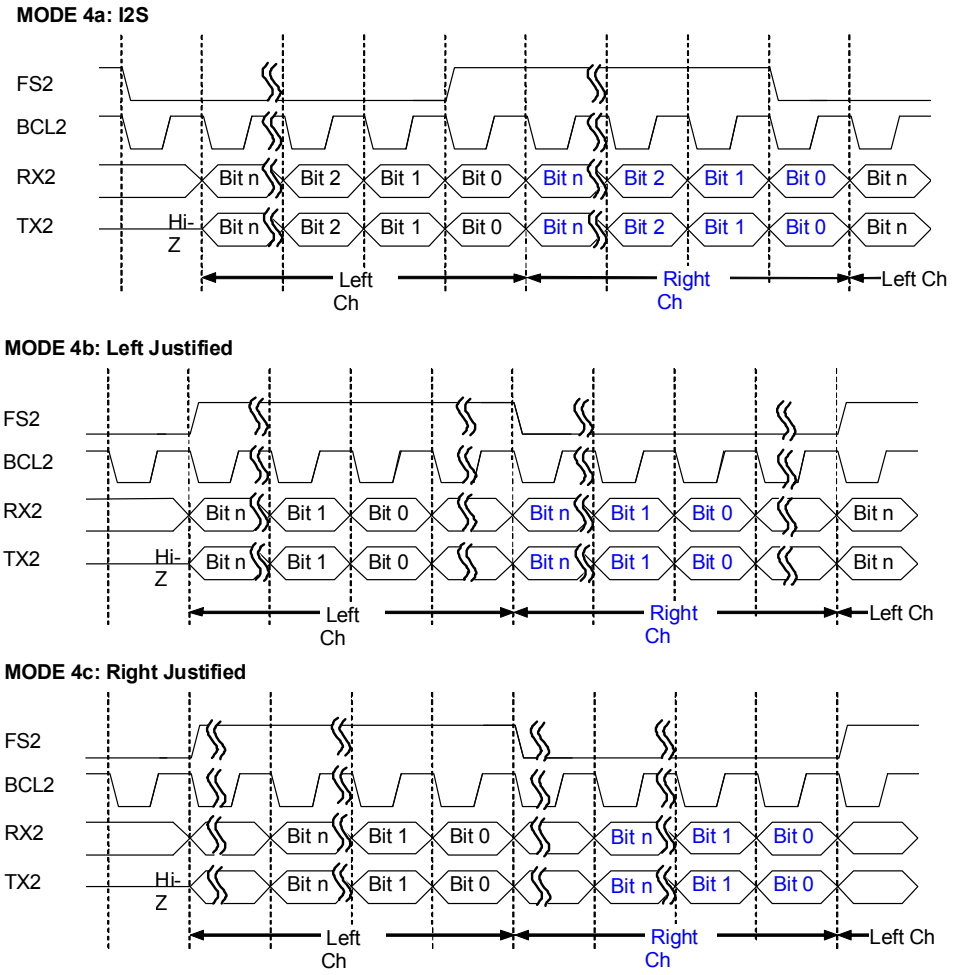

Figure 70. Stereo CODEC Serial Timing Diagram Examples, Mode 4

VOICE CODEC

The voice CODEC is based on two 14-bit A/D converters and a 14-bit D/A converter with integrated filtering. It supports several different clocking modes. The voice codec is supplied by V_{CORE} for its analog and $V_{COREDIG}$ for its digital sections. The analog is using the REFC bias and the half rail bias at REFA.

A/D CONVERTERS

The A/D portion of the voice CODEC consists of two A/D converters which convert the incoming analog audio signals coming from the microphone amplifiers into 14-bit linear PCM words at a rate of 8.0 kHz or 16 kHz. Following the A/D conversion, the audio signal is digitally band pass filtered. The A/D is enabled by setting the VCEADCEN bit. The sampling rate is set by the VCE8K16K bit.

Table 84. Voice CODEC A/D Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Input Range	0 dBFS (21)		1.36		V_{PP}
Absolute Gain	1.02 kHz, 0 dB Gain	-1.0		1.0	dB
PSRR	Relative to BP	80	90		dB_P
THD+N	1.02 kHz, 0 dBm0(22)			-60	dB_P
Idle Channel Noise	0 dB Gain		-78		$dBm0_P$
Intermodulation Distortion	SMTPE method 50 Hz/1020 Hz, 4:1 0 dBm0 total input level			-40	dB

Table 84. Voice CODEC A/D Performance Specifications

Crosstalk A/D to D/A	A/D 1.02 kHz, 0 dBm0, D/A 1.02 kHz, 0 dBm0 referred			-60	dB
Enable Time	Including filters		3.0		ms
FILTERING					
Pass Band		0.4535*FS			Hz
Pass Band Ripple		-0.5		0.5	dB
Stop Band				0.56*FS	Hz
Stop Band Attenuation		60			dB
Group Delay			1.7/FS		s

Notes
21. Equivalent to +3.0 dBm0
22. Equivalent to 340 mVrms

D/A CONVERTER

The D/A portion of the voice CODEC converts 14-bit linear PCM words entering at a rate of 8.0 kHz and 16 kHz into analog audio signals. Prior to this D/A conversion, the audio signal is digitally band-pass filtered. An optional high-pass filter can also be enabled by setting the VCEAUDHPF bit. The D/A is enabled by setting the PSCNTRX bit.

Table 85. Voice CODEC D/A Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Output Range	0 dBFS [23]		2.0		V_{PP}
Absolute Gain	1.02 kHz, 0 dB Gain	-1.0		1.0	dB
PSRR	Relative to BP	80	90		dBA
THD+N	1.02 kHz, 0 dBm0 [24]			-65	dBA
Idle Channel Noise	0 dB Gain		-90		dBm0A
Intermodulation Distortion	SMTPE method 50 Hz/1020 Hz, 4:1 0 dBm0 total input level			-40	dB
Crosstalk A/D to D/A	A/D 1.02 kHz, 0dBm0, D/A 1.02 kHz, 0dBm0 referred			-60	dB
Enable Time	Including filters		3.0		ms
FILTERING					
Pass Band		0.4535*FS			Hz
Pass Band Ripple		-0.5		0.5	dB
Stop Band				0.5465*FS	Hz
Stop Band Attenuation		60			dB
Group Delay			2.3/FS		s

Notes
23. Equivalent to +3.0 dBm0
24. Equivalent to 500 mVrms

STEREO CODEC

The stereo CODEC is based on two 16-bit A/D converters and two 24-bit D/A converters. It supports several different clocking modes. The stereo DAC and ADC are supplied by VCORE for its analog and VCOREDIG for its digital sections. The voice ADC and the stereo ADC use the same converter cores, so both cannot be used at the same time. The analog circuits use the REFD bias and the half rail bias at REFA. The stereo converters incorporate a PLL to generate the proper clocks. The PLL does not require any external filtering.

Both the stereo ADC and stereo DAC will always operate at the same sample frequency using the same digital interface bus. The stereo DAC can be operated in parallel to

the voice DAC, and their sampling rates are independent. The stereo ADC and DAC sampling rate is set by the STRSR[3:0] bits or may optionally be automatically detected in slave mode by setting the STRSRDET bit.

The audio CODEC supports the sampling frequencies of 8.0, 11.025, 12, 16, 22.05, 24, 26, 32, 44.1, and 48 kHz

D/A CONVERTERS

The stereo DAC is based on a 24-bit linear left and right channel D/A converter with integrated filtering. The stereo DAC is enabled by setting the PSCNTDA bit.

Table 86. Stereo DAC Main Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Output Range	0 dBFS (25)		2		V_{PP}
Absolute Gain	1.02 kHz, 0 dB gain	-0.5		+0.5	dB
PSRR	Relative to BP	90			dBA
THD+N	1.02 kHz, 0 dBm0 (26)		-85	-80	dBA
Dynamic Range	1.02 kHz	92	96		dBA
Signal to Noise Ratio	1.02 kHz	94	100		dBA
Intermodulation Distortion	SMTPE method 50 Hz/1020 Hz, 4:1 0 dBm0 total input level			-75	dB
Channel Separation				-75	dB
Enable Time	Including filters		3		ms
FILTERING					
Pass Band		0.4535*FS			Hz
Pass Band Ripple		-0.5		0.5	dB
Stop Band				0.5465*FS	Hz
Stop Band Attenuation		85			dB
Phase Linearity	In pass band	-15		+15	°

Notes
25. Equivalent to +3.0 dBm0
26. Equivalent to 500 mVrms

A/D CONVERTER

The stereo ADC is based on a 16-bit linear left and right channel A/D converter with integrated filtering. The stereo ADC is enabled by setting the STRADCEN bit. If the VCEADCEN bit is also set, it will take priority, so the ADC converters will be used in voice mode.

Table 1. Stereo ADC Main Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Input Range	0 dBFS (27)		2		V_{PP}
Absolute Gain	1.02 kHz, 0 dB gain	-0.5		+0.5	dB
PSRR	Relative to BP	80	90		dBA
THD+N	1.02 kHz, 0 dBm0 (28)		-83		dBA
Dynamic Range	1.02 kHz		90		dBA
Signal to Noise Ratio	1.02 kHz		90		dBA
Intermodulation Distortion	SMTPE method 50 Hz/1020 Hz, 4:1 0 dBm0 total input level			-75	dB
Channel Separation				-75	dB
Enable Time	Including filters		3		ms

Table 1. Stereo ADC Main Performance Specifications

FILTERING					
Pass Band		0.4535*FS			Hz
Pass Band Ripple		-0.5		0.5	dB
Stop Band				0.56*FS	Hz
Stop Band Attenuation		60			dB
Phase Linearity	In pass band	-15		+15	°

Notes
27. Equivalent to +3.0 dBm0
28. Equivalent to 500 mVrms

AUDIO TRANSMIT SECTION

Shown in Figure 71 is a schematic representation of the audio transmit section. The actual design implementation may differ.

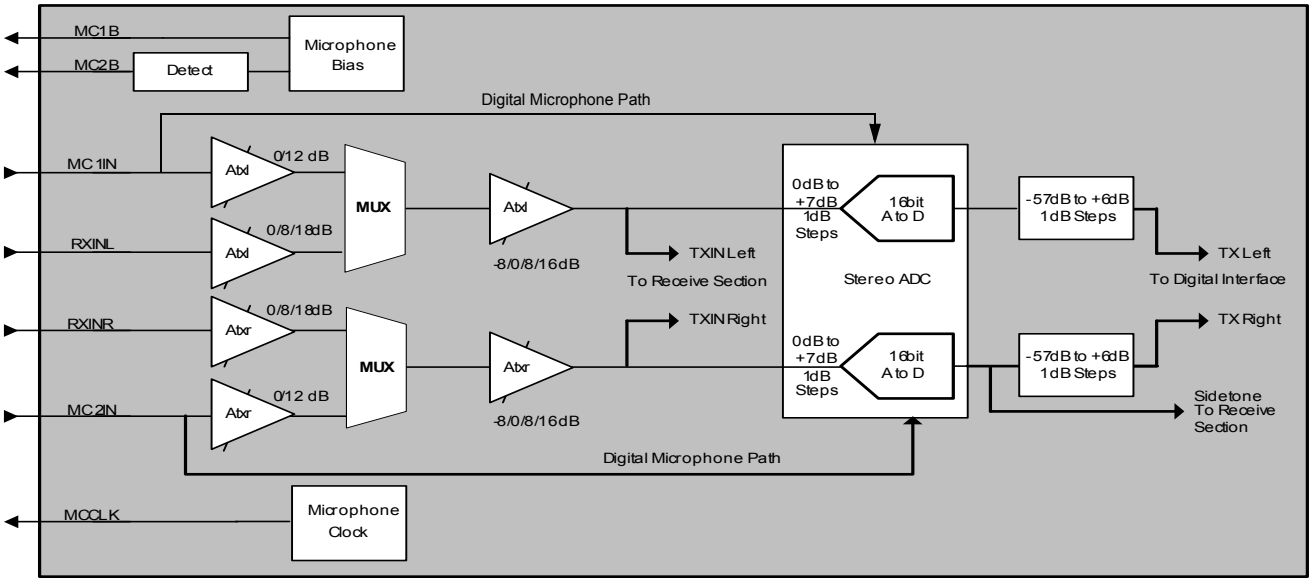

Figure 71. Audio Transmit Section

MICROPHONE BIAS

Two microphone bias circuits are provided. The microphone supplies can be used to supply digital microphones and electret microphones. In the latter case, an external sensitivity setting resistor needs to be added. The bias is enabled by setting respectively the MIC1BIAS and MIC2BIAS bit.

Table 87. Microphone Bias Parametric Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Microphone Bias Output Voltage	C_{LOAD}<100 pF	2.00		2.20	V
Microphone Bias Current			200		µA
Output Current Capability	Source only	1000			µA
PSRR	Relative to BP, 217 Hz	100			dB
Output Noise				2.5	µVrmsp
Microphone Detect Voltage	MC2BEN=0	0.4			V

Table 87. Microphone Bias Parametric Specifications

Microphone Detect Current Low	MC2BEN=1			50	µA
Microphone Detect Current High	MC2BEN=1 (29)	500		650	µA

Notes
29. For proper detection it is advised to use a microphone bias resistor not exceeding 2.7 kΩ

In case the supply voltage level is thought to be insufficient for digital microphones, the supply at MC1B can be raised from 2.1 to 2.7 V by setting the MIC1BIASMOD bit. However in this case, the output supply is no longer low noise. Raising the supply at MC1B has no effect on the output voltage at MC2B.

The microphone bias MC2B has an integrated accessory detection circuit for headphones, headset/microphone presence and for a button operation placed in parallel to the microphone. In order to operate properly, the headset must connect the microphone ring of the jack to the ground jack, in case no microphone is present. Accessory attach/detach events and headset button pushes are all debounced by 30 ms.

The accessory detect circuit can be enabled independently from the microphone or audio bias by setting the HSDETEN bit. When the audio bias and mic bias are both off, only the connection or disconnection of an accessory can be detected, not the specific type of accessory. In this mode, it is assumed that the accessory is a stereo headphone and the HPDET interrupt, which is sensitive to both edges, reflects attach and detach events. The HPDET interrupt can be masked by setting the MHPDET mask bit. Masking the interrupt does not prevent the interrupt from appearing in the interrupt registers, but prevents the PMICINT pin from asserting a hardware interrupt.

When the audio bias and MIC2 bias are enabled, the accessory detect circuit can distinguish between a stereo headphone (low-impedance), a headset microphone (medium-impedance), a headset button push (low-impedance) and connect/disconnect events. For headset button pushes, the circuit also distinguishes between momentary button pushes of less than 2 seconds duration and long button pushes of more than 2 seconds duration.

With audio bias and MIC2 bias enabled, connecting or disconnecting a headphone will assert the HPDET interrupt. Connecting a headset will assert the HSDET interrupt. Pushing the headset button and releasing it within 2 seconds will assert the SWMPINT (switch momentary push) interrupt and pushing the button and releasing it after more than 2 seconds will assert the SWLPINT (switch long push) interrupt. Each of these interrupts also has a corresponding mask bit. Note that if a headphone was detected and was later determined to be a headset, the HPDET interrupt will be cleared and the HSDET interrupt will be set. This situation can occur in two ways: (1) if the audio bias and MIC2 bias were off when the headset was connected, it will be detected as a headphone. If the biases are then turned on, the circuit will recognize that the accessory is actually a headset and will update the interrupts accordingly; (2) if the headset button was being pushed while the headset was being plugged into the jack, it will appear to be a low-impedance accessory and will be detected as a headphone. When the button is finally released, the circuit will recognize that the accessory is actually a headset and will update the interrupts accordingly.

TRANSMIT INPUTS

The transmit inputs accept signals from a low level signal electret microphone as well as high signal level MEMS based microphones. In addition, it allows connecting a digital microphone. Finally, it allows on chip routing from the stereo line-in inputs.

The microphone input amplifiers are enabled by setting the PSCNTMIC1 and PSCNTMIC2 bits. The right channel input is selectable between a microphone connected to MC2IN and the line input RXINR by setting the RAMPSEL bit. The left channel input is selectable between a microphone connected to MC1IN and the line input RXINL by setting the LAMPSEL bit. Note that the input signals must be AC coupled. When in voice mode, (PCM1) MC1IN or RXINL is sent to the left and right channels by default, depending on the PSCNTMIC1 and LAMPSEL bits. In order to send MC2IN or RXINR to the left and right channels when in voice mode, the MC1IN amplifier must be disabled by setting PSCNTMIC1IN=0.

When in stereo mode, the audio signal from MC1IN, RXINL, or digital microphone on the MC1IN pin, is sent exclusively to the left channel of PCM2 data. When in stereo mode, the audio signal from MC2IN, RXINR, or digital microphone in MC2IN pin, is sent exclusively to the right channel of PCM2 data, as shown in Figure 71. When in voice mode, the active transmit input signal is sent to the left and right channels, except for the digital microphone on MC1IN, which is not supported in voice mode.

The MC2IN input is amplified by the ATXR pre-amplifier with course gain setting controlled with MIC2PRE[1:0]. The input amplifiers can also be muted by setting the RAMPMUT bit. The selected signal can be routed to the receive section and it can be converted by the ADC right channel. The ADC gain can be adjusted with the VCEPGATX[4:0] bits. Before transmitting to the digital serial interface, the volume of the digitized signal can be controlled with a fine gain setting through RAMPVL[5:0].

The MC1IN input is amplified by the ATXL pre-amplifier with course gain setting controlled with MIC1PRE[1:0]. The input amplifiers can also be muted by setting the LAMPMUT bit. The selected signal can be routed to the receive section and it can be converted by the ADC left channel. The ADC gain can be adjusted with the VCEPGATX[4:0] bits. Before

transmitting to the digital bus interface, the volume of the converted signal can be controlled with a fine gain setting through LAMPVL[5:0].

Table 88. Transmit Amplifiers Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Gain Accuracy		-0.5		+0.5	dB
Amplifier Bias Current			200		μA
Crosstalk Between Inputs				-60	dB
PSRR	Relative to BP, 217 Hz	90			dB
THD	MC1IN, 1.02 kHz, 10 mVrms			-60	dB
Input Noise	Referred to REFA			1.5	μVrmsp

Digital microphones can be connected to the MC1IN and MC2IN inputs. The digital microphone is supplied from the microphone bias and clocked through the microphone clocking output, MCCLK. The resulting Pulse Density Modulated signal from the digital microphone is directly routed to the filter section of the ADC.

If a single digital microphone is used in the application, it should be connected to MC2IN, and PCM1 voice mode should be used in order to get the same data in the left and right channels. If PCM2 stereo mode is used, the digital microphone on the MC2IN signal is sent on the right channel of PCM1 data only. Voice mode is not supported for the digital microphone connected to the MC1IN pin.

If two digital microphones (dual dmics) are used in the application, PCM2 stereo mode must be used. In dual digital microphone mode, DMIC1 (MC1IN) data and DMIC2 (MC2IN) data is sent to the left and right channels of PCM2, respectively.

The MCCLK signal is enabled by setting the DMICCLKEN bit, and its frequency is selectable between 1.0 MHz and 2.0 MHz by setting the DMICCLK[0] bit. The exact clock frequency will vary as a function of the ADC sample rate. The MC2IN input is configured for digital microphone use by setting the MUXIN bit. Both the clock and the data stream are referenced with respect to MC2B. The gain of the digital microphone data to the digital serial interface can be controlled with the DMICVOL[5:0] bits. The signal from the digital microphone can be routed into the receive voice DAC path as a side tone, by clearing the DMICMUTFB bit, and its gain can be controlled with the DMICVLFB[5:0] bits. The digital mic data to the digital serial interface can be muted with the DMICMUT bit and the digital mic data to the voice DAC can be muted with the DMICMUTEFB bit.

The data routed to the PCM1 digital serial interface is selectable between the digital mic, and the right channel ADC by the PCM1RCH bit. Similarly, the data routed to the PCM2 digital serial interface is selectable between the digital mic and the left channel ADC, by the PCM2LCH bit, and is selectable between the digital mic and the right channel ADC by the PCM2RCH bit

Table 89. Transmit Gain Control

Gain and Volume Setting for Bits RAMPVL[5:0], LAMPVL[5:0]	Gain and Volume Setting DMICVOL[5:0]	Gain	Units	Gain and Volume Setting for Bits MIC1PRE[1:0], MIC2PRE[1:0] *	Gain Mic / RXin	Units
000000	111111	-57	dB	00	0 / 0	dB
000001	111110	-56	dB	01	12 / 8	dB
…	…	…	…	10	20 / 18	dB
111001 (default)	000110	0	dB	11	28 / 26	dB
…	…	…	…	* These gain settings are obtained by a combination of the 0/+12 dB, 0/+8/+18 dB and -8/0/+8/+16 dB. The 0 dB to +7.0 dB settings in the ADC are not used		
111110	000001	+5	dB			
111111	000000	+6	dB			

AUDIO RECEIVE SECTION

The block diagram of the audio receive section is shown in Figure 72.

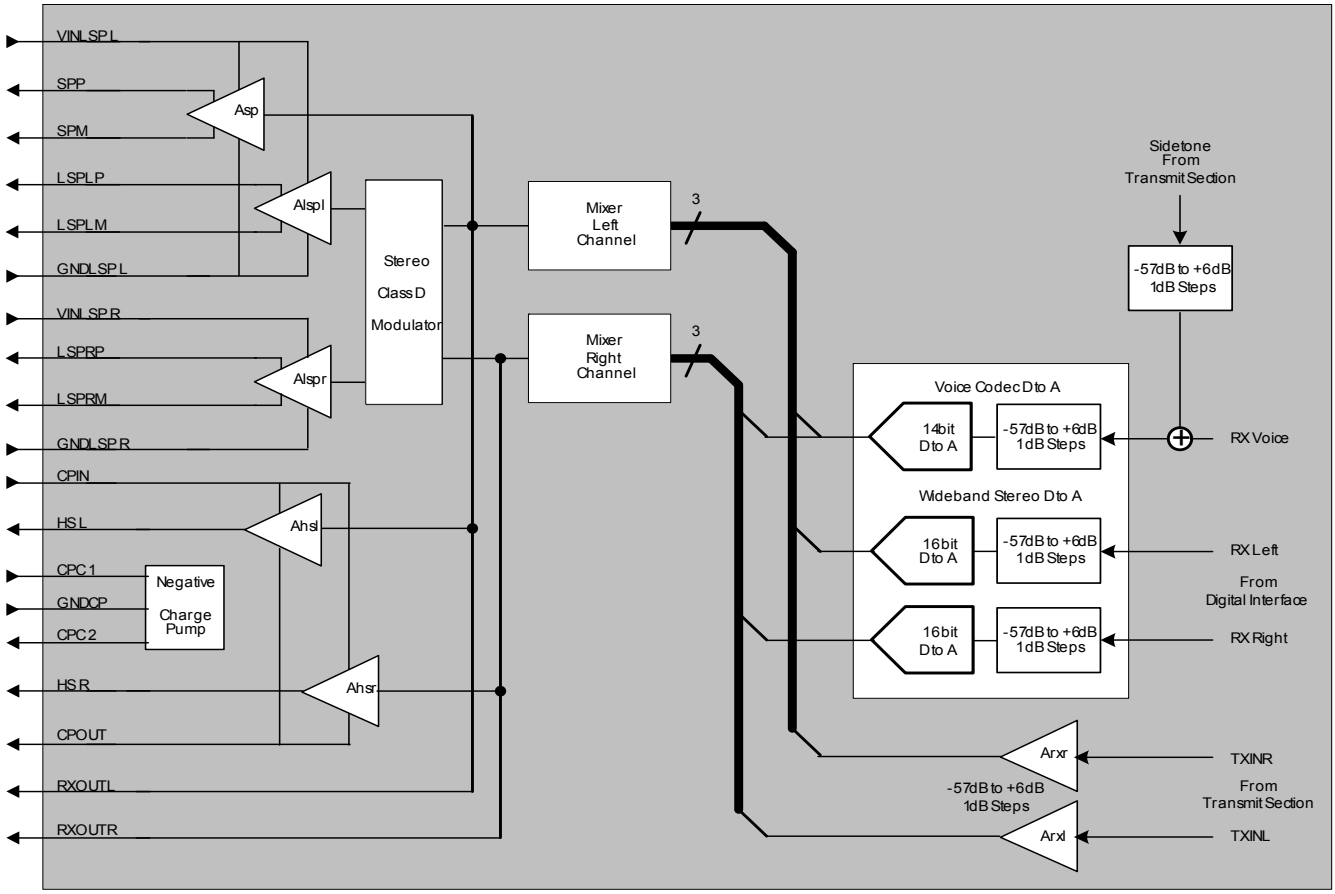

Figure 72. Audio Receive Section Diagram

GAIN CONTROL, MONO ADDER AND ROUTER

The gain of the digital audio in both left and right channels is controlled in the programmable digital gain amplifiers. To facilitate programming, independent settings are available for the voice call and stereo audio use cases through VDACVL[5:0], ADACVLR[5:0] and ADACVLL[5:0] respectively. The gain of the feedback path of the digital microphone can be set through DMICVLFB[5:0]. The gain of the analog audio from RXINR and RXINL or pre-amplified microphone inputs is controlled through the RAMPVLFB[5:0] and LAMPVLFB[5:0] bits. All the gain settings have the same granularity and range.

Table 90. Receive Gain Control

Gain and Volume Setting Bits xxx[5:0]	Gain	Units
000000	-57	dB
000001	-56	dB
…	…	…
111001 (default)	0	dB

Table 90. Receive Gain Control

…	…	…
111110	+5	dB
111111	+6	dB

The signal paths can be muted through the VMUTL, AMUTL, AMUTR bits. The muting of analog inputs is described in the transmit section.

The analog signal from the stereo DAC, the voice DAC, and the transmit section can be mixed; the left channels and voice DAC on the left channel mixer through MXLAUDL, MXLLINL, and MXLMNDAC. The right channels and voice DAC on the right channel mixer through MXRAUDR, MXRLINR, and MXRMNDAC. The resulting mixed analog signal is routed to the different output amplifiers.

EAR PIECE SPEAKER AMPLIFIER ASP

The left channel audio can be routed to the Asp amplifier, which drives the ear piece of the application in a bridge tied load configuration. The amplifier is supplied from the battery

power which avoids the use of an intermediate regulator stage. Its output is referenced with respect to REFA. The feedback network is fully integrated. The amplifier is enabled by setting the PSCNTSPKR bit, with the output signal muted by setting the MUTASP bit.

Table 91. Amplifier Asp Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Differential Output Swing		4.0			Vpp
Gain	SPP-SPM	9.5	10	10.5	dB
Amplifier Bias Current			1.75		mA
THD	Output 4.0 V_{PP}			-60	dB
PSRR	Relative to BP	90			dBA
Noise	Input referred			8.0	μVrmsA
Startup Time			100		μs
Isolation	Not routed	80			dB
Load-impedance	Resistance Inductance Capacitance	25.6	32	 1.0 100	Ω mH pF

LOUDSPEAKER AMPLIFIERS ALSPR AND ALSPL

The Class-D loudspeaker amplifiers Alspr and Alspl drive a set of low ohmic loudspeakers for speakerphone, ringing and music playback modes. The amplifiers are powered directly by the main battery and include a feedback system in order to reach a high PSRR performance. The amplifiers run at a frequency around 3.0 MHz. The outputs are half rail referenced. The feedback networks of the Alsp amplifiers are fully integrated. The right channel amplifier is enabled by setting the PSCNTSPR bit, the left channel amplifier by the PSCNTSPL bit. When enabled, the right and left channel audio paths are routed to their respective amplifiers. The output signal can be muted by setting the MUTSPKR and MUTSPKL bits.

Table 92. Amplifier Alspr and Alspl Class D Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Differential Output Power	BP = 3.4 V in 8.0 Ω BP = 3.6 V in 4.0 Ω	500 1.0	- -	- -	mW W
Gain	LSPxP-LSPxM	10.6	-	11.6	dB
THD	500 mW			-50	dB
PSRR	Relative to BP	75			dBA
Noise	Input referred			50	μVrmsA
Startup Time			1.0		ms
Isolation	Not routed	80			dB
Load-impedance		3.2	8.0		Ω

HEADSET AMPLIFIERS AHSR AND AHSL

The Ahsr and Ahsl amplifiers are dedicated for driving a stereo headset, the Ahsr for the right channel and Ahsl for the left channel. The feedback networks are fully integrated. The amplifiers are enabled by setting the PSCNTLHPR and PSCNTLHPL bits respectively. When enabled, the right channel audio is routed to the HSR output and the left channel audio to the HSL output. The output signal can be muted by setting the MUTHPR and MUTHPL bits.

Table 93. Amplifiers Ahsr and Ahsl Performance Specifications

Parameter	Condition (30)	Minimum	Typical	Maximum	Units
Single Ended Output Swing	In 32 Ω	2.0	-	-	V_{PP}
Gain		-0.5	0	0.5	dB

Table 93. Amplifiers Ahsr and Ahsl Performance Specifications

Amplifier Bias Current	Per Channel from CPIN	-	750	-	μA
THD	Output 2.0 V_{PP}, 32Ω	-		-60	dB
PSRR	Relative to BP	90	-	-	dBA
Noise	Input referred	-	-	8.0	μVrmsA
Startup Time	Including charge pump	-	1.0	-	ms
Isolation	Not routed	80	-	-	dB
Channel Separation		-	-	-75	dB
Load-impedance		12.8	32	-	Ω

Notes
30. Applies for Ahsr and Ahsl activated individually and simultaneously with CPIN=1.8 V

The outputs of the amplifiers are driven relative to true ground, which avoids using coupling capacitors for connecting a headset. The amplifiers are supplied from CPIN = 1.8 V while a single stage negative charge pump provides the CPOUT = -1.8 V supply rail. The charge pump is enabled when one of the headset amplifiers get enabled. The charge pump input pin (CPIN) can be connect to the internal VDDQ buck regulator in the application. In that case, VDDQ must be enabled prior to the headset amplifier, to ensure proper headset operation.

STEREO LINE OUT

The audio can be routed to the line-outs RXOUTR and RXOUTL. These outputs can be used for instance to route the audio to an accessory connected to a bottom connector, such as for a docking station with playback speakers. These outputs are enabled by setting the PCCNTLOR and PSCNTLOL bits.

Table 94. Line Out Performance Specifications

Parameter	Condition	Minimum	Typical	Maximum	Units
Single Ended Output Swing		2.0	-	-	V_{PP}
Gain		-0.5	0	0.5	dB
Amplifier Bias Current	Per channel	-	200	-	μA
THD	Output 2.0 V_{PP}	-	-	-60	dB
PSRR	Relative to BP	90	-		dBA
Noise	Input referred	-	-	10	μVrmsA
Startup Time		-	100	-	us
Isolation	Not routed	80	-	-	dB
Channel Separation		-	-	-75	dB
Load Impedance		10	-	-	kΩ

HEADPHONE/HEADSET DETECTION

The accessory detection of a headset, headphone or a push to talk button switch is done through the MIC2BIAS circuit (MC2B and MC2IN pins) in the 900841. A basic detection that there is an accessory attached to the system is enabled even when MIC2BIAS is off (MIC2BIAS=0) in order to save system power. After a first detection is made, the firmware must enable MIC2BIAS in order to detect what kind of accessory or to detect between long or short button switches.

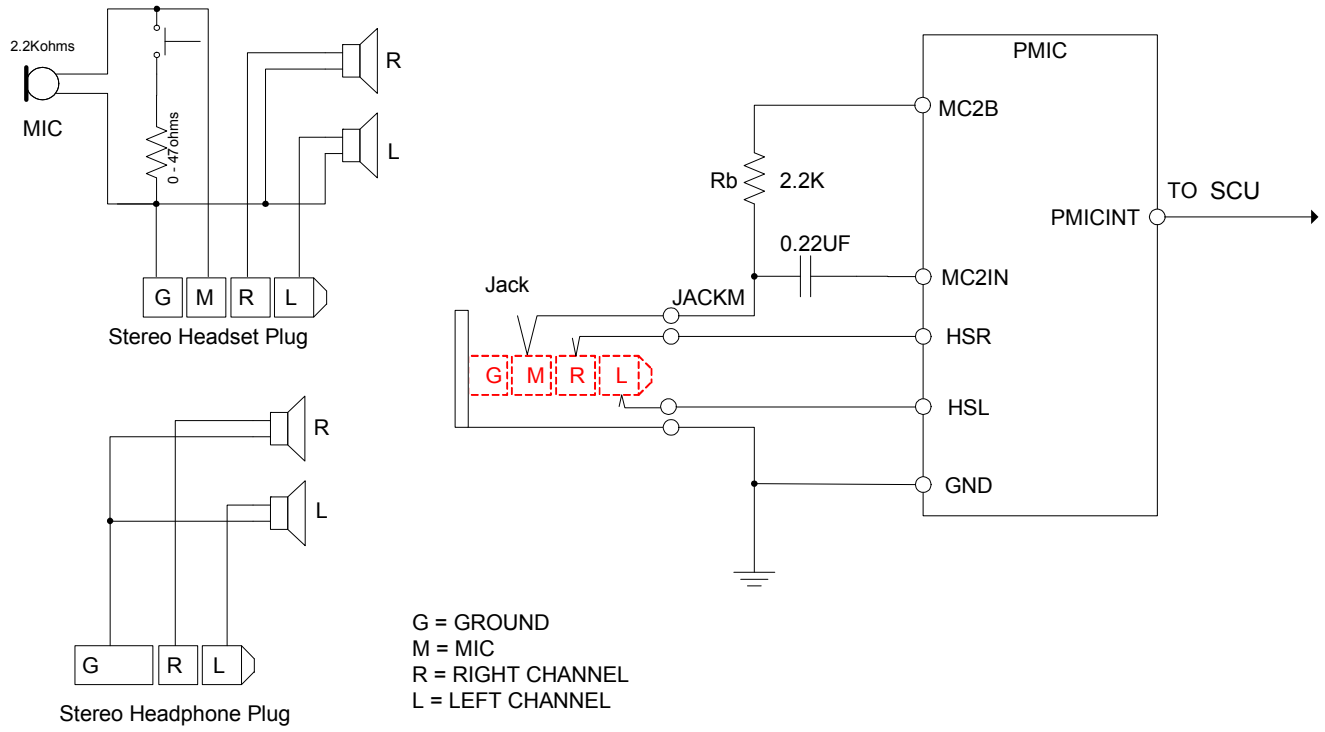

Figure 73. Connection of Audio Accessory Plug to SC900841 Pins

Figure 73 show the connection of an audio accessory plug to the 900841 audio pins.

There are four audio interrupts to distinguish between a headphone, a headset (cellular headset with a microphone), and push-to-talk (PPT) button switch press:

HPDET

- If MIC2BIAS = 0 : Accessory Attached
- If MIC2BIAS = 1 : Headphone Inserted/Removed
  - Detect a 0.4 V threshold in MC2IN when a headphone is inserted / removed
  - Interrupt mask bit: MHPDET (1=masked, 0=unmasked)

HSDET = Headset Inserted/Removed

- Detect current drawing in MC2B pin when headset is inserted/removed
- Interrupt mask bit: MHSDET (1=masked, 0=unmasked)

SWMPINT = Momentary Button Press

- Detect a short button press of < 2.0 s in headset button.
- Interrupt is set after the button is released
- Interrupt mask bit: MSWMPINT (1=masked, 0=unmasked)

SWLPINT = Long Button Press

- Detect a long button press of > 2.0 s in headset button
- Interrupt is set after the button is released
- Interrupt mask bit: MSWLPINT (1=masked, 0=unmasked)

These four interrupts are Level 2 interrupts that when set will trigger the Level 1 AUX interrupt (MAUX interrupt mask). All the above interrupts must be unmasked (by writing '0' to its respective interrupt mask) to be enabled. A SPI read will clear these interrupts and allow the detection of a following interrupt.

It is important to point out that HSDET and HPDET interrupts are used for insertion and removal of an audio accessory. For example, if a headset is inserted to the audio jack, a HPDET interrupt will be set and that will trigger the AUX interrupt. After the firmware does a SPI read both HPDET and AUX these bits will be automatically cleared ('0') by the PMIC . If the headphone is removed from the jack, HPDET will be set again to indicate that the headphone was removed.

The sequence of events below explains the flowchart in Figure 74 should be followed by software to process and to enable these audio interrupts.

HSDETEN and AUDIOFF spi bits must be both set to '1' to enable the audio accessory detection circuit. All external jack inputs are debounced by 30 Lms.

- The insertion of an accessory in the headphone or headset jack when MIC2BIAS=0 will initially generate an HPDET interrupt independently if there is a headset or a headphone in the jack. The first HPDET interrupt means that an accessory was attached to the jack.
- The software must clear the first HPDET interrupt, and setup MIC2BIAS = 1 and AUDIOFF=0, according to the flowchart to be able to detect between HSDET, HPDET, SWMPINT, and SWLPINT
- Once MIC2BIAS=1, the PMIC is able to detect all four accessory interrupts, depending on the load, voltage, or button press time. After the MIC2BIAS is enabled, a second occurrence of HPDET or HSDET means that the accessory was removed. These two interrupts are sensitive to both edges with a jack insertion or jack removal.

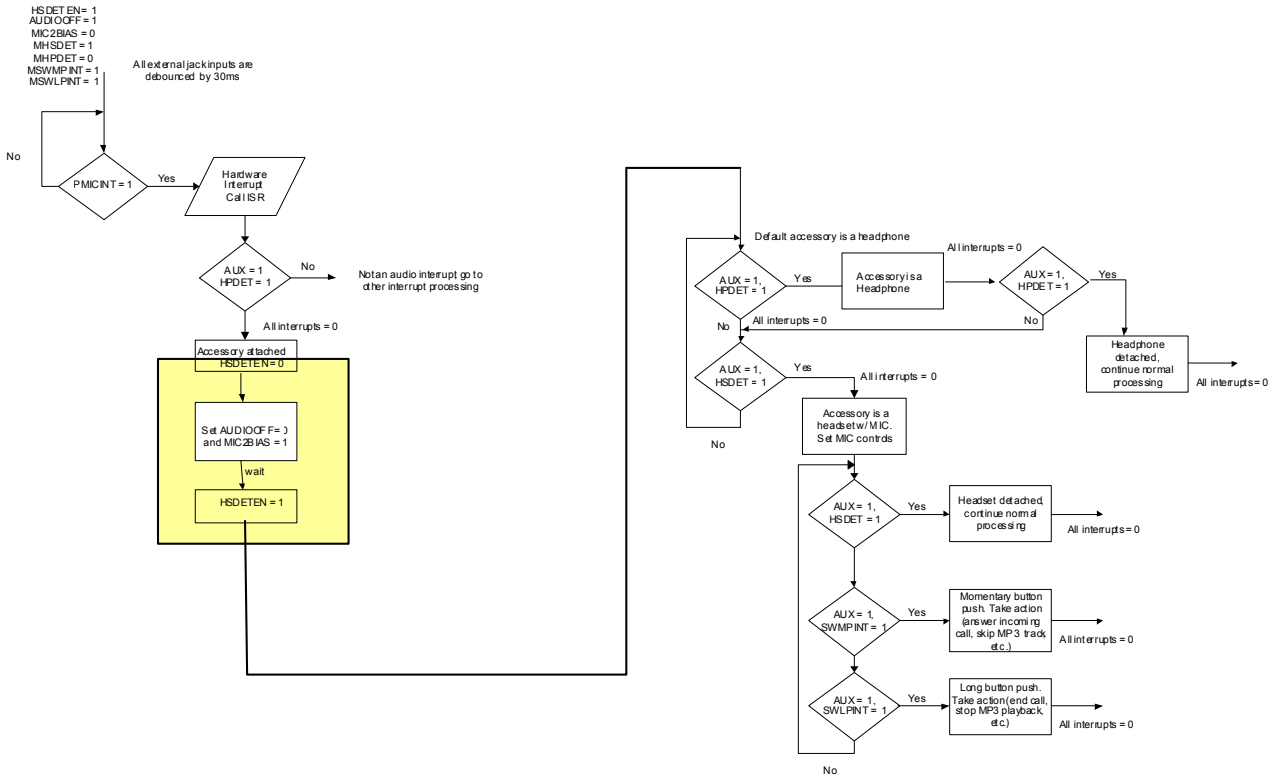

Figure 74. Audio Interrupt Processing FLowchart

AUDIO REGISTERS AND BIT DESCRIPTIONS

Table 95. Audio Registers

Name	Bits	Description
AUD1 (ADDR 0x180 - R/W - Default Value: 0x80)		
VCEWORDLEN	2:0	Number of time slots per frame x0 = 1 Time slot x5 = 2 Time slots x6 = 4 Time slots x1-x4, x7 = Reserved
VCELONGFS	3	Length of frame sync x0 = Bit long x1 = Word long

Table 95. Audio Registers

VCEFSJST	4	Selects left or right justified frame for Mode 3
VCEBCLINV	5	Data clocking x0 = On falling edge BCL1 x1 = On rising edge BCL1
VCEMASTEN	6	Bus operation x0 = Slave mode x1 = Master mode
VCETSB	7	State of TX1 x0 = Tri-stated x1 = Active

AUD2 (ADDR 0x181 - R/W - Default Value: 0x00)

VCERESET	0	Voice ADC / DAC digital filters reset x0 = Self cleared x1 = Reset
VCE8K16K	1	Sample rate voice ADC/DAC x0 = 8.0 kHz x1 = 16 kHz
VCETXSLOT	3:2	Slot assignment voice data x0 = Not active in any slot x1 = Assigned to slot 0 x2 = Assigned to slot 1 x3 = Assigned to slot 2
VCECLKFRQ	6:4	Selects clock speed BCL1 x0 = 2.048 MHz x1 = 256 kHz x2 = 128 kHz x3-x7 = Reserved
VCETRNARND	7	Extra clock cycle inserted between slots x0 = No extra clock cycle x1 = Extra clock cycle

AUD3 (ADDR 0x182 - R/W - Default Value: 0x80)

STRWORDLEN	2:0	Number of time slots per frame	
		x0 = Reserved x1 = 2 Time slots 16 bit significant x2 = 2 Time slots 18 bit significant x3 = 2 Time slots 20 bit significant	x4 = 2 Time slots 24 bit significant x5 = 2 Time slots 28 bit significant x6 = 2 Time slots 32 bit significant x7 = Reserved
RSVD	3	Reserved (not used)	
RSVD	4	Reserved (not used)	
STRBCLINV	5	Data clocking x0 = On falling edge BCL2 x1 = On rising edge BCL2	
STRMASTEN	6	Bus operation x0 = Slave mode x1 = Master mode	
STRTSB	7	State of TX2 x0 = Tri-stated x1 = Active	

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Table 95. Audio Registers

AUD4 (ADDR 0x183 - R/W - Default Value: 0x00)

STRSR	3:0	Sample rate stereo ADC/DAC	
		x0 = 8.0 kHz x1 = 11.025 kHz x2 = 12 kHz x3 = 16 kHz x4 = 22.05 kHz x5 = 24 kHz	x6 = 26 kHz x7 = 32 kHz x8 = 44.1 kHz x9 = 48 kHz xA-xF = Reserved
STRCLKFRQ	6:4	Selects clock speed BCL2 x0 = 32 times FS2 x1 = 64 times FS2 x2 = 128 times FS2 x3-x7 = Reserved	
STRSRDET	7	Sample rate detection x0 = Not enabled x1 = Enabled	

AUD5 (ADDR 0x184 - R/W - Default Value: 0x00)

VCEDLM	0	Voice channel digital loop back mode x0 = normal operation x1 = digital loop back enabled
VCEFSINV	1	Frame sync FS1 polarity inversion x0 = Not inverted x1 = Inverted
VCECLKEN	2	Control FS and BITCLK generation in Master mode x0 = clk gen disabled x1 = clk gen enabled
VCEAUDHPF	3	Voice DAC high pass filter x0 = Disabled x1 = Enabled
VCERXSLOT	5:4	Selects which slot will be used to receive PCM data
Reserved	7:6	Reserved

AUD6 (ADDR 0x185 - R/W - Default Value: 0x00)

STRMODESEL	1:0	PCM2 mode select x0 = I^2S mode x1 = Left-justified x2 = Right-justified x3 = Reserved (defaults to right-justified)
VCE2PCM2	2	Send voice data to PCM2 when '1'
STRMONO	3	Digitally mix ADC input to both left and right channels
Reserved	4	Reserved
STRFSINV	5	Frame sync FS2 polarity inversion x0 = Not inverted x1 = Inverted

Table 95. Audio Registers

STRCLKEN	6	Enable fsync and bitclk generation in master mode x0 = clk gen disabled x1 = clk gen enabled
STRRESET	7	Audio ADC / DAC digital filters reset x0 = Self cleared x1 = Reset
AUD7 (ADDR 0x186 - R/W - Default Value: 0x00)		
DMICVOL	5:0	Digital microphone volume
MIC1BIASMOD	6	Microphone bias MC1B operating mode x0 = Electret microphone supply mode x1 = Digital microphone supply mode
Reserved	7	Reserved
AUD8 (ADDR 0x187 - R/W - Default Value: 0x80)		
DMICVOLFB	5:0	Digital microphone volume
DMICMUTEFB	6	Digital microphone side tone path mute x0 = Not muted x1 = Muted
AUDIOOFF	7	Audio bias references on/off control x0 = references enabled x1 = references disabled
AUD9 (ADDR 0x188 - R/W - Default Value: 0x00)		
DMICCLK	1:0	Digital microphone clock speed x0 = Around 1.0 MHz x1 = Around 2.0 MHz x2, x3 = Reserved
PCM1RCH	2	Voice interface TX1 right channel selector x0 = ADC right x1 = Digital microphone input
RSVD	3	Reserved (not used)
MIC2BIAS	4	Microphone bias MC2B enable x0 = Not enabled x1 = Enabled
DMICMUTE	5	Digital microphone mute x0 = Not muted x1 = Muted
MIC1BIAS	6	Microphone bias MC1B enable x0 = Not enabled x1 = Enabled
DMICCLKEN	7	Clock for digital microphone x0 = Disabled x1 = Enabled

Table 95. Audio Registers

AUD10 (ADDR 0x189 - R/W - Default Value: 0x00)

LAMPVL	5:0	Left transmit amplifier volume control	
LAMPMUT	6	Left transmit amplifier signal mute x0 = Not muted x1 = Muted	
LAMPSEL	7	Left transmit amplifier input selection x0 = MC1IN x1 = RXINL	

AUD11 (ADDR 0x18A - R/W - Default Value: 0x00)

RAMPVL	5:0	Right transmit amplifier volume control	
RAMPMUT	6	Right transmit amplifier signal mute x0 = Not muted x1 = Muted	
RAMPSEL	7	Right transmit amplifier input selection x0 = MC2IN x1 = RXINR	

AUD12 (ADDR 0x18B - R/W - Default Value: 0x00)

MIC2PRE	1:0	Preamplifier gain MC2IN input	
MIC1PRE	3:2	Preamplifier gain MC1IN input	
HSDETEN	4	Headset or headphone detect through MC2B detect circuit x0 = Disabled x1 = Enabled	
MUXIN	5	MC1IN Mode select x0 = Analog input x1 = Digital input	
PCM2RCH	6	Audio interface TX2 right channel selector x0 = ADC right x1 = Digital microphone input	
PCM2LCH	7	Audio interface TX2 left channel selector x0 = ADC left x1 = Digital microphone input	

AUD13 (ADDR 0x18C - R/W - Default Value: 0x00)

VCEPGATX	4:0	Volume control of voice ADC	
		x0 = -8.0 dB x1 = -7.0 dB x2 = -6.0 dB x3 = -5.0 dB x4 = -4.0 dB x5 = -3.0 dB x6= -2.0 dB x7= -1.0 dB	x8 = 0 dB x9 = 1.0 dB xA = 2.0 dB xB = 3.0 dB xC = 4.0 dB xD = 5.0 dB xE = 6.0 dB xF = 7.0 dB x10 - x1F = Reserved.
VCECLK	7:5	Selects voice clkin frequency, default is 26 MHz	

Table 95. Audio Registers

AUD14 (ADDR 0x18D - R/W - Default Value: 0x00)		
STRADC16PG	2:0	Audio ADC PGA steps
STRADC16PGEN	3	Enable ADC PGA
STRCLK	6:4	Selects stereo clkin frequency, default is 26 MHz
Reserved	7	Reserved
AUD15 (ADDR 0x18E - R/W - Default Value: 0x00)		
VDACVL	5:0	Voice DAC volume control
Reserved	6	Reserved
VMUT	7	Voice DAC signal mute x0 = Not muted x1 = Muted
AUD16 (ADDR 0x18F - R/W - Default Value: 0x00)		
ADACVLL	5:0	Audio DAC left volume control
Reserved	6	Reserved
AMUTL	7	Audio DAC left signal mute x0 = Not muted x1 = Muted
AUD17 (ADDR 0x190 - R/W - Default Value: 0x00)		
ADACVLR	5:0	Audio DAC right volume control
Reserved	6	Reserved
AMUTR	7	Audio DAC Right signal mute x0 = Not muted x1 = Muted
AUD18 (ADDR 0x191 - R/W - Default Value: 0x00)		
MUTASP	0	Ear piece amplifier signal mute x0 = Not muted x1 = Muted
MUTHPR	1	Headset amplifier right mute x0 = Not muted x1 = Muted
MUTHPL	2	Headset amplifier left mute x0 = Not muted x1 = Muted
Reserved	3	Reserved
MXLAUDL	4	Audio DAC left signal mixing x0 = Not mixed on left mixer x1 = Mixed on left mixer
MXLMNDAC	5	Voice DAC signal mixing x0 = Not mixed on left mixer x1 = Mixed on left mixer
Reserved	6	Reserved
MXLLINL	7	Line in RXINL signal mixing x0 = Not mixed on left mixer x1 = Mixed on left mixer

Table 95. Audio Registers

AUD19 (ADDR 0x192 - R/W - Default Value: 0x00)

Reserved	0	Ear piece amplifier signal mute x0 = Not muted x1 = Muted
MUTSPKRR	1	Loudspeaker amplifier right mute x0 = Not muted x1 = Muted
MUTSPKRL	2	Loudspeaker amplifier left mute x0 = Not muted x1 = Muted
MXRAUDR	3	Audio DAC right signal mixing x0 = Not mixed on right mixer x1 = Mixed on right mixer
Reserved	4	Reserved
MXRMNDAC	5	Voice DAC signal mixing x0 = Not mixed on right mixer x1 = Mixed on right mixer
MXRLINR	6	Line in RXINR signal mixing x0 = Not mixed on right mixer x1 = Mixed on right mixer
Reserved	7	Reserved

AUD20 (ADDR 0x193 - R/W - Default Value: 0x00)

RAMPVLFB	5:0	Transmit right channel side tone volume
Reserved	7:6	Reserved

AUD21 (ADDR 0x194 - R/W - Default Value: 0x00)

LAMPVLFB	5:0	Transmit left channel side tone volume
Reserved	7:6	Reserved

AUD22 (ADDR 0x195 - R/W - Default Value: 0x00)

PSCNTSPKR	0	Ear piece amplifier enabling x0 = Disabled x1 = Enabled
PSCNTHPR	1	Headphone amplifier right enabling x0 = Disabled x1 = Enabled
PSCNTHPL	2	Headphone amplifier left enabling x0 = Disabled x1 = Enabled
PSCNTLOR	3	Line out amplifier right enabling x0 = Disabled x1 = Enabled
PSCNTLOL	4	Line out amplifier left amplifier enabling x0 = Disabled x1 = Enabled
Reserved	5	Reserved

Table 95. Audio Registers

PSCNTSPR	6	Loudspeaker amplifier right enabling x0 = Disabled x1 = Enabled
PSCNTSPL	7	Loudspeaker amplifier left enabling x0 = Disabled x1 = Enabled
AUD23 (ADDR 0x196 - R/W - Default Value: 0x00)		
VCEADCEN	0	Voice ADC enabling x0 = Disabled x1 = Enabled
STRADCEN	1	Audio ADC enabling x0 = Disabled x1 = Enabled
PSCNTMIC2	2	MC2IN amplifier enabling x0 = Disabled x1 = Enabled
PSCNTMIC1	3	MC1IN amplifier enabling x0 = Disabled x1 = Enabled
PSCNTDA	4	Audio DAC enabling x0 = Disabled x1 = Enabled
PSCNTRX	5	Voice DAC enabling x0 = Disabled x1 = Enabled
SLOPESEL	7:6	Voice and audio bus drive strength
AUD24 (ADDR 0x197 - R - Default Value: 0x00)		
SWLPINT	0	Long switch push (> 2.0 sec) interrupt x0 = No long switch push detected x1 = Long switch push detected
SWMPINT	1	Momentary switch push interrupt x0 = No momentary switch push detected x1 = Momentary switch push detected
HPDET	2	Headphone detect interrupt x0 = Headphone detected x1 = No headphone detected
HSDET	3	Headset detect interrupt x0 = No headset detected x1 = Headset detected
Reserved	7:4	Reserved
AUD25 (ADDR 0x198 - R/W - Default Value: 0x00)		
MSWLPINT	0	Long switch push interrupt mask x0 = Long switch push interrupt is unmasked x1 = Long switch push interrupt is masked

Table 95. Audio Registers

MSWMPINT	1	Momentary switch push interrupt mask x0 = Momentary switch push interrupt is unmasked x1 = Momentary switch push interrupt is masked
MHPDET	2	Headphone detect interrupt mask x0 = Headphone detect interrupt is unmasked x1 = Headphone detect interrupt is masked
MHSDET	3	Headset detect interrupt mask x0 = Headset detect interrupt is unmasked x1 = Headset detect interrupt is masked
Reserved	7:4	Reserved
AUD26 (ADDR 0x199 - R/W - Default Value: 0x00)		
TRIMEN	1:0	Enable trim offsets
Reserved	7:2	Reserved

ADC SUBSYSTEM

CONVERTER CORE

The ADC core is a 10 bit converter. The ADC core and logic run at an internally generated frequency of approximately 1.33 MHz. If an ADC conversion is requested while the PLL was not active, it will automatically be enabled by the ADC. A 32.768 kHz equivalent time base is derived from the 2.0 MHz clock to time ADC events. The ADC is supplied from VCORE. The ADC core has an integrated auto calibration circuit which reduces the offset and gain errors.

The ADC will be used for sensing the current through select voltage regulators, touch screen support, PMIC thermal sensor, battery voltage, battery current, battery temperature and for sampling the battery coulomb counter.

Figure 75 is a representation of the ADC block.

Figure 75. ADC Block Representation

INPUT SELECTOR

The ADC has 22 input channels selected through the ADSEL[4:0] bits in the ADCADDRx register. Table 96 gives an overview of the characteristics of each of these channels.

Table 96. ADC Inputs

Channel	SELECT[4:0]	ADC Input Signal	Input Level	Scaling	Scaled Version
0	00000	PMIC Die Temperature	1.2 – 2.4 V	x1	1.2 – 2.4 V
1	00001	VCC Current Sense	0 – 2.4 V	x1	0 – 2.4 V
2	00010	VNN Current Sense	0 – 2.4 V	x1	0 – 2.4 V
3	00011	VCC180 Current Sense	0 – 2.4 V	x1	0 – 2.4 V
4	00100	VDDQ Current Sense	0 – 2.4 V	x1	0 – 2.4 V
5	00101	V33 Current Sense	0 – 1.8 V	x4/3	0 – 2.4 V
6	00110	Battery Voltage (V_{BAT})	0 – 4.8 V	/2	0 – 2.4 V
7	00111	Battery Current ($V_{BAT} – V_{ISNSBATN}$)	-60 – +60 mV (31)	x20	-1.2 – +1.2 V
8	01000	Adaptor Voltage	0 – 20 V	/10	0 – 2.0 V
9	01001	Battery Pack Thermistor	0 – 2.4 V	x1	0– 2.4 V

Table 96. ADC Inputs

Channel	SELECT[4:0]	ADC Input Signal	Input Level	Scaling	Scaled Version
10	01010	General Purpose ADIN10 Touch screen X+	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
11	01011	General Purpose ADIN11 Touch screen X-	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
12	01100	General Purpose ADIN12 Touch screen Y+	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
13	01101	General Purpose ADIN13 Touch screen Y-	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
14	01110	General Purpose ADIN14	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
15	01111	General Purpose ADIN15	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
16	10000	General Purpose ADIN16	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
17	10001	General Purpose ADIN17	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
18	10010	General Purpose ADIN18	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
19	10011	General Purpose ADIN19	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
20	10100	General Purpose ADIN20	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
21	10101	General Purpose ADIN21	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
22	10110	Reserved	Reserved	Reserved	Reserved
23	10111	Reserved	Reserved	Reserved	Reserved
24	11000	Reserved	Reserved	Reserved	Reserved
25	11001	Reserved	Reserved	Reserved	Reserved
26	11010	Reserved	Reserved	Reserved	Reserved
27	11011	Reserved	Reserved	Reserved	Reserved
28	11100	Reserved	Reserved	Reserved	Reserved
29	11101	Reserved	Reserved	Reserved	Reserved
30	11110	Reserved	Reserved	Reserved	Reserved
31	11111	Reserved	Reserved	Reserved	Reserved

Notes
31. Equivalent to -3.0 to +3.0 A of current with a 20 mOhm sense resistor

Some of the internal signals are first scaled to adapt the range to the input range of the ADC. Note that the 10 bit ADC core will convert over the entire scaled version of the input channel, so always from a 2.40 V full scale.

For some applications, an external resistor divider network may be used to scale down the voltage to be measured to the ADC input range. The source resistance presented by this may be greater than the maximum specified Rs, see ADC Section on Table 3. In that case, the readout value will be lower than expected due to the dynamic input impedance of the ADC converter. This readout error presents itself as a gain error which can be compensated for by factory phasing. An alternative is to place a 100 nF bypass capacitor at the ADIN input concerned.

RESERVED CHANNELS POSSIBLE USAGE

Only 22 of the possible 32 ADC channels are currently associated with an specific function. The remaining channels are currently designated as reserved channels for future needs. Table 97 is a proposed usage for some of these channels for additional flexibility.

Table 97. Possible Reserved Channels Usage

Channel	ADC Input Signal	Input Level	Scaling	Scaled Version
22	Application Supply (V_{PWR})	0 – 4.8 V	/2	0 – 2.4 V
23	Reserved	Reserved	Reserved	Reserved

Table 97. Possible Reserved Channels Usage

24	Charger Current ($V_{ISNSBATP} - V_{ISNSBATN}$)	-300 – 300 mV (32)	x4	-1.2– +1.2 V
25	Backup Voltage ($V_{COINCELL}$)	0 – 3.6 V	x2/3	0 – 2.4 V
26	Battery Detect	0 – V_{CORE}	x5/6	0 – 2.31 V
27	Reserved	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved	Reserved
29	Reserved	Reserved	Reserved	Reserved
30	Reserved	Reserved	Reserved	Reserved
31	Reserved	Reserved	Reserved	Reserved

Notes
32. Equivalent to -3.0 to +3.0 A of current with a 100 mOhm sense resistor

Activating the prior channels to provide the signal specified occurs by asserting the following bits to 1. If the following bits are 0, then these channels are reserved:

- VPWRCON for channel 22
- CHRGICON for channel 24
- LICON for channel 25
- BATDETVCON for channel 26

CONTROL

The ADC block consists of a 5-bit wide, 32-entry register file, which stores the address of the analog input for sampling. The 10-bit result is then stored in a separate register file 10+1 bits wide and 32 entries deep.

In order to operate the ADC, it has to be enabled first by setting the ADEN bit high in the ADCCNTL1 register. When the register ADCCNTL1 ADSTRT bit is enabled, the PMIC will cycle through the 3 + 5 bit selector addresses in registers ADCADDRx. The high 3-bits control the touch screen bias FETs, as described in Touch Screen Interface. The lower 5-bits address the ADC selector to connect one of 32 channels to the ADC. The result of the ADC conversion is stored into the result registers (ADCSNSx), along with the input gain setting (1 MSB). An address in the selector table of 0x1F designates the stop location of the selection loop. At which point the interrupt flag bit 0 (RND), which can be masked through the MRND bit in the MADCINT register, is set in register ADCINT, bit 1 of the INTERRUPT register (ADC) is set, and the external PMICINT signal is asserted, if bit 1 of the INTMASK register is clear. The ADC sleeps for 0 to 27 ms as set by ADC register ADCCNTL1 through the ADSLP[2:0] bits and then repeats the selector cycle. The new data overwrites the old in the result registers. At most, all 32 result registers will be filled within 15.625 ms (2048/32 = 1/64 Hz). The result registers will not be read until the RND flag is set.

DEDICATED CHANNELS READING

Two different LSB value settings are possible by using the LSBSEL bit in the FSLADCCNTL register. LSBSEL = 0 is the default setting. See Table 98 for more information

Table 98. ADC LSB Settings

#	SELECT[4:0]	ADC INPUT SIGNAL	SIGNAL RANGE	LSB VALUE (LSBSEL = 0)	LSB VALUE (LSBSEL = 1)
0	00000	PMIC Die Temperature	1.2 – 2.4 V	0.4244 K	1C
1	00001	VCC Current Sense	4.2 A	4.1015 mA	10 mA
2	00010	VNN Current Sense	1.9 A	1.8554 mA	10 mA
3	00011	VCC180 Current Sense	0.5 A	0.4883 mA	10 mA
4	00100	VDDQ Current Sense	1.8 A	1.7578 mA	10 mA
5	00101	V33 Current Sense	1.7 A	1.6602 mA	10 mA
6	00110	Battery Voltage (V_{BAT})	4.8 V	4.6875 mV	10 mV
7	00111	Battery Current ($V_{BAT} - V_{ISNSBATN}$)	6.0 A (-3.0 to 3.0 A)	5.8594 mA	10 mA
8	01000	Adaptor Voltage	24 V	23.4375 mV	10 mV
9	01001	Battery Pack Thermistor	2.4 V	2.3438 mV	10mV

Table 98. ADC LSB Settings

10	01010	General Purpose ADIN10 Touch screen X+	0-200 mV / 0-2.0 V 0 – 1.2	195.3 µV - 1.953 mv 1.17 mV	195.3 µV - 1.953 mv 1.17 mV
11	01011	General Purpose ADIN11 Touch screen X-	0-200 mV / 0-2.0 V 0 – 1.2	195.3 µV - 1.953 mv 1.17 mV	195.3 µV - 1.953 mv 1.17 mV
12	01100	General Purpose ADIN12 Touch screen Y+	0-200 mV / 0-2.0 V 0 – 1.2	195.3 µV - 1.953 mv 1.17 mV	195.3 µV - 1.953 mv 1.17 mV
13	01101	General Purpose ADIN13 Touch screen Y-	0-200 mV / 0-2.0 V 0 – 1.2	195.3 µV - 1.953 mv 1.17 mV	195.3 µV - 1.953 mv 1.17 mV
14	01110	General Purpose ADIN14	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
15	01111	General Purpose ADIN15	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
16	10000	General Purpose ADIN16	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
17	10001	General Purpose ADIN17	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
18	10010	General Purpose ADIN18	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
19	10011	General Purpose ADIN19	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
20	10100	General Purpose ADIN20	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
21	10101	General Purpose ADIN21	0-200 mV / 0-2.0 V	195.3 µV - 1.953 mv	195.3 µV - 1.953 mv
22	10110	Application Supply (V_{PWR})	0 – 4.8 V	4.6875 mV	4.6875 mV
23	10111	Reserved	Reserved	Reserved	Reserved
24	11000	Charger Current ($V_{ISNSBATP}$ – $V_{ISNSBATN}$)	-300– 300 mV (33)	2.9297 mA	2.9297 mA
25	11001	Backup Voltage ($V_{COINCELL}$)	0 – 3.6 V	3.5156 mV	3.5156 mV
26	11010	Battery Detect	0 – V_{CORE}	2.71 mV	2.71 mV
27	11011	Reserved	Reserved	Reserved	Reserved
28	11100	Reserved	Reserved	Reserved	Reserved
29	11101	Reserved	Reserved	Reserved	Reserved
30	11110	Reserved	Reserved	Reserved	Reserved
31	11111	Reserved	Reserved	Reserved	Reserved

Notes
33. Equivalent to -3.0 to +3.0 A of current with a 100 mOhm sense resistor

PMIC DIE TEMPERATURE

The die temperature can be read out on Channel 0 of the ADC. The relation between the read out code and temperature is given in Table 99.

Table 99. PMIC Die Temperature Voltage Reading

Parameter	Typical
Die Temperature Read Out Code at 25°C	1011000001
Temperature change per LSB	+0.4244 °C
Customer Defined LSB Value	1.0000 °C
Multiplier Value for Output Register	x2.36

CURRENT SENSING

The load current sourced by a select set of regulators can be measured and recorded by the ADC on channels 1 through 5. Table 100 shows a summary of these regulators, type, and their current ranges.

Table 100. Regulators Current Sensing

Regulator	Type	Current Range
VCC	Buck	0A – 3.5 A
VNN	Buck	0A – 1.6 A
VCC180	LDO	0A – 0.39 A
VDDQ	Buck	0A – 1.4 A
V33	Buck/Boost	0A – 1.4 A

BATTERY VOLTAGE

The battery voltage is read at the VBAT pin at channel 6. The battery voltage is first scaled by subtracting 2.40 V in order to fit the input range of the ADC.

Table 101. Battery Voltage Reading Coding

Conversion Code	Voltage at ADC input	Voltage at VBAT
1 111 111 111	2.400 V	4.800 V
1 000 010 100	1.250 V	2.500 V
0 000 000 000	0.000 V	0.000 V

BATTERY CURRENT

The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop across the sense resistor between the VBAT and ISNSBATN pins. The battery terminal voltage at VBAT and the voltage difference between VBAT and ISNSBATN are sampled simultaneously, but converted one after the other. This is done to efficiently perform the voltage and current reading at the same time.

The voltage difference between VBAT and ISNSBATN is first amplified to fit the ADC input range as V(VBAT - VISNSBATN)*20. Since battery current can flow in both directions, the conversion is read out in 2's complement format. Positive readings correspond to the current flow out of the battery, and negative readings to the current flowing into the battery.

The value of the sense resistor used, determines the accuracy of the result as well as the available conversion range. Note that excessively high values can impact the operating life of the system, due to extra voltage drop across the sense resistor.

Table 102. Battery Current Reading Coding

Conversion Code	Voltage at ADC input ADC	V_{BAT}-$V_{ISNSBAT}$	Current Through 20 m	Current Flow
0 111 111 111	1200 mV	60.000 mV	3.000 A	From Battery
0 000 000 001	2.346 mV	0.117 mV	0.0059 A	From Battery
0 000 000 000	0.000 mV	0.000 mV	0.000 A	-
1 111 111 111	-2.346 mV	-0.117 mV	0.0059 A	To Battery
1 000 000 000	-1200 mV	-60.000 mV	3.000 A	To Battery

CHARGER INPUT VOLTAGE

One of the spare options is to read the charger voltage measured at the RAWCHG pin at Channel 8. The charger voltage is first scaled in order to fit the input range of the ADC.

Table 103. Charger Input Voltage Reading Coding

Conversion Code	Voltage at ADC input	Voltage at VBAT
1 101 010 100	2.000 V	20.000 V
0 000 000 000	0.000 V	0.000 V

BATTERY THERMISTOR

Channel 9 is used to read out the battery pack thermistor. The thermistor will have to be biased with an external pull-up to a voltage rail greater than the ADC input range. In order to save current when the thermistor reading is not required, the thermistor is biased from VCORE through a cutoff switch connected to VNTC pin. A resistor divider network should assure the resulting voltage falls within the ADC input range.

GENERAL PURPOSE ANALOG INPUTS

There are twelve general purpose analog input channels that can be measured through the ADIN10-ADIN21 pins. Two voltage scaling (gain) settings can be selected to accommodate a wider range of inputs through the ADCCNTL3 and ADCCNTL4 registers. A gain of 0 sets a corresponding scaling factor of 1 (for an input range of 2.0 V) and a gain of 1 sets a corresponding scaling factor of 10 (for an input range of 200 mV).

Table 104. General Purpose Analog Inputs Reading Coding

Conversion Code	Voltage at ADC input	Voltage at ADINx Input	GAIN
1 111 111 111	2.400	0.200	1
1 011 111 111	1.800	0.150	
0 011 111 111	0.600	0.050	
0 000 000 000	0.000	0.000	
1 111 111 111	2.400	2.000	0
1 011 111 111	1.800	1.500	
0 011 111 111	0.600	0.500	
0 000 000 000	0.000	0.000	

APPLICATION SUPPLY (IF USED)

Channel 22 can be used to read the application supply voltage at the VPWR pin. This can be enabled by setting the VPWRCON bit in the FSLADCCNTL register high. The battery voltage is first scaled as VPWR/2 in order to fit the input range of the ADC.

Table 105. Application Supply Voltage Reading Coding

Conversion Code	Voltage at ADC input	Voltage at VPWR
1 111 111 111	2.400 V	4.800 V
1 000 010 100	1.250 V	2.500 V
0 000 000 000	0.000 V	0.000 V

CHARGER CURRENT (IF USED)

Channel 24 can be used to read the charge current by monitoring the voltage drop over the charge current sense resistor. This can be enabled by setting the CHRGICON bit in the FSLADCCNTL register to 1. This resistor is connected between the ISNSBATP and ISNSBATN pins. The voltage difference is first amplified to fit the ADC input range as V(VISNSBATP-VISNSBATN)*4. The conversion is read out in a 2's complement format, see Table 106. The positive reading corresponds to the current flow from charger to battery, the negative reading to the current flowing into the charger terminal.

The value of the sense resistor used determines not only the accuracy of the result as well as the available conversion range, but also the charge current levels. It is therefore advised not to select another value other than those suggested in the ADC section of Table 3.

Table 106. Charger Current Reading Coding

CONVERSION CODE	VOLTAGE AT ADC INPUT	V_{BAT}- $V_{ISNSBAT}$	CURRENT THROUGH 20 M	CURRENT FLOW
0 111 111 111	1200 mV	300.000 mV	3.000 A	To Application/ Battery
0 000 000 001	2.346 mV	0.600 mV	0.0059 A	To Application/ Battery
0 000 000 000	0.000 mV	0.000 mV	0.000 A	-
1 111 111 111	-2.346 mV	-0.600 mV	0.0059 A	To Charger Connection
1 000 000 000	-1200 mV	-300.000 mV	3.000 A	To Charger Connection

BACKUP VOLTAGE (IF USED)

Channel 25 can be used to read the voltage of the coin cell connected to the COINCELL. This is enabled by setting the LICON bit in the FSLADCCNTL register to 1. Since the voltage range of the coin cell exceeds the input voltage range of the ADC, the COINCELL voltage is first scaled as V_{COIN}*2/3.

Table 107. Backup (Coin Cell) Voltage Reading Coding

Conversion Code	Voltage at ADC input	Voltage at COINCELL
1 111 111 111	2.400 V	3.600 V
1 000 000 000	1.200 V	1.800 V
0 000 000 000	0.000 V	0.000 V

BATTERY DETECT (IF USED)

When a phone is on and supplied by the charger, SIM removal has to be detected to avoid fraudulent use of the phone. An easy way of doing so is to place the SIM card holder under the battery pack and perform a battery thermistor presence check. When the thermistor terminal becomes high-impedance, the battery is considered being removed. This detection function can be available at Channel 26 of the ADC by setting the BATDETVCON bit in the FSLADCCNTL register to 1. When not charging, the SIM removal function is not required to operate. Although the additional current drain due to the battery detect function is small, it is advised to disable the function when not charging to save this current.

TOUCH SCREEN INTERFACE

The PMIC touch screen support consists of four analog input channels with built in bias control. The BIAS FET control bits are part of the ADC round robin address register ADCADDRx. The touch screen X plate is connected to ADIN10 (X+) and ADIN11 (X-), while the Y plate is connected to ADIN12(Y+) and ADIN13(Y-). A local supply, TSREF, of 1.2 V will serve as a reference.

The system processor will handle the touch screen sequencing and any necessary conversion delays. The system processor will direct the desired bias control for every reading though the ADCADDRx registers. If FET biasing is enabled though the ADCADDRx registers, then touch screen readings will start according based on the channels chosen, and also by the ADCADDRx registers. If the touch screen is not used, then the above inputs can be used as general purpose inputs. In this case, the bias control will always be programmed to no bias.

Figure 76 is a touch screen representation.

Figure 76. Touch Screen Configuration Example

Touch Screen Pen detection bias can be enabled via the PENDETEN bit in the ADCCNTL1 register. When this bit is enabled and a pen touch is detected, the PENDET bit in register ADCINT is set and the PMICINT pin is asserted. This is to interrupt the system, because a touch screen pen touch has been detected at the next ADC cycle, unless the interrupt is masked.

The prior reference for the touch screen (Touch Bias) is TSREF and is powered from VCORE. In touch screen operation, TSREF is a dedicated regulator. No loads other than the touch screen should be connected here. When the ADC performs non touch screen conversions, the ADC does not rely on TSREF and the reference can be disabled.

The readouts are designed such that the on chip switch resistances are of no influence to the overall readout. The readout scheme does not account for contact resistances, as present in the touch screen connectors. Therefore, the touch screen readings have to be calibrated by the user or in the factory, where one has to point with a stylus to the opposite corners of the screen. When reading out the X-coordinate, the 10-bit ADC reading represents a 10-bit coordinate with '0' for a coordinate equal to X- and full scale '1023' when equal to X+. When reading out the Y-coordinate, the 10-bit ADC reading represents a 10-bit coordinate with '0' for a coordinate equal to Y- and full scale '1023' when equal to Y+. When reading the contact resistance the 10-bit ADC reading represents the voltage drop over the contact resistance created by the known current source multiplied by 2.

Table 108. Touch Screen System Requirements

Plate Resistance X, Y	-	100	-	1000	Ω
Resistance Between Plates, Contact	-	180	-	1200	Ω
Capacitance Between Plates	-	0.5	2	-	nF
Contact Resistance Current Source	-	-	100	-	μA
Interrupt Current Source	-	-	20	-	μA
Interrupt Threshold	-	40	-	60	kΩ
Current Source Inaccuracy	-	-	-	20	%
Quiescent Current (Active Mode)		-	20	-	μA
Max Load Current (Active Mode)		-	-	20	mA
Settling Time (Position Measurement)	-	3.0	-	5.5	μs

BATTERY COULOMB COUNTER

OVERVIEW

The current into and from the battery can be read out through the general purpose ADC as a voltage drop over the RCC sense resistor, see Figure 77. Together with the battery voltage reading, the battery capacity can be estimated. More accurate battery capacity estimation can be obtained by using the integrated Coulomb Counter.

The Coulomb Counter (or CC) monitors the current flowing in/out of the battery by integrating the voltage drop across the battery current sense resistor RCC, followed by an A to D conversion. The result of the A to D conversion is used to increase/decrease the contents of an internal counter CCOUT[15:0]. This counter can be read out by software on

two registers each with 8 bits of data, CCACCH[7:0] representing the CC reading high 8-bits, and CCACCL[7:0] representing the CC reading low 8-bits. The primary coulomb count that is made available to the host firmware through the SPI interface, using the above mentioned two registers. A 2s complement 16-bit value in which a negative sign bit, means the battery is discharging. A positive sign bit means the battery is charging, and the magnitude of the value represents the state of the battery charge, i.e., how much charge remains. The unmodified coulomb count, CCOUT[15:0] is also made available through the SPI interface, and registers RAWCCH and RAWCCL for the 8 high and 8 low bits of the 16-bit data. These two registers reside in the Freescale dedicated space. These can also be used for applications that do not require the 2s complement format.

This function will require a 100 nF output capacitor to perform a first order filtering of the signal across RCC. Due to the sampling of the A to D converter and the filtering applied, the longer the software waits before retrieving the information from the CC, the higher the accuracy. The capacitor will be connected between the pins CFP and CFM, see Figure 77.

In the existing Freescale IP, the CCOUT counter is 16 bits. This counter is preferably reflecting 1 Coulomb per LSB. As a reminder, 1.0 Coulomb is the equivalent of 1.0 Ampere during 1.0 second, so a current of 20 mA during 1.0 hour is equivalent to 72 C. However, since the resolution is much finer than 1.0 C (LSB of 366.2 µC), the internal counts must first be rescaled. This can be done by setting the internal ONEC[14:0] bits. The CCOUT[15:0] counter is then increased by 1 with every ONEC[14:0] counts of the A to D converter. ONEC[14:0] = 2731 DEC yields 1C (2731*366.2 µC) count for CCOUT[15:0] with RCC=20 mOhm. For the current implementation, CCOUT[15:0] is desired to have an LSB of 10 mC. To achieve this, the ONEC register is set internally to 26 DEC yielding 10 mC count per LSB. The ONEC can be modified through the SPI in the Freescale dedicated space, using the ONECLREG and ONECHREG registers

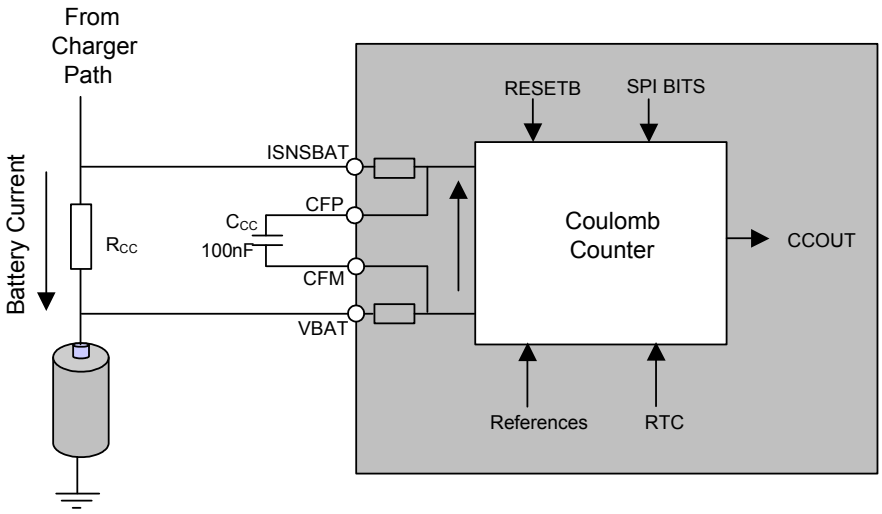

Figure 77. Coulomb Counter Block diagram

At initial power-up, all the digital portions of the CC will be reset to their default values. The ONEC[14:0] will be programmed to the value of 26 DEC by default. The next step is to reset the CC by setting the CCCLEAR bit in the ADCCNTL1 register. The CCCLEAR is automatically cleared by the PMIC. Finally, the CC will always be running and counting the battery charge, and recording the reading in the CCOUT[15:0] register for as long as the CCEN bit in the ADCCNTL1 register is asserted. Unless the CC has no power or is in reset, the count will continue.

CCOUT[15]=1 indicates that the battery is discharging, while CCOUT[15]=0 indicates it is charging. When the CC count has reached 50% of full value (CCOUT[14] = 1), the OVERFLOW bit in register ADCINT is set and the PMICINT pin is asserted, unless the interrupt is masked, in order to interrupt the system from reading the value of the CC at the next ADC cycle. The interrupt service routine for the OVERFLOW interrupt will clear the first 15 bits of the CCADCA register (0-14), and counting will continue. The CCADCA register is never expected to reach 0x7FFF or 0xFFFF (bits 0-14 being all 1's). Note that if the battery is discharging, bit 15 will not be cleared after the OVERFLOW interrupt.

The digital portion of the CC is by default permanently corrected for offset and gain errors. Digital calibration can be disabled by setting the CCCALDB bit in register CCREG to 1.

Redundant control bits STARTCC and RSTCC are also provided in the CCCREG register in the Freescale dedicated space, so the user has the option to perform all coulomb counter controls using the coulomb counter registers, instead of using the GPADC registers. The coulomb counter enable is a logical OR of CCEN and STARTCC, and the coulomb counter reset is a logical OR of CCCLEAR and RSTCC. The user must take note of this to avoid uncertainty of whether the

coulomb counter is enabled, or in reset. Note that there is no way to preset the CCOUT counter to an arbitrary value - only to all zeros. Fuel gauging software must account for this reset condition, which corresponds to a fully discharged battery.

The coulomb counter block also includes a dithering circuit that can be enabled through the CCDITHER bit in the CCCREG register, to reduce spurious tones in the frequency spectrum of the coulomb count values. The circuit performs a random dithering of the integration period by +/- one cycle of the 32 kHz sampling clock. The dither signal is a pseudo-random bit pattern generated by a linear feedback shift register (LFSR).

For analog offset calibration, the coulomb counter block includes an input that is driven by the CCCALA bit in the CCCREG register. When this bit is set, the input terminals of the ADC's integrator are shorted together, and the current sense resistor is disconnected. The user may integrate for as short or as long a period as desired, using any particular value of ONEC, to determine the rate at which the integrator is changing with zero input signal. From this, the DC offset can be calculated and subtracted from future Coulomb count values by the fuel gauging software.

The block also contains fault detection logic, which sets the CCFAULT bit in the CCCREG register, if the CCOUT counter overflows during charging - i.e., if the CCOUT count exceeds the maximum positive 15-bit value (32767) and causes a carry to the sign bit. This should not occur if the ONEC value is set appropriately for the total mAh of the battery (typically it is set to represent 1.0 C), due to the very large dynamic range of the Coulomb counter. If, however, a small ONEC value is set - representing much less than 1.0 C, the CCOUT counter may not have enough dynamic range to accommodate the total number of Coulombs of battery capacity, and the CCFAULT bit will be set. Note that CCFAULT does not cause an interrupt. It is simply a status bit that may be read at any time by the system firmware.

The block also includes a CCINVERT bit in the CCCREG register that allows the sense of coulomb counting to be reversed, so that negative values represent charging and positive values represent discharging.

ADC STATUS/CONTROL REGISTERS AND BIT DESCRIPTION

Reference the Table 109 for read/write conditions and default state for each of these registers

Table 109. ADC Interrupt/Mask Registers Structure and Bits Description

Name	Bits	Description
ADCINT (ADDR 0x5F - R - Default Value: 0x00)		
RND	0	ADC Round Robin Cycle Completion Interrupt x0 = Not Completed x1 = Completed
PENDET	1	Touch Screen Pen Detection Interrupt x0 = Pen Not Detected x1 = Pen Detected
OVERFLOW	2	Coulomb Counter reached 50% of it full scale value Interrupt x0 = CC did not reach 50% x1 = CC reached 50%
Reserved	7:3	Reserved
MADCINT (ADDR 0x60 - R/W -Default Value: 0x00)		
MRND	0	ADC Round Robin Cycle Completion Interrupt Mask x0 = Unmask x1 = Mask
MPENDET	1	Touch Screen Pen Detection Interrupt Mask x0 = Unmask x1 = Mask
MOVERFLOW	2	Coulomb Counter reached 50% of it full scale value Interrupt Mask x0 = Unmask x1 = Mask
Reserved	7:3	Reserved

Table 110. ADC Control Registers Structure and Bits Description

Name	Bits	Description	
ADCCNTL2 (ADDR 0x61 - R/W -Default Value: 0x00)			
ADSLP	2:0	ADC sleep time before starting another cycle	
		x0 = Continuous Loop x1 = 4.5 ms x2 = 9.0 ms x3 = 13.5 ms	x4 = 18 ms x5 = 22.5 ms x6 = 27 ms x7 = No Loop
CCEN	3	Coulomb Counter Enable x0 = Disable x1 = Enable	
CCCLEAR	4	Coulomb Counter Reset Enable x0 = Do not reset CC x1 = CC reset	
PENDETEN	5	Enable Touch Screen Pen Detect Bias x0 = Disabled x1 = Enabled	
ADSTRT	6	ADC Round Robin Start Signal x0 = Stop round robin after the current cycle x1 = Start round robin	
ADEN	7	Bring the ADC out of low power state, this overrides wake from sleep x0 = Disable in low power x1 = Enable at full power	
ADCCNTL3 (ADDR 0x62 - R/W -Default Value: 0x00)			
ADEXGAIN10	0	Gain bit for ADC channel 10, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN11	1	Gain bit for ADC channel 11, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN12	2	Gain bit for ADC channel 12, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN13	3	Gain bit for ADC channel 13, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN14	4	Gain bit for ADC channel 14 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN15	5	Gain bit for ADC channel 15 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN16	6	Gain bit for ADC channel 16 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	

Table 110. ADC Control Registers Structure and Bits Description

ADEXGAIN17	7	Gain bit for ADC channel 17 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
ADCCNTL4 (ADDR 0X63 - R/W -DEFAULT VALUE: 0X00)		
ADEXGAIN18	0	Gain bit for ADC channel 18 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
ADEXGAIN19	1	Gain bit for ADC channel 19 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
ADEXGAIN20	2	Gain bit for ADC channel 20 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
ADEXGAIN21	3	Gain bit for ADC channel 21 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
Reserved	7:4	Reserved

Table 111. ADC Channel Selector/Configuration Structure and bit Description

Name	Bits	Description
ADCSNSxH (x = 0 to 31)		
ADCHxH	6:0	7 MSBs of ADC result for Channel x
GAINx	7	Gain bit for ADC channel x, x = 0 to 31 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
ADCSNSxL (x = 0 to 31)		
ADCHxL	2:0	3 LSBs of ADC result for Channel x
Reserved	7:3	Reserved
ADCADDRX (X = 0 TO 31)		
ADSELx	4:0	ADC Channel to be read Selection bits x00 = Channel 0 x01 = Channel 1 ... x1F = Channel 31
XPXMx	5	Turns on X+ and X- bias FETs, Refer to Figure 76 x0 = FETS Off x1 = FETS On
YPYMx	6	Turns on Y+ and Y- bias FETs, Refer to Figure 76 x0 = FETS Off x1 = FETS On
XMYPx	7	Turns on X- and Y+ bias FETs, Refer to Figure 76 x0 = FETS Off x1 = FETS On

Table 111. ADC Channel Selector/Configuration Structure and bit Description

CCADCHA (ADDR 0xC4 - R - 0x00)		
CCACCH	7:0	8 MSBs of Coulomb counter result, CCOUT[15:8]
CCADCLA (ADDR 0xC5 - R - 0x00)		
CCACCL	7:0	8 LSBs of Coulomb counter result, CCOUT[7:0]

ADC STATUS/CONTROL REGISTERS AND BIT DESCRIPTION

Table 112. Extended ADC Control Register Structure and Bits Description

Name	Bits	Description
FSLADCCNTL (ADDR 0x1DE - R/W - Default Value: 0x00)		
VPWRCON	0	Enable channel 22 to read the V_{PWR} voltage x0 = Disable (Default) x1 = Enable
CHRGICON	1	Enable channel 24 to read the Battery charging current x0 = Disable (Default) x1 = Enable
LICON	2	Enable channel 25 to read the Backup Battery voltage x0 = Disable (Default) x1 = Enable
BATDETVCON	3	Enable channel 26 for battery detection x0 = Disable (Default) x1 = Enable
LSBSEL	4	ADC LSB Selection Bit x0 = Refer to Table 98 x1 = Refer to Table 98
Reserved	7:4	Reserved
CCCREG (ADDR 0x1DF - R/W -Default Value: 0x00)		
STARTCC	0	Redundant to CCEN
RSTCC	1	Redundant to CCCLEAR
CCDITHER	2	Coulomb Counter Dithering Enable x0 = Disable (Default) x1 = Enable
CCCALDB	3	Digital Offset and Gain Errors Calibration Enable x0 = Enable x1 = Disable (Default)
CCCALA	4	Analog Offset Calibration Enable x0 = Disable (Default) x1 = Enable
CCINVERT	5	Coulomb Counter Sign Inversion Bit x0 = Positive for Charging and Negative for Discharging (Default) x1 = Positive for Discharging and Negative for Charging
Reserved	6	Reserved

Table 112. Extended ADC Control Register Structure and Bits Description

CCFAULT	7	Charging Overflow Status Bit x0 = Coulomb Counter Reading is < Positive 32767 x1 = Coulomb Counter Reading is > Positive 32767
ONECLREG (ADDR 0x1E0 - R/W -Default Value: 0x1A)		
ONEC[7:0]	7:0	8 LSBs of ONEC[14:0] internal register
ONECHREG (ADDR 0x1E1 - R/W -Default Value: 0x00)		
ONEC[14:8]	6:0	7 MSBs of ONEC[14:0] internal register
Reserved	7	Reserved
RAWCCH (ADDR 0x1E2 - R/W - Default Value: 0x00		
RAWCCH	7:0	8 MSBs CCOUT Raw Data
RAWCCL (ADDR 0x1E3 - R/W - Default Value: 0x00)		
RAWCCL	7:0	8 LSBs of CCOUT Raw Data

GPIOS

DESCRIPTION

The 900841 has eight GPIOs, four GPOSWs for platform switches, and eight GPOs for platform control.

As outputs, the GPIOs and GPOSWs shall support CMOS/OD signaling levels, based on the voltage level on the GPIOVCC and GPOSWVCC. The GPOs shall support CMOS signaling levels, based on the voltage level on the GPOVCC pin. As inputs, they need to be 3.6 V tolerant and should be de-bounced for a period of no more than 10 ms minimum.

The 900841 will provide one bank of eight configurable GPIO inputs/outputs, GPIO[7:0] for general purpose sensing and platform control. Only GPIOs support an input function.

The PMIC shall provide one bank of four GPOSW outputs, whose primary function will be to serve as gating signals for discrete platform VR switches.

GPOSW outputs vary from GPIOs in an important way. They are designed to support dynamic gating of sub-circuits from a main well or always on supply, and therefore require additional attention when switching. Specifically, GPOSWs must implement slew rate control to prevent dangerously high instantaneous inrush currents to previously isolated rails. For CMOS configured outputs, slew rate control will be specified in terms of output resistance at the GPOSW output pin. When operating as an open drain output, the slew rate specification is the same, but will be interpreted assuming an externally connected 100 kΩ (±1%) pull-up resistance.

Both GPIOs and GPOSWs are expected to switch between a high-impedance (>1.0 MΩ) state and a low-impedance (20 Ω nominal) state when operating in open drain mode. When operating in CMOS mode, the outputs are expected to drive from the voltage supplied on the GPIOVCC pin with a 20 Ω output drive capability (for GPIOs) or GPOSWVCC pin (for GPOSWs).

The electrical characteristics of the output buffer will therefore be specified as relative percentages of the driving supply.

Any unused GPIO pin should be tied to ground on the board.

When any GPIO or GPOSW pin is configured as an open drain, the pull-up voltage cannot exceed that of the GPIOVCC and GPOSWVCC voltage level respectively.

Table 113 shows the default state of the different GPIOs and their capabilities.

Table 113. GPIOs Capabilities and Default States

GPIO	Input	Output	CMOS	OD	Slew CNTL	Default Mode	Default Level
GPIO0	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO1	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO2	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO3	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO4	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO5	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO6	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO7	Yes	Yes	Yes	Yes	No	Input	HI-Z

Table 113. GPIOs Capabilities and Default States

GPOSW0	No	Yes	Yes	Yes	Yes	OD	Low
GPOSW1	No	Yes	Yes	Yes	Yes	OD	Low
GPOSW2	No	Yes	Yes	Yes	Yes	OD	Low
GPOSW3	No	Yes	Yes	Yes	Yes	OD	Low
GPO0	No	Yes	Yes	No	No	CMOS	Low
GPO1	No	Yes	Yes	No	No	CMOS	Low
GPO2	No	Yes	Yes	No	No	CMOS	Low
GPO3	No	Yes	Yes	No	No	CMOS	Low
GPO4	No	Yes	Yes	No	No	CMOS	Low
GPO5	No	Yes	Yes	No	No	CMOS	Low
GPO6	No	Yes	Yes	No	No	CMOS	Low
GPO7	No	Yes	Yes	No	No	CMOS	Low

GPIO/GPOSW MODULE STRUCTURE

Figure 78 and Figure 79 illustrate the logical structure of the GPIOx and GPOSWx modules.

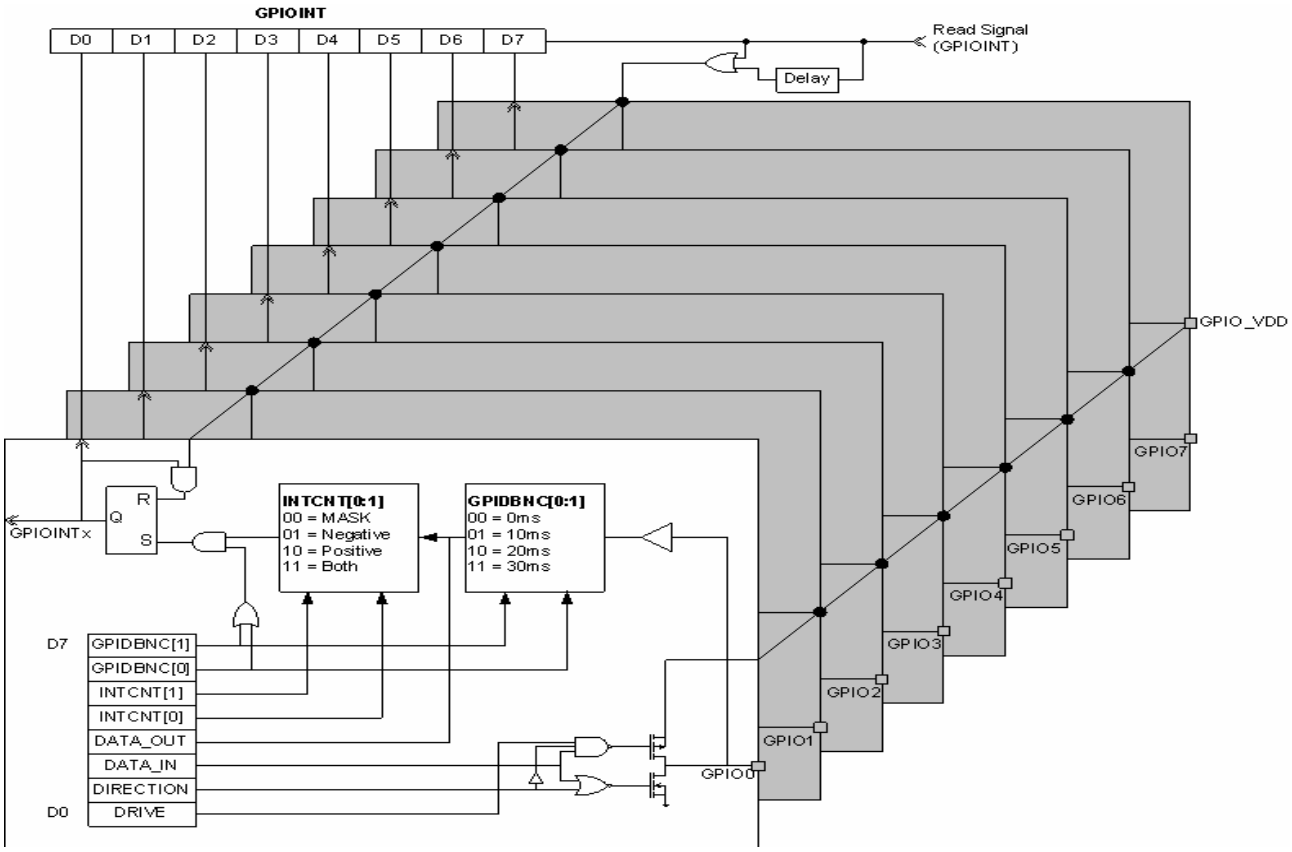

Figure 78. GPIO Module Structure

Figure 79. GPOSW Module Structure

GPOSW REQUIREMENTS

GPOSWs are recommended to be CMOS type outputs to utilize fully internal slew rate control, which is achieved through varying the output resistance.

GPOSWs are powered from GPOSWVCC.

When configured as an open drain, the slew rate specification is the same, but will be interpreted, assuming an externally connected 100 kΩ (±1%) pull-up resistance. See Figure 80

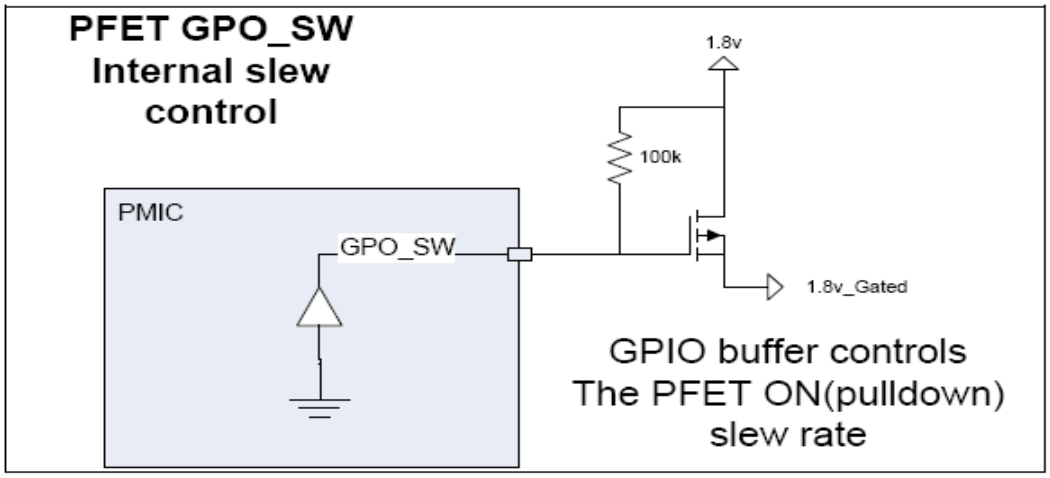

Figure 80. PFET GPOSW Schematics with Slew Rate Control

GPIO/GPOSW STATUS/CONTROL REGISTERS AND BIT DESCRIPTION

Each individual GPIO and GPOSW module shall have a single 8-bit status and control register assigned to it. See Table 114 for details.

The “x” in the bit names in the tables is from 0 to 7 for the GPIOs and 0 to 3 for the GPOSWs.

Table 114. GPIO/GPOSW Register Structure and Bits Description

Name	Bits	Description
		GPIOCNTLx (x = 0 to 7)
DRVx	0	GPIOx Output Driver Type x0 = Open Drain x1 = CMOS
DIRx	1	GPIOx Direction Configuration x0 = Output (Type selected by Bit 0) x1 = Input (Bit 0 is ignored)
DATAINx	2	The value in the DATA_IN bit reflects the electrical state of the GPIOx pin at the time the register read was initiated. When Bit 1, DIRECTION, is 0 (Output Mode), the contents of this register are not required to be updated on reads and is assumed to be invalid by the system controller. The PMIC should de-bounce the inputs over 1-10 ms to insure a clean transition. X0 = Electrical Low (34) x1 = Electrical High (34)
DATAOUTx	3	The value in the DATA_OUT bit reflects the desired electrical output state of the GPIOx pin. When Bit 1, DIRECTION, is 1 (Input Mode), the contents of this register may still be read or written, but will not be reflected until the GPIOx is reverted to an output (Bit 1, DIRECTION, is 0) x0 = Electrical Low (34) x1 = Electrical High (CMOS) or High-impedance Output (Open-Drain) (34)
INTCTLx	5:4	These bits set the interrupt definition. The MASK (00) determines if the corresponding interrupt flag bit is set or not on an interrupt. The other logic levels will set the corresponding interrupt flag bit in the register upon the specific edge detection defined by the level. They will also set bit 4 of the 1st level INTERRUPT register, see section Interrupt Controller for more details. (35) x0 = Mask. x1 = Negative Edge x2 = Positive Edge x3 = Both Edges
GPIDBNCx	7:6	These bits set the debounce time on the GPIOx when configured as inputs x0 = No Debounce x1 = 10 ms x2 = 20 ms x3 = 30 ms
		GPIOINT (ADDR 0xE8 - R - Default Value: 0x00)
GPIINT0	0	GPIO0 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT1	1	GPIO1 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT2	2	GPIO2 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT3	3	GPIO3 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred

Table 114. GPIO/GPOSW Register Structure and Bits Description

Name	Bits	Description
GPIINT4	4	GPIO4 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT5	5	GPIO5 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT6	6	GPIO6 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT7	7	GPIO7 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPOSWCTLx (x = 0 to 3)		
SWDRVx	0	GPOSWx Output Driver Type x0 = Open Drain x1 = CMOS
-	1	RESERVED
-	2	RESERVED
SWDOUTx	3	The value in the SWDOUTx bit reflects the desired electrical output state of the GPOSWx pin. X0 = Electrical Low (34) x1 = Electrical High (CMOS) or High-impedance Output (Open-drain) (34)
SLEWx	4:5	The value of the SLEWx Bits determines the level of slew rate control being exercised on the output's ramp rates. The level of slew rate control exercised is expected to hold true for both CMOS and Open Drain outputs. However, in the case of Open Drain outputs, the specified ramp rate is assuming an externally connected 100 kΩ (±1%) pull-up resistor (and no parallel capacitance). These values are met at the lowest supply voltage, GPOSWVCC = 1.8 V X0 = 50 Ω max (NFET) – 100 Ω max (PFET) X1 = 2.0 kΩ, ±35% at room temperature X2 = 20 kΩ, ±35% at room temperature X3 = 200 kΩ, ±25% at room temperature
SCRATCHx	6:7	These bits shall not exert any control over the operation of the GPOSWx, and are intended to be used as scratchpad registers by the system controller. Their contents are erased on POR.

Notes
34. See GPIOs electrical characteristics on Table 3
35. An unintended interrupt is caused if interrupt settings are reconfigured in the middle of an application, e.g. re-setting interrupt detection from detecting an interrupt on both edges to an interrupt on the rising edge. To mask any unwanted interrupt, change the GPIO interrupt detection to the new configuration, then clear Level 1 and level 2 interrupts. Finally unmask the GPIO Interrupt.

Table 115. GPO Register Structure and Bits Description

Name	Bits	Description
GPO (ADDR 0xF4 - R/W - Default Value: 0x00)		
GPO0	0	GPO0 Output Level x0 = Low0 x1 = High (To voltage supplied on GPOVCC Pin)
GPO1	1	GPO1 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)

Table 115. GPO Register Structure and Bits Description

GPO2	2	GPO2 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO3	3	GPO3 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO4	4	GPO4 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO5	5	GPO5 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO6	6	GPO6 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO7	7	GPO7 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)

SPI REGISTER MAP

OVERVIEW

The SPI frame is organized as 24 bits. The first 16 bits is the write enable bit, 10-bit address and 5 "dead" bits between the data and address fields. The next 8 bits are the data bits. The one write enable bit selects whether the SPI transaction is a read or a write.

The addressable register map spans 1024 registers of 8 data bits each. The map is not fully populated. A summarized structure of the register set is given in the following tables. Expanded bit descriptions are included in the individual functional sections for application guidance.

SPI BIT MAP

The tables include the following fields:

- Block: This corresponds directly to the chapter, section or topic in which the detailed register description is included.
- Address: The register memory map address allocation in HEX format
- Register Name
- R/W: Defines if the register is a Read/Write register or only a Read register
- D7-D0: The 8-bit data included in the register with each bit's name and location within the field included
- Initial: The register's default value after power up
- Function: A short description of the register's function

Some important notes about data in the table:

- Reserved registers/bits are not implemented in the design and they will always read as a 0
- Registers under the "FSL" block are Freescale dedicated registers and are not defined in the customer specifications. These registers represent additional functionality that Freescale is offering to enhance the performance of the overall system
- Registers under the "VD2" and "VD3" blocks are blocked from being used by Freescale
- The table only displays up to address 0x2FF. Address space between 0x300 and 0x3FF is reserved for future application use. Freescale is currently using the 0x300 to 0x3FF space for test and debug register implementation. This will not effect the application or any future use plans for this address space. The details of this space implementation are not discussed in this document.

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
Chip1	0x00	ID1	R	RSVD	RSVD	REV1[2:0]			VENDID1[2:0]			0x38	Chip1 ID
Chip2	0x01	ID2	R	RSVD	RSVD	REV2[2:0]			VENDID2[2:0]			0x00	Chip2 ID
Chip3	0x02	ID3	R	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Chip3 ID
Chip4	0x03	ID4	R	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Chip4 ID

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
IRQ	0x04	INTERRUPT	R	EXT	AUX	VRFAULT	GPIO	RTC	CHR	ADC	PWRBTN	0x00	PMIC_INT sources, read clears
IRQ	0x05	INTMASK	R/W	MEXT	MAUX	MVRFAULT	MGPIO	MRTC	MCHR	MADC	MPWRBTN	0xFA	IRQ mask
CNTRL	0x06	CHIPCNTRL	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	WARMRST	COLDRST	0x00	PWRGD/RESET# control
RSVD	0x07	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x08	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x09	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0A	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0B	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0C	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0D	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0E	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0F	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RTC	0x10	RTCS	R/W	RSVD	SEC[6:0]							0x00	RTC Second
RTC	0x11	RTCSA	R/W	SECALARM[7:0]								0x00	RTC Second Alarm
RTC	0x12	RTCM1	R/W	RSVD	MIN[6:0]							0x00	RTC Minutes
RTC	0x13	RTCMA	R/W	MINALARM[7:0]								0x00	RTC Minutes Alarm
RTC	0x14	RTCH	R/W	PA-H	RSVD	HRS[5:0]						0x00	RTC Hours
RTC	0x15	RTCHA	R/W	PA-HA	HRSALARM[6:0]							0x00	RTC Hours Alarm
RTC	0x16	RTCDW	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	DOW[2:0]			0x01	RTC Day Of Week
RTC	0x17	RTCDM	R/W	RSVD	RSVD	DOM[5:0]						0x01	RTC Day Of Month
RTC	0x18	RTCM2	R/W	19/20	RSVD	RSVD	MONTH[4:0]					0x01	RTC Month
RTC	0x19	RTCY	R/W	YEAR[7:0]								0x00	RTC
RTC	0x1A	RTCA	R	UIP	DV[2:0] (=010b FIXED)			RS[3:0] (=000b FIXED)				0x20	RTC Control A
RTC	0x1B	RTCB	R/W	SET	PIE (=0) FIX	AIE	UIE	SQWE (=0) FIX	DM	HRMODE	DSE (=0) FIX	0x02	RTC Control B
RTC	0x1C	RTCC	R	IRQF	PF (=0) FIX	AF	UF	RSVD	RSVD	RSVD	RSVD	0x00	RTC Control C
RTC	0x1D	RTCD	R	VRT	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RTC Control D
RTC	0x1E	RTCE	R/W	SCRATCH[4:0]					POR	BKDET	OSCSTP	0x05	RTC Optional Detection
RTC	0x1F	ADJ	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ADJ	0x00	RTC Adjustment
RTC	0x20	TRIM	R/W	RSVD	SIGN	TRIMVAL[5:0]						0x00	RTC Trimming
RTC	0x21	CLKOUT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	M32KCLK	0x00	32kHz clock output enable
RSVD	0x22	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x23	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x24	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
LED	0x25	LEDBRT0	R/W	LED1BLNK[1:0]		LED1BRT[1:0]		LED0BLNK[1:0]		LED0BRT[1:0]		0x00	LED current
LED	0x26	LEDBRT1	R/W	LED3BLNK[1:0]		LED3BRT[1:0]		LED2BLNK[1:0]		LED2BRT[1:0]		0x00	LED current
LED	0x27	LEDBRT2	R/W	LED5BLNK[1:0]		LED5BRT[1:0]		LED4BLNK[1:0]		LED4BRT[1:0]		0x00	LED current
LCD	0x28	BKLTCNT	R/W	MLED3EN	MLED2EN	MLED1EN	RSVD	RSVD	RSVD	BKLTSS[1:0]		0x00	LCD Backlight enable
LCD	0x29	BKLTFREQ	R/W	RSVD	PWMEN	RSVD	RSVD	RSVD	BKLTFREQ[2:0]			0x00	PWM freq for external LCD-Driver
LCD	0x2A	BKLTBRTL	R/W	BKLTBRT[7:0]								0x00	LCD Backlight brightness
LCD	0x2B	SSTRING	R/W	RSVD	RSVD	RSVD	RSVD	SILTBRT[2:0]			SLEDEN	0x00	4th String
RSVD	0x2C	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x2D	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x2E	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
RSVD	0x2F	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
POWER	0x30	VRFAULTINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	VRFAIL	BATOCP	THRM	0x00	Voltage Regulators Fault interrupt
POWER	0x31	MVRFAULTINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MVRFAIL	MBATOCP	MTHRM	0x03	Voltage Regulators Fault interrupt Mask
POWER	0x32	VCCLATCH	R/W	DVP1VRD	VIDVCC[6:0]							0x7F	VCC VID CONTROL
POWER	0x33	VNNLATCH	R/W	DVP2VRD	VIDVNN[6:0]							0x7F	VNN VID CONTROL
POWER	0x34	PWRMASK	R/W	M7	M6	M5	M4	M3	M2	M1	M0	0x00	Power register write mask
POWER	0x35	VCCCNT	R/W	RSVD	RSVD	AOACTLVCC[2:0]			CTLVCC[2:0]			0x24	VCC
POWER	0x36	VNNCNT	R/W	RSVD	RSVD	AOACTLVNN[2:0]			CTLVNN[2:0]			0x04	VNN
POWER	0x37	VDDQCNT	R/W	RSVD	RSVD	AOACTLVDDQ[2:0]			CTLVDDQ[2:0]			0x04	VDDQ
POWER	0x38	V21CNT	R/W	RSVD	RSVD	AOACTLV21[2:0]			CTLV21[2:0]			0x07	V21
POWER	0x39	V15CNT	R/W	SELV15[1:0]		AOACTLV15[2:0]			CTLV15[2:0]			0x07	V15
POWER	0x3A	V33CNT	R/W	RSVD	RSVD	AOACTLV33[2:0]			CTLV33[2:0]			0x24	V33
POWER	0x3B	VYMX3GPACNT	R/W	SELYMX3GPA[1:0]		AOACTLYMX3GPA[2:0]			CTLYMX3GPA[2:0]			0x24	YMX3GPA
POWER	0x3C	VYMX3GDCNT	R/W	SELYMX3GD[1:0]		AOACTLYMX3GD[2:0]			CTLYMX3GD[2:0]			0x24	VMX3GD
POWER	0x3D	VCCPAOACCNT	R/W	RSVD	RSVD	AOACTLVCCPAOAC[2:0]			CTLVCCPAOAC[2:0]			0x07	VCCPAOAC
POWER	0x3E	VCCPDDRCNT	R/W	RSVD	RSVD	AOACTLVCCPDDR[2:0]			CTLVCCPDDR[2:0]			0x3C	VCCPDDR
POWER	0x3F	VLBGCNT	R/W	RSVD	RSVD	AOACTLVLBG[2:0]			CTLVLBG[2:0]			0x24	VLBG
POWER	0x40	VCCACNT	R/W	RSVD	RSVD	AOACTLVCCA[2:0]			CTLVCCA[2:0]			0x3C	VCCA
POWER	0x41	VPMICCNT	R/W	RSVD	RSVD	AOACTLVPMIC[2:0]			CTLVPMIC[2:0]			0x07	VPMIC
POWER	0x42	VIMG25CNT	R/W	RSVD	RSVD	AOACTLVIMG25[2:0]			CTLVIMG25[2:0]			0x04	VIMG25
POWER	0x43	VCC180CNT	R/W	RSVD	RSVD	AOACTLVCC180[2:0]			CTLVCC180[2:0]			0x3C	VCC180
POWER	0x44	VCCPCNT	R/W	RSVD	RSVD	AOACTLVCCP[2:0]			CTLVCCP[2:0]			0x3C	VCCP
POWER	0x45	VAONCNT	R/W	RSVD	RSVD	AOACTLVAON[2:0]			CTLVAON[2:0]			0x07	VAON
POWER	0x46	VPANEL18CNT	R/W	RSVD	RSVD	AOACTLVPANEL18[2:0]			CTLVPANEL18[2:0]			0x24	VPANEL18
POWER	0x47	VMMCNT	R/W	RSVD	RSVD	AOACTLVMM[2:0]			CTLVMM[2:0]			0x24	VMM
POWER	0x48	VIMGACNT	R/W	SELIMGA[1:0]		AOACTLVIMGA[2:0]			CTLVIMGA[2:0]			0x24	VIMGA
POWER	0x49	VIBCNT	R/W	SELVIB[1:0]		AOACTLVIB[2:0]			CTLVIB[2:0]			0x24	VIB
POWER	0x4A	VGYMXIOCNT	R/W	SELVGYMXIO[1:0]		AOACTLVGYMXIO[2:0]			CTLVGYMXIO[2:0]			0x24	GPS_YMX_IO
POWER	0x4B	VWDYMXACNT	R/W	SELVWDYMXA[1:0]		AOACTLVWDYMXA[2:0]			CTLVWDYMXA[2:0]			0x24	WiFiBT_DIG_YMX_ANALOG
POWER	0x4C	VWYMXARFCNT	R/W	RSVD	RSVD	AOACTLVWYMXARF[2:0]			CTLVWYMXARF[2:0]			0x24	WiFiBT_YMX_ANALOGRF
POWER	0x4D	VSDIOCNT	R/W	SELVSDIO[1:0]		AOACTLVSDIO[2:0]			CTLVSDIO[2:0]			0x64	VSDIO
POWER	0x4E	GYMX33CNT	R/W	RSVD	RSVD	AOACTLGYMX33[2:0]			CTLGYMX33[2:0]			0x24	GPS_ANALOGRF_WiMAX3.3
POWER	0x4F	VPANEL33CNT	R/W	RSVD	RSVD	AOACTLVPANEL33[2:0]			CTLVPANEL33[2:0]			0x24	VCC_PANEL_3.3
POWER	0x50	VGP33CNT	R/W	RSVD	RSVD	AOACTLVGP33[2:0]			CTLVGP33[2:0]			0x24	VCC_GP_3.3
POWER	0x51	VAUDIOCNT	R/W	RSVD	RSVD	AOACTLVAUDIO[2:0]			CTLVAUDIO[2:0]			0x00	VAUDIOCNT
RSVD	0x52	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x53	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x54	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
MEMORY	0x55	MEM1	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x56	MEM2	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x57	MEM3	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x58	MEM4	R/W	SCRATCH[7:0]								0x00	Backup memory

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
MEMORY	0x59	MEM5	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x5A	MEM6	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x5B	MEM7	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x5C	MEM8	R/W	SCRATCH[7:0]								0x00	Backup memory
RSVD	0x5D	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x5E	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
ADC	0x5F	ADCINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	OVERFLOW	PENDET	RND	0x00	ADC interrupt
ADC	0x60	MADCINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MOVERFLOW	MPENDET	MRND	0x00	ADC interrupt Mask
ADC	0x61	ADCCNTL2	R/W	ADEN	ADSTRT	PENDETEN	CCCLEAR	CCEN	ADSLP[2:0]			0x00	ADC control
ADC	0x62	ADCCNTL3	R/W	ADEXGAIN17	ADEXGAIN16	ADEXGAIN15	ADEXGAIN14	ADEXGAIN13	ADEXGAIN12	ADEXGAIN11	ADEXGAIN10	0x00	GAIN for AN10-AN17
ADC	0x63	ADCCNTL4	R/W	RSVD	RSVD	RSVD	RSVD	ADEXGAIN21	ADEXGAIN20	ADEXGAIN19	ADEXGAIN18	0x00	GAIN for AN18-AN21
ADC	0x64	ADCSNS0H	R	GAIN0	ADCH0H[9:3]							0x00	ADC result
ADC	0x65	ADCSNS0L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH0L[2:0]			0x00	ADC result
ADC	0x66	ADCSNS1H	R	GAIN1	ADCH1H[9:3]							0x00	ADC result
ADC	0x67	ADCSNS1L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH1L[2:0]			0x00	ADC result
ADC	0x68	ADCSNS2H	R	GAIN2	ADCH2H[9:3]							0x00	ADC result
ADC	0x69	ADCSNS2L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH2L[2:0]			0x00	ADC result
ADC	0x6A	ADCSNS3H	R	GAIN3	ADCH3H[9:3]							0x00	ADC result
ADC	0x6B	ADCSNS3L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH3L[2:0]			0x00	ADC result
ADC	0x6C	ADCSNS4H	R	GAIN4	ADCH4H[9:3]							0x00	ADC result
ADC	0x6D	ADCSNS4L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH4L[2:0]			0x00	ADC result
ADC	0x6E	ADCSNS5H	R	GAIN5	ADCH5H[9:3]							0x00	ADC result
ADC	0x6F	ADCSNS5L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH5L[2:0]			0x00	ADC result
ADC	0x70	ADCSNS6H	R	GAIN6	ADCH6H[9:3]							0x00	ADC result
ADC	0x71	ADCSNS6L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH6L[2:0]			0x00	ADC result
ADC	0x72	ADCSNS7H	R	GAIN7	ADCH7H[9:3]							0x00	ADC result
ADC	0x73	ADCSNS7L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH7L[2:0]			0x00	ADC result
ADC	0x74	ADCSNS8H	R	GAIN8	ADCH8H[9:3]							0x00	ADC result
ADC	0x75	ADCSNS8L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH8L[2:0]			0x00	ADC result
ADC	0x76	ADCSNS9H	R	GAIN9	ADCH9H[9:3]							0x00	ADC result
ADC	0x77	ADCSNS9L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH9L[2:0]			0x00	ADC result
ADC	0x78	ADCSNS10H	R	GAIN10	ADCH10H[9:3]							0x00	ADC result
ADC	0x79	ADCSNS10L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH10L[2:0]			0x00	ADC result
ADC	0x7A	ADCSNS11H	R	GAIN11	ADCH11H[9:3]							0x00	ADC result
ADC	0x7B	ADCSNS11L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH11L[2:0]			0x00	ADC result
ADC	0x7C	ADCSNS12H	R	GAIN12	ADCH12H[9:3]							0x00	ADC result
ADC	0x7D	ADCSNS12L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH12L[2:0]			0x00	ADC result
ADC	0x7E	ADCSNS13H	R	GAIN13	ADCH13H[9:3]							0x00	ADC result
ADC	0x7F	ADCSNS13L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH13L[2:0]			0x00	ADC result
ADC	0x80	ADCSNS14H	R	GAIN14	ADCH14H[9:3]							0x00	ADC result
ADC	0x81	ADCSNS14L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH14L[2:0]			0x00	ADC result
ADC	0x82	ADCSNS15H	R	GAIN15	ADCH15H[9:3]							0x00	ADC result
ADC	0x83	ADCSNS15L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH15L[2:0]			0x00	ADC result
ADC	0x84	ADCSNS16H	R	GAIN16	ADCH16H[9:3]							0x00	ADC result
ADC	0x85	ADCSNS16L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH16L[2:0]			0x00	ADC result

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
ADC	0x86	ADCSNS17H	R	GAIN17	ADCH17H[9:3]							0x00	ADC result
ADC	0x87	ADCSNS17L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH17L[2:0]			0x00	ADC result
ADC	0x88	ADCSNS18H	R	GAIN18	ADCH18H[9:3]							0x00	ADC result
ADC	0x89	ADCSNS18L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH18L[2:0]			0x00	ADC result
ADC	0x8A	ADCSNS19H	R	GAIN19	ADCH19H[9:3]							0x00	ADC result
ADC	0x8B	ADCSNS19L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH19L[2:0]			0x00	ADC result
ADC	0x8C	ADCSNS20H	R	GAIN20	ADCH20H[9:3]							0x00	ADC result
ADC	0x8D	ADCSNS20L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH20L[2:0]			0x00	ADC result
ADC	0x8E	ADCSNS21H	R	GAIN21	ADCH21H[9:3]							0x00	ADC result
ADC	0x8F	ADCSNS21L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH21L[2:0]			0x00	ADC result
ADC	0x90	ADCSNS22H	R	GAIN22	ADCH22H[9:3]							0x00	ADC result
ADC	0x91	ADCSNS22L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH22L[2:0]			0x00	ADC result
ADC	0x92	ADCSNS23H	R	GAIN23	ADCH23H[9:3]							0x00	ADC result
ADC	0x93	ADCSNS23L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH23L[2:0]			0x00	ADC result
ADC	0x94	ADCSNS24H	R	GAIN24	ADCH24H[9:3]							0x00	ADC result
ADC	0x95	ADCSNS24L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH24L[2:0]			0x00	ADC result
ADC	0x96	ADCSNS25H	R	GAIN25	ADCH25H[9:3]							0x00	ADC result
ADC	0x97	ADCSNS25L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH25L[2:0]			0x00	ADC result
ADC	0x98	ADCSNS26H	R	GAIN26	ADCH26H[9:3]							0x00	ADC result
ADC	0x99	ADCSNS26L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH26L[2:0]			0x00	ADC result
ADC	0x9A	ADCSNS27H	R	GAIN27	ADCH27H[9:3]							0x00	ADC result
ADC	0x9B	ADCSNS27L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH27L[2:0]			0x00	ADC result
ADC	0x9C	ADCSNS28H	R	GAIN28	ADCH28H[9:3]							0x00	ADC result
ADC	0x9D	ADCSNS28L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH28L[2:0]			0x00	ADC result
ADC	0x9E	ADCSNS29H	R	GAIN29	ADCH29H[9:3]							0x00	ADC result
ADC	0x9F	ADCSNS29L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH29L[2:0]			0x00	ADC result
ADC	0xA0	ADCSNS30H	R	GAIN30	ADCH30H[9:3]							0x00	ADC result
ADC	0xA1	ADCSNS30L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH30L[2:0]			0x00	ADC result
ADC	0xA2	ADCSNS31H	R	GAIN31	ADCH31H[9:3]							0x00	ADC result
ADC	0xA3	ADCSNS31L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH31L[2:0]			0x00	ADC result
ADC	0xA4	ADCADDR0	R/W	XMYP0	YPYM0	XPXM0	ADSEL0[4:0]					0x00	ADC selector address
ADC	0xA5	ADCADDR1	R/W	XMYP1	YPYM1	XPXM1	ADSEL1[4:0]					0x00	ADC selector address
ADC	0xA6	ADCADDR2	R/W	XMYP2	YPYM2	XPXM2	ADSEL2[4:0]					0x00	ADC selector address
ADC	0xA7	ADCADDR3	R/W	XMYP3	YPYM3	XPXM3	ADSEL3[4:0]					0x00	ADC selector address
ADC	0xA8	ADCADDR4	R/W	XMYP4	YPYM4	XPXM4	ADSEL4[4:0]					0x00	ADC selector address
ADC	0xA9	ADCADDR5	R/W	XMYP5	YPYM5	XPXM5	ADSEL5[4:0]					0x00	ADC selector address
ADC	0xAA	ADCADDR6	R/W	XMYP6	YPYM6	XPXM6	ADSEL6[4:0]					0x00	ADC selector address
ADC	0xAB	ADCADDR7	R/W	XMYP7	YPYM7	XPXM7	ADSEL7[4:0]					0x00	ADC selector address
ADC	0xAC	ADCADDR8	R/W	XMYP8	YPYM8	XPXM8	ADSEL8[4:0]					0x00	ADC selector address
ADC	0xAD	ADCADDR9	R/W	XMYP9	YPYM9	XPXM9	ADSEL9[4:0]					0x00	ADC selector address

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
ADC	0xAE	ADCADDR10	R/W	XMYP10	YPYM10	XPXM10	ADSEL10[4:0]					0x00	ADC selector address
ADC	0xAF	ADCADDR11	R/W	XMYP11	YPYM11	XPXM11	ADSEL11[4:0]					0x00	ADC selector address
ADC	0xB0	ADCADDR12	R/W	XMYP12	YPYM12	XPXM12	ADSEL12[4:0]					0x00	ADC selector address
ADC	0xB1	ADCADDR13	R/W	XMYP13	YPYM13	XPXM13	ADSEL13[4:0]					0x00	ADC selector address
ADC	0xB2	ADCADDR14	R/W	XMYP14	YPYM14	XPXM14	ADSEL14[4:0]					0x00	ADC selector address
ADC	0xB3	ADCADDR15	R/W	XMYP15	YPYM15	XPXM15	ADSEL15[4:0]					0x00	ADC selector address
ADC	0xB4	ADCADDR16	R/W	XMYP16	YPYM16	XPXM16	ADSEL16[4:0]					0x00	ADC selector address
ADC	0xB5	ADCADDR17	R/W	XMYP17	YPYM17	XPXM17	ADSEL17[4:0]					0x00	ADC selector address
ADC	0xB6	ADCADDR18	R/W	XMYP18	YPYM18	XPXM18	ADSEL18[4:0]					0x00	ADC selector address
ADC	0xB7	ADCADDR19	R/W	XMYP19	YPYM19	XPXM19	ADSEL19[4:0]					0x00	ADC selector address
ADC	0xB8	ADCADDR20	R/W	XMYP20	YPYM20	XPXM20	ADSEL20[4:0]					0x00	ADC selector address
ADC	0xB9	ADCADDR21	R/W	XMYP21	YPYM21	XPXM21	ADSEL21[4:0]					0x00	ADC selector address
ADC	0xBA	ADCADDR22	R/W	XMYP22	YPYM22	XPXM22	ADSEL22[4:0]					0x00	ADC selector address
ADC	0xBB	ADCADDR23	R/W	XMYP23	YPYM23	XPXM23	ADSEL23[4:0]					0x00	ADC selector address
ADC	0xBC	ADCADDR24	R/W	XMYP24	YPYM24	XPXM24	ADSEL24[4:0]					0x00	ADC selector address
ADC	0xBD	ADCADDR25	R/W	XMYP25	YPYM25	XPXM25	ADSEL25[4:0]					0x00	ADC selector address
ADC	0xBE	ADCADDR26	R/W	XMYP26	YPYM26	XPXM26	ADSEL26[4:0]					0x00	ADC selector address
ADC	0xBF	ADCADDR27	R/W	XMYP27	YPYM27	XPXM27	ADSEL27[4:0]					0x00	ADC selector address
ADC	0xC0	ADCADDR28	R/W	XMYP28	YPYM28	XPXM28	ADSEL28[4:0]					0x00	ADC selector address
ADC	0xC1	ADCADDR29	R/W	XMYP29	YPYM29	XPXM29	ADSEL29[4:0]					0x00	ADC selector address
ADC	0xC2	ADCADDR30	R/W	XMYP30	YPYM30	XPXM30	ADSEL30[4:0]					0x00	ADC selector address
ADC	0xC3	ADCADDR31	R/W	XMYP31	YPYM31	XPXM31	ADSEL31[4:0]					0x00	ADC selector address
ADC	0xC4	CCADCHA	R	CCACCH[15:8]								0x00	Coulomb Counter ADC result
ADC	0xC5	CCADCLA	R	CCACCL[7:0]								0x00	Coulomb Counter ADC result
RSVD	0xC6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC8	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC9	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCB	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCC	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCE	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
CHARGER	0xD0	CHRGINT	R	USBOVP	DCLMT	BATDET	USBDET	COMP	TEMP	BATOVP	RSVD	0x00	Charger Interrupt
CHARGER	0xD1	MCHRGINT	R/W	MUSBOVP	MDCLMT	MBATDET	MUSBDET	MCOMP	MTEMP	MBATOVP	RSVD	0x00	Charger Interrupt Mask
CHARGER	0xD2	SCHRGINT	R	SUSBOVP	SDCLMT	SBATDET	SUSBDET	SCOMP	STEMP	SBATOVP	RSVD	0x00	Charger State
CHARGER	0xD3	CHRGSTATE	R	RSVD	RSVD	RSVD	RSVD	RDSTATE[3:0]				0x00	charge State
CHARGER	0xD4	CHRGCNTL	R/W	OTGB	BATISO	CHRG	USBDETHEN	RDSTEN	WDTEN	TRICKLE	CHRENB	0xA1	Charger control
CHARGER	0xD5	CHRGCRNT	R/W	RSVD	CHRGCOMP[2:0]			CHRGCC[3:0]				0x00	Max charge current rate (CC)
CHARGER	0xD6	CHRGVOLT	R/W	RSVD	RSVD	VDSSET[1:0]		CHRGCV[3:0]				0x07	Max charge voltage (CV)
CHARGER	0xD7	CHRGPROT	R/W	USBLMT [1:0]		OVRVOLT [1:0]		WDTSET [1:0]		RSVD	RSVD	0x3C	V, I, and temp protection
CHARGER	0xD8	CHRGPROT2	R/W	TOCP[2:0]			RSVD	RSVD	RSVD	BATOCPSET[1:0]		0x60	Battery Current Limit (during discharge)
CHARGER	0xD9	PROTCMD	W	*	*	*	*	*	*	*	*	0x00	
CHARGER	0xDA	WDTCLR	W	*	*	*	*	*	*	*	*	0x03	
CHARGER	0xDB	CHRGTIMER	R/W	RSVD	RSVD	RSVD	RSVD	CHGTIMER[3:0]				0x03	Charger Timer
RSVD	0xDC	DISCHRG	R/W	RSVD	RSVD	BATDETEN	RSVD	RSVD	TEMPEN	BATOVPEN	BATOCPEN	0x04	Reserved
RSVD	0xDD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDE	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
GPIO	0xE0	GPIOCNTL0	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE1	GPIOCNTL1	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE2	GPIOCNTL2	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE3	GPIOCNTL3	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE4	GPIOCNTL4	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE5	GPIOCNTL5	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE6	GPIOCNTL6	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE7	GPIOCNTL7	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE8	GPIOINT	R	GPIINT7	GPIINT6	GPIINT5	GPIINT4	GPIINT3	GPIINT2	GPIINT1	GPIINT0	0x00	GPIO Interrupt
RSVD	0xE9	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xEA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xEB	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
GPIO	0xEC	GPOSWCTL0	R/W	SCRATCH8[1:0]		SLEW0[1:0]		SWDOUT0	RSVD	RSVD	SWDRV0	0x20	GPIO control
GPIO	0xED	GPOSWCTL1	R/W	SCRATCH9[1:0]		SLEW1[1:0]		SWDOUT1	RSVD	RSVD	SWDRV1	0x20	GPIO control
GPIO	0xEE	GPOSWCTL2	R/W	SCRATCH10[1:0]		SLEW2[1:0]		SWDOUT2	RSVD	RSVD	SWDRV2	0x20	GPIO control
GPIO	0xEF	GPOSWCTL3	R/W	SCRATCH11[1:0]		SLEW3[1:0]		SWDOUT3	RSVD	RSVD	SWDRV3	0x20	GPIO control
GPIO	0xF0	GPOSWCTL4	R/W	SCRATCH12[1:0]		SLEW4[1:0]		SWDOUT4	RSVD	RSVD	SWDRV4	0x00	GPIO control
GPIO	0xF1	GPOSWCTL5	R/W	SCRATCH13[1:0]		SLEW5[1:0]		SWDOUT5	RSVD	RSVD	SWDRV5	0x00	GPIO control
RSVD	0xF2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
GPIO	0xF4	GPO	R/W	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0	0x00	GPO control
RSVD	0xF5	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF8	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
VD2	0xF9 - 0xFF	-	-	VD2								-	Reserved by Customer

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
VD3	0x100 - 0x132	-	-	VD3								-	Reserved by Customer
RSVD	0x133 - 0x17F	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x180	AUD1	R/W	VCETSB	VCEMASTEN	VCEBCLINV	VCEFSJST	VCELONGFS	VCEWORDLEN[2:0]			0x80	Voice Port PCM1
FSL	0x181	AUD2	R/W	VCETRNARND	VCECLKFRQ[2:0]			VCETXSLOT[1:0]		VCE8K16K	VCERESET	0x00	Voice Port PCM1
FSL	0x182	AUD3	R/W	STRTSB	STRMASTEN	STRBCLINV	RSVD	RSVD	STRWORDLEN[2:0]			0x80	Audio Port PCM2
FSL	0x183	AUD4	R/W	STRSRDET	STRCLKFRQ[2:0]			STRSR[3:0]				0x00	Audio Port PCM2
FSL	0x184	AUD5	R/W	RSVD	RSVD	VCERXSLOT[1:0]		VCEAUDHPF	VCECLKEN	VCEFSINV	VCEDLM	0x00	Misc Voice Control
FSL	0x185	AUD6	R/W	STRRESET	STRCLKEN	STRFSINV	RSVD	STRMONO	VCE2PCM2	STRMODESEL	RSVD	0x00	Misc Audio Control
FSL	0x186	AUD7	R/W	RSVD	MIC1BIASMOD	DMICVOL[5:0]						0x00	Digital MIC Control
FSL	0x187	AUD8	R/W	AUDIOOFF	DMICMUTEFB	DMICVOLFB[5:0]						0x80	Digital MIC Control
FSL	0x188	AUD9	R/W	DMICCLKEN	MIC1BIAS	DMICMUTE	MIC2BIAS	DMIC2EN	PCM1RCH	DMICCLK[1:0]		0x00	MIC Control
FSL	0x189	AUD10	R/W	LAMPSEL	LAMPMUT	LAMPVL[5:0]						0x00	MIC / Line-In Control
FSL	0x18A	AUD11	R/W	RAMPSEL	RAMPMUT	RAMPVL[5:0]						0x00	MIC / Line-In Control
FSL	0x18B	AUD12	R/W	PCM2LCH	PCM2RCH	MUXIN	HSDETEN	MIC1PRE[1:0]		MIC2PRE[1:0]		0x00	MIC / Line-In Control
FSL	0x18C	AUD13	R/W	VCECLK[2:0]			VCEPGATX[4:0]					0x00	Voice ADC Control
FSL	0x18D	AUD14	R/W	RSVD	STRCLK[2:0]			STRADC16PGEN	STRADC16PG[2:0]			0x00	Stereo ADC Control
FSL	0x18E	AUD15	R/W	VMUT	RSVD	VDACVL[5:0]						0x00	Voice DAC Control
FSL	0x18F	AUD16	R/W	AMUTL	RSVD	ADACVLL[5:0]						0x00	Audio DAC Left Control
FSL	0x190	AUD17	R/W	AMUTR	RSVD	ADACVLR[5:0]						0x00	Audio DAC Right Control
FSL	0x191	AUD18	R/W	MXLLINL	RSVD	MXLMNDAC	MXLAUDL	RSVD	MUTHPL	MUTHPR	MUTASP	0x00	Left Mixer and Output Select
FSL	0x192	AUD19	R/W	RSVD	MXRLINR	MXRMNDAC	RSVD	MXRAUDR	MUTSPKRL	MUTSPKRR	RSVD	0x00	Right Mixer and Output Select
FSL	0x193	AUD20	R/W	RSVD	RSVD	RAMPVLFB[5:0]						0x00	Analog loop back Right ch Control
FSL	0x194	AUD21	R/W	RSVD	RSVD	LAMPVLFB[5:0]						0x00	Analog loop back Left ch Control
FSL	0x195	AUD22	R/W	PSCNTSPL	PSCNTSPR	RSVD	PSCNTLOL	PSCNTLOR	PSCNTHPL	PSCNTHPR	PSCNTSPKR	0x00	Power Control
FSL	0x196	AUD23	R/W	SLOPESEL[1:0]		PSCNTRX	PSCNTDA	PSCNTMIC1	PSCNTMIC2	STRADCEN	VCEADCEN	0x00	Power Control
FSL	0x197	AUD24	R	RSVD	RSVD	RSVD	RSVD	HSDET	HPDET	SWMPINT	SWLPINT	0x00	Headset Detect Interrupt
FSL	0x198	AUD25	R/W	RSVD	RSVD	RSVD	RSVD	MHSDET	MHPDET	MSWMPINT	MSWLPINT	0x0F	Headset Detect Interrupt Mask
FSL	0x199	AUD26	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	TRIMEN		0x00	Trim enable
FSL	0x19A	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19B	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19C	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19D	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19E	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19F	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A0	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
FSL	0x1A1	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A4	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A5	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A8	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A9	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AB	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AC	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AE	FSLMEM1	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1AF	FSLMEM2	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B0	FSLMEM3	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B1	FSLMEM4	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B2	FSLMEM5	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B3	FSLMEM6	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B4	FSLMEM7	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B5	FSLMEM8	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B6	FSLMEM9	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B7	FSLMEM10	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B8	FSLMEM11	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B9	FSLMEM12	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BA	FSLMEM13	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BB	FSLMEM14	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BC	FSLMEM15	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BD	FSLMEM16	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BE	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1BF	FSLOUTDRVCNTL1	R/W	RESETBDRV[1:0]		PMICINTDRV[1:0]		VRCOMPBDRV[1:0]		PWRGDDRV[1:0]		0x00	Digital Outputs Drive Strength
FSL	0x1C0	FSLOUTDRVCNTL2	R/W	V33ENDRV[1:0]		V3GPAENDRV[1:0]		CLK26MDRV[1:0]		CLK32KDRV[1:0]		0x04	Digital Outputs Drive Strength
FSL	0x1C1	FSLOUTDRVCNTL3	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SPISDODRV		0x01	Digital Outputs Drive Strength
FSL	0x1C2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C4	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C5	FSLVOTGCNTL1	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VOTGDISDSCH	0x01	VOTG Discharge Enable Control
FSL	0x1C6	FSLVOTGCNTL2	R/W	RSVD	RSVD	AOACTLVOTG[2:0]			CTLVOTG[2:0]			0x24	VOTG Control
FSL	0x1C7	FSLVYMXPACNTL	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VYMXPADISDSCH	0x01	VYMXPA Discharge Enable Control
FSL	0x1C8	FSLTONTCNTL1	R/W	VYMX3GTONT	RSVD	VDDQTONT	RSVD	VNNTONT	RSVD	VCCTONT	RSVD	0xAA	Buck Turn On time control (DVS Clk)
FSL	0x1C9	FSLVCCLATCH	R	RSVD	VIDVCC[6:0]							0x7F	VCC VID CONTROL
FSL	0x1CA	FSLVNNLATCH	R	RSVD	VIDVNN[6:0]							0x7F	VNN VID CONTROL

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
FSL	0x1CB	FSLTONTCNTL2	R/W	RSVD	RSVD	RSVD	RSVD	V15TONT	RSVD	V21TONT	RSVD	0xAA	Buck Turn On time control (DVS Clk)
FSL	0x1CC	FSLFAULT1	R	V3GPAFAULT	VYMX3GFAULT	V33FAULT	V15FAULT	V21FAULT	VDDQFAULT	VNNFAULT	VCCFAULT	0x00	Regulator Fault Flag
FSL	0x1CD	FSLFAULT2	R	VPMICFAULT	VPNL18FAULT	VCC180FAULT	VCCAFAULT	VBGFAULT	VBKLTFAULT	VOTGFAULT	VYMXPAFAULT	0x00	Regulator Fault Flag
FSL	0x1CE	FSLFAULT3	R	VCCPFAULT	VMMFAULT	VAONFAULT	VCCPDDRFAULT	VCCPAOACFAULT	VYMCGPSFAULT	VYMXYFIFAULT	VYMXYFI18FAULT	0x00	Regulator Fault Flag
FSL	0x1CF	FSLFAULT4	R	RSVD	RSVD	RSVD	RSVD	VSDIOFAULT	VVIBFAULT	VIMG28FAULT	VIMG25FAULT	0x00	Regulator Fault Flag
FSL	0x1D0	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D1	FSLCHRGCNTL	R/W	RSVD	BUCKDIS	ITRKL	VCOIN[4:2]			COINCHEN	CHGBYP	0x13	Charger Control
FSL	0x1D2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D3	FSLVBKLTCNTL	R/W	TWOPTWOEN	BKLTFREQ2[2:0]	BKLTFREQ2[2:0]	BKLTFREQ2[2:0]	MLED4EN	BKLTLED[2:0]	BKLTIMAX	BKLTIMAX	0x07	Backlight LED Control
FSL	0x1D4	FSL4STRING	R/W	BKLTBRT2[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Secondary Backlight Duty Cycle
FSL	0x1D5	FSLVBKLTADAPT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	S4ADAPT	0x00	Adaptive Boost Control
FSL	0x1D6	FSLLEDR1CNTL	R/W	LEDR1DC[5:0]						LEDR1BLNK		0xFC	Duty Cycle Control for LEDR1
FSL	0x1D7	FSLLEDG1CNTL	R/W	LEDG1DC[5:0]						LEDG1BLNK		0xFC	Duty Cycle Control for LEDG1
FSL	0x1D8	FSLLEDB1CNTL	R/W	LEDB1DC[5:0]						LEDB1BLNK		0xFC	Duty Cycle Control for LEDB1
FSL	0x1D9	FSLLEDR2CNTL	R/W	LEDR2DC[5:0]						LEDR2BLNK		0xFC	Duty Cycle Control for LEDR2
FSL	0x1DA	FSLLEDG2CNTL	R/W	LEDG2DC[5:0]						LEDG2BLNK		0xFC	Duty Cycle Control for LEDG2
FSL	0x1DB	FSLLEDB2CNTL	R/W	LEDB2DC[5:0]						LEDB2BLNK		0xFC	Duty Cycle Control for LEDB2
FSL	0x1DC	FSLLEDRAMPCNTL	R/W	RSVD	RSVD	LEDB2RAMP	LEDG2RAMP	LEDR2RAMP	LEDB1RAMP	LEDG1RAMP	LEDR1RAMP	0x00	Ramp Control for RGB LEDs
FSL	0x1DD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1DE	FSLADCCNTL	R/W	RSVD	TSPAS	ADCCAL	LSBSEL	BATDETVCON	LICON	CHRGICON	VPWRCON	0x00	ADC Spare Channel Control
FSL	0x1DF	CCCREG	R/W	CCFAULT	RSVD	RSVD	CCCALA	CCCALDB	CCDITHER	RSTCC	STARTCC	0x00	Coulomb Counter control & status
FSL	0x1E0	ONECLREG	R/W	ONEC[7:0]								0x1A	Coulomb Counter “oneC” value
FSL	0x1E1	ONECHREG	R/W	RSVD	ONEC[14:8]							0x00	Coulomb Counter “oneC” value
FSL	0x1E2	RAWCCH	-	RAWCC[15:8]								0x00	Unmodified Coulomb Counter output
FSL	0x1E3	RAWCCL	-	RAWCC[7:0]								0x00	Unmodified Coulomb Counter output
FSL	0x1E4	FSLPLLCNTL	R/W	RSVD	RSVD	RSVD	PLLEN	PLL16MEN	PLLDIVIDE[2:0]			0x1B	Reserved
RSVD	0x1E5 - 0x1FA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1FB	BUCK_TOP_LVSH_5	R/W	BUCK_V15_EN	BUCK_V15_PWRSTG_EN<6:0>							0x7F	Switching Regulator Debug
FSL	0x1FC	BUCK_TOP_LVSH_4	R/W	BUCK_V21_EN	BUCK_V21_PWRSTG_EN<6:0>							0x7F	Switching Regulator Debug
FSL	0x1FD	BUCK_TOP_LVSH_3	R/W	BUCK_VYMX3G_EN	BUCK_VYMX3G_PWRSTG_EN<6:0>							0x7F	Switching Regulator Debug
FSL	0x1FE	BUCK_TOP_LVSH_2	R/W	BUCK_VDDQ_EN	BUCK_VDDQ_PWRSTG_EN[6:0]							0x7F	Switching Regulator Debug

Table 116. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
RSVD	0x1FF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
VD2	0x200 - 0x227	-	-	VD2								-	Reserved by Customer
RSVD	0x228 - 0x2FF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved

HARDWARE DESIGN CONSIDERATIONS

EXTERNAL COMPONENT REQUIREMENT

Table 117. External Components BOM

Component	Value	Package	Description	Qty	Part #	Manufacturer
PMIC Chipset						
900841	-	MAPBGA	Main PMIC	1	-	Freescale
900842	-	WLCSP	Buck-Boost Regulator (3.3 V rail)	1	-	Freescale
VCC - (0.65 - 1.2 V) / 3.5 A VID CPU BUCK with External FETs						
Cincc	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Cocc	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	4	AMK107BJ226MA-T	Taiyo Yuden
Lcc	0.68 µH	4x4x2	Saturation current = 4.8 A for 10% drop, DCR_max = 25.3 mohm	1	XPL4020	Coilcraft
Mhscc	46 mohm	BGA	High Side P-FET	1	FDZ293P	Fairchild
Mlscc	23 mohm	BGA	Low Side N-FET	1	FDZ294N	Fairchild
VNN - (0.65 - 1.2 V) / 1.6 A VID CPU BUCK with External FETs						
Cinnn	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Conn	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	2	AMK107BJ226MA-T	Taiyo Yuden
Lnn	1.0 µH	3.3x3.3x1.4	Saturation current = 2.3 A for 10% drop, DCR_max = 55 mohm	1	LPS3314-102ML	Coilcraft
Mnn	95 mohm 68 mohm	MicroFET	High Side P-FET and Low Side N-FET housed in one package	1	FDMA1032CZ	Fairchild
VDDQ - 1.8 V / 1.3 A BUCK						
Cinddq	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Coddq	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	2	AMK107BJ226MA-T	Taiyo Yuden
Lddq	0.50 µH	2.0x2.0x1.0	Saturation current = 1.8 A for 10% drop, DCR_max = 45 mohm	1	XPL2010-501ML	Coilcraft
V21 - 2.1 V / 1.0 A BUCK						
Cin21	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Co21	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	1	AMK107BJ226MA-T	Taiyo Yuden
L21	0.50 µH	2.0x2.0x1.0	Saturation current = 1.8 A for 10% drop, DCR_max = 45 mohm	1	XPL2010-501ML	Coilcraft
V15 - 1.5 V(or 1.6 V) / 1.5 A BUCK						
Cin15	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Co15	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	2	AMK107BJ226MA-T	Taiyo Yuden
L15	0.50 µH	2.0x2.0x1.0	Saturation current = 1.8 A for 10% drop, DCR_max = 45 mohm	1	XPL2010-501ML	Coilcraft
VYMX3G - (YMX: 1.25 V or 3G: 0.6 - 1.375 V) / 1.0 A BUCK						
Cinymx3g	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Coymx3g	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	1	AMK107BJ226MA-T	Taiyo Yuden
Lymx3g	0.50 µH	2.0x2.0x1.0	Saturation current = 1.8 A for 10% drop, DCR_max = 45 mohm	1	XPL2010-501ML	Coilcraft
VYMXPA - 4.2 V / 0.7 A Non-Sync Boost						
Cinymxpa	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata

Table 117. External Components BOM

Component	Value	Package	Description	Qty	Part #	Manufacturer
Coymxpa	22 µF	0805	Ceramic Capacitor, 10 V, X5R	1	LMK212BJ226MG-T	Taiyo Yuden
Lymxpa	2.2 µH	3x3x1.5	Saturation current = 2.1 A for 20% drop, DCR_max = 110 mohm	1	LPS3015-222M	Coilcraft
Dymxpa	-	MICROSMP	SCHOTTKY 1.0 A 20 V	1	MSS1P2L-E3/89A	Vishay
Mymxpa	46 mohm	BGA	P-FET Switch	0	FDZ293P	Fairchild
VOTG - 5.0 V / 0.35 A Non-Sync Boost						
Cinotg	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Cootg	47 µF	0805	Ceramic Capacitor, 6.3 V, X5R	1	JMK212BJ476MG-T	Taiyo Yuden
Lotg	2.2 µH	3x3x1.0	Saturation current = 1.4 A for 20% drop, DCR_max = 220 mohm	1	LPS3010-222M	Coilcraft
Dotg	-	FLIPKY	SCHOTTKY 30 V 0.5 A	1	IR0530CSPTR	Vishay
Motg	85 mohm	WLCSP	P-FET Switch	1	FDZ191P	Fairchild
VBKLT - 5s3p (Backlight) and 5s1p (Camera Scene) / 120 mA Non-sync Boost						
Cinbklt	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Cobklt	10 µF	1206	Ceramic Capacitor, 25 V, X5R	1	GRM31CR61E106KA12L	Murata
Lbklt	2.2 µH	3x3x1.5	Saturation current = 2.1 A for 20% drop, DCR_max = 110 mohm	1	LPS3015-222M	Coilcraft
Dbklt	-	FLIPKY	SCHOTTKY 30 V 0.5 A	1	IR0530CSPTR	Vishay
V33 - 3.3 V / 1.4 A Buck-Boost - Standalone Chip						
Cin33	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
Co33	22 µF	0805	Ceramic Capacitor, 10 V, X5R	2	LMK212BJ226MG-T	Taiyo Yuden
L33	1.0 µH	3.3x3.3x1.4	Saturation current = 2.3 A for 10% drop, DCR_max = 55 mohm	1	LPS3314-102ML	Coilcraft
Ccore33	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
Cbgbyp33	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
VBG - 1.25 V/2.0 mA LDO & VCCA - 1.5 V/150 mA LDO						
Cin1p8	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Cobg	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
Cocca	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VCC180- 1.8 V/390 mA LDO & VPNL18- 1.8 V/225 mA LDO & - 1.8 V/50 mA LDO						
Cin2p1	0.47 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J474KE19D	Murata
Cocc180	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
Copnl18	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
Copmic	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VYMXYFI18 - (YMX:1.8 V/200 mA - YFI:1.8 V/200 mA) LDO						
Cinymxyfi18	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Coymxyfi18	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VYMXYFI - (YMX:2.5 V/150 mA - YFI:1.2 V/60 mA) LDO						
Cinymxyfi	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Coymxyfi	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VYMXGPS - (YMX:1.3 V/350 mA - GPS:1.8 V/170 mA) LDO						
Cinymxgps	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Coymxgps	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VCCPAOAC- 1.05 V/155 mA LDO & VCCPDDR - 1.05 V/60 mA LDO & VAON - 1.2 V/250 mA LDO &VMM- 1.2 V/5.0 mA LDO & VCCP - 1.05 V/445 mA LDO						
Cin1p5	0.47 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J474KE19D	Murata
Coccpaoac	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
Coccpddr	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
Coaon	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata

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Table 117. External Components BOM

Component	Value	Package	Description	Qty	Part #	Manufacturer
Comm	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
Coccp	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VIMG25- 2.5 V/80 mA LDO & VIMG28- 2.8 V/225 mA LDO						
Cinimg	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Coimg25	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
Coimg28	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VVIB - xV/200 mA LDO						
Cinvib	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Covib	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VPNL33 - 3.3 V/100 mA Switch & VGP33 - 3.3 V/60 mA Switch & VYMXGPS33 - 3.3 V/60 mA Switch						
Copnl33	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Cogp33	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Coymxgps33	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
VSDIO - 3.3 V/215 mA Switch OR 1.8 V/215 mA LDO						
Cinsdio	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Cosdio	4.7 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	ECJ-0EB0J475M	Panasonic
Rsdio	470 mohm	0402	Chip Resistor, 1%	1	ERJ-2BQFR47X	Panasonic
Msdio	95 mohm	SC70	PFET, switch	1	FDG332PZ	Fairchild
Internal Supplies						
Ccore	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
Ccoredig	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
Ccoreref	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Audio						
Rmcbiasr	2.2 kohm	0201	Chip Resistor, 5% - Handset Microphone	1	ERJ-1GEJ222C	Panasonic
Cmc1r	220 nF	0201	Ceramic Capacitor, 6.3 V, X5R - Handset Microphone	1	GRM033R60G224ME15D	Murata
Rmcbiasl	2.2 kohm	0201	Chip Resistor, 5% - Handset Microphone 2, Optional	0	ERJ-1GEJ222C	Panasonic
Cmc1l	220 nF	0201	Ceramic Capacitor, 6.3 V, X5R - Handset Microphone 2, Optional	0	JMK063BJ224MP-F	Taiyo Yuden
Rmcbias2	2.2 kohm	0201	Chip Resistor, 5% - Headset Microphone	1	ERJ-1GEJ222C	Panasonic
Cmc2	220 nF	0201	Ceramic Capacitor, 6.3 V, X5R - Headset Microphone	1	JMK063BJ224MP-F	Taiyo Yuden
Crxinl	220 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	JMK063BJ224MP-F	Taiyo Yuden
Crxinr	220 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	JMK063BJ224MP-F	Taiyo Yuden
Crxoutl	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Crxoutr	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Ccpin	1.0 F	0402	Ceramic Capacitor, 6.3 V, X5R - Charge Pump Input Cap	1	GRM155R60J105ME19D	Murata
Ccpout	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
Ccp	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R - Charge Pump Flying Cap	1	GRM155R60J105ME19D	Murata
Crefa	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R - Reference A	1	GRM033R60J104KE19D	Murata
Crefb	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R - Reference B	1	GRM033R60J104KE19D	Murata
Crefd	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R - Reference D	1	GRM155R60J105ME19D	Murata
XTALAUDIO	26 MHz	2x1.6x0.45	26.000 MHz Crystal	1	NX2016AB-26MHZ SB1	NDK
Cxtalaudio1	15 pF	0201	Ceramic Capacitor, 25 V, C0G	1	GRM0335C1E150JD01D	Murata
Cxtalaudio2	15 pF	0201	Ceramic Capacitor, 25 V, C0G	1	GRM0335C1E150JD01D	Murata

Table 117. External Components BOM

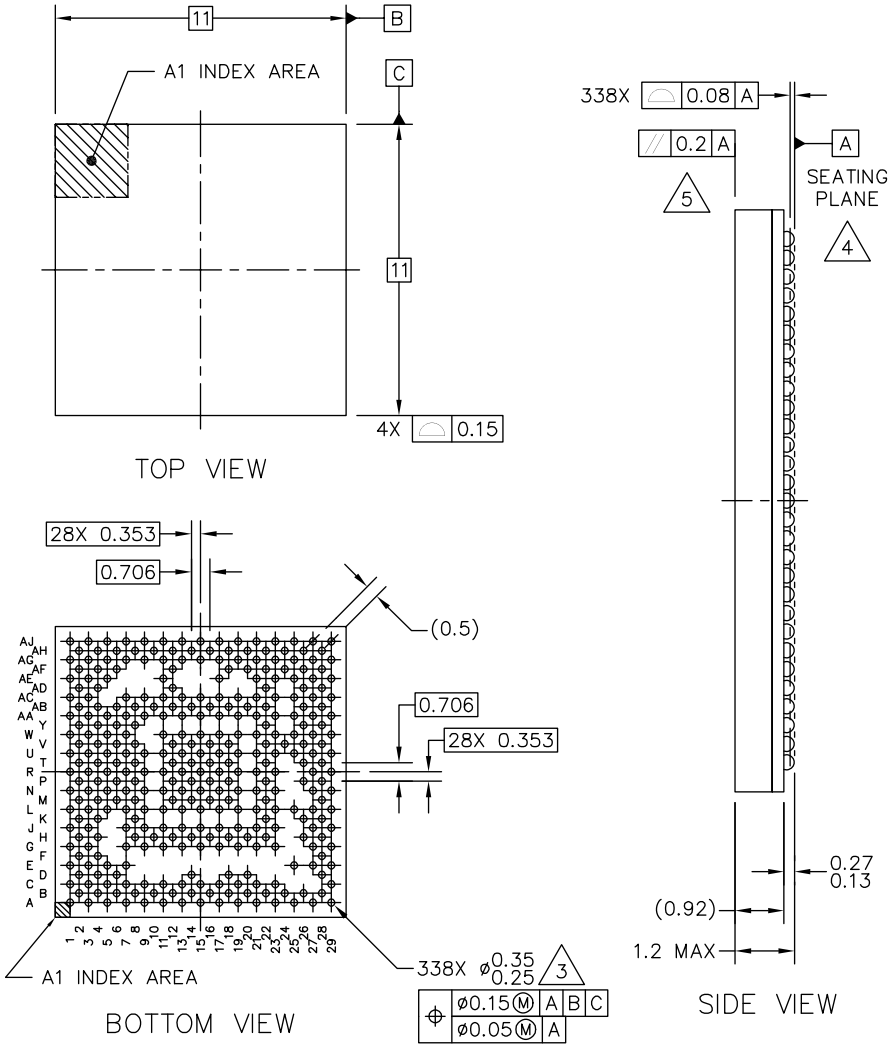
Component	Value	Package	Description	Qty	Part #	Manufacturer
Switching Charger						
Crawchg	1.0 µF	0603	Ceramic Capacitor, 35 V, X5R	1	GMK107BJ105KA-T	Taiyo Yuden
Movpchg	46 mohm	BGA	P-FET Switch, 20 V - Better area and efficiency	1	FDZ293P	Fairchild
Mrevpchg	46 mohm	BGA	P-FET Switch, 20 V - Better area and efficiency	1	FDZ293P	Fairchild
Rinsnschg	100 mohm	0805	Chip Resistor, 1%, 0.333 W	1	RP2012T-R10-F	Susumu
Cinchg	10 µF	0805	Ceramic Capacitor, 16 V, X5R	1	GRM21BR61C106KE15L	Murata
Mswchg	95 mohm 68 mohm	MicroFET	High Side P-FET and Low Side N-FET housed in one package	1	FDMA1032CZ	Fairchild
Lchg	1.0 µH	3.3x3.3x1.4	Saturation current = 2.3 A for 10% drop, DCR_max = 55 mohm	1	LPS3314-102ML	Coilcraft
Cochg	22 µF	0805	Ceramic Capacitor, 10 V, X5R	2	LMK212BJ226MG-T	Taiyo Yuden
Mchg	85 mohm	WLCSP	Pass FET for Linear Charger and Switch for application supply	1	FDZ191P	Fairchild
Mchgbyp	30 mohm	MicroFET	Bypass Switch to reduce drop from V_{BAT} to V_{PWR} - Optional	1	FDMA510PZ	Fairchild
Rsnsbat	100 mohm	1206	Chip Resistor, 1%, 0.5 W	1	ERJ-8BWFR100V	Panasonic
Rcc	20 mohm	0805	Chip Resistor, 1%, 0.25 W - Increased in power for 5.0 A operation	1	ERJ-6BWFR020V	Panasonic
Ccc	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Rntc	10 kohm	0201	Chip Resistor, 1%	1	ERJ-1GEF1002C	Panasonic
Coin cell						
Ccoin	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
ADC						
Cadref	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
Oscillator and Real Time Clock - RTC						
XTALRTC	32.768 kHz	3.2x1.5x0.9	CRYSTAL 32.768 kHZ 12.5 pF SMD	1	ABS07-32.768KHZ-T	Abracon
Cxtalrtc1	22 pF	0201	Ceramic Capacitor, 25 V, C0G	1	GRM0335C1E220JD01D	Murata
Cxtalrtc2	22 pF	0201	Ceramic Capacitor, 25 V, C0G	1	GRM0335C1E220JD01D	Murata
NotesGPIOs & GPOSWs & GPOs & Power Button						
Rpullupx	100 kohm	0201	Chip Resistor, 1% - Pull-up Resistors for OD configured GPIOs	0	ERJ-1GEF1003C	Panasonic
ESD/EMI Components						
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Handset Microphone Bias	1	GRM0335C1E330JD01D	Murata
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Handset Microphone 1	1	GRM0335C1E330JD01D	Murata
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Handset Microphone 2, Optional	0	GRM0335C1E330JD01D	Murata
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Headset Microphone Bias	1	GRM0335C1E330JD01D	Murata
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Handset Ear piece	1	GRM0335C1E330JD01D	Murata
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Handset Ear piece	1	GRM0335C1E330JD01D	Murata
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Handset Loudspeaker	1	GRM0335C1E330JD01D	Murata
-	33 pF	0201	Ceramic Capacitor, 25 V, C0G - Handset Loudspeaker	1	GRM0335C1E330JD01D	Murata
-	-	-	Headset Microphone and Headphones	1	EMI ESD	On Semi
-	-	-	Handset Loudspeaker	1	EMI ESD	On Semi
Total Component Count				134		

Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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TITLE: PBGA, THIN PROFILE, FINE PITCH, 338 I/O, 11 X 11 PKG, INTERSTITIAL PITCH (MAP)	DOCUMENT NO: 98ASA10841D	REV: O	
	CASE NUMBER: 2037–01	11 JUN 2008	
	STANDARD: NON–JEDEC		

VK SUFFIX
338-PIN
98ASA10841D
REVISION 0

900841

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: PBGA, THIN PROFILE, FINE PITCH, 338 I/O, 11 X 11 PKG, INTERSTITIAL PITCH (MAP)	DOCUMENT NO: 98ASA10841D	REV: O
	CASE NUMBER: 2037–01	06 JUN 2008
	STANDARD: NON–JEDEC	

VK SUFFIX
338-PIN
98ASA10841D
REVISION 0

900841

PACKAGE MECHANICAL OUTLINE DRAWING

The package style is an 11x11 fine interstitial pitch, thin profile PBGA. The package has a semi populated matrix that includes 338 balls. The ball count includes 322 assigned signal pins and four sets of 4 corner balls.

PACKAGE ASSEMBLY RECOMENDATIONS

For improved protection against mechanical shock, Freescale recommends applying corner glue to the mounted SC900841 BGA package. This corner glue application is described in the AN3954 - "PCB Layout Guidelines for SC900841 and SCCSP900842 application note.

Freescale's preferred material for the corner glue application is the Loctite 3128 board level adhesive applied at a 0° or 45° dispense angle in a continuous motion and with the fillet length extended to a minimum of 3 ball rows and columns at each corner.

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	2/2011	• Initial release

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