NILE Series

Bluetooth 5.0/Bluetooth Mesh/Thread/802.15.4 + NFC-A Standalone Module

NILE module Datasheet

Version 1.0

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1 Overview

NILE is an ultra-low power certified full featured Bluetooth 5.0 standalone module. This small form-factor module reduces design cost and time to market by integrating a powerful ARM Cortex-M4 with 1MB FLASH and 256KB RAM, high performance antenna, all the needed components and crystals. NILE with fine-tuned RF provides exceptional performance, long range and very low power. NILE can support 802.15.4 Thread/Zigbee concurrently with Bluetooth. By supporting Bluetooth Mesh, this module reduces the deployment cost and provides flexibility. NILE enables touch-to-pair feature by supporting NFC-A.

NILE reduces user's development cost and time to market with integrated Bluetooth stack, application APIs and all the advanced security features (ARM Trust Zone Cryptocell-310). NILE module is based on Nordic nRF52840 SoC and comes with a highly efficient development environment for ease of application development in various IoT verticals like Wearables, Home automation, Industrial IoT and smart medical.

Module specifications

- Wireless Protocols : Bluetooth 5, Thread, Zigbee, NFC, ANT^{+}
- Frequency : 2.402 – 2.480 GHz
- On-air Data rates :
  - Bluetooth 5 - 2Mbps, 1Mbps, 500kbps, 125kbps
  - 802.15.4 - 250kbps
  - NFC - 106kbps
- Security Features : ARM CryptoCell 310, 128-bit AES HW accelerator, Secure boot and all security features of BLE specification
- Antenna options : PCB Trace Antenna or MHF4 connector
- Operating modes : BLE, BLE Mesh(Adopted profiles), Zigbee, Thread, BLE + Zigbee, BLE + Thread and ANT $^{+}$
- Programmable output power : -40dBm to +8dBm
- Application Peak Throughput: 1317.47Kbps
- Receive Sensitivity : Bluetooth 5.0
  - -103dBm at 125kbps
  - -99dBm at 500kbps
  - -96dBm at 1Mbps
  - -92dBm at 2Mbps
- Receive Sensitivity : 802.15.4
  - -100dBm at 250kbps
- Current consumption :
  - 450nA – Deep sleep mode
  - 1.5µA – System standby mode, no RAM retention
  - 4.8mA – TX at 0dBm output power
- NFC : NFC-A (Type 2) Tag with wake-on field, "Touch to pair" support , OOB pairing

- GPIO : 46 configurable
- Range : > 1400 meters
- Power supply and operating voltage range : Integrated DC-DC, 1.7v to 5.5v
- Temperature : -40°C to 85°C
- Humidity : 5-90% non-condensing
- Package : 10 mm x 15 mm x 1.6 mm (including shield), 0.5mm pitch

2 Features

2.1 NILE Features

- Full featured Bluetooth 5.0 - Long Range, 2Mbps, improved co-existence and advertising extensions.
- Supports advanced mesh networking protocols - Certified software stacks for Bluetooth Mesh, Thread and Zigbee
- Powerful Open CPU: 32bit, 64MHz ARM Cortex-M4 CPU with Floating Point Unit (FPU) and has 1MB flash with cache and 256kB RAM that stands enough for customer's high end applications
- Highly optimized hardware for ultra-low power consumption with excellent performance
- Support for secure boot, BLE secure connections and privacy
- ARM® CryptoCell 310 cryptographic accelerator and AES 128 bit encryption
- Over the air device firmware upgrade (OTA DFU)
- Generic GATT client and server APIs
- Nordic SDK with examples and comprehensive documentation covers all the features supported by the module. SDKs are available for BLE, Bluetooth Mesh, Thread, Zigbee, ANT and HomeKit
- NFC Tag A support
- 3.3V or 5V power supply with integrated switching regulator

Interfaces

- 2 x UART
- Up-to 4 x SPI master/ 3x SPI slave
- 2 x I2C master, 1 x I2C slave
- 1 x I2S
- 1 x PWM
- 1 x Quadrature decoder
- 1 x PDM
- 12bit, 8 x ADC channels
- 32-bit timers x 5, RTC x 3
- 20 channel programmable peripheral interface
- 1x USB

Certifications

- Regulatory certifications - FCC/IC, ETSI
- BT SIG 5 product level (module) certification

Full Featured Bluetooth 5

It supports all Bluetooth 5 features including Long range (125kbps and 500kbps), 2Mbps, advertising extensions and improved co-existence

Bluetooth mesh and Thread support

The NILE is ideal for building products and infrastructure employing mesh networking. It has hardware and software support for Bluetooth mesh with nRF5 SDK for Mesh. It is a Thread certified component and is supported by the nRF5 SDK for Thread for those building Thread compatible products

Processing power and flash flexibility

The NILE incorporates the powerful ARM Cortex-M4 CPU with Floating Point Unit (FPU) running at 64 MHz enabling the most demanding applications with complex arithmetic requirements to be realized in a single chip solution.

It has got a flash-based SoC and offers all the flexibility associated with using flash memory. It supports Over-The-Air Device Firmware Updates (OTA-DFU) when it is in the field.

On-chip NFC tag support

NFC™-A tag support is included on chip. NFC Type 2 and Type 4 tag emulation protocol stacks are provided by Nordic opening up a range of new applications, like NFC payment, and improved user experience for existing Bluetooth applications with Out-of-Band (OOB) pairing. OOB pairing using NFC simplifies the process of authenticated pairing between two Bluetooth devices by exchanging authentication information over an NFC link.

- NFC-A listen mode operation
- 13.56 MHz input frequency
- Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode

Applications:

- Advanced high performance wearable’s
- Wearables for secure payments
- Virtual Reality/Augmented Reality systems
- Smart Home sensor networks
- Smart city sensor networks
- High performance HID controllers
- Internet of Things (IoT) sensor networks

- Smart door locks
- Smart lighting networks
- Connected white goods

3 Module block Diagram

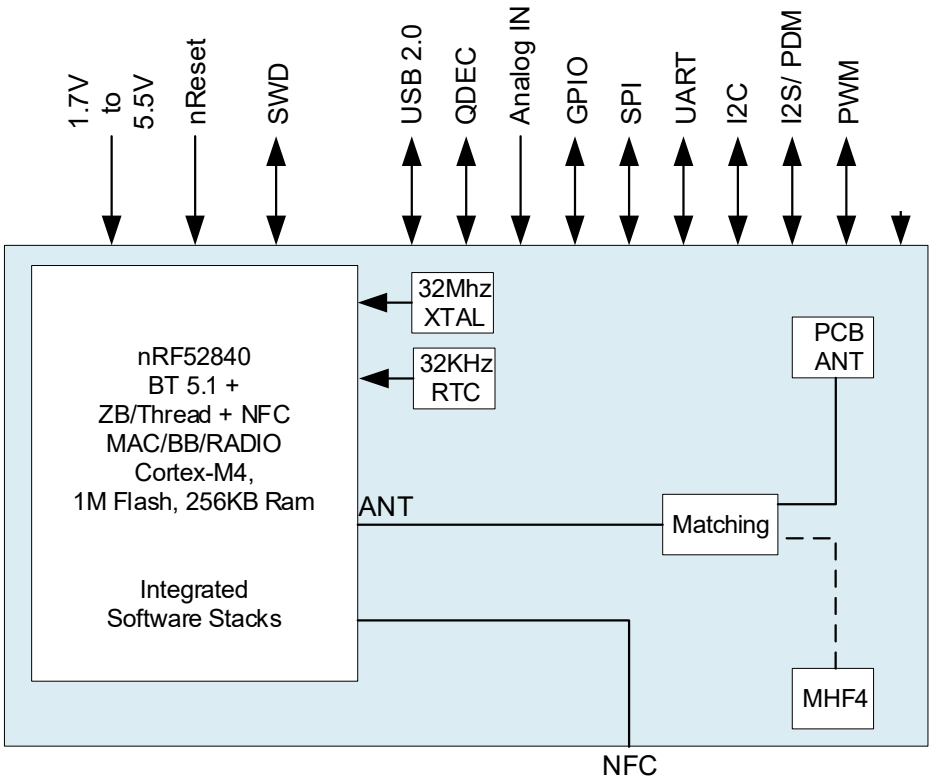

Figure 1 : Block diagram

4 Pin Definition

4.1 Pin-out with description

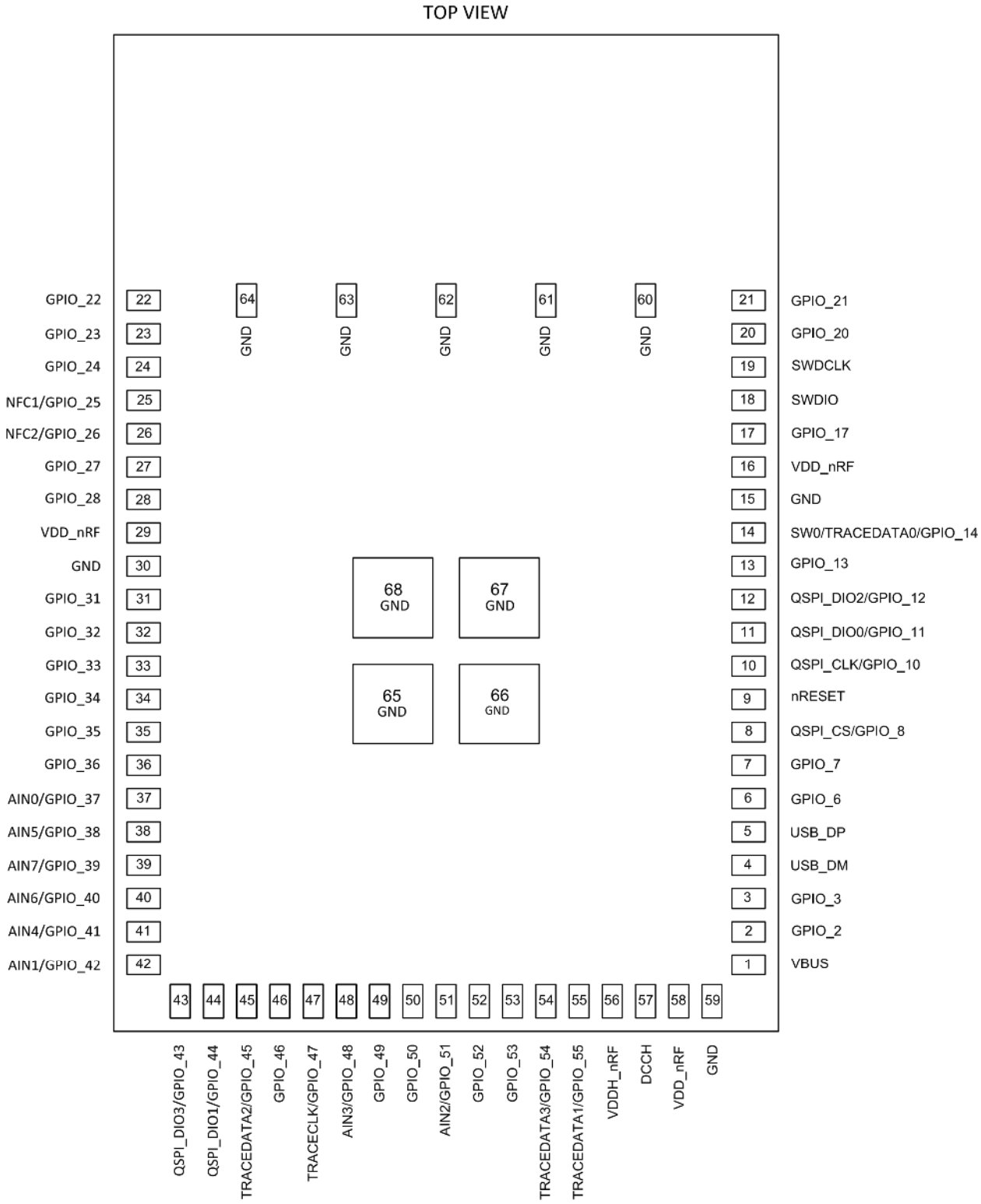

Figure 2 : Showing pin out

4.2 Pin Table

Pin Number	Pin Name	Pin Type	Description	nRF52 Pin
1	VBUS	Power	5V input from USB	
2	GPIO_2	I/O	General purpose IO	P0.13
3	GPIO_3	I/O	General purpose IO	P0.15
4	USB_DM	AI/AO	Digital I/O USB D+	
5	USB_DP	AI/AO	Digital I/O USB D-	
6	GPIO_6	I/O	General purpose IO	P0.14
7	GPIO_7	I/O	General purpose IO	P0.16
8	QSPI_CS/GPIO_8	I/O	General purpose IO Recommended pin for QSPI_CS	P0.17
9	nRESET	I/O	Active low reset	P0.18
10	QSPI_CLK/GPIO_10	I/O	General purpose IO Recommended pin for QSPI_CLK	P0.19
11	QSPI_DIO0/GPIO_11	I/O	General purpose IO Recommended pin for QSPI_DIO0	P0.20
12	QSPI_DIO2/GPIO_12	I/O	General purpose IO Recommended pin for QSPI_DIO2	P0.22
13	GPIO_13	I/O	General purpose IO	P0.24
14	SWO/TRACEDATA0/GPIO_14	I/O	General purpose IO May be used for parallel/serial trace debug	P1.00
15	GND	Ground	Ground pad	
16	VDD_nRF	Power	3.3V DCDC output Power supply. When 5V input is used, this pin can supply 3.3V accessories (max 20mA drive)	
17	GPIO_17	I/O	General purpose IO	P0.25
18	SWDIO	I/O	Serial wire debug I/O for debug and programming	
19	SWDCLK	I	Serial wire debug clock input for debug and programming	
20	GPIO_20	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.01
21	GPIO_21	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.02
22	GPIO_22	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.03
23	GPIO_23	I/O	General purpose IO	P1.04
24	GPIO_24	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.06
25	NFC1/GPIO_25	I/O	May be configured as General purpose IO if NFC is not used Recommended for Standard drive, low frequency I/O	P0.09
26	NFC2/GPIO_26	I/O	May be configured as General purpose IO if NFC is not used Recommended for Standard drive, low frequency I/O	P0.10
27	GPIO_27	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.07
28	GPIO_28	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.05
29	VDD_nRF	Power	3.3V DCDC output Power supply. When 5V input is used, this pin can supply 3.3V accessories (max 20mA drive)	
30	GND	Ground	Ground pad	
31	GPIO_31	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.14
32	GPIO_32	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.10
33	GPIO_33	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.11

34	GPIO_34	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.12
35	GPIO_35	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.13
36	GPIO_36	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.15
37	AIN0/GPIO_37	AI/IO	General purpose IO / Analog input 0 Recommended for Standard drive, low frequency I/O	P0.02
38	AIN5/GPIO_38	AI/IO	General purpose IO / Analog input 5 Recommended for Standard drive, low frequency I/O	P0.29
39	AIN7/GPIO_39	AI/IO	General purpose IO / Analog input 7 Recommended for Standard drive, low frequency I/O	P0.31
40	AIN6/GPIO_40	AI/IO	General purpose IO / Analog input 6 Recommended for Standard drive, low frequency I/O	P0.30
41	AIN4/GPIO_41	AI/IO	General purpose IO / Analog input 4 Recommended for Standard drive, low frequency I/O	P0.28
42	AIN1/GPIO_42	AI/IO	General purpose IO / Analog input 1 Recommended for Standard drive, low frequency I/O	P0.03
43	QSPI_DIO3/GPIO_43	I/O	General purpose IO Recommended pin for QSPI_DIO3	P0.23
44	QSPI_DIO1/GPIO_44	I/O	General purpose IO Recommended pin for QSPI_DIO1	P0.21
45	TRACEDATA2/GPIO_45	I/O	General purpose IO	P0.11
46	GPIO_46	I/O	General purpose IO	P1.08
47	TRACECLK/GPIO_47	I/O	General purpose IO	P0.07
48	AIN3/GPIO_48	AI/IO	General purpose IO / Analog input 3	P0.05
49	GPIO_49	I/O	General purpose IO	P0.27
50	GPIO_50	I/O	General purpose IO	P0.26
51	AIN2/GPIO_51	AI/IO	General purpose IO / Analog input 2	P0.04
52	GPIO_52	I/O	General purpose IO	P0.06
53	GPIO_53	I/O	General purpose IO	P0.08
54	TRACEDATA3/GPIO_54	I/O	General purpose IO	P1.09
55	TRACEDATA1/GPIO_55	I/O	General purpose IO	P0.12
56	VDDH_nRF	Power	5V external supply	
57	DCCH	Power	First DCDC (5V to 3.3V) output. Add a 10uH between this pin and pin 16 when 5V DCDC is enabled	
58	VDD_nRF	Power	3.3V DCDC output Power supply. When 5V input is used, this pin can supply 3.3V accessories (max 20mA drive)	
59	GND	Ground	Ground pad	
60	GND	Ground	Ground pad	
61	GND	Ground	Ground pad	
62	GND	Ground	Ground pad	
63	GND	Ground	Ground pad	
64	GND	Ground	Ground pad	
65	GND	Ground	Ground pad	
66	GND	Ground	Ground pad	
67	GND	Ground	Ground pad	
68	GND	Ground	Ground pad	

Table 1: NILE Pin Table

5 Electrical Specifications

5.1 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Parameter	Min.	Max.	Units
Supply voltages			
VDD	-0.3	+3.9	V
VDDH	-0.3	+5.8	V
VBUS	-0.3	+5.8	V
VSS		0	V
I/O pin voltage			
$V_{I/O}$, VDD <=3.6V	-0.3	VDD + 0.3	V
$V_{I/O}$, VDD >=3.6V	-0.3	3.9	V
NFC antenna pin current			
$I_{NFC1/2}$		80	mA
Radio			
RF input level		10	dBm
Environmental aQFN™ package			
Storage temperature	-40	+125	^{0}C
Moisture Sensitivity Level		2	
ESD Human Body Model		2	kV
ESD Human Body Model Class		2	
ESD Charged Device Model		750	V
Flash memory			

Endurance		10000	Write/erase cycles
Retention		10 years at 40^{0}C	

Table 2: Absolute maximum ratings

5.2 Recommended operating conditions

The operating conditions are the physical parameters that the module can operate within.

Symbol	Parameter	Min.	Nom.	Max.	Units
VDD	VDD supply voltage, independent of DCDC enable	1.7	3.0	3.6	V
VDD_{POR}	VDD supply voltage needed during power-on reset	1.75			V
VDDH	VDDH supply voltage, independent of DCDC enable	2.5	3.7	5.5	V
VBUS	VBUS USB supply voltage	4.35	5	5.5	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)			60	ms
t_{R_VDDH}	Supply rise time (0 V to 3.7 V)			100	ms
TA	Operating temperature	-40	25	85	^{0}C

Table 3: Recommended operating conditions

Important: The module power-on reset circuitry may not function properly for rise times longer than the specified maximum.

5.3 Performance specifications

5.3.1 Radio performance specifications

5.3.1.1 General radio characteristics

Symbol	Description	Min.	Typ.	Max.	Units
f_{op}	Operating frequencies	2360		2500	MHz
$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,1M}$	Frequency deviation @1 Mbps		±170		kHz

$f_{DELTA,BLE,1M}$	Frequency deviation @BLE 1 Mbps		±250		kHz
$f_{DELTA,2M}$	Frequency deviation @2 Mbps		±320		kHz
$f_{DELTA,BLE,2M}$	Frequency deviation @BLE 2 Mbps		±500		kHz
fsk_{BPS}	On-the-air data rate	125		2000	kbps
$f_{Chip,\ IEEE\ 802.15.4}$	Chip rate in IEEE 802.15.4 mode		2000		kchips

Table 4: General radio characteristics

5.3.1.2 Receiver characteristics

Symbol	Description	Min.	Typ.	Max.	Units
$P_{RX,MAX}$	Maximum received signal strength at < 0.1% PER		0		dBm
$P_{SENS,IT,1M}$	Sensitivity, 1 Mbps nRFmode ideal transmitter[18]		-93		dBm
$P_{SENS,IT,2M}$	Sensitivity, 2 Mbps nRF mode ideal transmitter[19]		-89		dBm
$P_{SENS,IT,SP,1M,BLE}$	Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≤ 37 bytes BER=1E-3[20]		-95		dBm
$P_{SENS,IT,LP,1M,BLE}$	Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≥ 128 bytes BER=1E-4[21]		-94		dBm
$P_{SENS,IT,SP,2M,BLE}$	Sensitivity, 2 Mbps BLE ideal transmitter, packet length ≤ 37 bytes		-92		dBm
$P_{SENS,IT,BLE\ LE125k}$	Sensitivity, 125 Kbps BLE mode		-103		dBm
$P_{SENS,IT,BLE\ LE500K}$	Sensitivity, 500 Kbps BLE mode		-99		dBm
$P_{SENS,IEEE\ 802.15.4}$	Sensitivity in IEEE 802.15.4		-100		dBm

Table 5: Receiver characteristics

[18] Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR [1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3 dB

[19] Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR [1...7] are Used for receiver address correlation, the typical sensitivity for this mode is degraded by 3 dB

[20] As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

[21] Equivalent BER limit < 10E-04

5.3.1.3 Transmitter characteristics

Symbol	Description	Min.	Typ.	Max.	Units
P_{RF}	Maximum output power		8.0		dBm
P_{RFC}	RF power control range		28.0		dB
P_{RFCR}	RF power accuracy			±4	dB
$P_{RF1,1}$	1st Adjacent Channel Transmit Power 1 MHz (1 Mbps)		-24.8		dBc
$P_{RF2,1}$	2nd Adjacent Channel Transmit Power 2 MHz (1 Mbps)		-54.0		dBc
$P_{RF1,2}$	1st Adjacent channel Transmit Power 2 MHz (2 Mbps)		-25		dBc
$P_{RF2,2}$	2nd Adjacent Channel Transmit Power 4 MHz (2 Mbps)		-54.0		dBc
E_{VM}	Error vector magnitude IEEE 802.15.4		8		%rms
$P_{harm2nd, IEEE 802.15.4}$	2nd harmonics in IEEE 802.15.4 mode		-51.0		dBm
$P_{harm3rd, IEEE 802.15.4}$	3rd harmonics in IEEE 802.15.4		-48.0		dBm

Table 6: Transmit characteristics

5.3.1.4 RSSI Specifications

Symbol	Description	Min.	Typ.	Max.	Units
$RSSI_{ACC}$	RSSI accuracy valid range -90 to -20 dBm		±2		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	RSSI sampling time from RSSI_START task		0.25		µs
$RSSI_{SETTLE}$	RSSI settling time after signal level change		15		µs

Table 7: RSSI

5.3.2 NFC Power and Performance

5.3.2.1 NFCT active (Near Field Communication Tag)

Symbol	Description	Min.	Typ.	Max.	Units
I_{sense}	Current in SENSE STATE		100		nA
$I_{activated}$	Current in ACTIVATED STATE		400		µA

Table 8: NFCT active

5.3.2.2 NFCT Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
f_c	Frequency of operation		13.56		MHz
C_{MI}	Carrier modulation index	95			%
DR	Data Rate		106		kbps
V_{sense}	Peak differential Field detect threshold level on NFC1 NFC2		1.2		Vp
I_{max}	Maximum input current on NFCT pins			80	mA

Table 9: NFCT electrical specification

6 Functional description

6.1 RTC

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). This counter can generate multiple interrupts and events to the CPU and radio as well as internal and external hardware blocks. These events can be precisely timed ranging from microseconds up to hours, and allows for periodic BLE advertising events etc., without involving the CPU. The RTC can be operated in the active and standby modes.

6.2 RESET pin

Module reset can be triggered by following methods

- Power on reset generator
- Pin reset
- Wake up from system off mode
- Soft reset
- Brownout reset

6.3 CPU and Memory

The Nordic Semiconductor nRF52840 chip in the NILE series modules includes a powerful Arm Cortex M4 processor. The processor works with a superset of 16 and 32-bit instructions (Thumb-2) at 64 MHz clock speed. It can use up to 37 interrupt vectors and 3 priority bits. The nRF52840 chip has 1 MB of flash and 256 KB of RAM for code and data storage. Additionally, up to 4 GB of external memory can be added with Execute in Place (XIP) support via the QSPI interface.

RAM can be retained in system OFF/ ON modes. A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source.

6.4 DMA

EasyDMA is a module implemented by some peripherals to gain direct access to Data RAM. EasyDMA cannot access the flash. A peripheral can implement multiple EasyDMA instances to provide dedicated channels.

6.5 UART

UART is a 4-wire serial interface which supports hardware flow control and baud rate up to 1Mbps.

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) is used to for direct data transfer from/to RAM.

Features:

- Full-duplex operation
- Automatic hardware flow control (Disabled by default)
- Parity checking and generation for the 9th data bit
- UART uses TXD and RXD registers to transmit and receive data. UART uses one or two STOP bit.
- Disable all peripherals that have the same ID as UART. It is important to configure all relevant UART registers explicitly to ensure UART operates correctly.

6.6 USB

The USB device (USBD) controller implements a full speed USB 2.0 device function

Features:

- Full speed 12Mbps USB 2.0 controller including on-chip PHY USB transceiver which is powered separately from rest of device.
- Provides CDC driver/Virtual UART as well as usb_audio, usb_hid, usb_generic, usb_msc (mass storage device) classes via Nordic SDK

Pin description:

The signal pins consist of the D+ and D- pins, which are to be connected to the USB host and will operate only while VBUS is in its valid voltage range (4.35V to 5.5V)

6.7 SPI

Features:

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. CPU must use available GPIOs to select the correct slave and control this independently of the SPI master.

Supports up to three Serial Peripheral Interfaces with serial clock frequencies of up to 8 MHz

Pin description:

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

Pin configuration in master mode:

- SCLK, Serial clock output, up to 8 MHz
- MOSI, Master Output Slave Input data line
- MISO, Master Input Slave Output data line
- CS, Chip/Slave select output, active low, selects which slave on the bus to talk to.
- Only one select line is enabled by default but more can be added by customizing a GPIO pin. DCX, Data/Command signal, this signal is optional but is sometimes used by the SPI slaves to distinguish between SPI commands and data.

Pin configuration in slave mode:

- SCLK, Serial clock input
- MOSI, Master Output Slave Input data line
- MISO, Master Input Slave Output data line
- CS, Chip/Slave select input, active low, connects/disconnects the slave interface from the bus.

The serial clock supports both normal and inverted clock polarity (CPOL) and data should be captured on rising or falling clock edge (CPHA).

6.8 I2C interface

- The TWI master is compatible with I2C operating at 100 kHz and 400 kHz.
- This TWI master supports clock stretching performed by the slaves.
- When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.
- TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus
- Supports data rates: 100 kbps, 250 kbps, or 400 kbps
- The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA).

- The protocol makes it possible to interconnect up to 127 individually addressable devices.
- The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

6.9 I2S interface

Features:

The I2S (Inter-IC Sound) module, supports the original two-channel I2S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention. The I2S module supports both transmission (TX) and reception (RX) of serial data. The most significant bit (MSB) is always transmitted first.

The I2S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bidirectional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

Pin description:

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I2S module are mapped to physical pins

- MCK - The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode. The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.
- SCK - The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT. When operating in Master mode the SCK is generated from the MCK
- LRCK - The Left Right Clock (LRCK) is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN

6.10 QSPI interface

Features:

Quad Serial Peripheral Interface enables external memory to be connected to NILE module to increase the application program size.

- 2–32 MHz configurable clock frequency
- Single-word read/write access from/to external flash
- Execute in place (XIP) for executing program directly from external flash
- XIP execution speed: Up to 8 million instructions fetches per second for 16 bit instructions, up to 4 million instruction fetches per second for 32 bit instructions.
- Configure, write, read, erase, execute in place, send custom instructions
- The external flash memory can be put in deep power-down mode (DPM) to minimize its current consumption when there is no need to access the memory

Pin description:

The QSPI always operates in master mode and uses the following pin configuration:

- CLK, serial clock output, up to 32 MHz
- CS, Chip/Slave select output, active low, selects which slave on the bus to talk to
- D0, MOSI serial output data in single mode, data I/O signal in dual/quad mode
- D1, MISO serial input data in single mode, data I/O signal in dual/quad mode
- D2, data I/O signal in quad mode (optional)

D3, data I/O signal in quad mode (optional)

6.11 PWM interface

Features:

- The pulse width modulation (PWM) module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs. These waveforms can be used to control motors, dim LEDs, or as audio signals if connected to the speakers. The PWM output signal has a frequency and duty cycle property. Frequency is adjustable (up to 1 MHz) and the duty cycle can be set over a range from 0% to 100%.
- Programmable PWM frequency.

- Up to four PWM channels with individual polarity and duty cycle values change of polarity, duty cycle, and base frequency possibly on every PWM period.

6.12 PDM interface

Features:

- The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. It supports single or dual-channel (left and right) data input over a single GPIO pin.
- Supports 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- Selectable ratio of 64 or 80 between PDM_CLK and output sample rate

6.13 SAADC

Features:

- The SAADC is a differential successive approximation register (SAR) analog-to-digital converter. It supports up to eight external analog input channels, depending on package variant.
- Comprises single ended (8 channels) or differential inputs (4 channels) leading to 8/10/12 bit resolution when continuous sampling, 14 bit resolution when oversampling. Each channel can use pins AIN0 through AIN7, the VDD pin, or the VDDH pin as input.
- Output samples are automatically written to RAM using EasyDMA.

Individual reference selection for each channel VDD or internal reference.

6.14 COMP

Features:

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived from an analog input pin (AIN0-AIN7). VIN- can be derived from multiple sources depending on the operation mode of the comparator differential mode and single ended mode.

- Differential mode: Derived directly from AIN0 to AIN7
- Single-ended mode: Derived from VREF. VREF can be derived from VDD, AIN0-AIN7 or internal 1.2 V, 1.8 V and 2.4 V references.

Event generation on output changes

- UP event on VIN- > VIN+

- DOWN event on VIN- < VIN+
- CROSS event on VIN+ and VIN- crossing
- READY event on core and internal reference (if used) ready

Three speed/power consumption modes: low-power, normal and high-speed

Comparator will generate a READY event to indicate that it is ready for use and its output is correct.

6.15 LPCOMP

Features:

LPCOMP is an ultra-Low power comparator that compares an input voltage against a reference voltage. Characteristics of LPCOMP include:

- Wake Up the system from OFF mode
- Input voltage range from 0 - VDD and eight analog input options from AIN0 - AIN7

Reference voltage options include two external analog reference inputs, or 15-level internal reference ladder (VDD/16).

6.16 GPIO

- The NILE series modules are versatile concerning pin-out. In non-configured state, there will be 46 GPIO pins in total and no analog or digital interfaces.
- All interfaces or functions must then be allocated to a GPIO pin before use. 8 out of the 46 GPIO pins are analog enabled, meaning that they can have an analog function allocated to them.

6.17 Debug interfaces

The module can be programmed and debugged using the serial two wire debug interface SWD on the module.

- Debug system offers a flexible and powerful mechanism for non-intrusive debugging which does not affect size and speed characters of code.
- Two-pin(SWDCLK and SWDIO) serial wire debug (SWD) interface for flashing and debugging

7 Package Description

7.1 Mechanical characteristics

Parameter	Value (L X W X H)	Units
Module Dimensions	10 X 15 X 1.6	mm
Tolerance	+/- 0.15	mm

Table 10: Mechanical characteristics

7.2 Landing pattern

Please see NILE Module Integration guide

7.3 Physical Dimensions and pad Location

Please see NILE Module Integration guide

8 Power management

The SoC employs power and resource management to maximize application energy efficiency and battery life. The supply range between 1.7V and 5.5V supports primary and secondary cell battery technologies and direct USB supply without the need for external regulators. All peripherals have independent and automated clock and power management to ensure they are powered down when not required for task operation to keep power consumption to a minimum without the application having to implement and test complex power management schemes.

8.1 Sleep modes

8.1.1 System OFF mode

System OFF is the deepest power saving mode the module can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.
When in System OFF mode, the device can be woken up through one of the following wakeup sources:

1. A reset
2. GPIO interrupt
3. NFC Field (adds 100nA)
4. External analog signal generated by the LPCOMP module
5. Detecting a valid USB voltage on the VBUS pin

The system is reset when it wakes up from the System OFF mode. One or more RAM sections can be retained in System OFF mode. Before entering the System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed. See peripheral specific chapters for more information about how to acquire the status of EasyDMA transactions.

8.1.2 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing. The system can switch the appropriate internal power sources on and off, depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

8.2 Current consumption numbers

S.no	Case	Min.	Typ.	Max.	Units
1	Deep sleep		0.4		µA
2	Standby (no RAM retention and timer/RTC wakeup)		1.5		µA
3	Idle mode with full RAM retention		2.37		µA
4	Peak TX Power (no CPU, DCDC)		4.9		mA
5	Peak RX power (no CPU, DCDC)		4.7		mA

Table 11: Current consumption numbers

9 Security

ARM Cryptocell-310 is a powerful on-chip cryptographic coprocessor providing cryptographic functions and services to speed up security-related operations significantly, save CPU processing time and reduce energy consumption. It incorporates a true random number generator (TRNG) offering true entropy and support for a wide range of asymmetric, symmetric and hashing cryptographic services for secure applications

The following cryptographic features are provided:

- True random number generator (TRNG) compliant with NIST 800-90B 16, AIS-31, and FIPS 140-2/3 16
- Pseudorandom number generator (PRNG) using underlying AES engine compliant with NIST 800-90A
- RSA public key cryptography
- Up to 2048-bit key size
- PKCS#1 v2.1/v1.5
- Optional CRT support
- Elliptic curve cryptography (ECC)
- NIST FIPS 186-4 recommended curves using pseudorandom parameters, up to 521 bits:
- Prime field: P-192, P-224, P-256, P-384, P-521
- SEC 2 recommended curves using pseudorandom parameters, up to 521 bits:
- Prime field: secp160r1, secp192r1, secp224r1, secp256r1, secp384r1, secp521r1
- Koblitz curves using fixed parameters, up to 256 bits:
- Prime field: secp160k1, secp192k1, secp224k1, secp256k1
- Edwards/Montgomery curves:
- Ed25519, Curve25519
- ECDH/ECDSA support
- Secure remote password protocol (SRP)
- Up to 3072-bit operations
- SHA-1, SHA-2 up to 256 bits
- Keyed-hash message authentication code (HMAC)
- AES symmetric encryption
- General purpose AES engine (encrypt/decrypt, sign/verify)
- 128-bit key size
- Supported encryption modes: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM*
- ChaCha20/Poly1305 symmetric encryption
- Supported key size: 128 and 256 bits
- Authenticated encryption with associated data (AEAD) mode
- BLE Secure connections
- LE 4.2 Privacy and scanner filter policies
- NFC out of band pairing

10 Software architecture

10.1 NILE Software Block diagram

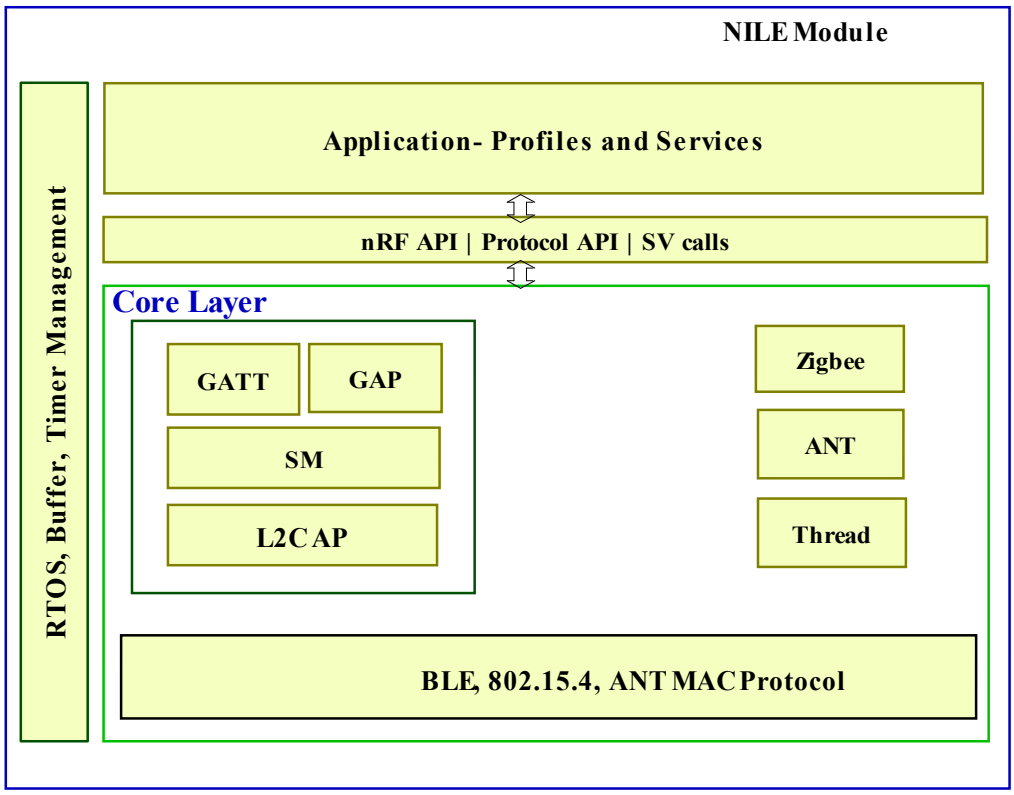

Figure 3: NILE Software Block Diagram

10.2 Software development

Please refer to the NILE EVK User guide for information on how to get started with existing examples testing or developing new applications in standalone and embedded modes.

11 Regulatory qualifications and approvals

NILE modules are certified for FCC, IC and CE/ETSI. Note that any changes to the module's configuration including (but not limited to) the programming values of the RF Transceiver and Baseband can cause the performance to change beyond the scope of the certification. These changes, if made, may result in the module having to be certified afresh.

11.1 Approvals

11.1.1 European Union regulatory compliance

In Progress

11.1.2 FCC Compliance

In Progress

11.1.3 IC compliance

In Progress

11.1.4 Japan radio equipment compliance

In Progress

12 Product Shipping, Storage and Handling

12.1 Package Information

The NILE series modules are delivered as hermetically sealed trays and reels. For more information please refer to IVATIV Package Information Guide.

12.2 Storage and Baking Instructions

NILE modules are moisture sensitive devices and are rated at MSL 4. For more information please refer to IVATIV Package Information Guide.

12.3 Mounting process and soldering recommendations

Please see Ivativ Module Integration Guide

13 Product label and ordering information

The figure below illustrates the marking on the modules which indicates Ivativ logo, model number, date code and lot number. Due to small size of the module label certification IDs are shown only in the user manual and not on the label.

Figure 4: Module Label

The table below describes the markings on the label.

Reference	Description
1	Data Matrix with unique serial number, Variant and HW version
2	Date Code. YYWWT: Year/Week/Temp Grade
3	Lot Number. FAY.XXX FAY: Fab, assembly and single digit year of make XXX: Lot number
4	Product Name

Table 12: Module Label Description

Note: Pin1 is marked with round logo icon or pin1 mark

13.1 Part Ordering

NILE module

I540M0L8-2ILT	NILE multi-protocol module with PCB Antenna, Tray packing
I540M0L8-2ILR	NILE multi-protocol module with PCB Antenna, Tape and Reel packing
I540M0L8-3ILT	NILE multi-protocol module with MHF4 Antenna connector, Tray packing
I540M0L8-3ILR	NILE multi-protocol module with MHF4 Antenna connector, Tape and Reel packing

Table 13: Part Ordering for NILE module

NILE EVK/DVK

I540M0L8-2L-DVK	NILE DVK kit with PCB Antenna
I540M0L8-3L-DVK	NILE DVK kit with MHF4 Antenna connector

Table 14: Part Ordering for NILE EVK/DVK

Contact Information

Please contact www.ivativ.com