120 mA Switched Capacitor Voltage Inverter with Regulated Output

Data Sheet **ADP3605**

FEATURES

- Fully regulated adjustable output voltage
- High output current: 120 mA
- Output accuracy: ±3%
- 250 kHz switching frequency
- Low shutdown current: 2 µA typical
- Input voltage range: 3 V to 6 V
- 8-Lead SOIC package
- −40°C to +85°C ambient temperature range

APPLICATIONS

- Voltage inverters
- Voltage regulators
- Computer peripherals and add-on cards
- Portable instruments
- Battery powered devices
- Pagers and radio control receivers
- Disk drives
- Mobile phones

FUNCTIONAL BLOCK DIAGRAM

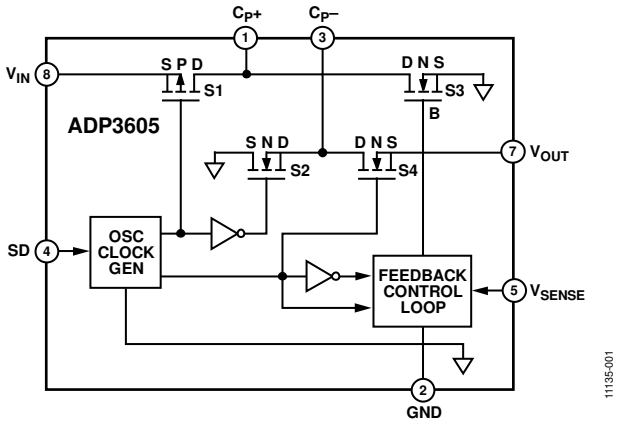


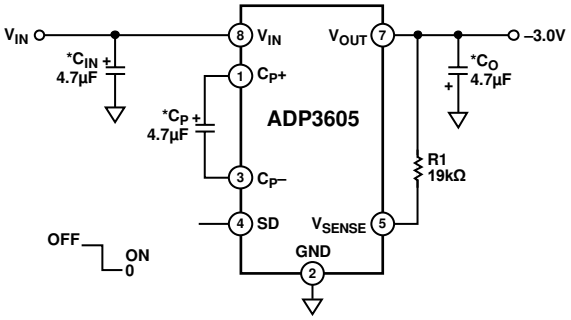
Figure 1.

GENERAL DESCRIPTION

The ADP3605 is a 120 mA regulated output, switched capacitor voltage inverter. It provides a regulated output voltage with minimum voltage loss and requires a minimum number of external components. In addition, the ADP3605 does not require the use of an inductor.

Pin-for-pin and functionally compatible with the ADP3604, the internal oscillator of the ADP3605 runs at a 500 kHz nominal frequency that produces an output switching frequency of 250 kHz. This allows for the use of smaller charge pump and filter capacitors.

The ADP3605 provides an accuracy of ±3% with a typical shutdown current of 2 µA. It can also operate from a single positive input voltage as low as 3 V. The ADP3605 is adjustable via external resistors over a −3 V to −6 V range.



*FOR BEST PERFORMANCE, 10µF IS RECOMMENDED
C_P: SPRAGUE, 293D475X0010B2W
C_{IN}, C_O: TOKIN, 1E475ZY5UC205F

Figure 2. Typical Application Circuit

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

TABLE OF CONTENTS

REVISION HISTORY

12/12—Rev. A to Rev. B

Updated Format ... Universal
Deleted 14-Lead TSSOP ... Universal
Changes to Features Section, General Description Section, and Figure 2 ... 1
Changes to Table Summary Text Prior to Table 1 and Table 1 ... 3
Changes to Table 2 ... 4
Deleted Other Members of ADP36xx Family Table I; Renumbered Sequentially ... 4
Deleted Figure 4; Renumbered Sequentially ... 4
Deleted Improved Load Regulation Section ... 6
Deleted Maximum Output Voltage Section and Figure 15 ... 7
Changes to Figure 10 Caption ... 7
Changes to Power Dissipation Section, Regulated Adjustable Output Voltage Section, and Figure 17 ... 10
Updated Outline Dimensions ... 12
Changes to Ordering Guide ... 12

7/99—Rev. 0 to Rev. A

SPECIFICATIONS

V_{IN} = 5.0 V at T_A = 25°C, C_P = C_O = 4.7 µF, unless otherwise noted. The C_{IN}, C_O, and C_P capacitors in the typical application circuit (see Figure 2) are 4.7 µF. See Figure 2 conditions. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING SUPPLY RANGE	V_S		3		6	V
SUPPLY CURRENT	I_S	−40°C < T_A < +85°C		3	6	mA
Shutdown Mode		V_{SD} = V_{IN}, −40°C < T_A < +85°C		2	15	µA
OUTPUT RESISTANCE						
Open Loop	R_O			9		Ω
OUTPUT RIPPLE VOLTAGE	V_{RIPPLE}	C_{IN} = C_O = 4.7 µF, I_{LOAD} = 60 mA		38		mV
		I_{LOAD} = 120 mA		75		mV
SWITCHING FREQUENCY	f_S	V_{IN} = 5 V, −40°C < T_A < +85°C	212	250	288	kHz
SHUTDOWN						
Logic Input High	V_{IH}		2.4			V
Input Current	I_{IH}			1		µA
Logic Input Low	V_{IL}				0.4	V
Input Current	I_{IL}			1		µA

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Input Voltage (V_{IN} to GND, GND to V_{OUT})	7.5 V
Input Voltage (V_{IN} to V_{OUT})	11 V
Output Short-Circuit Protection	1 sec
Power Dissipation, 8-Lead SOIC	660 mW
θ_{JA}[1]	150°C/W
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] θ_{JA} is specified for the worst-case conditions with the device soldered on a circuit board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 3. Alternative Capacitor Technologies

Type	Life	High Frequency	Temperature	Size	Cost
Aluminum Electrolytic Capacitor	Fair	Fair	Fair	Small	Low
Multilayer Ceramic Capacitor	Long	Good	Poor	Fair[1]	High
Solid Tantalum Capacitor	Above average	Average	Average	Average	Average
OS-CON Capacitor	Above average	Good	Good	Good	Average

[1] Refer to capacitor manufacturer's data sheet for operation below 0°C.

Table 4. Recommended Capacitor Manufacturers

Manufacturer	Capacitor	Capacitor Type
Sprague	672D, 673D, 674D, 678D	Aluminum electrolytic
Sprague	675D, 173D, 199D	Tantalum
Nichicon	PF and PL	Aluminum electrolytic
Mallory	TDC and TDL	Tantalum
TOKIN	MLCC	Multilayer ceramic
Murata	GRM	Multilayer ceramic

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

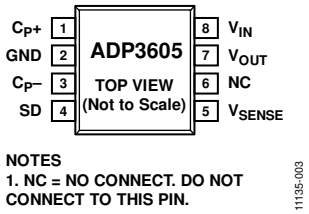


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	C_P+	Positive Terminal for the Pump Capacitor.
2	GND	Device Ground.
3	C_P-	Negative Terminal for the Pump Capacitor.
4	SD	Logic Level Shutdown Pin. Apply logic high or connect to V_{IN} to shut down the device. In shutdown mode, the charge pump is turned off, and the quiescent current is reduced to 2 µA (typical). Apply a logic low or connect to ground for normal operation.
5	V_{SENSE}	Output Voltage Sense Line. Connect a resistor between this pin and V_{OUT} to set the desired output voltage.
6	NC	No Connect. Do not connect to this pin.
7	V_{OUT}	Regulated Negative Output Voltage. Connect a low ESR, 4.7 µF or larger, capacitor between this pin and the device ground.
8	V_{IN}	Positive Supply Input Voltage. Connect a low ESR bypass capacitor between this pin and the device ground to minimize supply transients.

TYPICAL PERFORMANCE CHARACTERISTICS

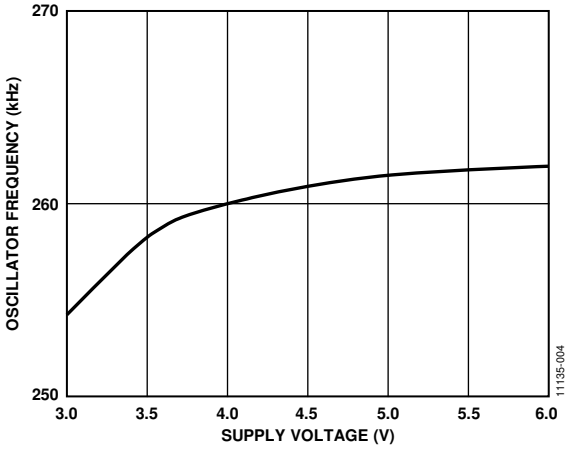


Figure 4. Oscillator Frequency vs. Supply Voltage

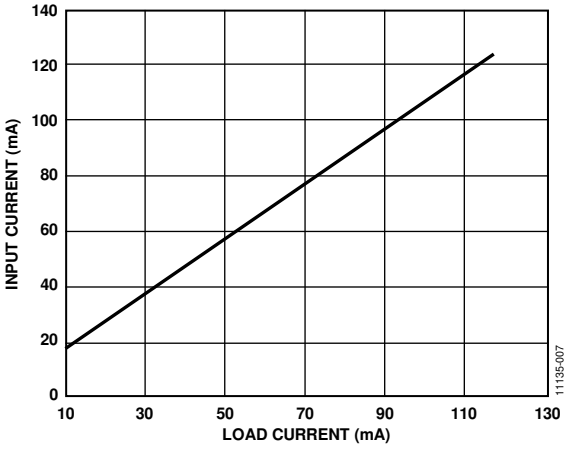


Figure 7. Average Input Current vs. Output Current

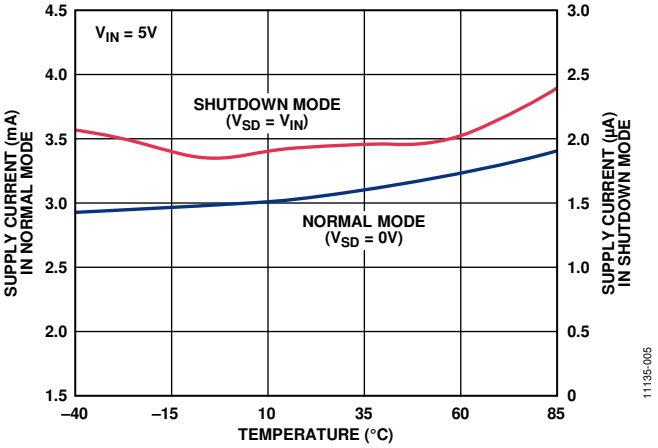


Figure 5. Supply Current vs. Temperature

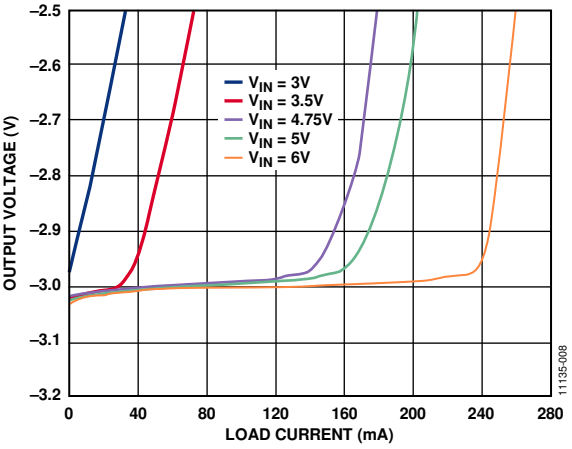


Figure 8. Output Voltage vs. Load Current, V_{OUT} = –3.0 V

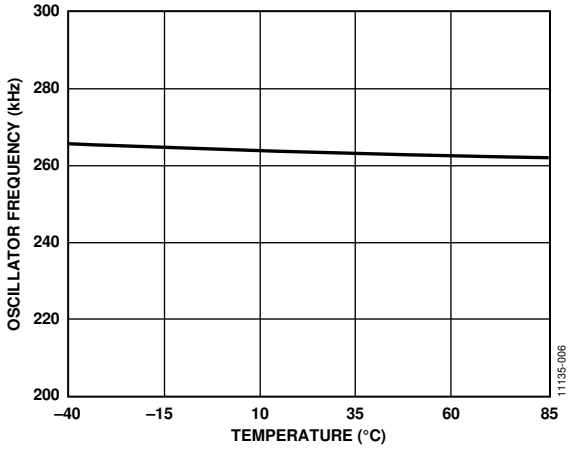


Figure 6. Oscillator Frequency vs. Temperature

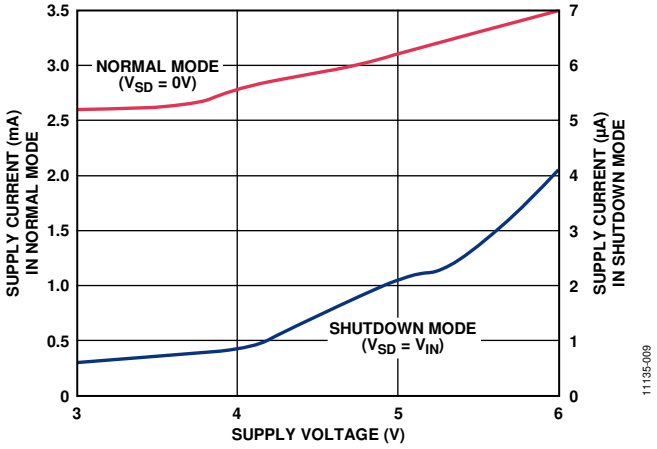


Figure 9. Supply Current vs. Supply Voltage

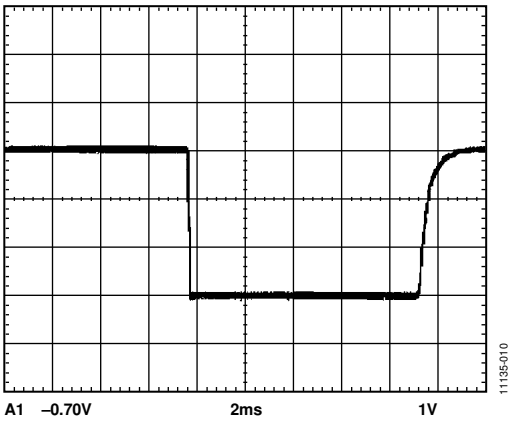


Figure 10. Start-Up Under Full Load

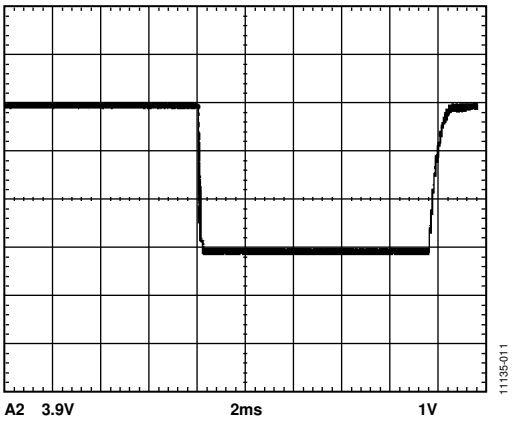


Figure 11. Enable/Disable Time Under Full Load

THEORY OF OPERATION

The ADP3605 uses a switched capacitor principle to generate a negative voltage from a positive input voltage. An onboard oscillator generates a 2-phase clock to control a switching network that transfers charge between the storage capacitors. The switches turn on and off at a 250 kHz rate, which is generated from an internal 500 kHz oscillator. The basic principle behind the voltage inversion scheme is illustrated in Figure 12 and Figure 13.

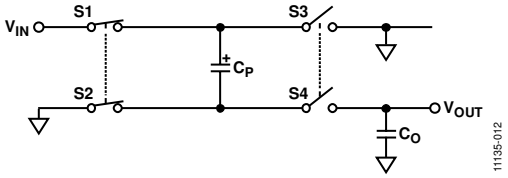


Figure 12. ADP3605 Switch Configuration Charging the Pump Capacitor

During phase one, S1 and S2 are on, charging the pump capacitor to the input voltage. Before the next phase begins, S1 and S2 are turned off as well as S3 and S4 to prevent any overlap. S3 and S4 are turned on during the second phase (see Figure 13), and the charge stored in the pump capacitor is transferred to the output capacitor.

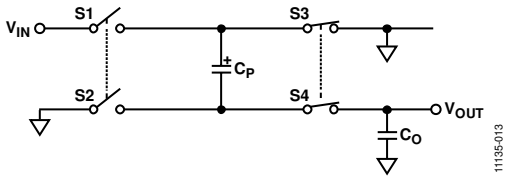


Figure 13. ADP3605 Switch Configuration Charging the Output Capacitor

During the second phase, the positive terminal of the pump capacitor is connected to ground through the variable resistance switch (S3), and the negative terminal is connected to the output, resulting in a voltage inversion at the output terminal. Figure 1 shows the ADP3605 block diagram.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

The high internal oscillator frequency of the ADP3605 permits the use of small capacitors for both the pump and the output capacitors. For a given load current, factors affecting the output voltage performance are the following:

- Pump (C_P) and output (C_O) capacitance
- ESR of the C_P and C_O

When selecting the capacitors, keep in mind that not all manufacturers guarantee capacitor ESR in the range required by the circuit. In general, the ESR of the capacitor is inversely proportional to its physical size; therefore, larger capacitance values and higher voltage ratings tend to reduce ESR. Because the ESR is also a function of the operating frequency, when selecting a capacitor, ensure that its value is rated at the operating frequency of the circuit.

Temperature is another factor affecting capacitor performance. Figure 14 illustrates the temperature effect on various capacitors. If the circuit has to operate at temperatures significantly different from 25°C, the capacitance and the ESR values must be carefully selected to adequately compensate for the change. Various capacitor technologies offer improved performance over temperature; for example, certain tantalum capacitors provide good low temperature ESR; however, at a higher cost. Table 3 provides the ratings for different types of capacitor technologies to help the designer select the right capacitors for the application. The exact values of C_{IN} and C_O are not critical. However, low ESR capacitors, such as solid tantalum and multilayer ceramic capacitors, are recommended to minimize voltage loss at high currents. Table 4 shows a partial list of the recommended low ESR capacitor manufacturers.

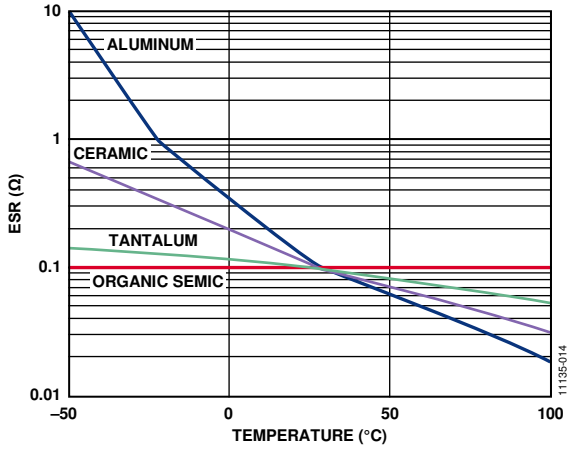


Figure 14. ESR vs. Temperature

INPUT CAPACITOR

A small 1 µF input bypass capacitor, preferably with low ESR, such as tantalum or multilayer ceramic, is recommended to reduce noise and supply transients and to supply part of the peak input current drawn by the ADP3605. A large capacitor is recommended if the input supply is connected to the ADP3605 through long leads, or if the pulse current drawn by the device may affect other circuitry through supply coupling.

OUTPUT CAPACITOR

The output capacitor (C_O) is alternately charged to the C_P voltage when C_P is switched in parallel with C_O. The ESR of C_O introduces steps in the V_{OUT} waveform whenever the charge pump charges C_O, which contributes to V_{OUT} ripple. Thus, ceramic or tantalum capacitors are recommended for C_O to minimize ripple on the output. Figure 15 illustrates the output ripple voltage effect for various capacitance and ESR values. Note that as the capacitor value increases beyond the point where the dominant contribution to the output ripple is due to the ESR, no significant reduction in V_{OUT} ripple is achieved by added capacitance. Because output current is supplied solely by the output capacitor, C_O, during one-half of the charge pump cycle, peak-to-peak output ripple voltage is calculated by

$$V_{RIPPLE} = \frac{I_L}{2 \times f_S \times C_O} + 2 \times I_L \times ES_{RC_O}$$

where:
I_L = load current
f_S = 250 kHz nominal switching frequency
C_O = 10 µF with an ESR of 0.15 Ω

$$V_{RIPPLE} = \frac{120\ \text{mA}}{2 \times 250\ \text{kHz} \times 10\ \mu\text{F}} + 2 \times 120\ \text{mA} \times 0.15 = 60\ \text{mV}$$

Multiple smaller capacitors can be connected in parallel to yield lower ESR and lower cost. For lighter loads, proportionally smaller capacitors are required. To reduce high frequency noise, bypass the output with a 0.1 µF ceramic capacitor in parallel with the output capacitor.

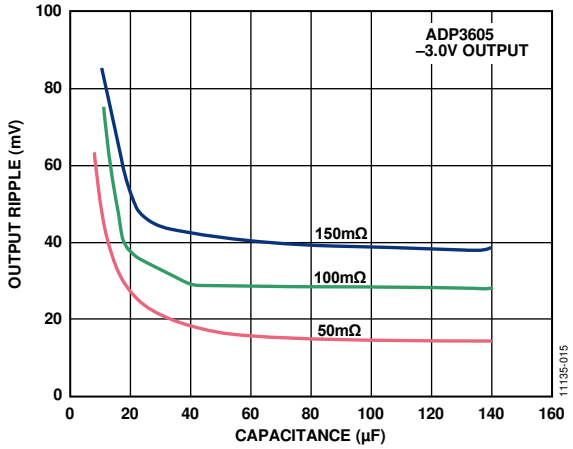


Figure 15. Output Ripple Voltage vs. Capacitance and ESR

PUMP CAPACITOR

The ADP3605 alternately charges C_P to the input voltage when C_P is switched in parallel with the input supply, and then transfers charge to C_O when C_P is switched in parallel with C_O.

During the time C_P is charging, the peak current is approximately two times the output current. During the time C_P is delivering charge to C_O, the supply current drops down to about 3 mA.

A low ESR capacitor has a much greater impact on performance for C_P than C_O because current through C_P is twice the C_O current. Therefore, the voltage drop due to C_P is about four times the ESR of C_P times the load current. While the ESR of C_O affects the output ripple voltage, the voltage drop generated by the ESR of C_P, combined with the voltage drop due to the output source resistance, determines the maximum available V_{OUT}.

SHUTDOWN MODE

The output of the ADP3605 can be disabled by pulling the SD pin (Pin 4) high to a TTL/CMOS logic compatible level that stops the internal oscillator. In shutdown mode, the quiescent current is reduced to 2 µA (typical). Applying a digital low level or tying the SD pin to ground turns on the output. If the shutdown feature is not used, Pin 4 must be tied to the ground pin.

POWER DISSIPATION

The power dissipation of the ADP3605 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature rating. Total power dissipation is calculated as

$$P = (V_{IN} - |V_{OUT}|)\, I_{OUT} + (V_{IN})\, I_S$$

where:
I_{OUT} and I_S are output current and supply current, respectively.
V_{IN} and V_{OUT} are input and output voltages, respectively.

For example, assuming worst-case conditions, V_{IN} = 6 V, V_{OUT} = −2.9 V, I_{OUT} = 120 mA, and I_S = 5 mA. Calculated device power dissipation is

$$P \approx (6\text{ V} - |-2.9\text{ V}|)\, 0.12 + (6\text{ V})\, 0.005\text{ A} = 402\text{ mW}$$

This is far below the 660 mW power dissipation capability of the ADP3605.

GENERAL BOARD LAYOUT GUIDELINES

Because the internal switches of the ADP3605 turn on and off very fast, good printed circuit board (PCB) layout practices are critical to ensure optimal operation of the device. Improper layouts results in poor load regulation, especially under heavy loads. Output performance can be improved by following these simple layout guidelines:

- Use adequate ground and power traces or planes
- Use single point ground for device ground and input and output capacitor grounds
- Keep external components as close to the device as possible
- Use short traces from the input and output capacitors to the input and output pins, respectively

ADP3605 REGULATED ADJUSTABLE OUTPUT VOLTAGE

The regulated output voltage is programmed by a resistor that is inserted between the V_{SENSE} and V_{OUT} pins, as illustrated in Figure 16. The inherent limit of the output voltage of a single inverting charge pump stage is −1 times the input voltage. The inverse (that is, negative) scaling factor of 1.00 is reduced somewhat due to losses that increase with output current. To increase the scaling factor to attain a more negative output voltage, an external pump stage can be added with passive components, as is shown in Figure 17. This single stage increases the inverse scaling factor to a limit of two, although the diode drops limits the ability to attain that exact 2.00 scaling factor noticeably. Even further increases can be achieved with additional external pump stages.

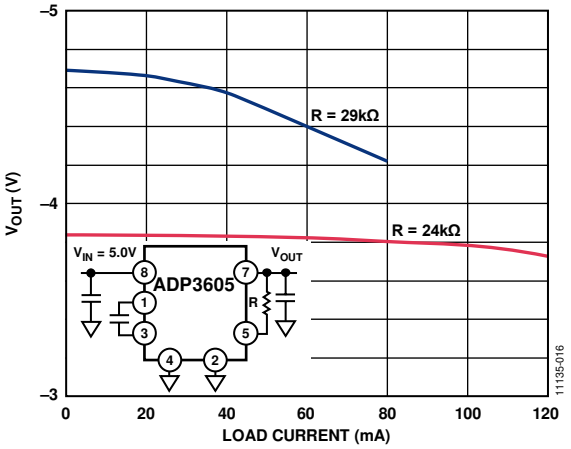


Figure 16. Adjustable Regulated Output Voltage

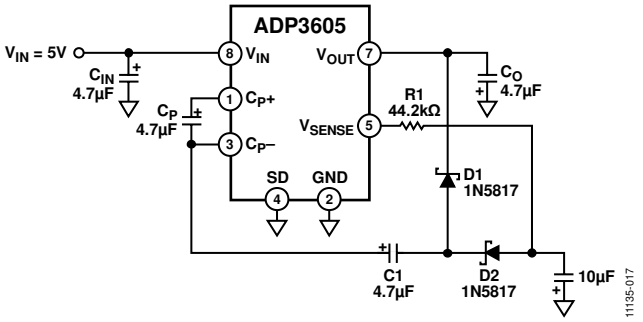


Figure 17. Regulated –7 V from a 5 V Input

High accuracy on the adjustable output voltage is achieved with the use of precision trimmed internal resistors, which eliminate the need to trim the external resistor or add a second resistor to form a divider. The adjustable output voltage is set by

$$V_{OUT} = \frac{1.5}{9.5\text{ k}\Omega} R$$

where V_{OUT} is in volts and R is in kΩ.

REGULATED DUAL SUPPLY SYSTEM

The circuit in Figure 18 provides regulated positive and negative voltages for systems that require dual supplies from a single battery or power supply.

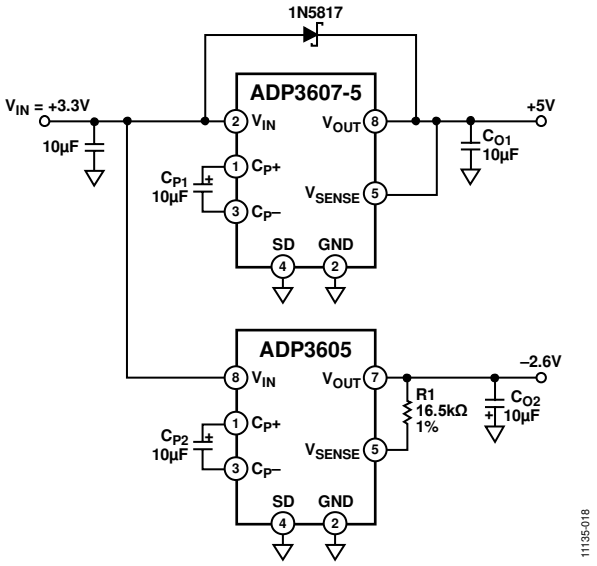


Figure 18. Dual Supply System

OUTLINE DIMENSIONS

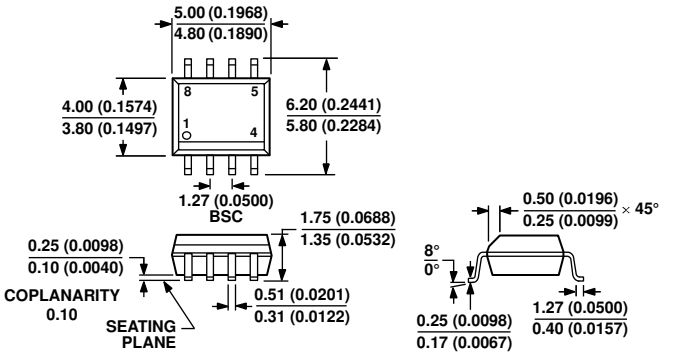


Figure 19. 8-LeadStandard Small Outline Package [SOIC_N]
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Output Voltage	Temperature Range	Package Description	Package Option
ADP3605ARZ	Adjustable	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N], Tube	R-8
ADP3605ARZ-R7	Adjustable	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N], 7″ Tape and Reel	R-8

[1] Z = RoHS Compliant Part.

D11135-0-12/12(B)