

Automotive-grade N-channel 40 V, 1.3 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

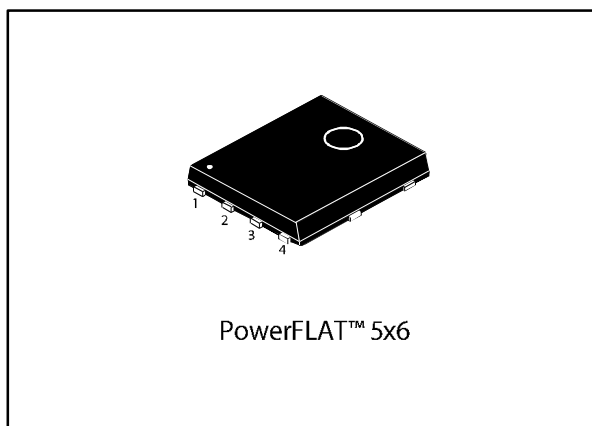
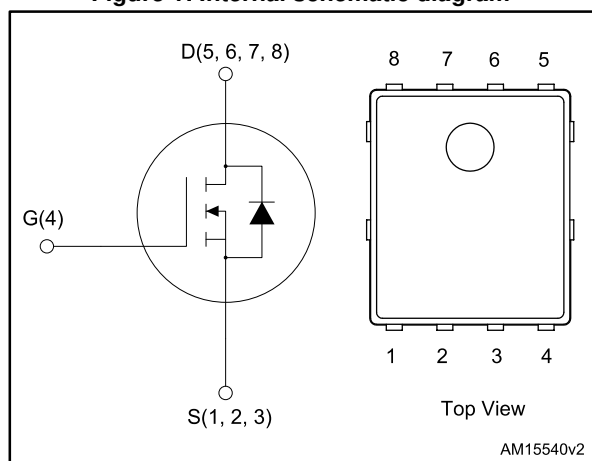


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL210N4F7AG	40 V	1.6 mΩ	120 A

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL210N4F7AG	210N4F7	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package mechanical data	9
	4.1 PowerFLAT™ 5x6 WF type C package information.....	9
	4.2 PowerFLAT™ 5x6 packing information.....	11
5	Revision history	13

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V _{GS}	Gate-source voltage	± 20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	120	A
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	120	A
I _{DM} ⁽¹⁾⁽²⁾	Drain current (pulsed)	480	A
P _{TOT}	Total dissipation at T _C = 25 °C	150	W
I _{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	40	A
E _{AS}	Single pulse avalanche energy (T _j = 25 °C, I _D = 20 A, V _{DD} = 25 V)	300	mJ
T _j	Operating junction temperature	-55 to 175	°C
T _{stg}	Storage temperature		

Notes:

⁽¹⁾Drain current is limited by package, the current capability of the silicon is 229 A at 25 °C.

⁽²⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max.	31.3	°C/W
R _{thj-case}	Thermal resistance junction-case max.	1.0	°C/W

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 40\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 16\text{ A}$		1.3	1.6	m Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3600	-	pF
C_{oss}	Output capacitance		-	1240	-	pF
C_{rss}	Reverse transfer capacitance		-	56	-	pF
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	43	-	nC
Q_{gs}	Gate-source charge		-	19	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	27	-	ns
t_r	Rise time		-	6	-	ns
$t_{d(off)}$	Turn-off delay time		-	34	-	ns
t_f	Fall time		-	6	-	ns

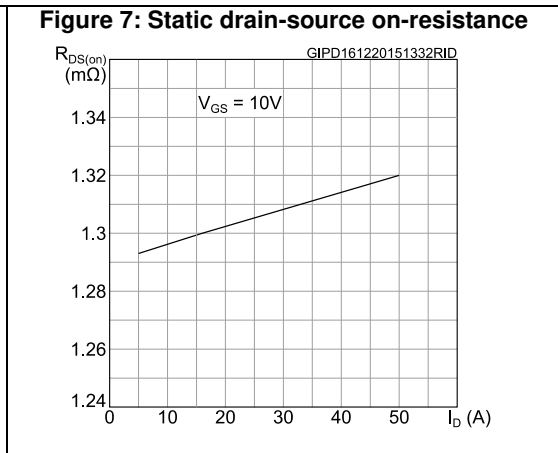
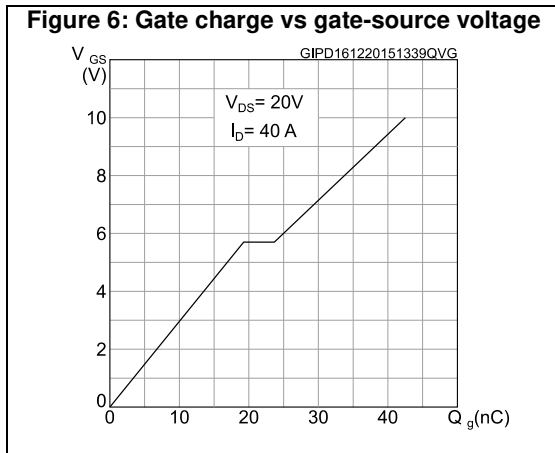
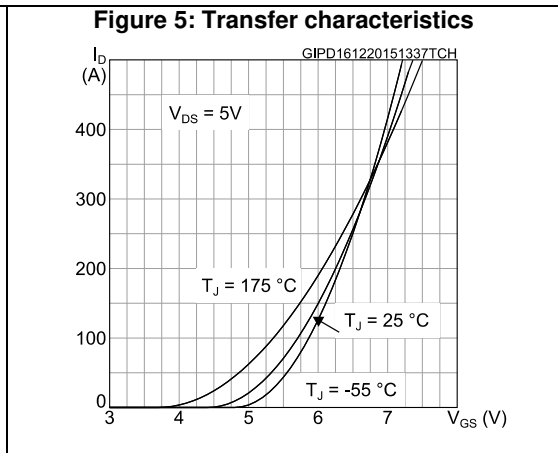
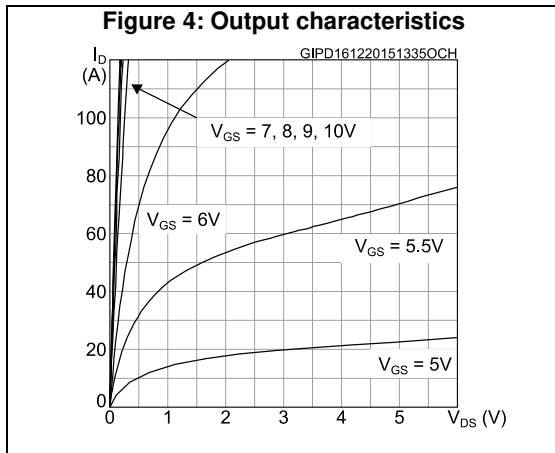
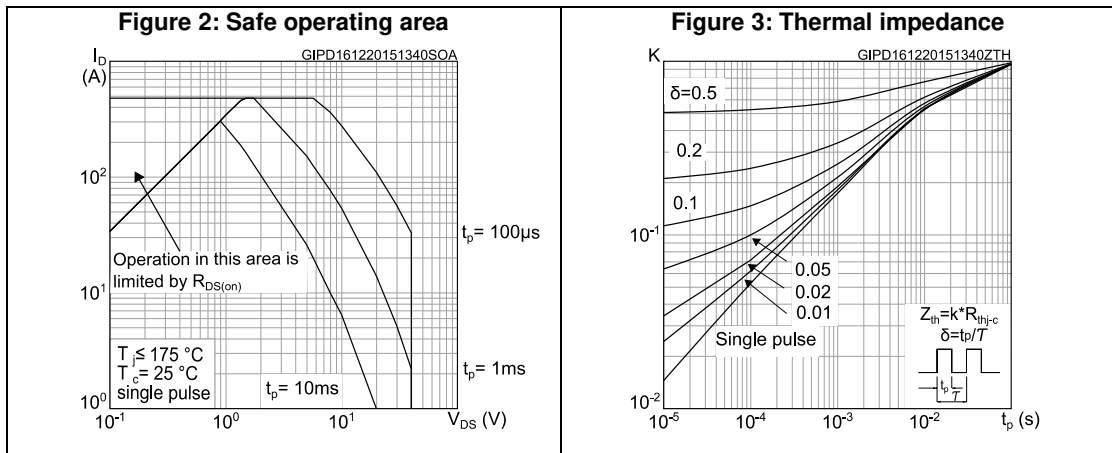
Table 7: Source-drain diode

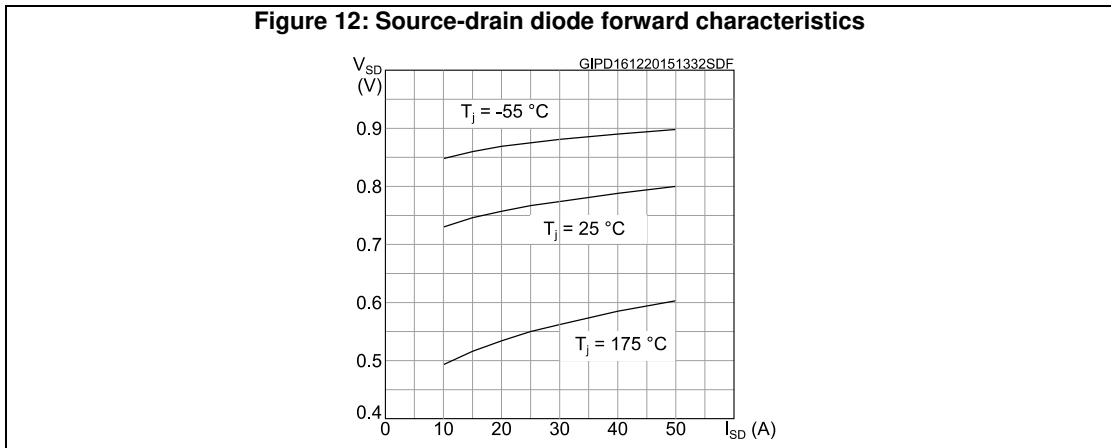
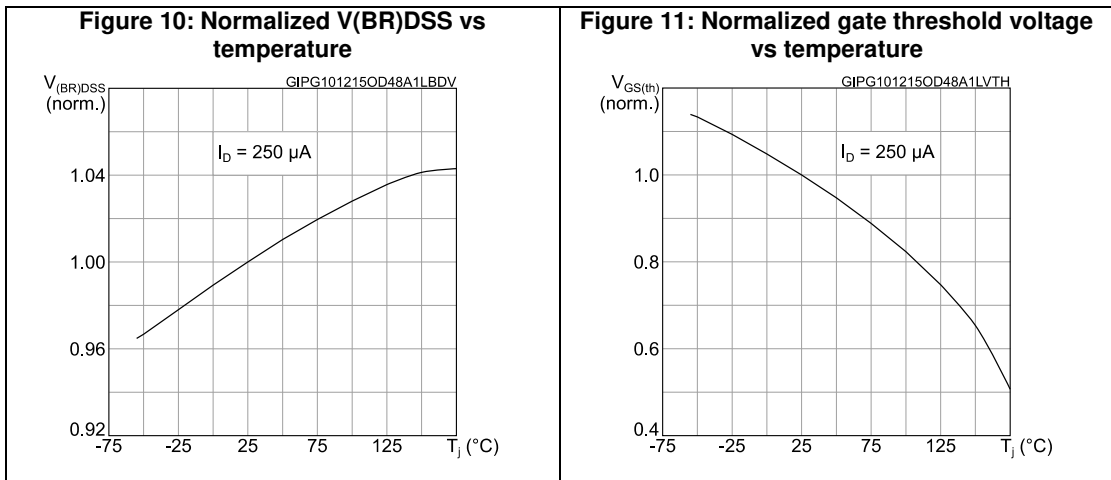
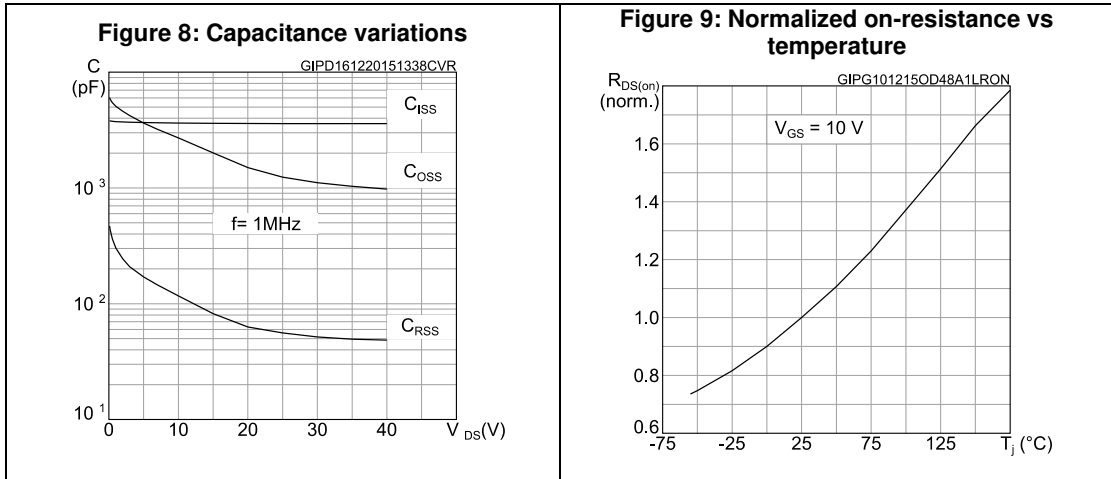
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 40 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_D = 40 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 32 \text{ V}$ (see <i>Figure 15: "Test circuit for inductive load switching and diode recovery times"</i>)	-	53		ns
Q_{rr}	Reverse recovery charge		-	71		nC
I_{RRM}	Reverse recovery current		-	2.7		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

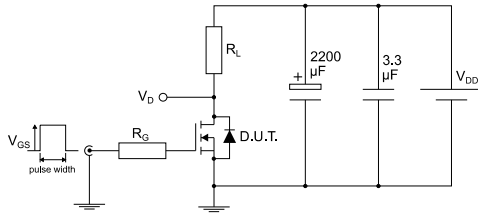
2.1 Electrical characteristics (curves)





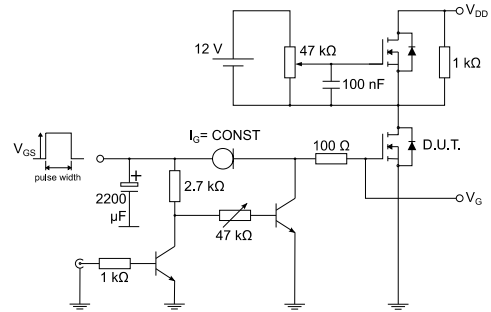
3 Test circuits

Figure 13: Test circuit for resistive load switching times



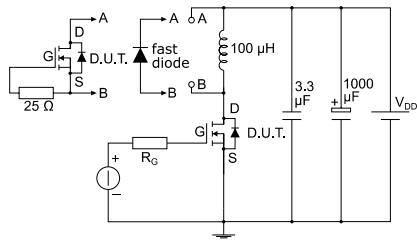
AM01468v1

Figure 14: Test circuit for gate charge behavior



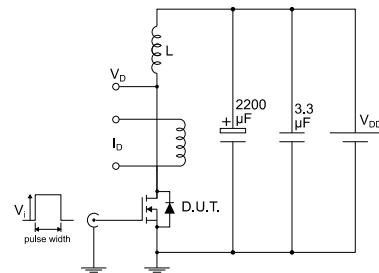
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



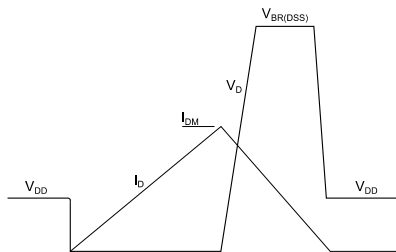
AM01470v1

Figure 16: Unclamped inductive load test circuit



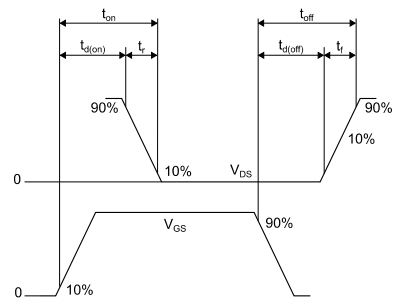
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

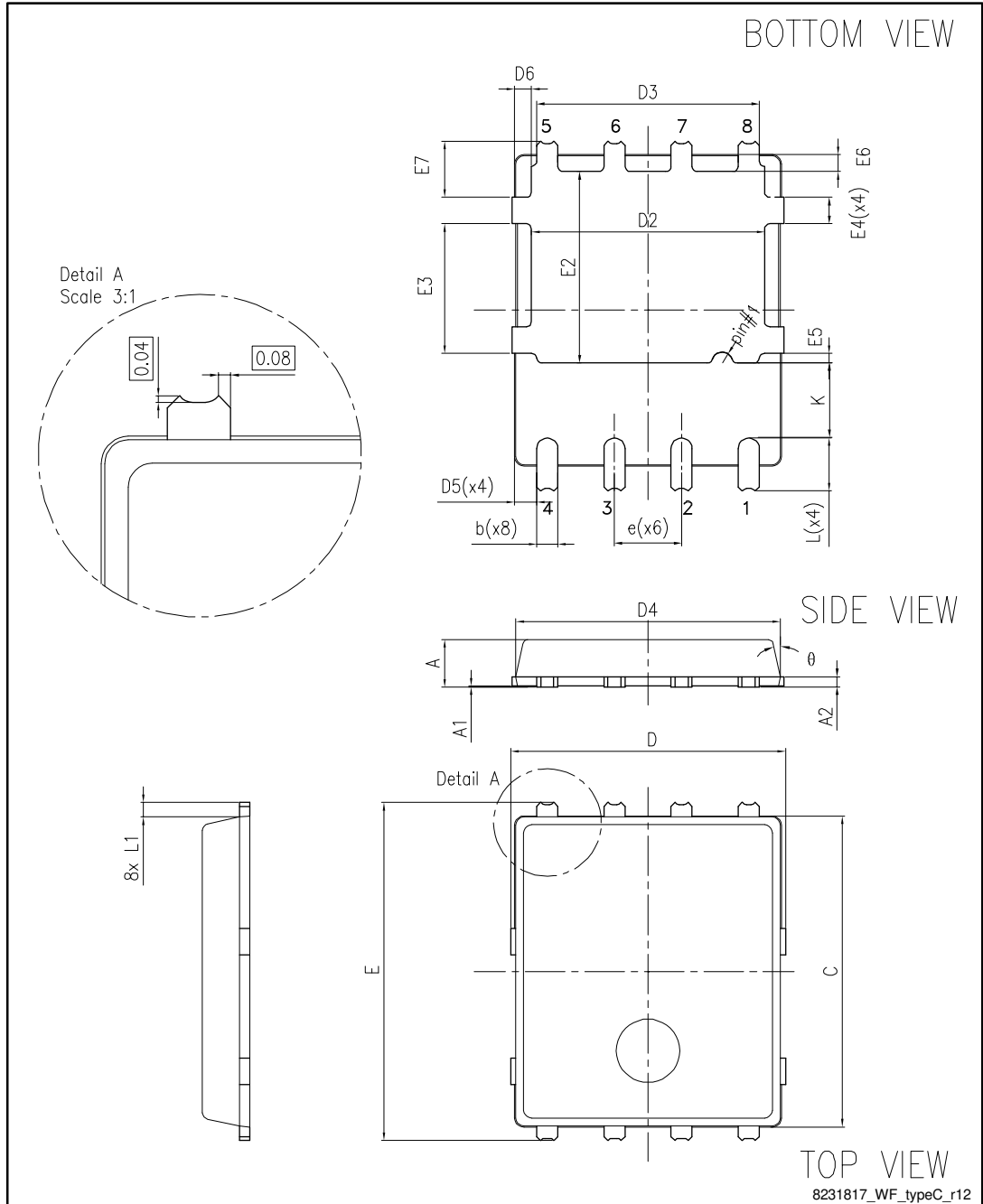
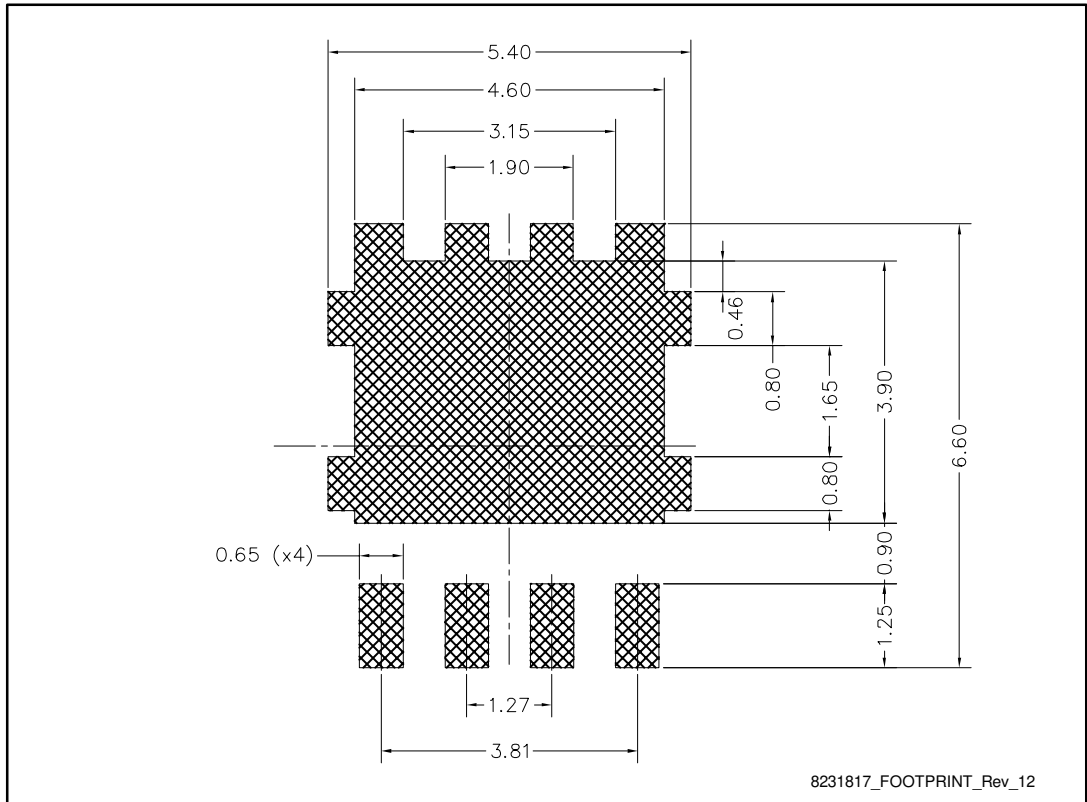


Table 8: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.2	0.325	0.450
E7	0.85	1.00	1.15
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 WF tape

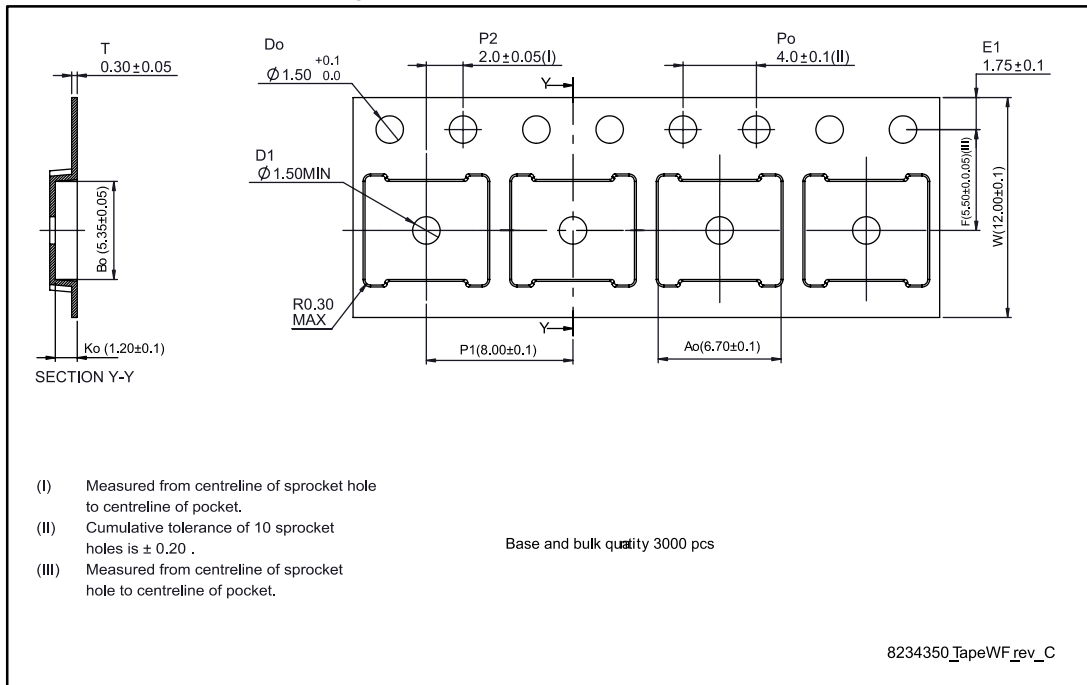


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

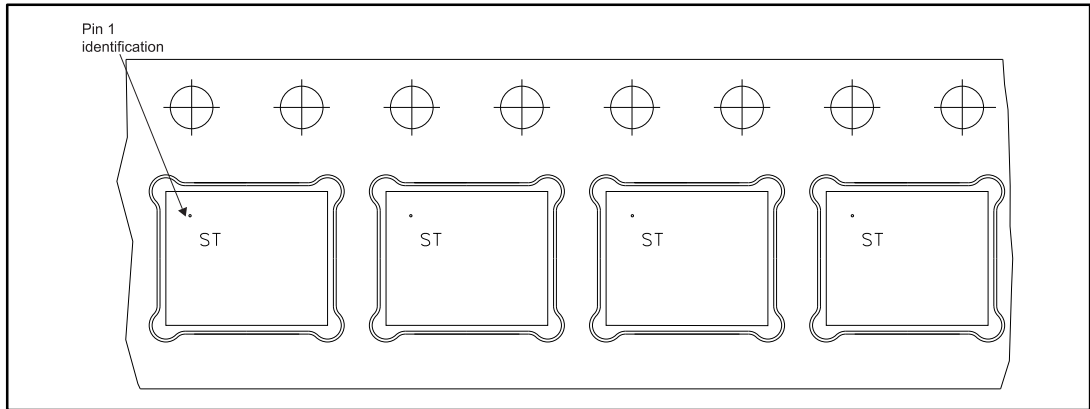
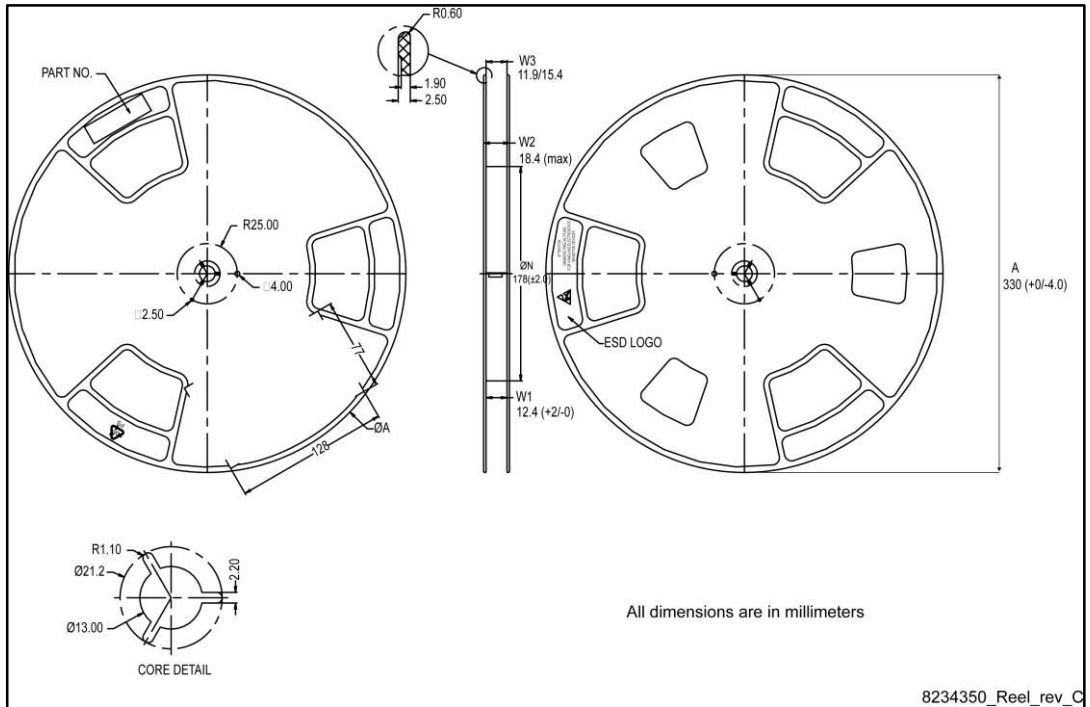


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
07-Jan-2016	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved