ISL97632

LED Driver with 1-Wire Dimming

FN9239
Rev 4.00
March 22, 2010

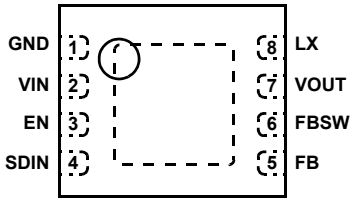
The ISL97632 represents an efficient and highly integrated PWM boost LED driver that is suitable for 1.8” to 3.5” LCDs that employ 2 to 7 white LEDs for backlighting. With integrated Schottky diode, OVP, and dynamic digital dimming capability, the ISL97632 provides a simple, reliable, and flexible solution to the backlight designers.

The ISL97632 features a simple 1-Wire digital interface that provides a 5-bit dimming control. The dimming signal adjusts the FB voltage and therefore the LED brightness in a DC manner in 32 linear steps. An EN pin can be used to provide a zero brightness setting or shutdown power saving function.

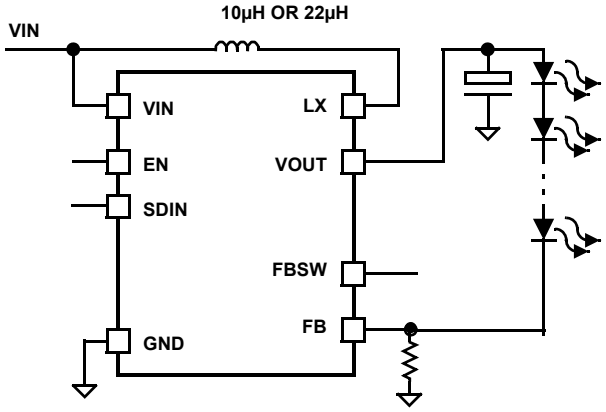
The ISL97632 is available in the 8 Ld TDFN (2mmx3mm) package. There are 14V, 18V, and 26V OVP options that are suitable for 3, 4, and 7 LEDs (3.5V/20mA type) backlight applications respectively. The ISL97632 is specified for operation over the -40°C to +85°C ambient temperature at input voltage from 2.4V to 5.5V.

Pinout

ISL97632
(8 LD 2x3 TDFN)
TOP VIEW



Typical Application Circuit



Features

- 1-Wire 5-Bit Digital Dimming
- Drives Up to 7 LEDs in Series (3.5V/20mA type)
- OVP (14V, 18V and 26V for 3, 4, and 7 LEDs applications)
- Integrated Schottky Diode
- 2.4V to 5.5V input
- 86% Efficiency
- 1.4MHz Switching Frequency Allows Small LC
- Enable for Shutdown Function or Zero Brightness Setting
- 1µA Shutdown Current
- Internally Compensated
- 8 Ld TDFN (2mmx3mm)
- Pb-Free (RoHS Compliant)

Applications

- LED backlighting for
  - Cell phones
  - Smartphones
  - MP3
  - PMP
  - Automotive Navigation Panel
  - Portable GPS

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-Free)	PKG. DWG. NO.
ISL97632IRT14ZT*	ELB	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97632IRT14ZTK*	ELB	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97632IRT18ZT*	ELC	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97632IRT18ZTK*	ELC	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97632IRT26ZT*	ELD	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97632IRT26ZTK*	ELD	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A

* Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Input Voltage (V_{IN}) . . . . . -0.3V to 6V
LX Voltage . . . . . -0.3V to 28V
FBSW Voltage . . . . . -0.3V to 28V
All Other Pins . . . . . -0.3V to 6V

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TDFN Package	70	10.5

Maximum Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed over temperature of -40°C to +85°C unless otherwise stated. Typical values are for information purposes only at TJ = TC = TA = +25°C.

NOTES:

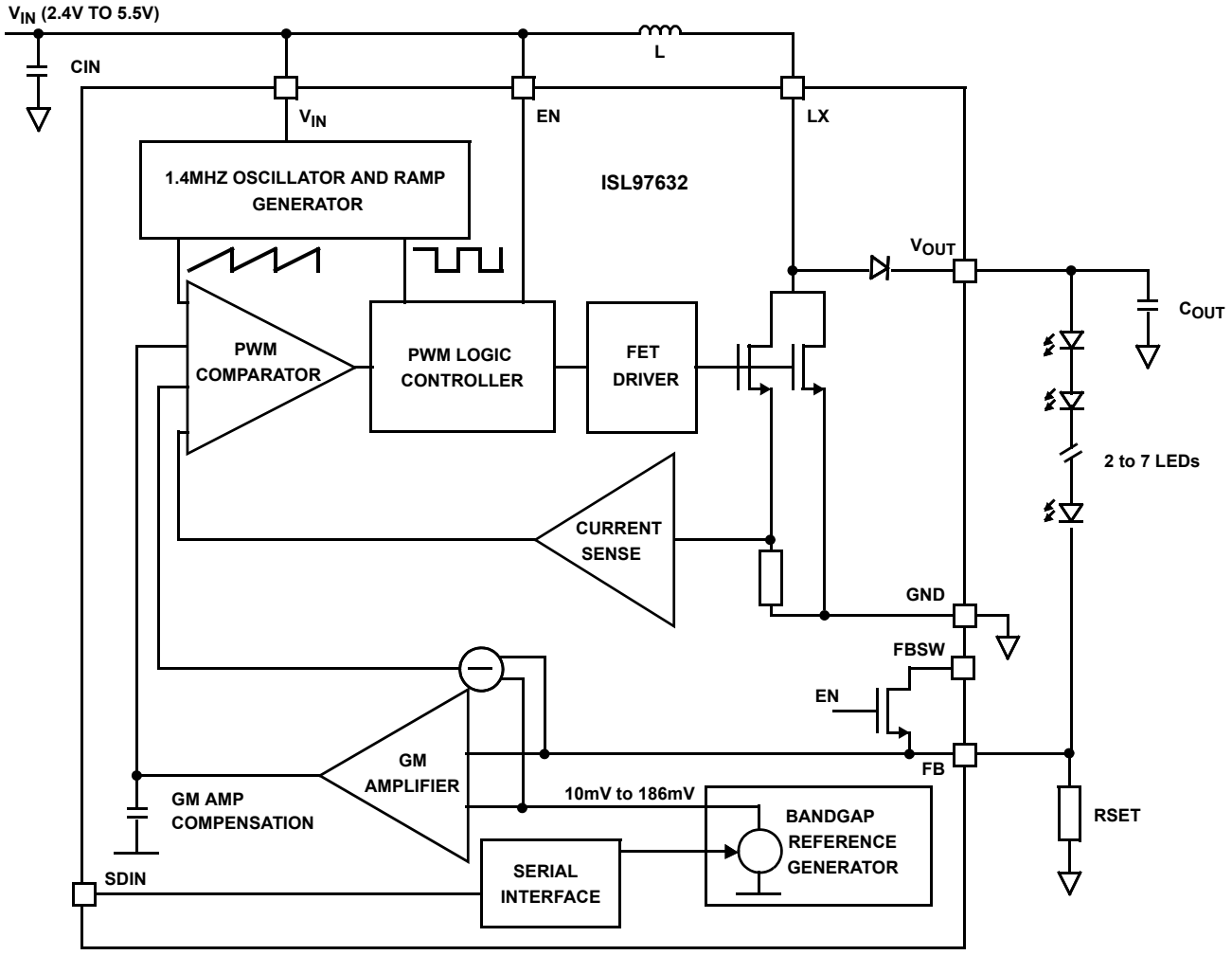
1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = V_{EN} = 3V. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Supply Voltage		2.4		5.5	V
I_{IN}	Supply Current	EN = 3V, enabled, not switching		0.8	1.5	mA
		EN = 0V, disabled			1	µA
Fsw	Switching Frequency		1,300	1,450	1,600	kHz
DMAX	Maximum Duty Cycle		90	95		%
I_{LIM}	LX Current		400	470		mA
$R_{SW(LX)}$	LX Switch ON-Resistance	ILX = 100mA		900		mΩ
ILEAK	LX Switch Leakage Current	VLX = 28V			1	µA
VFB	Feedback Voltage	Serial interface setting = 15 (center)	90	95	100	mV
		Serial interface setting = S (S = 0,1 ..31)		9.8 + 5.68 x S		mV
		Serial interface setting = 0		9.8		mV
IFB	FB Pin Bias Current	VFB = 95mV			1	µA
$R_{SW(FBSW)}$	FBSW Switch ON-Resistance			10		Ω
V_{DIODE}	Schottky Diode Forward Voltage	IDIODE = 100mA, T_A = +25°C	600		850	mV
OVP	Overvoltage Protection	ISL97632IRT14Z	14			V
		ISL97632IRT18Z	18			V
		ISL97632IRT26Z	26		28	V
VIL	Logic Low Voltage				0.6	V
VIH	Logic High Voltage		1.5			V
$t_{LOGIC}1$	Timing Range for Logic 1	SDIN = low	15		45	µs
$t_{LOGIC}0$	Timing Range for Logic 0	SDIN = low	90		120	µs
$t_{LOGIC-LOAD}$	Timing Range for Load	SDIN = low	215			µs
$t_{LOGIC-HIGH}$	Minimum Valid SDIN High Time	SDIN = high	3			µs

Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	GND	Ground Pin. Connect to local ground.
2	VIN	Input Supply Pin. Connect to the input supply voltage, the inductor and the input supply decoupling capacitor.
3	EN	Enable Pin. Connect to enable signal to turn-on or off the device. Active High.
4	SDIN	Single-Wire XSD Digital Interface (1-Wire Interface).
5	FB	Feedback Pin. Connect to the cathode of bottom LED and the sense resistor.
6	FBSW	Optional FB Disconnect Switch.
7	VOUT	Output Pin. Connect to the anode of the top LED and the output filter capacitor.
8	LX	Switching Pin. Connect to inductor.

Single-Wire Serial Interface

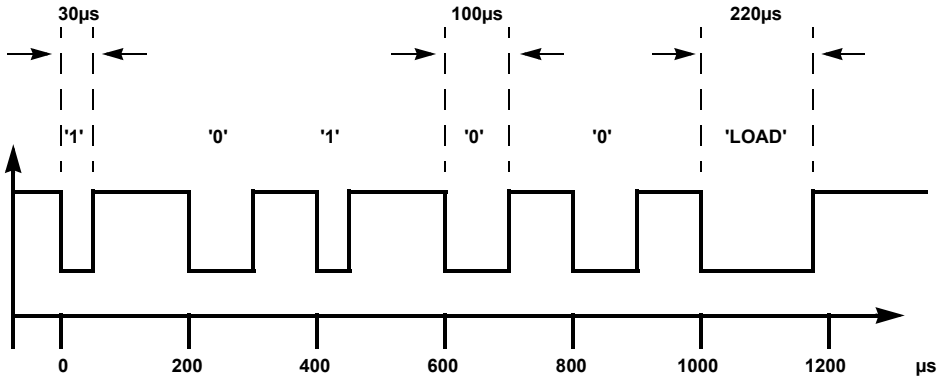


FIGURE 1. 1-WIRE XSD INTERFACE

The ISL97632 uses a simple single-wire serial interface for programming the output brightness of the LEDs. A 5-bit interface is used to give a total of 32 levels of output brightness. The interface uses a normally high connection for use with open-drain driving schemes and Intersil's proprietary 1-Wire XSD bus. When held low for between 15µs and 45µs, the interface registers a logic 1. When held low for between 90µs and 120µs the interface registers a logic 0. When held low for greater that 215µs, the interface loads the last 5 bits into the brightness control register and updates the brightness level. The required minimum high time is 3µs. This simple single-wire programming is summarized as follows:

- Logic 0 = Negative pulse >90µs and <120µs
- Logic 1 = Negative pulse >15µs and <45µs
- Load = Negative pulse >215µs

Figure 1 shows an example of programming a binary code of 10100 and load it in to the device serial register.

The serial interface is automatically reset to 0 when the device is disabled, or enters UVLO. Therefore, when the part is enabled, the output brightness is automatically set to the minimum level.

Typical Performace Curves

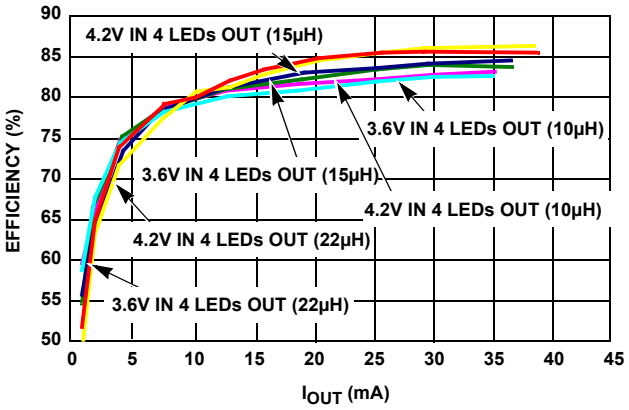


FIGURE 2. EFFICIENCY vs LED CURRENT

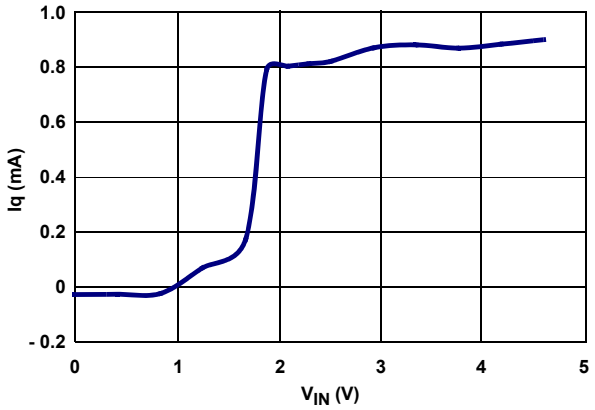


FIGURE 3. QUIESCENT CURRENT vs V_{IN} (ENAB = HI)

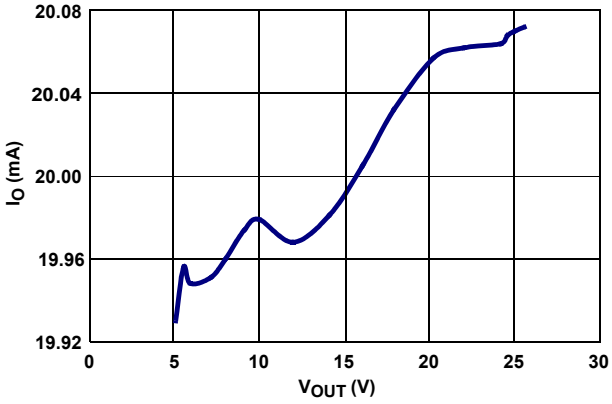


FIGURE 4. LOAD REGULATION (V_{IN} = 4V)

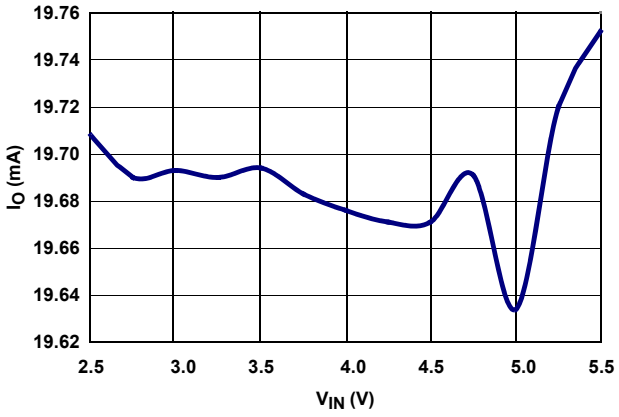


FIGURE 5. LINE REGULATION

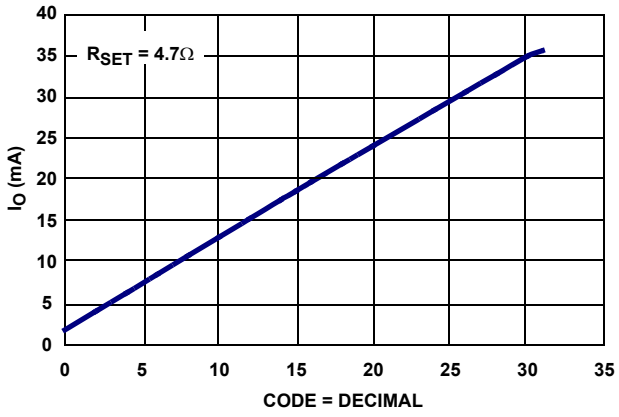


FIGURE 6. ILED vs PROGRAMMING CODES

Detailed Description

The ISL97632 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. There are three OVP models for driving 3, 4, and 7 LEDs (3.5V/20mA type) and their OVP thresholds are set at 14V, 18V, and 26V respectively. The ISL97632 operates from an input voltage of 2.4V to 5.5V and ambient temperature from -40°C to +85°C. The switching frequency is around 1.45MHz and allows the driver circuit to employ small LC components. The forward current of the LED is set using the R_{SET} resistor. In the steady state mode, the LED current is given by Equation 1:

$$I_{LED}(S) = \frac{V_{FB}(S)}{R_{SET}} = \frac{9.8mV + 5.68mV \times S}{R_{SET}} \quad \text{(EQ. 1)}$$

where S is the 5-bit Serial Interface Setting or Digital code from 0 to 31 programmed in the XSD single-wire interface. The default setting is 0 and the VFB is at minimum.

Dimming Control

The ISL97632 powers up to provide minimium current. By programming the digital code with the Intersil's 1-Wire XSD interface as shown in Figure 1, the current can be changed linearly with the digital code from 0 to 31. Figure 6 shows LED current versus the programming codes.

Overvoltage Protection

The ISL97632 comes with overvoltage protection. The OVP trip points are at 14V, 18V, and 26V for ISL97632IRT14Z, ISL97632IRT18Z, and ISL97632IRT26Z respectively. The maximum numbers of LEDs and OVP threshold are shown in Table 1. When the device reaches the OVP, the LX stops switching, disabling the boost circuit until V_{OUT} falls about 7% below the OVP threshold. At this point, LX will be allowed to switch again. The OVP event will not cause the device to shutdown.

TABLE 1.

PART NO.	OVP	MAX NO. OF LEDS	MAX ILED
ISL97632IRT14Z	14V	3	70mA
ISL97632IRT18Z	18V	4	50mA
ISL97632IRT26Z	26V	7	30mA

There are three OVP options. The 3 LEDs application should use the 14V OVP device. The 7 LEDs application should use the 26V OVP device. An output capacitor that is only rated for the required voltage range can therefore be used which will optimize the component costs in some cases.

Shut-Down

An active high EN pin is normally on but this pin can be used as a shutdown power saving function or zero brightness setting. When taken low the EN pin places the ISL97632 into power down mode down where the supply current is reduced to less than 1µA. The EN pin cannot be used as PWM input, as the part resets to 0 whenever EN is low. To resume previous setting, the device needs to be reprogrammed.

Output Disconnect

The ISL97632 features a FBSW feedback disconnect switch that can be used in between the LED and R_{SET} for an optional short-circuit protection. For example, the user may build an external short circuit detection to monitor the V_{OUT}. If the V_{OUT} goes low due to one or more LEDs which are shorted, the circuit can release the EN and FBSW switch to disconnect the LEDs.

Components Selection

The input capacitance is typically 0.22µF to 4.7µF. The output capacitor should be in the range of 0.22µF to 1µF. X5R or X7R type of ceramic capacitors of the appropriate voltage rating are recommended.

When choosing an inductor, make sure the average and peak current ratings are adequate by using Equations 2, 3 and 4 (80% efficiency assumed):

$$I_{LAVG} = \frac{I_{LED} \cdot V_{OUT}}{0.8 \cdot V_{IN}} \quad \text{(EQ. 2)}$$

$$I_{LPK} = I_{LAVG} + \frac{1}{2} \cdot \Delta I_L \quad \text{(EQ. 3)}$$

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{L \cdot V_{OUT} \cdot f_{OSC}} \quad \text{(EQ. 4)}$$

Where:

- ΔI_L is the peak-to-peak inductor current ripple in Amps
- L is the inductance in H.
- f_{OSC} is the switching frequency, typically 1.45MHz

The ISL97632 supports a wide range of inductance values (10µH~82µH). For lower inductor values or lighter loads, the boost inductor current may become discontinuous. For high boost inductor values, the boost inductor current will be in continuous mode.

In addition to the inductor value and switching frequency, the input voltage, the number of LEDs and the LED current also affect whether the converter operates in continuous conduction or discontinuous conduction mode. Both operating modes are allowed and normal. The discontinuos conduction mode yields lower efficiency due to higher peak current.

Compensation

The product of the output capacitor and the load create a pole while the inductor creates a right half plane zero. Both attributes degrade the phase margin but the ISL97632 has an internal compensation network that ensures the device operates reliably under the specified conditions. The internal compensation and the highly integrated functions of the ISL97632 make it a design friendly device to be used in high volume high reliability applications.

Applications

Efficiency Improvement

Figure 2 on page 5 shows the efficiency measurements. The choice of the inductor has a significant impact on the power efficiency. As shown in Equation 4, the higher the inductance, the lower the peak current therefore the lower the conduction and switching losses. On the other hand, it has also a higher series resistance. Nevertheless, the efficiency improvement from lowering the peak current is greater than the impact of the resistance increase with larger value of inductor. Efficiency can also be improved for systems that have high supply voltages. Since the ISL97632 can only supply from 2.4V to 5.5V, V_{IN} must be separated from the high supply voltage for the boost circuit as shown in Figure 7 and the efficiency improvement is shown in Figure 8.

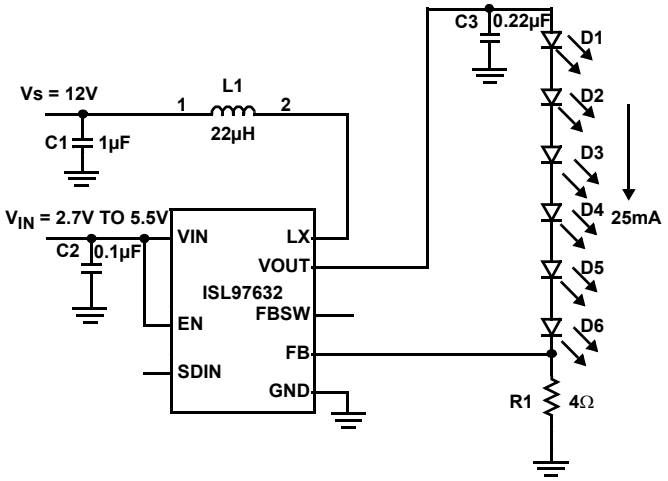


FIGURE 7. SEPARATE HIGH INPUT VOLTAGE FOR HIGHER EFFICIENCY OPERATION

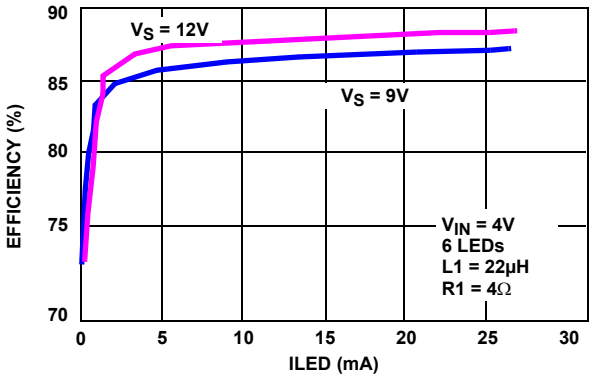


FIGURE 8. EFFICIENCY IMPROVEMENT WITH 9V AND 12V INPUTS

9 LEDs Operation

For medium size LCDs that need more than 7 low power LEDs for backlighting, such as a Portable Media Player or Automotive Navigation Panel displays, the voltage range of the ISL97632 is not sufficient. However, the ISL97632 can be used as an LED controller with an external protection MOSFET connected in cascode fashion to achieve higher output voltage. A conceptual 9 LEDs driver circuit is shown in Figure 9. A 40V logic level N-Channel MOSFET is configured such that its drain ties between the inductor and the anode of Schottky diode, its gate ties to the input, and its source ties to the ISL97632 LX node connecting to the drain of the internal switch. When the internal switch turns on, it pulls the source of M1 down to ground, and LX conducts as normal. When the internal switch turns off, the source of M1 will be pulled up by the follower action of M1, limiting the maximum voltage on the ISL97632 LX pin to below V_{IN}, but allowing the output voltage to go much higher than the breakdown limit on the LX pin. The switch current limit and maximum duty cycle will not be changed by this setup, so input voltage will need to be carefully considered to make sure that the required output voltage and current levels are achievable. Because the source of M1 is effectively floating when the internal LX switch is off, the drain-to-source capacitance of M1 may be sufficient to capacitively pull the node high enough to breaks down the gate oxide of M1. To prevent this, V_{OUT} should be connected to V_{IN}, allowing the internal Schottky to limit the peak voltage. This will also hold the V_{OUT} pin at a known low voltage, preventing the built in OVP function from causing problems. This OVP function is effectively useless in this mode as the real output voltage is outside its intended range. If the user wants to implement their own OVP protection (to prevent damage to the output capacitor, they should insert a zener from V_{OUT} to the FB pin. In this setup, it would be wise not to use the FBSW to FB switch as otherwise the zener will have to be a high power one capable of dissipating the entire LED load power. Then the LED stack can then be connected directly to the sense resistor and via a 10k resistor to FB. A zener can be placed from V_{OUT} to the FB pin allowing an over voltage event to pull up on FB with a low breakdown current (and thus low power zener) as a result of the 10k resistor.

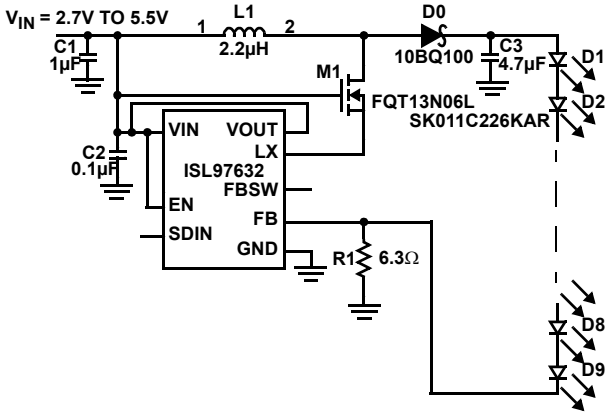


FIGURE 9. CONCEPTUAL 9 LEDS HIGH VOLTAGE DRIVER

SEPIC Operation

For applications where the output voltage is not always above the input voltage, a buck or boost regulation is needed. A SEPIC (Single Ended Primary Inductance Converter) topology, (see Figure 10), can be considered for such an application. A single cell Li-Ion battery operating a cellphone backlight or flashlight is one example. The battery voltage is between 2.5V and 4.2V depending on the state of charge. On the other hand, the output may require only one 3V to 4V medium power LED for illumination because the light guard of the backlight assembly is optimized or it is a cost efficiency trade off reason.

In fact, a SEPIC configured LED driver is flexible enough to allow the output to be well above or below the input voltage, unlike the previous example. Another example is when the number of LEDs and input requirements are different from platform to platform, a common circuit and PCB that fit all the platforms, in some cases, may be beneficial enough that it outweighs the disadvantage of adding additional component cost. L1 and L2 can be a coupled inductor in one package.

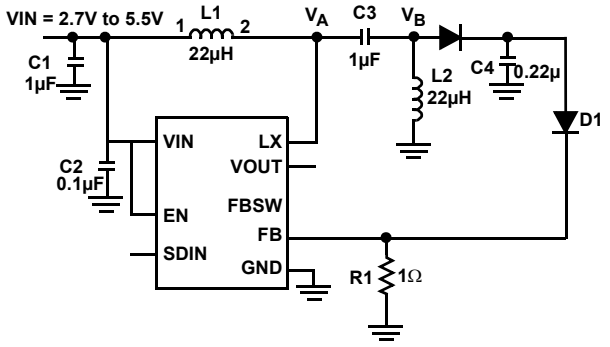


FIGURE 10. SEPIC LED DRIVER

The simplest way to understand SEPIC topology is to think about it as a boost regulator in which the input volute is level shifted downward at the same magnitude and the lowest reference level starts at $-V_{IN}$ rather than 0V.

The SEPIC works as follows: Assume the circuit in Figure 10 operates normally when the ISL97632 internal switch opens, and it is in the PWM 'OFF' state. After a short duration where few LC time constants elapsed, the circuit is considered in the steady-state within the PWM 'OFF' period that L1 and L2 are shorted. V_B is therefore shorted to the ground and C3 is charged to V_{IN} with $V_A = V_{IN}$. When the ISL97632 internal switch closes, and the circuit is in the PWM on state, V_A is now pulled to ground. Since the voltage in C3 cannot be changed instantaneously, V_B is shifted downward and becomes $-V_{IN}$. The next cycle, when the ISL97632 switch opens, V_B boosts up to the targeted output like the standard boost regulator operation, except the lowest reference point is at $-V_{IN}$. The output is approximated as shown in Equation 5:

$$V_{OUT} = V_{IN}\frac{D}{(1-D)} \quad \text{(EQ. 5)}$$

where D is the on-time of the PWM duty cycle.

The convenience of SEPIC comes with some trade off in addition to the additional L and C costs. The efficiency is usually lowered because of the relatively large efficiency loss through the Schottky diode if the output voltage is low. The L2 series resistance also contributes additional loss. Figure 11 shows the efficiency measurement of a single LED application as the input varies between 2.7V and 4.2V.

Note, V_B is considered the level-shifted LX node of a standard boost regulator. The higher the input voltage, the lower the V_B voltage will be during PWM on period. The result is that the efficiency will be lower at higher input voltages because the SEPIC has to work harder to boost up to the required level. This behavior is the opposite to the standard boost regulator's and the comparison is shown in Figure 11.

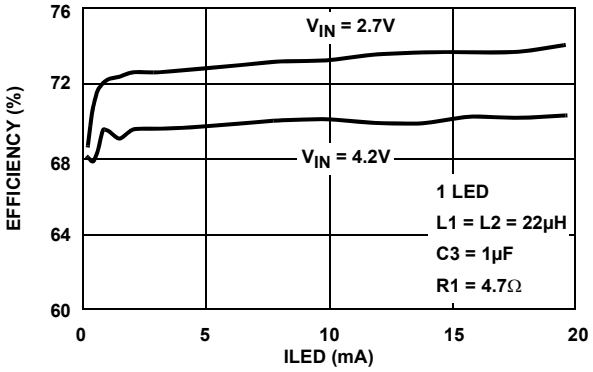


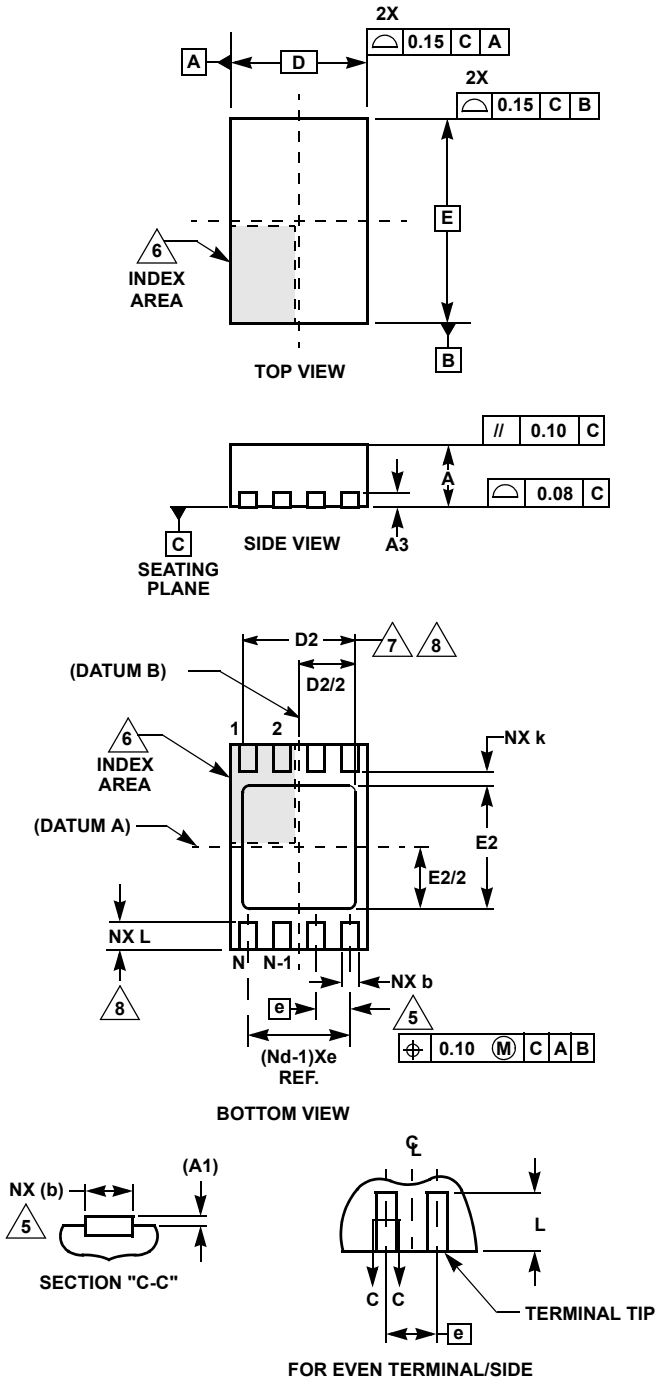
FIGURE 11. EFFICIENCY MEASUREMENT OF 1 LED SEPIC DRIVER

PCB Layout Considerations

The layout is very important for the converter to function properly. R_{SET} must be located as close as possible to the FB and GND pins. Longer traces to the LEDs are acceptable. Similarly, the supply decoupling capacitor and the output filter capacitor should be as close as possible to the VIN and VOUTpins.

The heat of the IC is mainly dissipated through the thermal pad of the package. Maximize the copper area connected to this pad if possible. In addition, a solid ground plane is always helpful for the EMI performance.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.2x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.