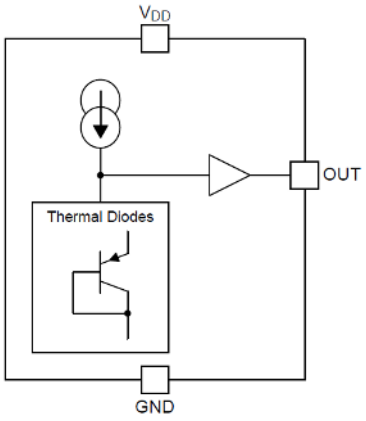
TMP9A00-EP ±2.5 °C Low-Power, Analog Out Temperature Sensor

1 Features

- ±2.5 °C Accuracy from –55 °C to +130 °C
- ±3.5 °C Accuracy from –55 °C to +150 °C
- Supply voltage range: 1.8 V to 5.5 V
- Low power: 4 µA (maximum)
- Microsize package: SC70
- Supports defense, aerospace, and medical applications
  - Controlled baseline
  - One assembly/test site
  - One fabrication site
  - Extended product life cycle
  - Extended product-change notification
  - Product traceability

2 Applications

- Defense radio
- Radar
- Avionics
- Sensors and imaging



Device Block Diagram

3 Description

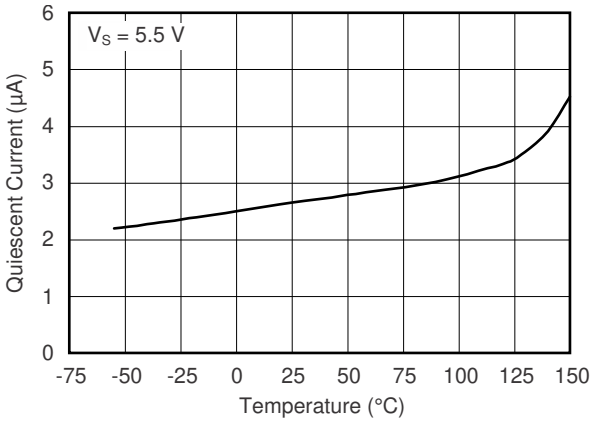
The TMP9A00-EP device is a CMOS, precision analog output temperature sensor available in a tiny 5-pin SC70 package. The TMP9A00-EP operates from –55 °C to 150 °C on a supply voltage of 1.8 V to 5.5 V with a supply current of 4 µA. Operation as low as 1.8 V is possible for temperatures between 15 °C and 150 °C. The linear transfer function has a slope of –11.77 mV/°C (typical) and an output voltage of 1.8639 V (typical) at 0 °C. The TMP9A00-EP has a ±2.5 °C accuracy a from –55 °C to 130 °C and ±3.5 °C from 130 °C to 150 °C.

The 4-µA (maximum) supply current of the TMP9A00-EP limits self-heating of the device to less than 0.01 °C. When V+ is less than 0.5 V, the device is in shutdown mode and consumes less than 20 nA (typical).

The TMP9A00-EP is available in a 5-pin SC70 package that reduces the overall required board space.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP9A00-EP	SC70 (5)	2.00 mm × 1.25 mm



Device Quiescent Current Over Temperature

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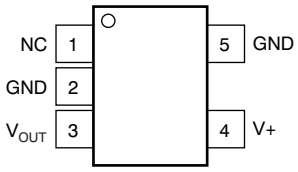
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (February 2021)	Page
• Updated Wirebond Life Derating Curve	12

5 Pin Configuration and Functions



NC- no internal connection

Figure 5-1. DCK Package 5-Pin SC70 Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	DCK (SC70)		
GND	2	—	This pin must be grounded or left floating. For best thermal response, connect to GND plane. See *Layout Example* for more information.
	5	—	Ground pin
NC	1	—	This pin must be grounded or left floating. See *Layout Example* for more information.
V_{OUT}	3	O	Analog output
V+	4	I	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}	-0.3	7	V
Operating junction temperature, T_J		-65	150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.8	3.3	5.5	V
T_A	Operating ambient temperature	-55		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP9A00-EP
		DCK
		6-pins
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229.0
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.9
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A
$R_{\theta JB}$	Junction-to-board thermal resistance	73.4
ψ_{JT}	Junction-to-top characterization parameter	42.5
ψ_{JB}	Junction-to-board characterization parameter	73.0

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.8 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR}	Temperature accuracy(1)	-55 °C to 130 °C		-2.5		2.5	°C
		130 °C to 150 °C		-3.5		3.5	°C
PSR	DC power supply rejection	V_{DD} = 1.8 V to 5.5 V T_A = 15 °C to 150 °C		-0.05		0.05	°C/V
		V_{DD} = 2.7 V to 5.5 V T_A = -55 °C to 150 °C		-0.15		0.15	°C/V
T_{SENS}	Temperature sensitivity(2)	T_A = -55 °C to 150 °C			-11.77		mV/°C
V_{OUT}	Output voltage(3)	T_A = 0 °C			1863.9		mV
		T_A = 25 °C			1574		mV
NL	Nonlinearity(4)	TA = -55 °C to 150 °C			±0.4		%
ANALOG OUTPUT							
V_{OUT_R}	Output resistance	I_{LOAD} = -600 µA to 600 µA			10		Ω
L_R	Load regulation	I_{LOAD} = -600 µA to 600 µA			6		mV
C_L	Maximum capacitive load			1			nF
POWER SUPPLY							
V_{DD}	Operating voltage	T_A = -55 °C to 150 °C		2.7		5.5	V
		T_A = 15 °C to 150 °C(5)		1.8		5.5	V
I_{DD}	Supply current	V_{DD} = 5.5 V T_A = 25 °C			2.6	4	µA
		V_{DD} = 5.5 V T_A = -55 °C to 150 °C				7	µA
I_{DD_SD}	Shutdown current	V_{DD} < 0.5 V			20		nA

(1) Power-supply rejection is encompassed in the accuracy specification.

(2) Temperature sensitivity is the average slope to the equation VO = (–11.77 × T) + 1.860 V

(3) VOUT is calculated from temperature with the following equation:
VO = (–3.88 × 10–6 × T 2) + (–1.15 × 10–2 × T) + 1.8639 V, where T is in °C.

(4) Nonlinearity is the deviation of the calculated output voltage from the best fit straight line.

(5) The TMP9A00-EP transfer function requires the output voltage to rise above the 1.8-V supply as the temperature decreases below 15°C. When operating at a 1.8-V supply, it is normal for the TMP9A00-EP output to approach 1.8 V and remain at that voltage as the temperature continues to decrease below 15°C. This condition does not damage the device. Once the temperature rises above 15°C, the output voltage resumes changing as the temperature changes, according to the transfer function specified in this document.

6.6 Typical Characteristics

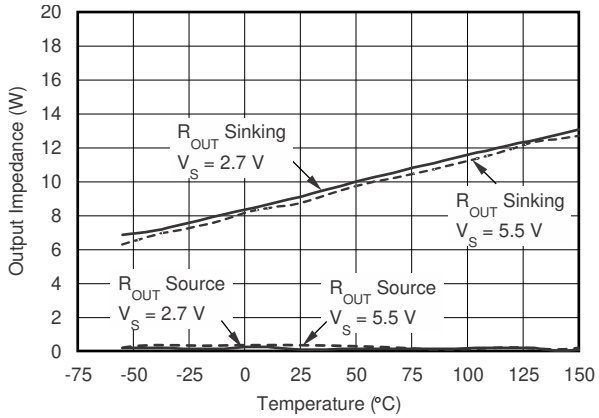


Figure 6-1. Output Impedance vs Temperature

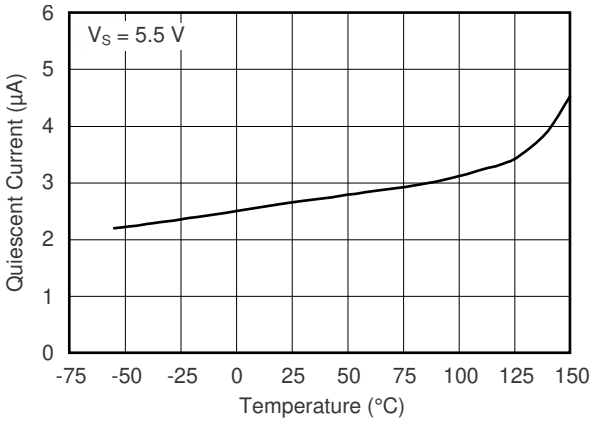


Figure 6-2. Quiescent Current vs Temperature

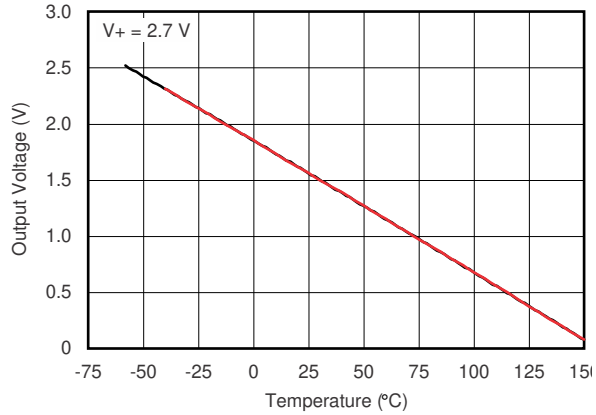


Figure 6-3. Output Voltage vs Temperature

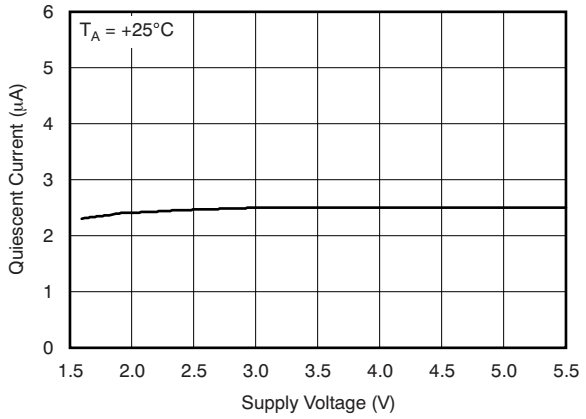


Figure 6-4. Quiescent Current vs Supply Voltage

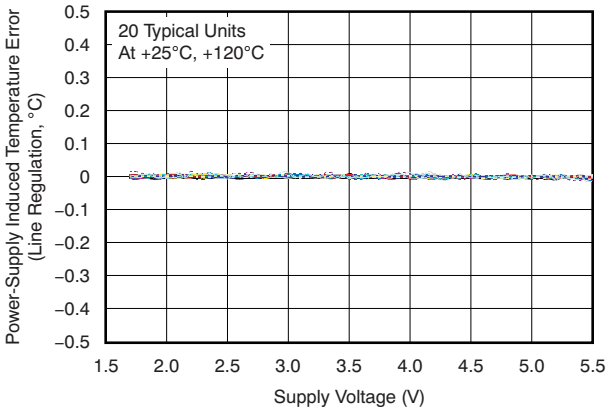


Figure 6-5. Power-Supply Rejection vs Temperature

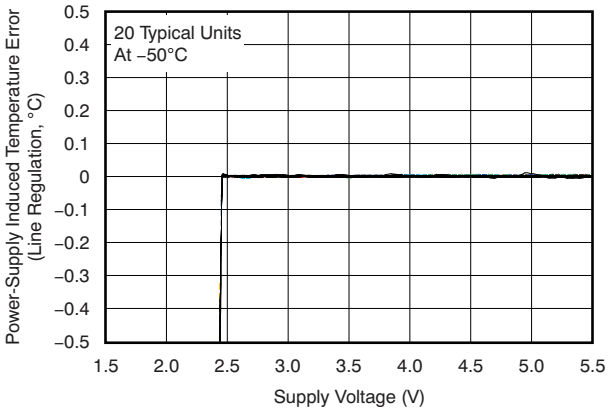


Figure 6-6. Power-Supply Rejection vs Temperature

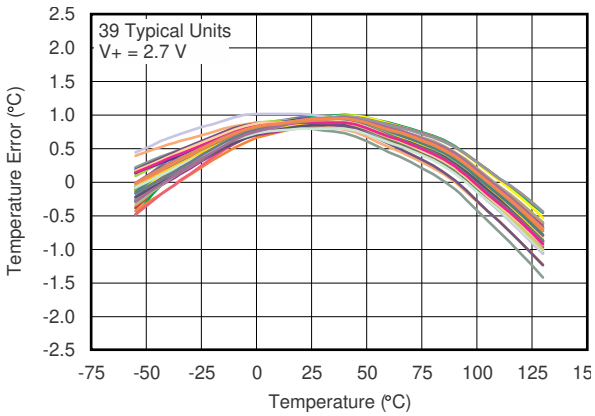


Figure 6-7. Temperature Error vs Temperature

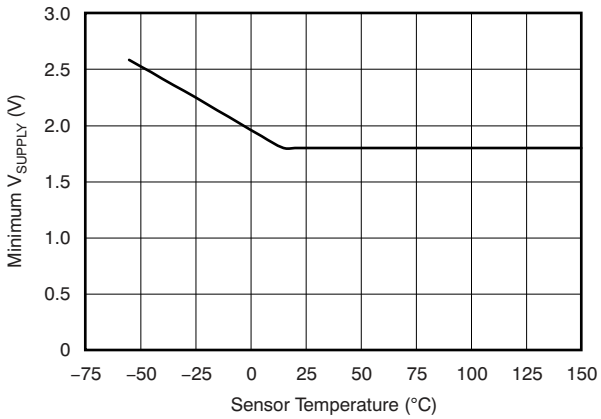


Figure 6-8. Minimum Supply Voltage vs Temperature

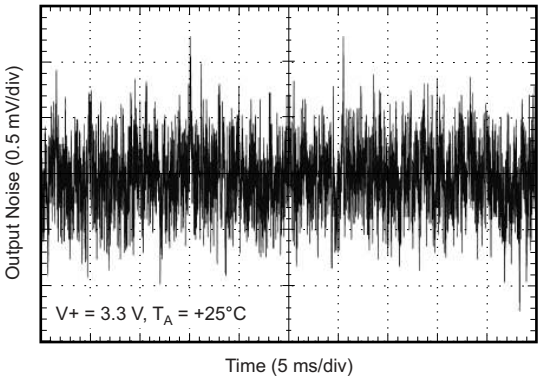


Figure 6-9. Wideband Output Noise Voltage

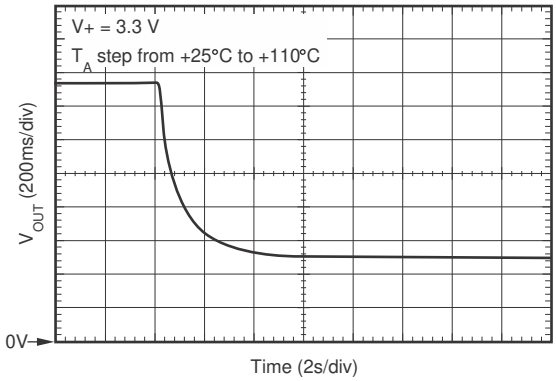


Figure 6-10. Thermal Settling (Fluid-Filled Temperature Bath)

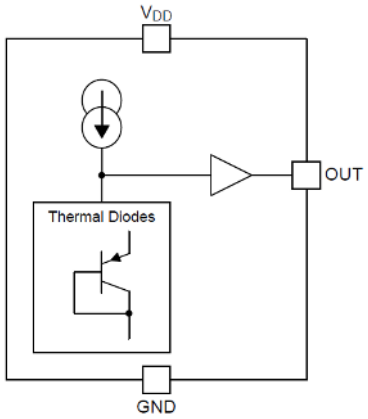
7 Detailed Description

7.1 Overview

The TMP9A00-EP device is a precision analog output temperature sensor. The temperature range of operation is –55 °C to 150 °C with supply voltages of 1.8 V to 5.5 V. The TMP9A00-EP operates from power-supply voltages as low as 1.8 V over a temperature range of 15 °C to 150 °C.

TI recommends power supply bypassing. Use a 100-nF capacitor placed as close to the supply pin as possible.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Transfer Function

The analog output of the TMP9A00-EP over the –55 °C to 150 °C temperature range corresponds to the parabolic transfer function shown in Equation 1:

$$V_{OUT} = \left(-3.88 \times 10^{-6} \times T^2\right) + \left(-1.15 \times 10^{-2} \times T\right) + 1.8639\ V \quad (1)$$

Where:

- The temperature (T) is in °C.

When solving for temperature, the equation is shown as Equation 2.

$$T = -1481.96 + \sqrt{2.1962 \times 10^{6} + \frac{\left(1.8639 - V_O\right)}{3.88 \times 10^{-6}}} \quad (2)$$

These equations apply over the entire operating range of –55 °C to 150 °C.

A simplified linear transfer function referenced at 0 °C is shown in Equation 3:

$$V_{OUT} = -11.69\ mV/°C \times T + 1.8863\ V \quad (3)$$

Linear transfer functions are calculated for limited temperature ranges by calculating the slope and offset for that limited range, where slope is calculated by Equation 4:

$$m = -7.76 \times 10^{-6} \times T - 0.0115 \quad (4)$$

Where:

- T equals the temperature at the middle of the temperature range of interest.

The offset in the linear transfer function is calculated with Equation 5:

$$b = \left(V_{OUT}\left(T_{MAX}\right) + V_{OUT}\left(T\right) - m \times \left(T_{MAX} + T\right)\right) / 2 \quad (5)$$

where

- $V_{OUT}(T_{MAX})$ is the calculated output voltage at T_{MAX}.

7.3.1.1 Example 1

Determine the linear transfer function for –40 °C to 110 °C.

T_{MIN} = –40 °C; T_{MAX} = 110 °C; therefore, T = 35 °C

m = –11.77 mV/°C

V_{OUT} (110 °C) = 0.5520 V

V_{OUT} (35 °C) = 1.4566 V

b = 1.8576 V

The linear transfer function for –40 °C to 110 °C is shown in Equation 6:

$$V_{OUT} = -11.77\ mV/°C \times T + 1.8576\ V \quad (6)$$

Table 7-1 lists common temperature ranges of interest and the corresponding linear transfer functions for these ranges. Note that the error (maximum deviation) of the linear equation from the parabolic equation increases as the temperature ranges widen.

Table 7-1. Common Temperature Ranges and Corresponding Linear Transfer Functions

TEMPERATURE RANGE		LINEAR EQUATION (V)	MAXIMUM DEVIATION OF LINEAR EQUATION FROM PARABOLIC EQUATION (°C)
T_{MIN} (°C)	T_{MAX} (°C)		
–55	130	V_{OUT} = –11.79 mV/°C × T + 1.8528	±1.41
–40	110	V_{OUT} = –11.77 mV/°C × T + 1.8577	±0.93
–30	100	V_{OUT} = –11.77 mV/°C × T + 1.8605	±0.70
–40	85	V_{OUT} = –11.67 mV/°C × T + 1.8583	±0.65
–10	65	V_{OUT} = –11.71 mV/°C × T + 1.8641	±0.23
35	45	V_{OUT} = –11.81 mV/°C × T + 1.8701	±0.004
20	30	V_{OUT} = –11.69 mV/°C × T + 1.8663	±0.004

7.4 Device Functional Modes

The singular functional mode of the TMP9A00-EP is an analog output inversely proportional to temperature.

8 Application and Implementation

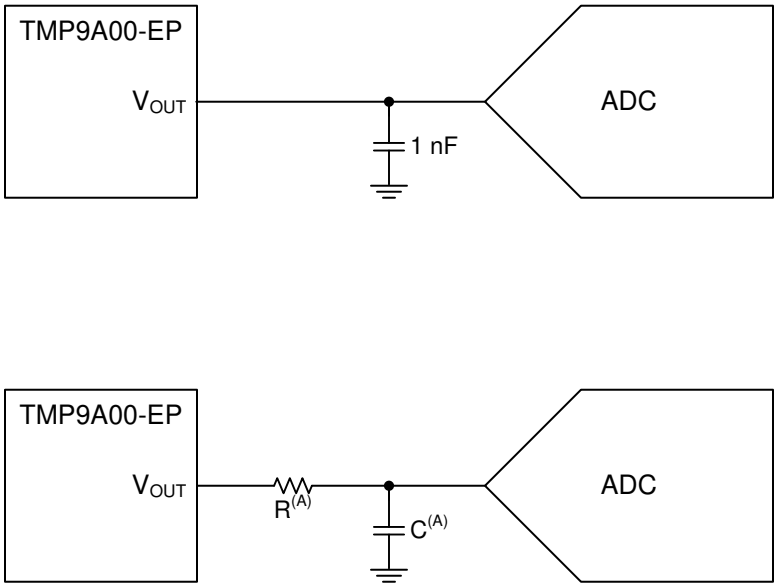
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Drive and Capacitive Loads

When used in noisy environments, adding a capacitor from the output to ground with a series resistor filters the TMP9A00-EP output as shown in Figure 8-1. The TMP9A00-EP can drive up to 1-nF load capacitance while sourcing and sinking 600 µA. While sinking or sourcing 600 µA, capacitive loads in the range of 1 nF to 10 µF require a 150-Ω series output resistor to achieve a stable temperature measurement. The output impedance of the TMP9A00-EP is typically 10 Ω when sinking currents and less than 1 Ω when sourcing current as shown in Figure 6-1.

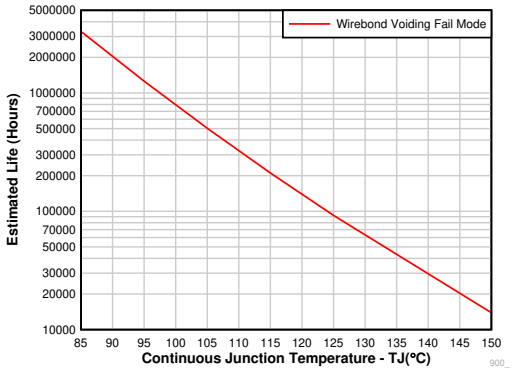


A. A series resistor (R) may be required depending on the amount of capacitance (C) and the amount of source and sink current drawn from the output of the TMP9A00-EP.

Figure 8-1. TMP9A00-EP Output Filtering

8.1.2 Operating Life Deration

The information in this section is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.



1. Silicon operating life design goal is 100000 power-on hours (POH) at 105 °C junction temperature (does not include package interconnect life).
2. The predicted operating lifetime versus junction temperature is based on reliability modeling using wirebond lifetime as the dominant failure mechanism affecting device wear out for the specific device process and design characteristics.

Wirebond Life Derating Curve

8.2 Typical Application

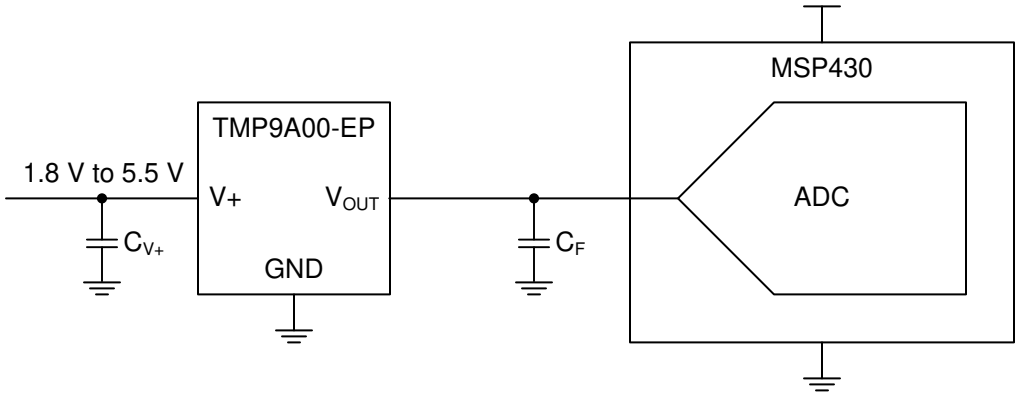


Figure 8-2. Suggested Connections to a MCU ADC

8.2.1 Design Requirements

ADCs that are found in microcontrollers have leakage current during the sampling phase to charge the sampling capacitor. A high sampling frequency can have higher average input leakage that sags the output voltage of the TMP9A00-EP, which results in a reading that is hotter than normal. To mitigate this, place a capacitor (C_F) between the TMP9A00-EP and the ADC. The capacitor functions as a charge reservoir to smooth out the output voltage and remove the voltage sag.

The TMP9A00-EP output voltage has a negative slope and can not output a voltage higher than the VDD voltage. For this reason the effective operating temperature range of the device is restricted by supply. At 2.7 V, the device will output accurate temperature results from –55 °C to 150 °C. Using a supply voltage of 1.8 V will rail the output unless the temperature range is between 15 °C to 150 °C. Equation 7 can be used to find the minimum operating temperature of the device in this region. The minimum VDD must also satisfy the Recommended Operating Conditions 1.8 V regardless of ambient temperature.

$$VDD_{MIN} = \frac{(1863.9 - 11.77 \times T_A + 110)}{1000} \quad (7)$$

8.2.2 Detailed Design Procedure

The size of C_F depends on the size of the internal sampling capacitor and the sampling frequency. The charge requirements may vary because not all ADCs have identical input stages. This general ADC application is shown as an example only.

Equation 8 shows an example of how to translate the VOUT of the TMP9A00-EP into temperature. This can be implemented in the microcontroller in control of the ADC to record temperature. Another possible way to use the TMP9A00-EP is as a temperature switch in software. The same equation can be used to translate different temperature points into discrete voltages. For example, if a desired overtemperature condition is 105 °C, the corresponding voltage output would be 628 mV.

$$T = \frac{(1.8639 - V_{OUT})}{0.01177} \quad (8)$$

8.2.3 Application Curves

Figure 8-3 shows the quiescent current versus temperature.

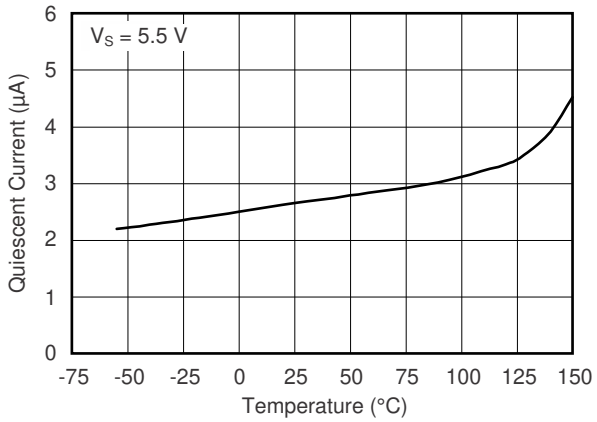


Figure 8-3. Quiescent Current vs Temperature

9 Power Supply Recommendations

The low supply current and supply range of 1.8 V to 5.5 V enable the TMP9A00-EP to be powered from a variety of supply topologies.

Power supply bypassing is optional and is typically dependent on the noise of the power supply. In noisy systems, adding bypass capacitors may be necessary to decrease the noise that couples to the output of the TMP9A00-EP.

10 Layout

10.1 Layout Guidelines

The substrate on the TMP9A00-EPAIDCK package is directly connected through a conductive epoxy to pin 2 on the lead frame. Consequently, pin 2 is the best lead for a conductive thermal connection to the TMP9A00-EP die. The optimal electrical connection for this pin is ground (GND).

CAUTION

Do not attempt to connect pin 2 (DCK package) to any electrical potential other than ground.

If it is not possible to connect pin 2 to ground, it is possible to electrically isolate this pin (that is, leave it floating). Take care when electrically isolating this pin because any noise or electromagnetic interference or radio frequency interference (EMI or RFI) spikes that couple in through this pin can cause erroneous temperature results.

10.2 Layout Example

Figure 10-1 shows a layout of the TMP9A00-EP with proper electrical and thermal connections to pin 2.

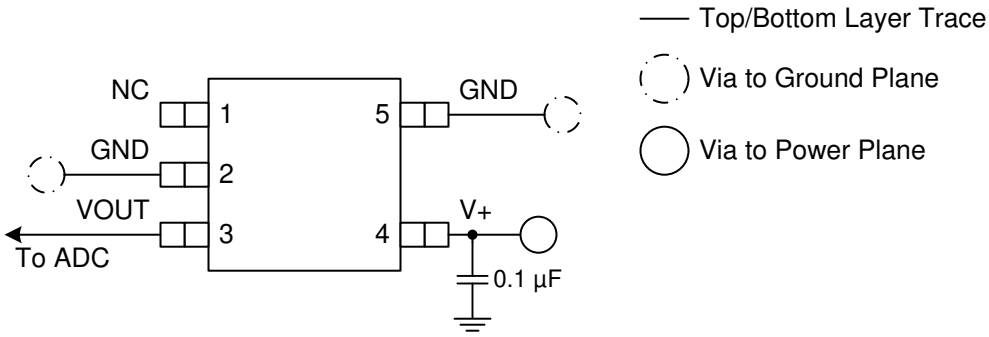


Figure 10-1. TMP9A00-EP Layout With Proper Electrical and Thermal Connections

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Introduction to Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP9A00MDCKREP	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	1I7	Samples
TMP9A00MDCKTEP	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	1I7	Samples
V62/20606-01EX	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	1I7	Samples
V62/20606-01EX-T	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	1I7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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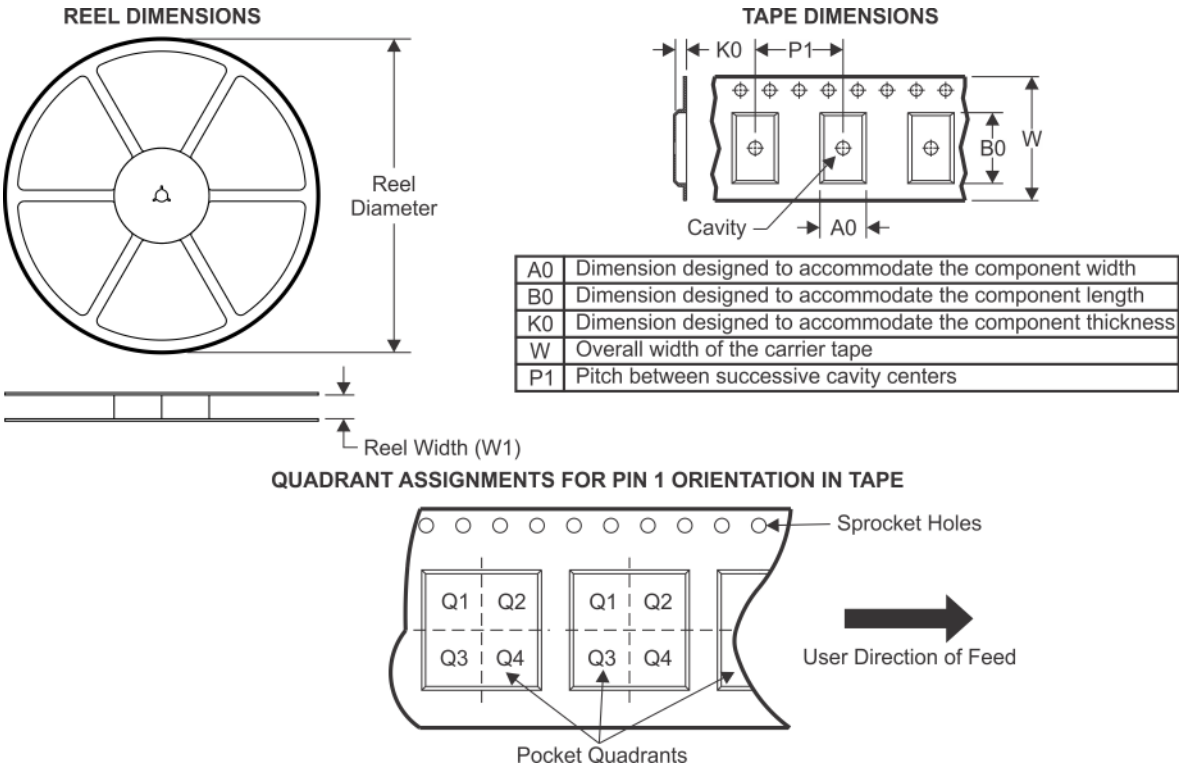
TAPE AND REEL INFORMATION

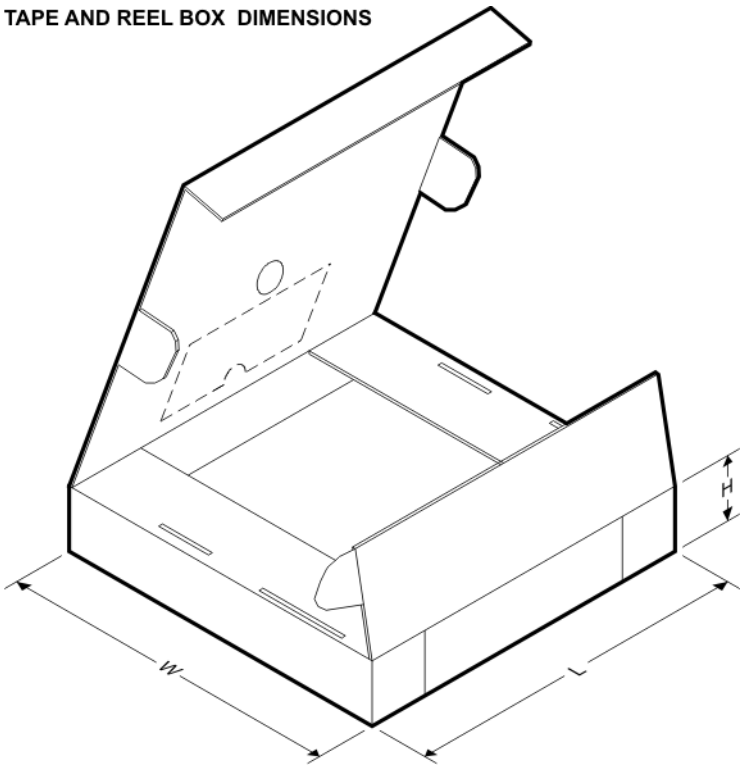


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP9A00MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TMP9A00MDCKTEP	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

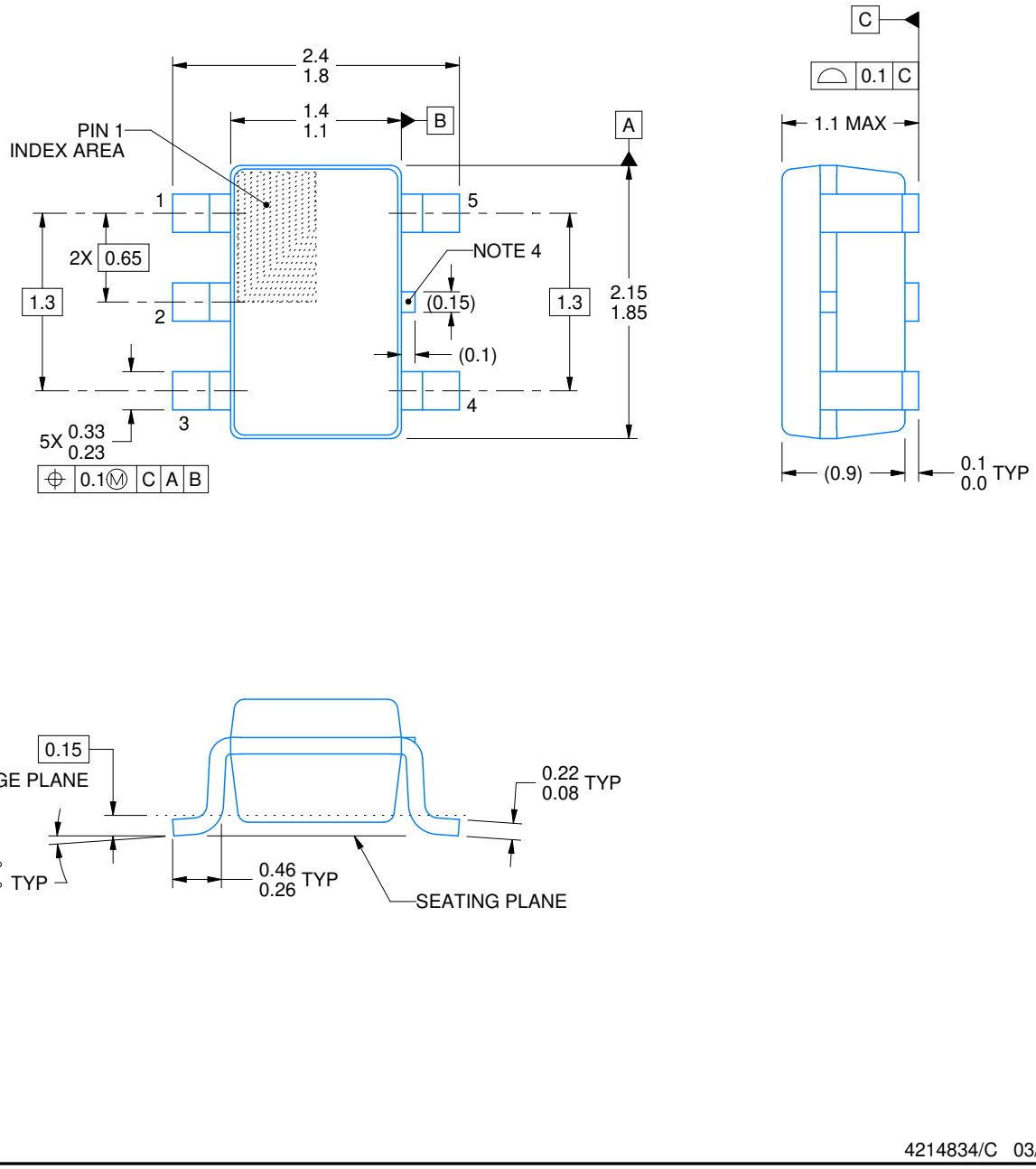
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP9A00MDCKREP	SC70	DCK	5	3000	213.0	191.0	35.0
TMP9A00MDCKTEP	SC70	DCK	5	250	213.0	191.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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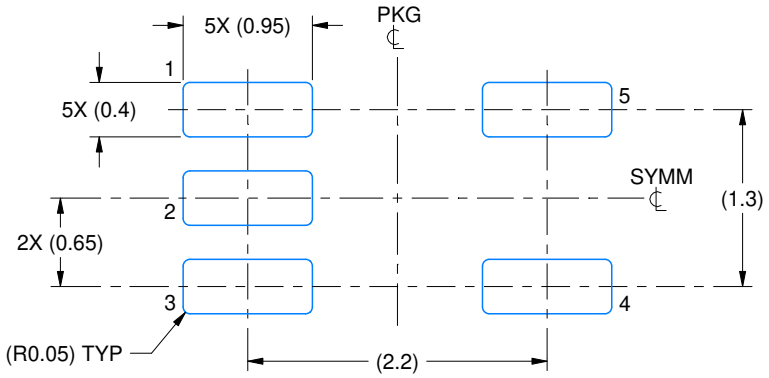
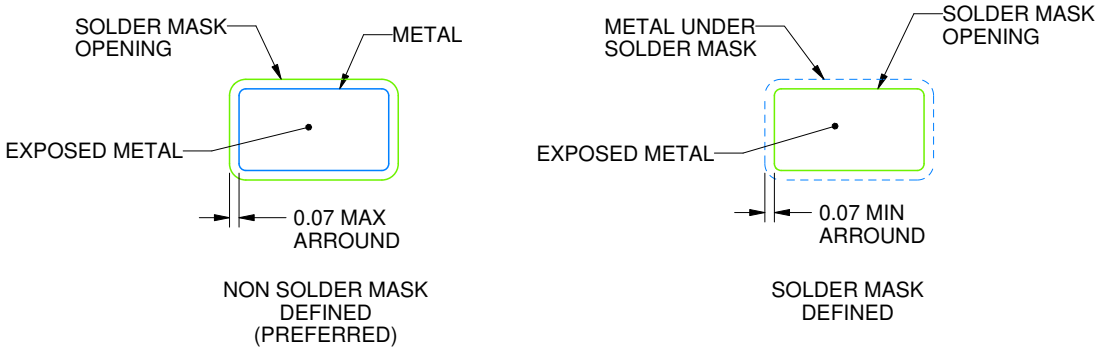
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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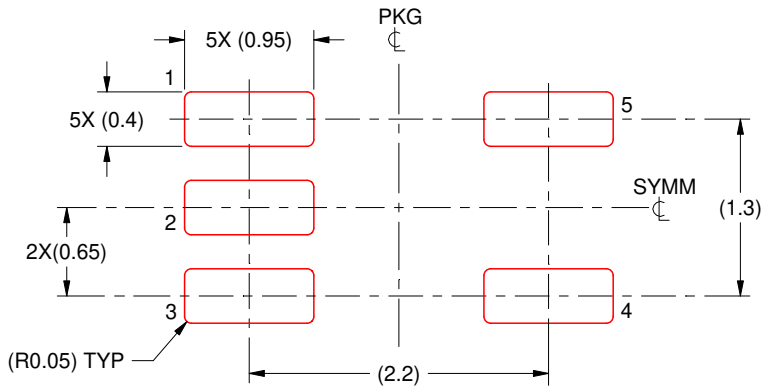
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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