19-0379; Rev 1; 11/99

MAXIM

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

General Description

The MAX3270 is a complete Clock Recovery and Data Retiming IC for 155Mbps and 622Mbps SDH/SONET and ATM applications. The MAX3270 meets Bellcore and CCITT jitter tolerance specifications ensuring error-free data recovery. Recovered clock and data are phase aligned using a fully integrated phase-locked loop (PLL). An output frequency monitor (FM) is included to detect loss of PLL acquisition or a loss of input data.

The MAX3270 has differential ECL input and output interfaces, so it is less susceptible to noise in a high-frequency environment. The fully integrated PLL includes an integrated phase-frequency detector that eliminates the need for external references.

Applications

155Mbps (STM-1/OC-3)/622Mbps (STM-4/OC-12) SDH/SONET Transmission Systems

155Mbps/622Mbps ATM/SONET Access Nodes

Add/Drop Multiplexers

Cross-Connects

Features

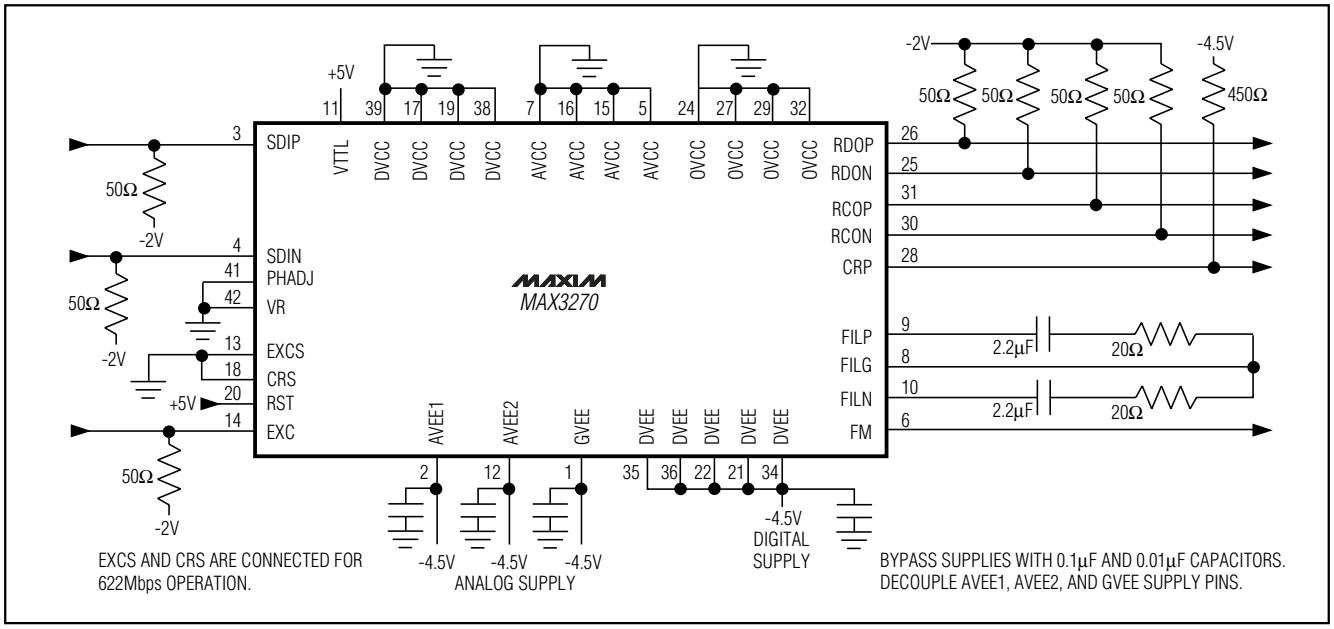
- **Supports Both 155Mbps and 622Mbps Clock Recovery and Data Retiming**
- **Fully Integrated Phase/Frequency Detector**
- **Capable of Switching to an External Clock**
- **Differential 100K ECL Data and Clock I/Os**
- **Output Monitor Provides Lock Detection**
- **No External Reference Clock Required**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3270EMH	-40°C to +85°C	44 MQFP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- VTTL to GND .....-0.5V to +8.0V
- V_{CC} to GND .....-0.5V to +8.0V
- V_{EE} to GND .....-8.0V to +0.5V

SDIP, SDIN, EXC .....-8.0V to +0.5V
RDOP, RDON, RCOP, RCON, CRP .....-8.0V to +0.5V
EXCS, RST, CRS .....-0.5V to +8.0V
FILP, FILG, FILN .....-8.0V to +0.5V
PHADJ, VR .....-8.0V to +8.0V
FM .....-8.0V to +8.0V
Input Differential Voltage Level, SDIP, SDIN .....+3.0V
Continuous Power Dissipation (T_A = +85°C) 1.3W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V ±5%, VTTL = 5V ±5%, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Voltage Supply (with respect to ground)	V_{TTL}		4.75	5.00	5.25	V
Negative Voltage Supply (with respect to ground)	V_{EE}		-4.725	-4.50	-4.275	V
Static Supply Current from VTTL	I_{TTL}			2.4	5	mA
Static Supply Current from V_{EE}	I_{VEE}			150	210	mA
ECL INPUTS: EXC, SDIP, SDIN						
Input High Voltage	V_{IH}		-1165		-870	mV
Input Low Voltage	V_{IL}		-1830		-1475	mV
Input High Current	I_{IH}	V_{IN} = V_{OH} (typ)	0		100	µA
Input Low Current	I_{IL}	V_{IN} = V_{OL} (typ)	-100		100	nA
ECL OUTPUTS: RCOP, RCON, RDOP, RDON						
Output High Voltage	V_{OH}	Loaded with 50Ω to -2V	-1025	-955	-870	mV
Output Low Voltage	V_{OL}	Loaded with 50Ω to -2V	-1830	-1705	-1550	mV
LOW-POWER ECL OUTPUT: CRP						
Output High Voltage	V_{OH}	Loaded with 470Ω to V_{EE}	-1025	-955	-870	mV
Output Low Voltage	V_{OL}	Loaded with 470Ω to V_{EE}	-1830	-1705	-1620	mV
TTL INPUTS: CRS, RST, EXCS						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	VTTL = 5.00V, VIN = 2V	0		40	µA
Input Low Current	I_{IL}	VTTL = 5.00V, VIN = 0.8V	0		40	µA
PHASE ADJUST INPUTS: PHADJ, VR						
Input Bias Current	I_{BIAS}	VR = PHADJ = 0, T_A = +25°C	0		10	µA

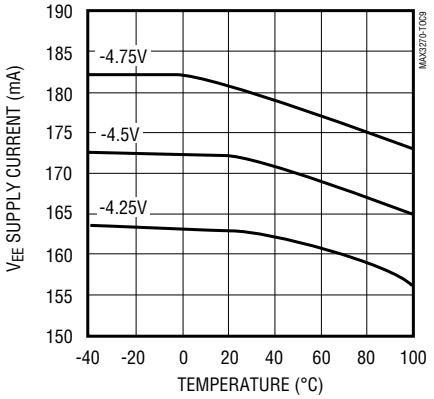
AC ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -4.5V, VTTL = 5V, T_A = 25°C, unless otherwise noted.)

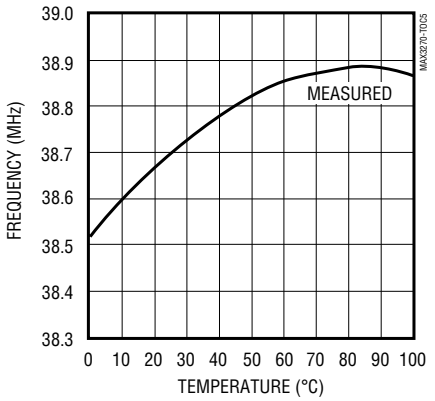
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ECL OUTPUTS: RDOP, RDON, RCOP, RCON						
Transition Time 20% to 80%	t_r, t_f	Loaded with 50Ω to -2V and 5pF to GND		600		ps
Time Difference between RDO and RCO	TD	Loaded with 50Ω to -2V and 5pF to GND		100		ps
PFD AND FILTER AMPLIFIER TEST LEVELS						
Output Offset Voltage of the Monitor Amplifier	V_O	PHADJ = 0, FILP and FILN shorted	-35		35	mV
Gain of the Monitor Amplifier	GFM	PHADJ = 0	0.95		1.05	V/V
Filter Amplifier Open-Loop Voltage Gain	GOL	FILP and FILN open	21	26		dB
VCO TEST PARAMETERS; CPR OUTPUT						
Center Frequency	F_O	FILP and FILN shorted, PFD = neutral state	38.00		39.50	MHz
Frequency Range	DF_O	FILP - FILN = 1.6V	6		10	MHz
Mean Frequency Sensitivity	K_O	FILP - FILN = 1.6V	3.75		6	MHz/V
Frequency Sensitivity to Power-Supply Voltage	K_{OV}	FILP and FILN shorted			550	kHz/V
PLL ELECTRICAL SPECIFICATIONS						
Frequency of VCO	F_O			622.08		MHz
Incremental Tuning Sensitivity (Incremental Slope, Δf/ΔVt)	K_O	f_t = 622.08MHz		75		MHz/V
Phase-Detector Gain	KD			192		mV/rad
Transconduction Gain of Filter Amplifier	Gm			1.25		mA/V
Phase Offset Sensitivity, ΔΦ/ΔPHADJ	K_{PHADJ}			2		rad/V

Typical Operating Characteristics

V_{EE} SUPPLY CURRENT vs. TEMPERATURE



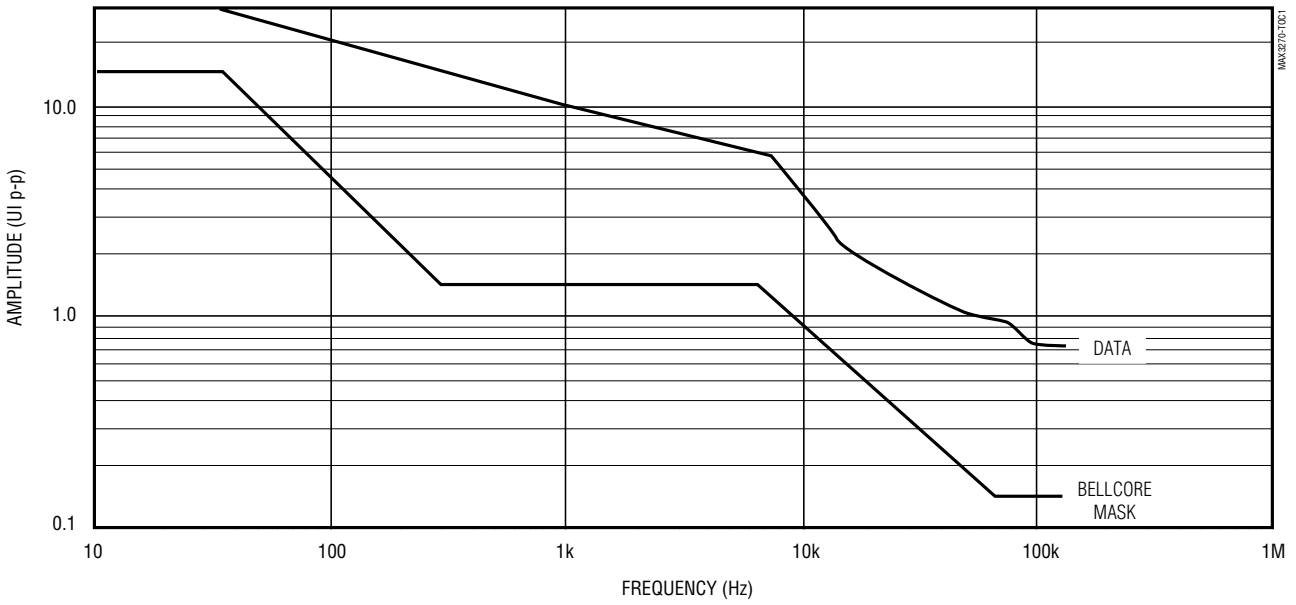
CRP FREE-RUNNING FREQUENCY (VCO/16) vs. DIE TEMPERATURE



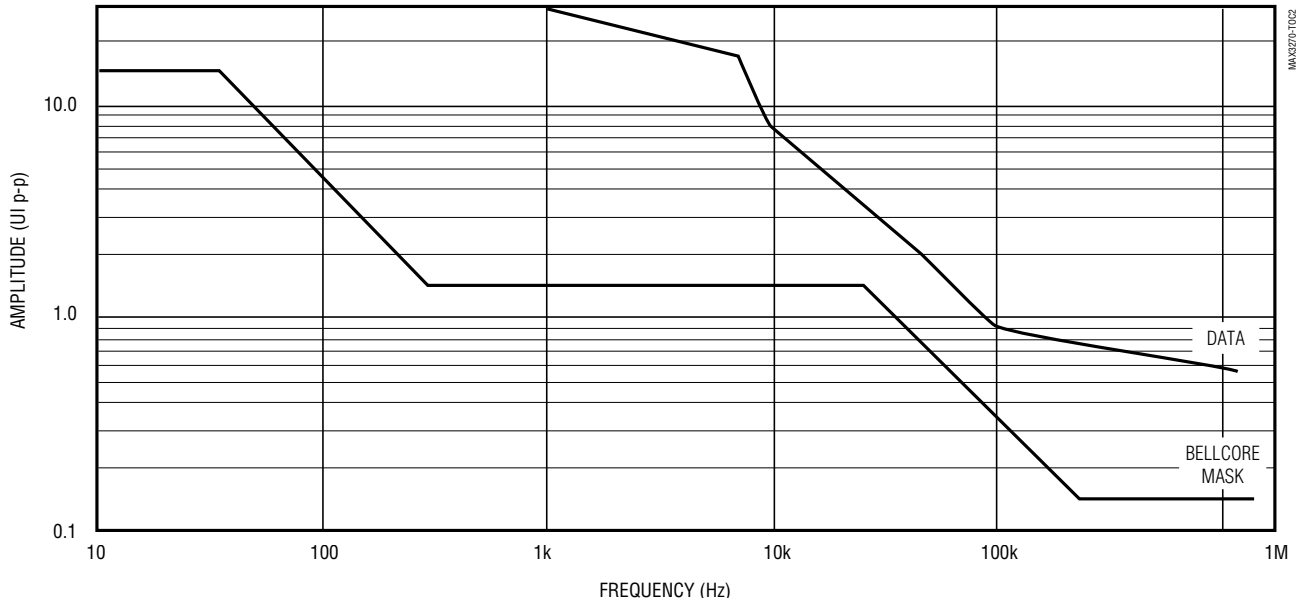
155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Typical Operating Characteristics (continued)

JITTER TOLERANCE
(155Mbps, 2^{23}-1 PRBS)



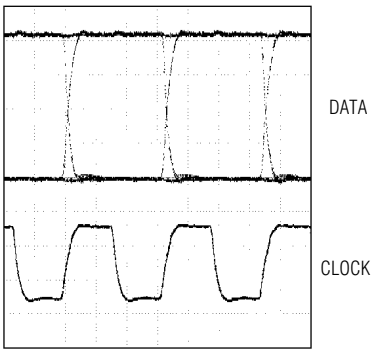
JITTER TOLERANCE
(622Mbps, 2^{23}-1 PRBS)



155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

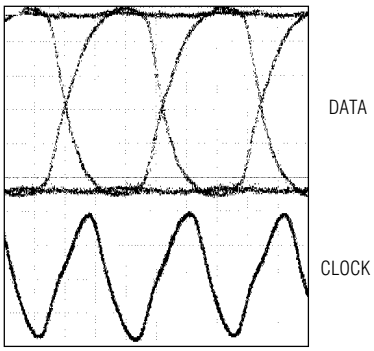
Typical Operating Characteristics (continued)

155Mbps RECOVERED CLOCK AND RETIMED DATA (SINGLE ENDED)



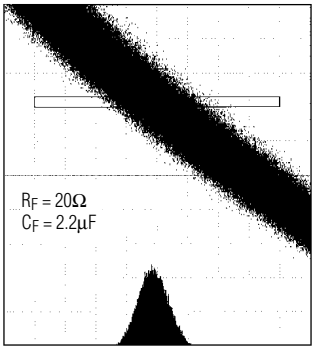
2ns/div

622Mbps RECOVERED CLOCK AND RETIMED DATA (SINGLE ENDED)



500ps/div

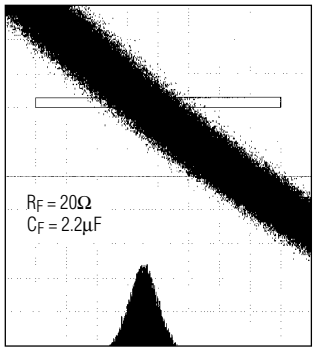
RECOVERED CLOCK JITTER (155Mbps, 2^7-1 PRBS, 5.1ps RMS)



10ps/div

Mean	40.61ns	µ±1σ	68.961%
RMSΔ	5.13ps	µ±2σ	95.844%
PkPk	45.6ps	µ±3σ	99.717%

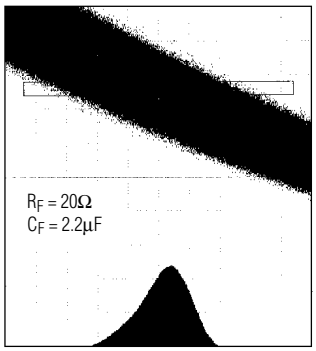
RECOVERED CLOCK JITTER (155Mbps, 1-0 PATTERN, 4.7ps RMS)



10ps/div

Mean	40.65ns	µ±1σ	69.674%
RMSΔ	4.7ps	µ±2σ	95.558%
PkPk	38.4ps	µ±3σ	99.698%

RECOVERED CLOCK JITTER (622Mbps 2^7-1 PRBS 9.0ps RMS)



10ps/div

Mean	38.68ns	µ±1σ	69.747%
RMSΔ	9.049ps	µ±2σ	95.453%
PkPk	79.4ps	µ±3σ	99.582%

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Pin Description

PIN	NAME	FUNCTION
1	GVEE	Guard-Ring Negative Supply to Substrate: -4.5V
2	AVEE1	Negative Supply for Input Buffers: -4.5V
3	SDIP	Serial Data Input: 155Mbps or 622Mbps. Differential ECL Positive.
4	SDIN	Serial Data Input: 155Mbps or 622Mbps. Differential ECL Negative.
5	AVCC	Ground for Input Buffers: 0V
6	FM	Frequency Monitor Output. This pin monitors the input voltage to the VCO. When the PLL is locked, the pin will be ≅ 0V.
7	AVCC	Guard-Ring Positive Supply to Epi: 0V
8	FILG	Loop Filter Ground. This pin connects to an external filter.
9	FILP	Loop Filter Positive. This pin connects to an external filter.
10	FILN	Loop Filter Negative. This pin connects to an external filter.
11	VTTL	TTL Positive Supply: +5.0V
12	AVEE2	Negative Supply for VCO: -4.5V
13	EXCS	External Clock-Select TTL Input. A logical high selects the external clock.
14	EXC	External Clock. Single-ended ECL input.
15, 16	AVCC	Ground for VCO: 0V
17, 19, 38, 39	DVCC	Digital Ground for Mux: 0V
18	CRS	Clock-Rate Select TTL Input. This selects the clock rate to be either 155Mbps or 622Mbps. A logic-low level selects the 622Mbps mode.
20	RST	Resets all digital flip-flops, TTL input. Reset is assert when low.
21, 22, 34, 35, 36	DVEE	Digital Negative Supply: -4.5V
23, 33, 37, 40, 43, 44	N.C.	No Connection
24, 27, 29, 32	OVCC	Output Driver Ground: 0V
25	RDON	Negative Recovered Data Output, differential ECL output: 155Mbps or 622Mbps.
26	RDOP	Positive Recovered Data Output, differential ECL output: 155Mbps or 622Mbps.
28	CRP	Clock-Reference Output Divide-by-4. ECL low-power single-ended: 38Mbps or 155Mbps.
30	RCON	Negative Recovered Clock Output, differential ECL output: 155Mbps or 622Mbps.
31	RCOP	Positive Recovered Clock Output, differential ECL output: 155Mbps or 622Mbps.
41	PHADJ	Phase Adjust. This is an analog adjustment that varies the static phase between the input data and the recovered clock. If not used, this input should be grounded. The range is from -1V to 1V.
42	VR	Phase Reference Voltage: 0V. The PHADJ pin compares to this voltage. Set to ground.

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Detailed Description

The block diagram of Figure 1 shows the MAX3270's architecture. The phase-locked loop (PLL) consists of a phase/frequency detector (PFD), a loop filter amplifier, and a voltage-controlled oscillator (VCO).

Phase Detector

The phase detector produces a voltage proportional to the phase difference of the incoming data and the output of the recovered clock. Because of its feedback nature, the PLL will drive the error voltage to zero, making the phase difference zero and aligning the recovered clock to the incoming data. An external phase-adjustment pin (PHADJ) allows the user to vary phase alignment.

Frequency Detector

A frequency detector is also incorporated into the PLL. Frequency detection aids in the acquisition of the input data; this frequency-aided acquisition is necessary during start-up conditions, since the input data stream and VCO difference frequency may be outside the PLL bandwidth. The input data stream is sampled by quadrature components of the VCO clock, generating a difference frequency. Depending on the rotation of the difference frequency, the PFD will drive the VCO so that the difference frequency is driven to zero. Once frequency acquisition is obtained, the frequency detector will return to a neutral state.

Loop Filter and VCO

The PLL is a second-order transfer function whose bandwidth is set by the loop filter. The VCO is integrated into the PLL and always operates at 622MHz. The center frequency is tightly controlled by laser trimming, limiting frequency drift when lock is lost. 155Mbps or 622Mbps mode is selected by the clock-rate select (CRS) pin. CRS selects the inputs to multiplexer MUX2.

The internal VCO can be bypassed with an external clock applied to the EXC input. The external clock select (EXCS) controls the input selections to multiplexers MUX1 and MUX2.

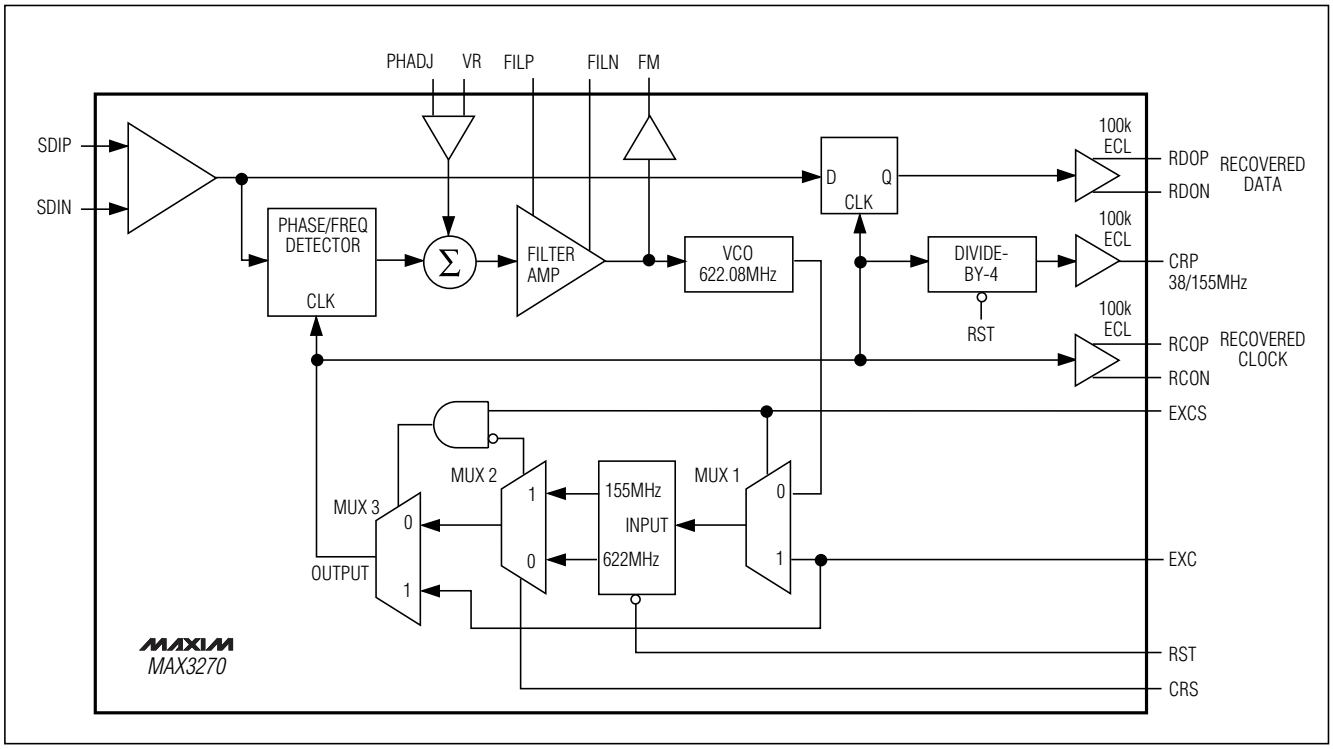


Figure 1. Block Diagram

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Design Procedure

Selecting the Data Rate

The MAX3270 is intended for use in SDH/SONET systems operating at 155.52Mbps or 622.08Mbps data rates. TTL inputs (CRS and EXCS) are provided for selecting the recovered clock rate (Table 1). It is also possible to switch to an externally supplied clock by enabling the EXC input. The EXC input is a high-speed single-ended ECL interface capable of handling serial clock rates of 155MHz and 622MHz.

Table 1. MAX3270 Logic Table

EXCS	CRS	RCOP/RCON	CRP
0	1	155.52Mbps	38.88Mbps
0	0	622.08Mbps	155.52Mbps
1	0	EXC	EXC/4
1	1	EXC/4	EXC/16

Setting the Loop Filter

The loop filter within the PLL consist of a transconductance amplifier and the external filter elements Rf and Cf (Figure 2). The closed-loop bandwidth of a PLL can be approximated by:

$$K_D\ K_O\ Gm\ Rf$$

where K_D is the gain of the phase detector, KO is the gain of the VCO, and Gm is the transconductance of the filter amplifier. Because this filter is an integrator, a zero in the open-loop gain is required for stability. This zero is set by the following equation:

$$w_Z = 1 / (Rf\ Cf)$$

where the recommended external values are Rf = 20Ω and Cf = 2.2µF. To decrease the PLL's closed-loop bandwidth, reduce the value of Rf. Decreasing this bandwidth will improve the MAX3270's jitter transfer performance but reduce jitter tolerance. The MAX3270 has been designed (using the recommended values of Rf and Cf) to meet the Bellcore and CCITT specifications for jitter tolerance of a Network Element. Carefully consider the application if a reduction in loop bandwidth is desired. By reducing Rf an order of magnitude, the PLL's bandwidth becomes more sensitive to the internal tolerances of the IC. As a result, the loop bandwidth may have a wider variation. If Rf is reduced, then Cf should also be increased to maintain loop stability and minimize jitter peaking.

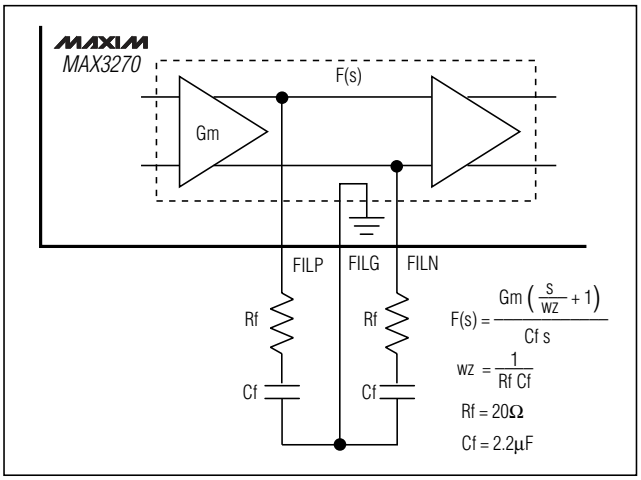


Figure 2. Loop Filter

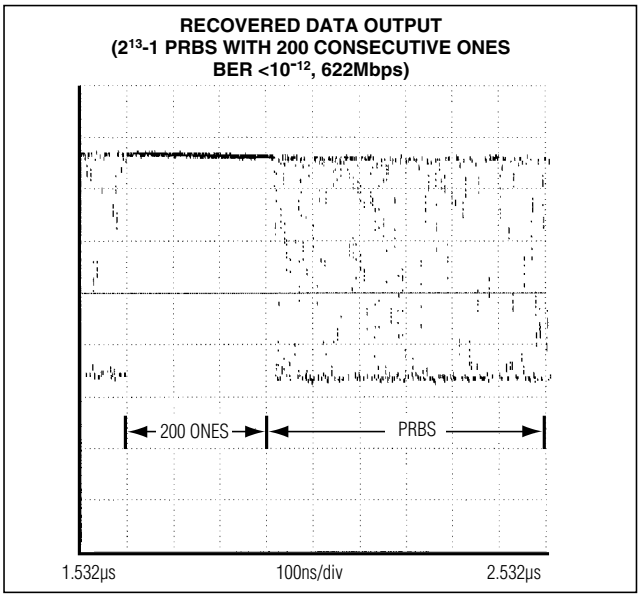


Figure 3. Recovered Data Output

The MAX3270 is optimally designed to acquire lock and to provide a bit-error rate (BER) of less than 10^{-12} for long strings of consecutive zeros or ones. Using the recommended external values for Rf = 20Ω and Cf = 2.2µF, measured results show that the MAX3270 can tolerate more than 200 consecutive ones or zeros. Figure 3 shows a bit stream of 2^{13} - 1 PRBS with 200 consecutive ones.

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Input and Output Termination

The MAX3270 data and clock I/Os (SDIP, SDIN, RDOP, RDON, RCOP, RCON, and EXC) are open emitters, designed to interface with ECL signal levels. It is important to bias these ports appropriately. A circuit that provides a Thevenin equivalent of 50Ω to -2V should be used with fixed-impedance transmission lines for proper termination. Figure 4 shows some typical input and output termination methods.

The serial data input signals (SDIP and SDIN) are the differential inputs to an emitter coupled pair. As a result, the MAX3270 can accept differential input signal levels as low as 250mV. The serial input (SDIP) can also be driven single-ended by externally biasing SDIN to the center of the voltage swing (approximately -1.3V). Make sure that the differential inputs and outputs each see the same termination impedance for balanced operation.

CRP is also an open-emitter ECL output, but it requires a termination resistor of 450Ω to -4.5V. If this output is not used, reduce power by connecting CRP to V_{EE} through a resistor valued at 10kΩ or more.

The MAX3270's performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductances and using fixed-impedance transmission lines on the data and clock signals. Power-supply decoupling should be placed as close to the VEE and VTTL pins as possible. AVEE1, AVEE2 and GVEE should each have their own bypass/decoupling elements, independent of each other and any other -4.5V supply. Make sure to isolate the inputs from the outputs to reduce feedthrough.

Applications Information

Lock Detection

The MAX3270 has an output (FM) that monitors the input voltage to the VCO. FM is an analog output that can be used as a flag to indicate that the PLL is locked. Under normal operation, the loop is locked and the FM output is approximately equal to 0V. When the PLL is unlocked, the VCO will drift. The FM output monitors this drift and will equal approximately ±1V in the limit.

Phase Adjust

In some applications, the optimum alignment point between the recovered clock and the serial data is not at the center of the eye diagram. The MAX3270 has a PHADJ input that can be used in these applications to introduce a phase difference between the recovered clock and the serial data. When no phase difference is desired, this input should be set to 0V. The VR pin is the reference input for PHADJ and is normally tied to GND.

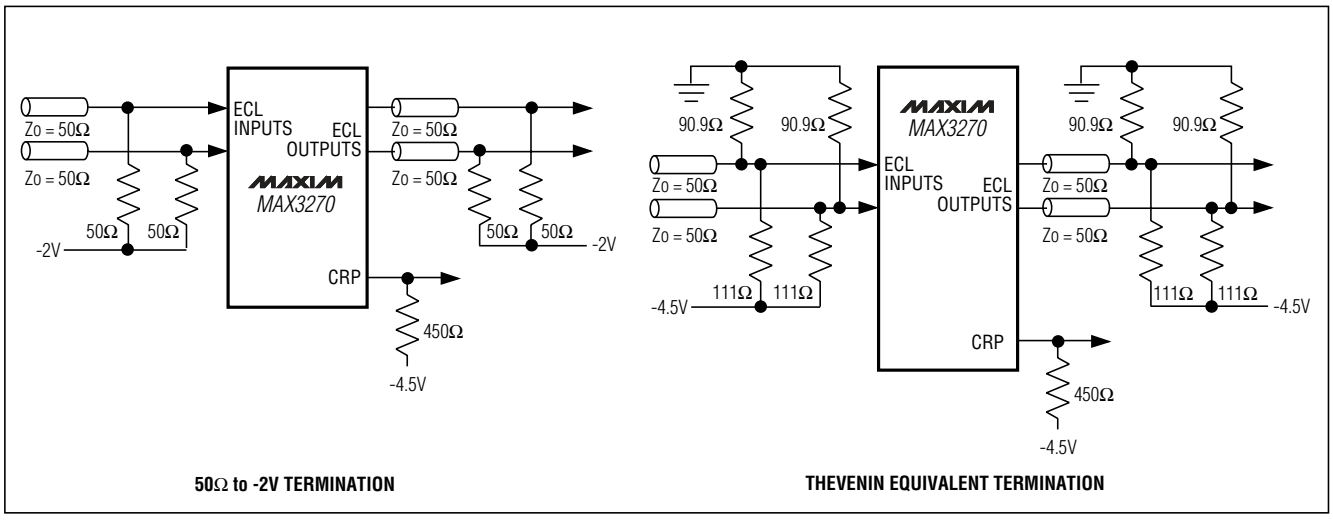
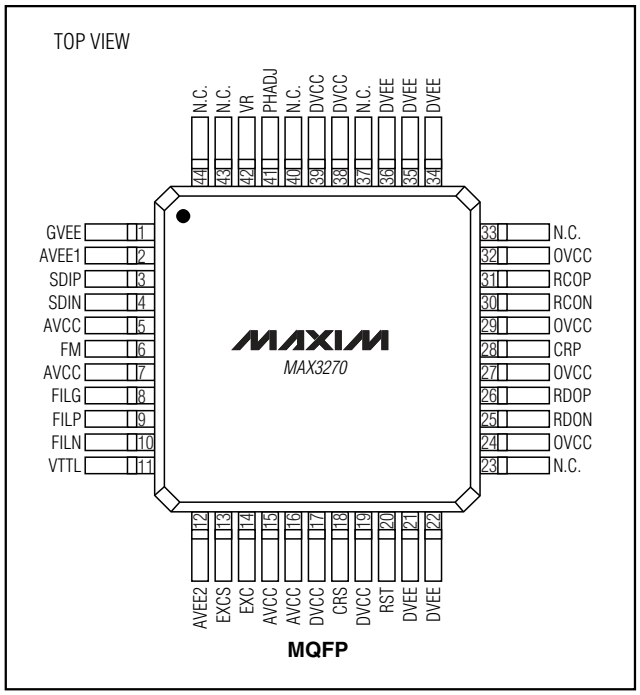


Figure 4. Typical Input and Output Terminations

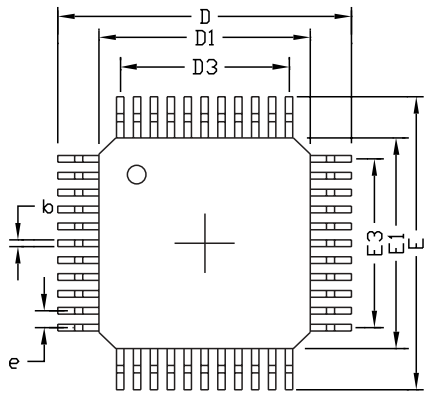
155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

Pin Configuration

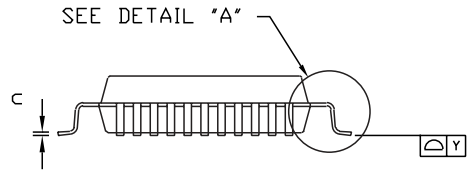


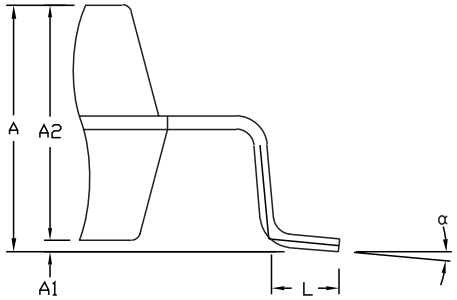
Package Information

MQFP44.EPS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.032	2.388	0.080	0.094
A1	0.102	0.254	0.004	0.010
A2	1.930	2.134	0.076	0.084
b	0.305	0.457	0.012	0.018
c	0.102	0.254	0.004	0.010
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.000 REF		0.315 REF	
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.000 REF		0.315 REF	
e	0.800 REF		0.0315 REF	
L	0.635	0.940	0.025	0.037
α	°0	°10	°0	°10





DETAIL "A"

NOTES:

1. D1&E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-AA-2.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, MQFP, 44L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0826	C	1/1

155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector