PHP73N06T; PHB73N06T

TrenchMOS™ standard level FET

Rev. 02 — 5 July 2002 **Product data**

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP73N06T in SOT78 (TO-220AB)

PHB73N06T in SOT404 (D^2-PAK).

2. Features

- Fast switching
- Very low on-state resistance.

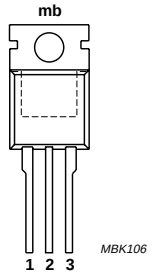
3. Applications

- General purpose switching
- Switched mode power supplies.

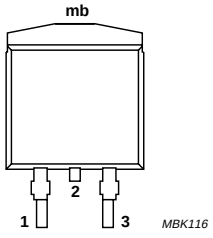
4. Pinning information

Table 1: Pinning - SOT78 and SOT404, simplified outline and symbol

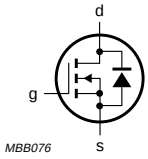
Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base; connected to drain (d)		



SOT78 (TO-220AB)



SOT404 (D^2-PAK)



[1] It is not possible to make connection to pin 2 of the SOT404 package.

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5. Quick reference data

Table 2: Quick reference data

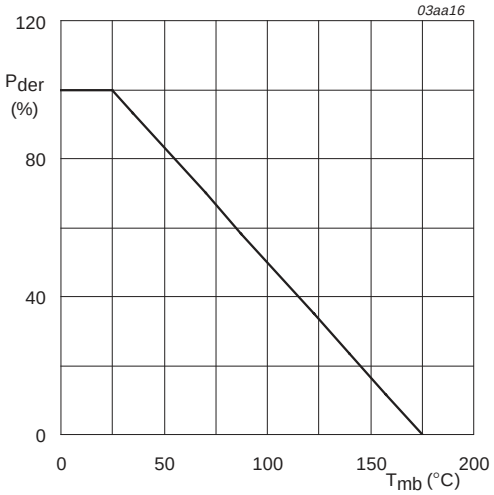
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	60	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V	-	73	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	149	W
T_j	junction temperature		-	175	°C
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 10 V; I_D = 25 A	12	14	mΩ

6. Limiting values

Table 3: Limiting values

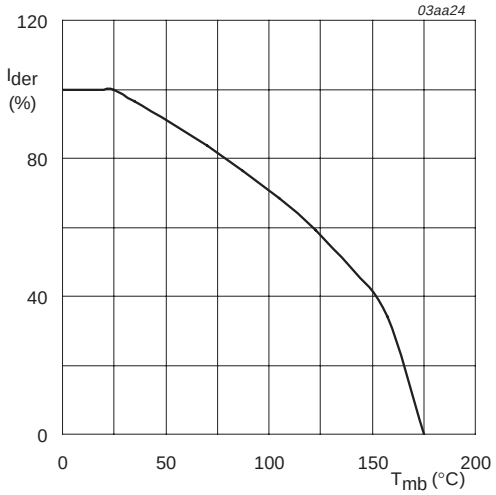
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	60	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	60	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	73	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2 and 3	-	52	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	266	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	166	W
T_{stg}	storage temperature		–55	175	°C
T_j	operating junction temperature		–55	175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	73	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	266	A
Avalanche ruggedness					
E_{AS}	non-repetitive avalanche energy	unclamped inductive load; I_{AS} = 50 A; t_p = 0.1 ms; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 5 V; starting T_j = 25 °C;	-	125	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

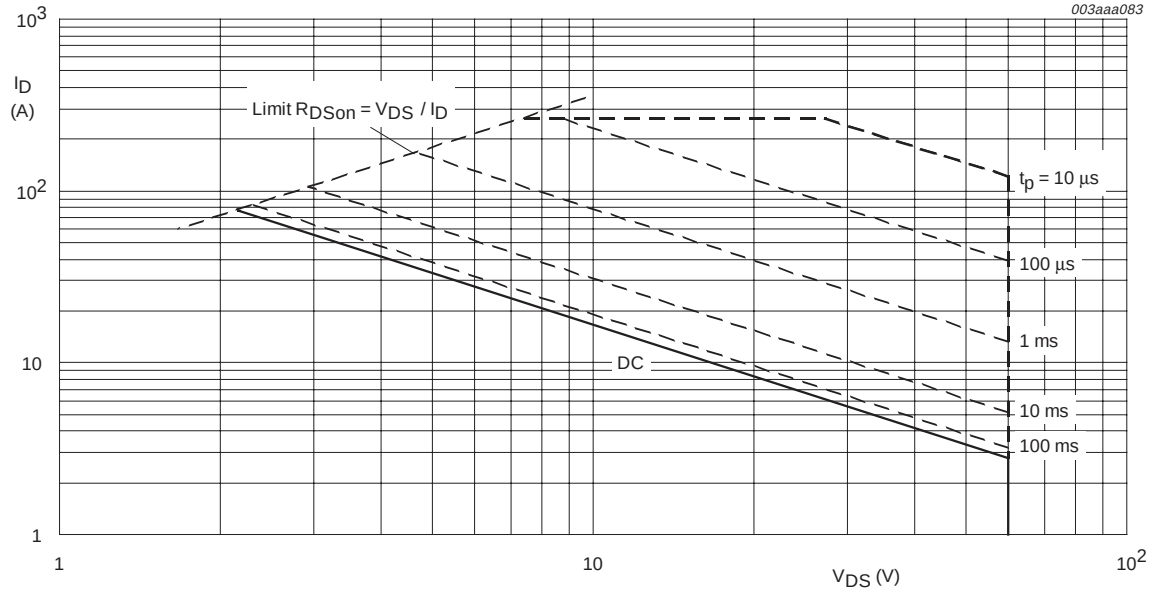
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT404	SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

7.1 Transient thermal impedance

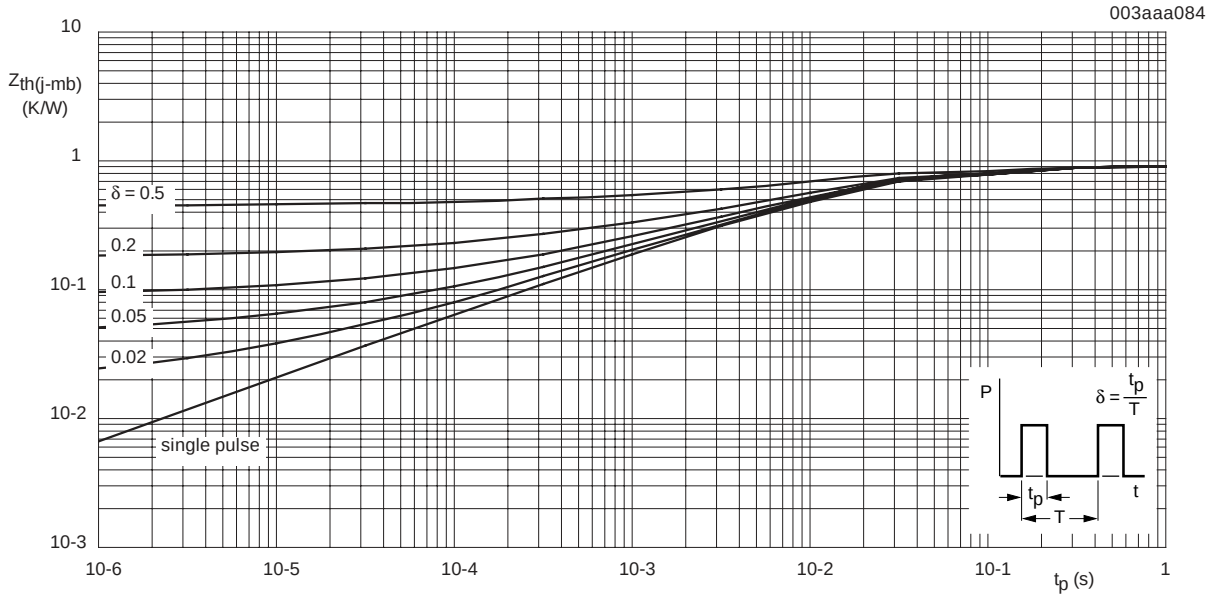


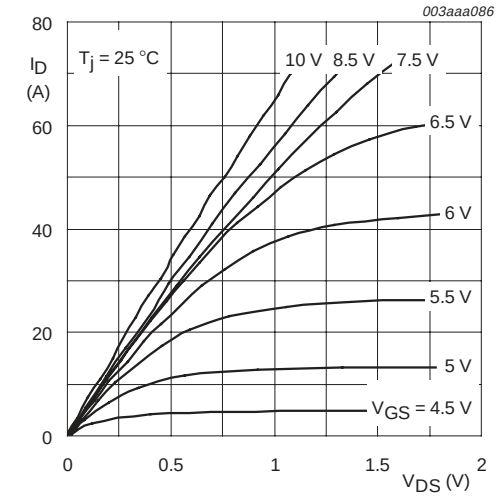
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

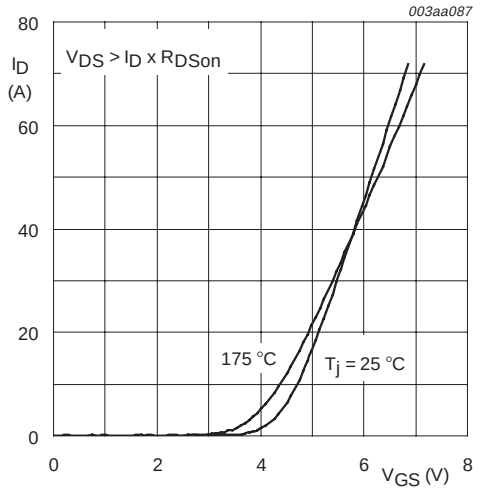
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	-	12	14	mΩ
		T_j = 175 °C	-	-	28	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 50 A; V_{DD} = 44 V; V_{GS} = 10 V; Figure 13	-	54	-	nC
Q_{gs}	gate-source charge		-	10	-	nC
Q_{gd}	gate-drain (Miller) charge		-	19	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	1848	2464	pF
C_{oss}	output capacitance		-	421	506	pF
C_{rss}	reverse transfer capacitance		-	231	317	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_D = 1.2 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	17	26	ns
t_r	rise time		-	79	119	ns
$t_{d(off)}$	turn-off delay time		-	57	80	ns
t_f	fall time		-	51	71	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 12	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 73 A; dI_S/dt = –100 A/µs; V_{GS} = –10 V; V_R = 30 V	-	54	-	ns
Q_r	recovered charge		-	0.12	-	µC



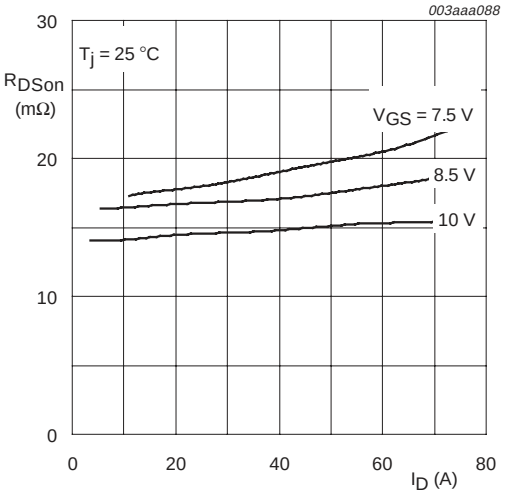
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



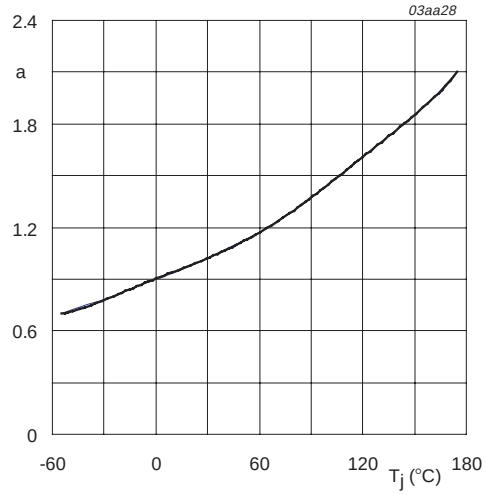
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



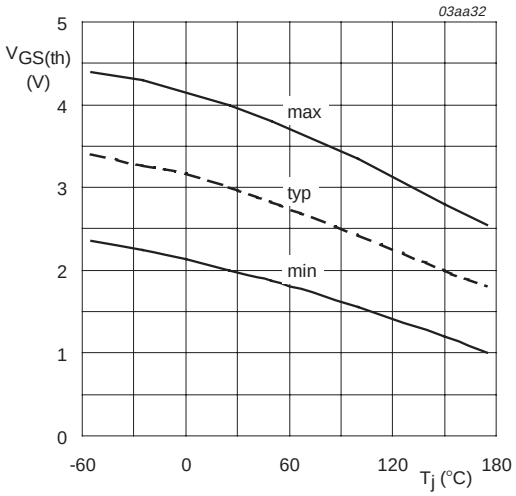
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



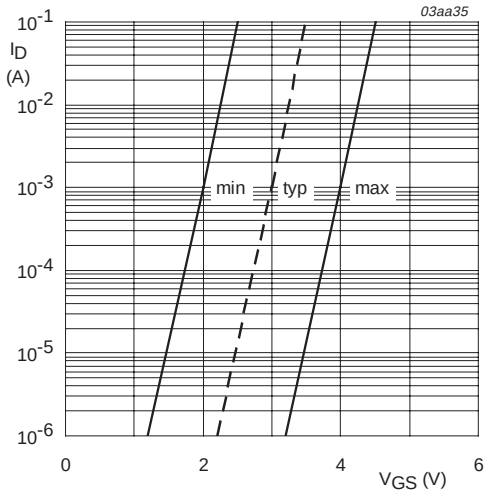
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



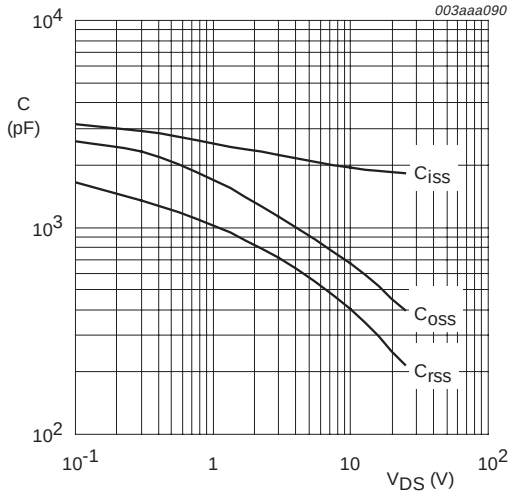
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



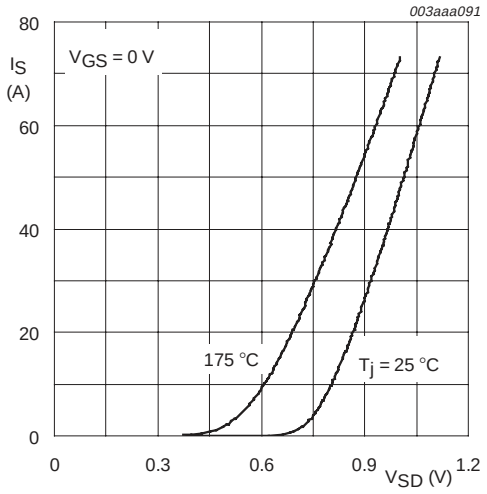
T_j = 25 °C

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



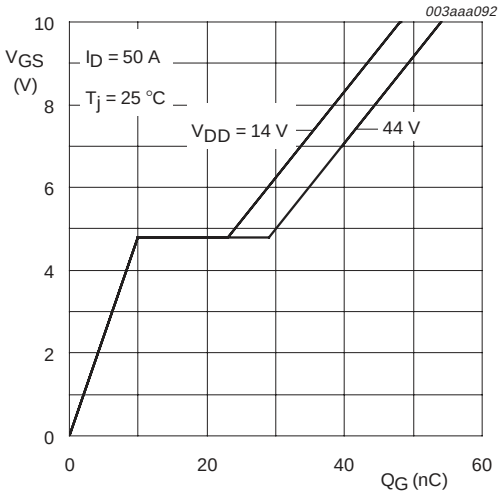
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

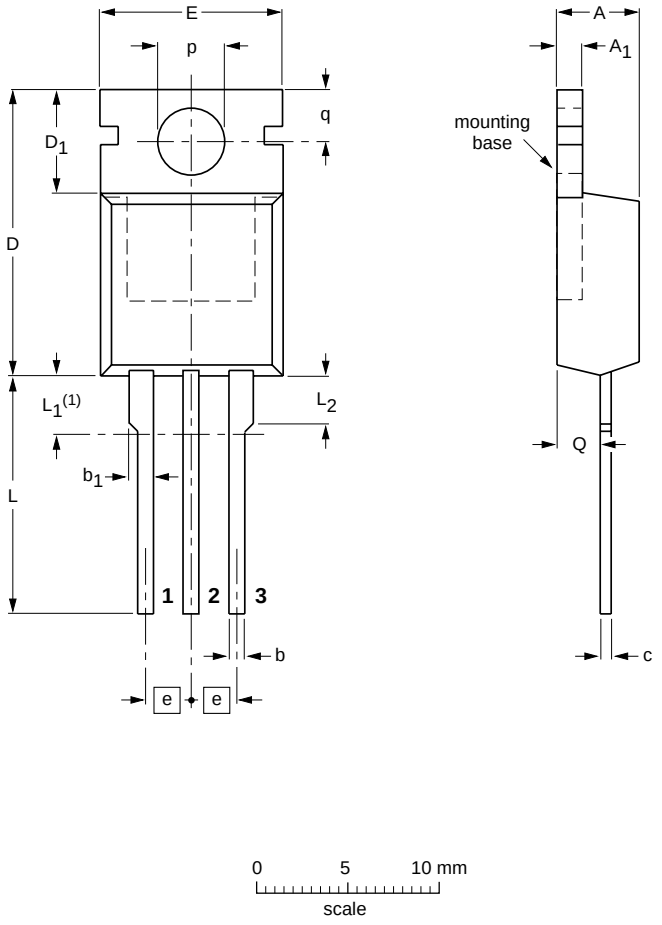


I_D = 50 A; V_{DD} = 14 V and 44 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1(1)	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

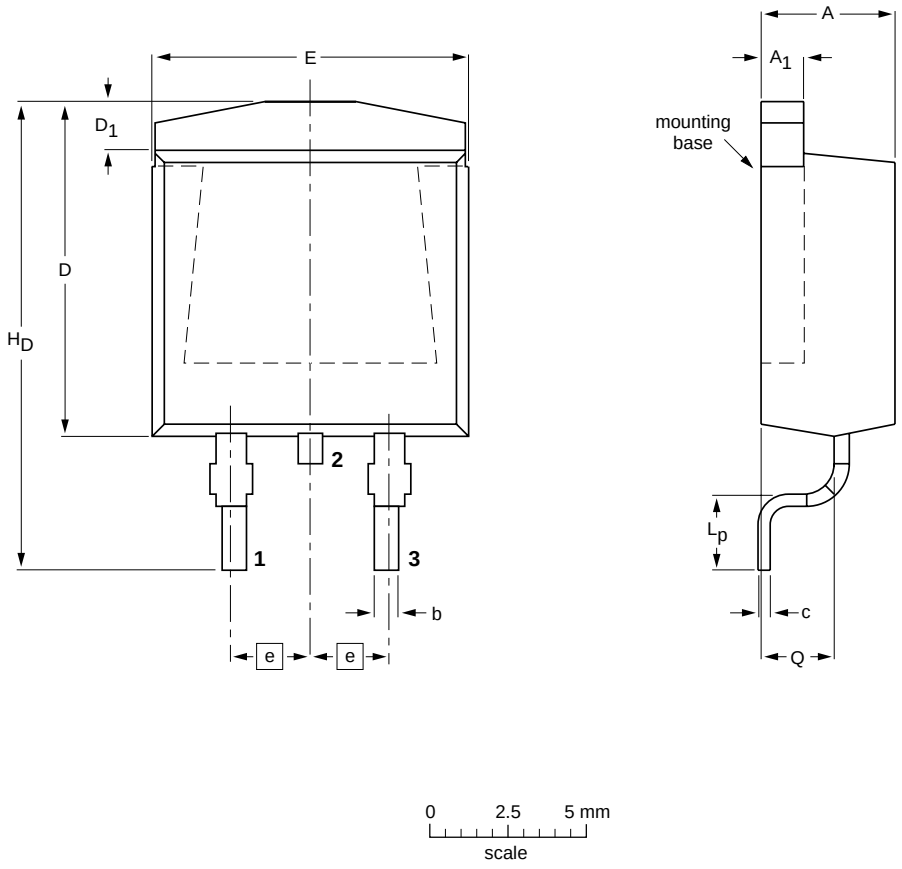
Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			~~00-09-07~~ 01-02-16

Fig 14. SOT78

Plastic single-ended surface mounted package (Philips version of D^2-PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						~~99-06-25~~ 01-02-12

Fig 15. SOT404 (D^2-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20020705	-	**Product data; second version; supersedes initial version 12 March 2001.** Section 5, 6, 8 Increase in V_{DS} Section 6 “Limiting values” Non-repetitive avalanche ruggedness derating graph removed Section 8 “Characteristics” Forward transconductance graph removed Section 7 “Thermal characteristics” Clarification of thermal resistance table Graphs updated to latest standard.
01	20010312	-	**Product specification. Initial version.**

11. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**. **Fax: +31 40 27 24825**

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