

# PCap04

# **Standard Board**

PCAP04-EVA-KIT

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### **Content Guide**

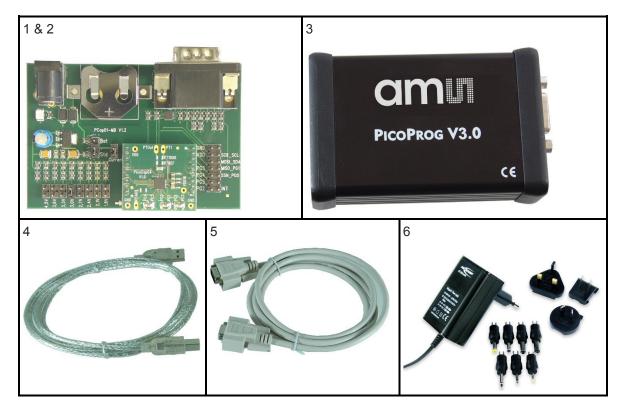
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#### 1 Introduction

The PCAP04-EVA-KIT evaluation system provides a complete system for generally evaluating the PCapØ4 IC. It is supplied with a main board, a plug-in board, a Windows based evaluation software, assembler software and the PICOPROG V3.0 programming device. The PCapØ4 evaluation board is connected to the PC's USB interface through the PICOPROG V3.0 programming device. The previous generation PICOPROG V2.0 programming device may also be used with the PCAP04-EVA-KIT.

#### Figure 1: Kit Content



Pos.	Item	Comment
1	PCapØ1-MB	Motherboard
2	PCapØ4-EVA-BOARD	Plug-in board based on PCapØ4 in QFN24 package
3	PICOPROG V3.0	Programmer and interface box
4	USB cable	Connects PICOPROG V3.0 to PC
5	High density DSUB15 cable	Connecting Evaluation board to programmer (optionally)
6	Wall power supply unit	9 V

The evaluation kit offers user-friendly operation of the PCapØ4 single-chip solution for capacitance measurement. This kit can be used to evaluate the capacitance measurement, temperature measurement and the pulse generation capabilities of the PCapØ4 chip. The kit also includes a CD-

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ROM containing software and data sheets. However, it is strongly recommended to use the latest data sheets and GUI software or get them on request.

### 2 Quick Start Guide

In this section, we described how to set up quickly the PCAP04-EVA-KIT and establish basic operation and make measurements.

### 2.1 Install the Software

It is crucial to install the software before connecting the evaluation kit to your computer. A default driver loading of your OS may interfere with correct installation.

- Download the latest zipped software installation package to the desired directory.
- Unzip the package to the desired directory.
- Open "setup.exe" from the unzipped directory.
- Follow the instructions on the screen.

#### 2.2 Install the Hardware:

- Install the software before proceeding with this step!
- Connect your computer with the PICOPROG V3.0 using USB cable.
- Connect PICOPROG V3.0 and the evaluation kit motherboard using the DB15 interfaces
- Mount the plug-in board on the corresponding socket on the motherboard.
- Set the power supply unit to 7.5 V output.
- Connect the motherboard to power via the power supply unit.
   The green LED on the EVA kit motherboard should be on.





### 2.3 Quick Start for Initial Measurements

From the "Start" menu, go to "All Programs" and then to the "acam" directory. Double click the "PCap04 Frontpanel" icon to begin execution of the evaluation kit software. The following screen should appear:

#### Figure 3: Setup page

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# 0 1 2 3 4 5 6	FR1 FR2 FR3 FR4	0	none 💉 S		1	0	AO	0			100	1.2

Click the "Verify Interface" Button to confirm communication with PICOPROG V3.0 is working:

#### Figure 4: Verify Message



The PCap04 plug-in board is pre-assembled with ceramic capacitors to emulate capacitive sensors. These capacitors, each 10 pF in value, are connected to the 6 ports PC0 to PC5.

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To begin measurements using these preinstalled components, it is necessary to make the following adjustments on the "CDC Frontend" tab:

- 1. "Capacitive Measurement Scheme" section should be set to "Floating | Single".
- 2. All the capacitance ports should be turned on using the Cap. Port. Select buttons
- 3. The Stray Compensation setting should be set to "Both".

The resulting settings under the CDC tab should look like this:

#### Figure 5: CDC Frontend page at the start

ile	Mem	on T	ools Ir	terface	Help										
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To begin measurements, on the right side of the window, click the following buttons in the order listed:

- 1. "Power On Reset"
- 2. "Write Complete"
- 3. "Start Measurement"

Measurements should now be running and your screen should resemble the following:

#### Figure 6: CDC Frontend page in use

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															Open Gra	ob
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D 1 2 3 4	Name C0/Cre C1/Cre C2/Cre C3/Cre	en al ef ef ef ef ef	Res 080 385 124 127 000	ults 0005E DFFCC 24D70 AD60A	Filter none none none			-27 -27 -27 -27 -27 -27	10p 10p 10p 10p	0 0 0 0	40 40 40 40	10p 10p 10p 10p	10p 74,209p 22,8237p 23,0998p	Mean (50 10p 74,204p 22,8228p 23,0987p	ombined E Std Dev 0 7,172f 3,324f 3,384f	SNR [b Inf 10,45 11,55
201	Name C0/Cre C1/Cre C2/Cre C3/Cre C4/Cre	rnal ef ef ef ef	Res 080 385 124 127 000 000	ults 0005E DFFCC 24D70 AD60A 00000	Filter none none none none			-27 -27 -27 -27 -27 -27 -27 -27	10p 10p 10p 10p 10p	0 0 0 0 0	40 40 40 40	10p 10p 10p 10p 10p	10p 74,209p 22,8237p 23,0998p 0	Mean ∰50 10p 74,204p 22,8228p 23,0987p 0	ombined E Std Dev 0 7,172f 3,324f 3,384f 0	SNR (b Inf 10,45 11,55 11,53 Inf

The C1 and C2 values should be continually updating but remain within a reasonably small standard deviation as shown.

At this point if the above steps have been successfully completed basic operation of the EVA kit should be achieved. The following sections provide a detailed description of the hardware and software for advanced operation.

### 3 Hardware Description

### 3.1 Connecting Capacitors and Resistors

This evaluation kit can be used for evaluating capacitance measurement by connecting capacitive sensors. Further, it can be used for evaluating temperature measurement by connecting external temperature sensitive resistors or for generating quasi analog voltage (pulse width/density modulated) that is dependent on the sensor connected to the system.

Depending on the purpose of evaluation, a modification has to be made to the same plug-in board. Following is a picture of the Mother board with the plug-in board.

# 

Figure 7: The evaluation kit's motherboard and plug-in board

The following sections describe the modifications for each application in detail.

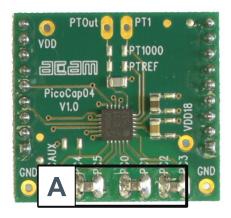
### 3.2 Hardware Architecture

#### 3.2.1 PCAP04 BOARD

For the purpose of evaluating the capacitance measurement using PCapØ4, the plug-in board is pre-assembled with ceramic capacitors to emulate capacitive sensors. These capacitors, each 10 pF in value, are connected to the 6 ports PC0 to PC5. They are connected as single sensors in floating mode, i.e. each capacitor is connected between 2 ports, and hence there are 3 x 10 pF on-board capacitors. Please refer to section 3 of the PCapØ4 data sheet for more information on how to connect capacitors to the chip. In case using external reference, the capacitor connected between ports PC0 and PC1 is taken as the reference capacitor.



#### Figure 8: Details of the plug-in board (A=three C0G ceramic capacitors)



In the process of evaluation, when you are comfortable with interpreting the measurement results from the chip, these fixed capacitors can be replaced with the actual capacitive sensors of your application.

If you want to connect your capacitive sensors in grounded mode, then GND points are provided at the two ends of the board, where the sensor ground connections ought to be soldered.

The typical value of the capacitive sensors that can be connected to the evaluation kit lies in the range of 30 pF to 3.5 nF. The reference capacitor should be in the same order of magnitude as the sensor. Depending on the value of the sensor, the value of the internal resistor for performing the measurement has to be selected. For the pre-assembled 10 pF capacitors, an internal discharge resistor of 90 k $\Omega$  works well. See section 3 of the PCapØ4 data sheet on how to select the value of the internal discharge resistor.

#### 3.2.2 Temperature Measurement

Temperature measurement or other resistive tasks may also be of interest for the user of this kit. The evaluation kit offers this possibility through the RDC (resistive-to-digital converter) ports. An onchip thermistor coupled with an on-chip temperature-stable reference resistor made of polysilicon is sufficient for observing the temperature measurement capability of the PCapØ4 chip.

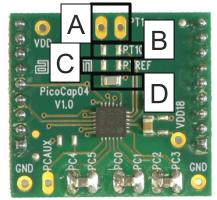


Figure 9 Temperature sensor connection pads

Pos.	Item	Comment
A	Port PT1 for second external temperature sensor	not supported by the standard firmware
В	Port PT0 for external temperature sensor	
С	Port PT2 for external reference resistor	
D	10 nF COG	

However, there is a possibility to connect the reference resistor and the thermistor externally to the chip, too. In case of external resistors, the temperature-stable reference resistor ought to be connected at port PT2REF on the plug-in board. The board allows you to connect the external thermistor, e.g. a PT1000 sensor at port PT0 (or PT1, not supported yet by the standard firmware). In any case, for the temperature measurement, an external capacitor 10 nF C0G has to be connected to the chip; it is already pre-assembled on board.

### 3.2.3 Pulse Code Generation

Any of the capacitance or temperature measurement results from the PCapØ4 chip can be given out as a pulse width modulated or pulse density modulated signal. This output can be filtered to generate an analog output signal that can be used for further controlling.

These pulse width or pulse density codes can be generated at Ports PG0, PG1, PG2 or PG3 (in block A). Since ports PG0 and PG1 are used for the SPI Interface in the board, the hardware allows to get a valid pulse width/density modulated signal on PG2 or PG3. However, when I2C communication mode is used the pulsed signals can be optionally obtained on the ports PG0 and PG1.

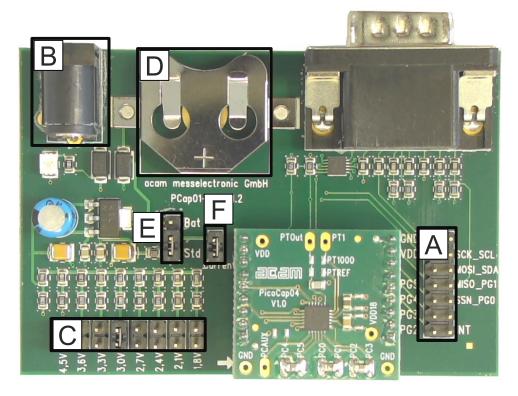


Figure 10 General purpose interface ports PG0 to PG3 in block A

### 3.2.4 Motherboard

The motherboard connects to the PICOPROG V3.0 programmer. It serves the various power options. It can be powered via wall plug supply (B), the voltage being set from 1.8 V to 4.5 V by jumpers (C). Further, it supports a battery power option (D). The power options are switchable via jumper (E). Power present is indicated by a green LED.

There is a jumper 'Current' on the mother board (F). The current consumption of the PCapØ4 chip during operation can be directly measured from these jumper terminals.

All interface signals and general purpose I/O signals can be monitored by means of a separate jumper in block A.

### 4 Software Description

#### 4.1 Initialization

Configuration files, Firmware, Settings and calibration data are subsumed in a project (.prj) file. When opening a project file then automatically the configuration and firmware data will be transferred to the chip and the chip is initialized.

Step 1: The first to do after starting the evaluation software is to read the device version from Chip by pressing the button or to select the supported PICOCAP device on the setup page. In the initial phase start with our standard firmware that calculates the capacitance ratios and resistance ratios. It automatically recognizes the operation mode and takes care of the set number of capacitors and the kind of connection. But it does no further processing.

Step 2: If you want to change from the default SPI to I2C interface, please select under Interface --> Bus --> I2C. The LED on the PICOPROG V3.0 programmer should now turn red. When the LED does not glow at all, then it indicates that the interface is faulty.

Step 3: By pressing the 'Standard'-button, the standard project file will be open.

You also may load your own project file.

Step 4: Open Graph window and press 'Start Measurement'.

#### 4.2 Graphical User Interface

Next, the main front panel comes up. Overall, the graphical user interface offers various windows for on-line configuration, for parameter and calibration data setting, and of course for the graphical and numerical display of the measurement data. The various windows will be explained in this chapter.

### 4.2.1 Front Panel

Open Graph	Open a window for graphic representation of measurement data
Start Measurement	Start or stop a running measurement
Write Config.	Transfer once more, the present settings in the evaluation software to the chip (in case of doubt)
Write Complete	Transfer the complete firmware, calibration data and configuration to the chip
Power On Reset	After Power up reset, 'Write Config.' may be necessary.
Init Reset	With an init reset, the chip is re-initialized with respect to its frontend and processor.

This is the main window. On the right side, the front panel shows six general buttons:

# 4.2.1.1 Setup Page

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		Configuratio			n Evalua		_			Sta	a <mark>rt Measur</mark>	ement
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	83	citance ratios		ty in rh% a		1	22		at RESO		ower On R	eset
	- Pure resis - Considers compensati		- C Sense - Floati - Interna sensor a - PDM PU - PDM PU	ature in °C : PCO & PCJ ng single al referen I temperat nd referen LSEO rh% LSE1 temp rate: 5 Hz	: ce ure ce	- C S - Fi - Int - Int sen: - PD - PD	ense loati itern erna sor a M PL M PL	e: PCO 8 ng sing al refe I temp nd refe ILSEO p	gle rence erature erence ressure in % emperature			nbit 🥥
	Name	Results	Filter	ify Interfa	ce Factor	Offset		Span	Final Result	PI	ombined E	_
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11		3B5DEA4B	none 💌	5 -27	10p	0	AO		74,2086p	74,2064p	100	10,54
ni K	C0/Cref		10.00	5 -27	10p	0	AO		22,82p	22,8232p	C. C	11,43
		12418816	none 💌	1218-3-47		100	10000	0.015		1000	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 220 X 1 2 2 4 1
	C1/Cref		none 💌	Manager V	10p	0	AO	10p	23,0963p	23,0993p	3,582f	11,45
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	C1/Cref C2/Cref C3/Cref C4/Cref	12418816 127A20FD 00000000	none 💌	5 <b>-</b> 27 5 <b>-</b> 27	10p	0	AO	10p 10p	0	0	0	Inf

Figure 11 Setup page

Options on 'Setup' page:

Select Device	Select the PICOCAP device which you use. <pcap04v0> means silicon version "Z" <pcap04v1> means release silicon version "v1"</pcap04v1></pcap04v0>
Read Device Version from Chip	Reads the device version from chip
Standard	Opens the <i><selected device="">_</selected></i> standard.prj project file with configuration and standard firmware.
Humidity	Opens the <i><selected device="">_</selected></i> humidity.prj project file with configuration and linearization firmware.
Pressure	Opens the <i><selected device="">_</selected></i> pressure.prj project file with configuration and linearization firmware.

When everything is in order, then pressing this button will indicate the release version number of the software and of the PICOPROG V3.0 Firmware. It also
confirms with 'Memory read/write: OK' if a supported PICOCAP device is present.

The lower part of the window is used for real-time numerical display of the measurement results. In principal it shows the content of the read registers. The content itself depends on the firmware. Figure 1-16 shows the content as it is given with the standard firmware. The first six rows show the capacitance ratios, the last two rows show the temperature result (resistance ratio or linearized temperature).

The tab has 12 columns of information, defining labels, data format, resolution specification (white background) and results (grey background). The information in the white fields increase convenience of reading and is stored in the project files (\*.prj). All number may get a character to indicate the well-known prefixes for denoting the factor in thousands ('p', 'f', 'a', 'k'... ).

Name	Label for the register content, depends on the firmware.
Results	Raw hex data display of the result register content. The column before shows the width. The button column after shows whether the result is signed or unsigned.
Filter	Selection of various software filters like Sinc (rolling average) and Median (non-linear filter).
fpp	This column shows the size of the fractional part of the fixed point number and the necessary shift. Depends on the firmware.
Factor	The factor is a scaling factor that allows to scale the result according to the reference capacitor. Factor = '1' gives back the initial capacitance ratio in column 'Final Result'.
Offset	Offset to be added or subtracted in the evaluation software.
Auto Offset	By pressing [AO], the software re-calculates the 'Offset', setting back the 'Final Result' to 0
Span	Number that defines the maximum span of the sensor. Is relevant only for the calculation of the resolution in column SNR [bit].
Final Result	Display of the final result, scaled by 'Factor' and the 'Offset' added.
Mean	Display of the mean value. The sample size can be selected.
Std.Dev	Standard deviation of the 'Final Result'.
SNR [bit]	Signal-to-Noise ratio in bit, calculated as 'Span'/ 'Std.Dev.'

# 4.2.1.2 CDC Frontend Page

-	ams PCap(													
Fil	e Memor	y Tools I	nterface	e Help										
S	etup CD	C Frontend	CDC	RDC	PDM	I/PWM	DSP/G	SPIO	Misc	Exp	ert	0	m	
		Capacitan	ce to D	Digital C	onve	ersion F	ronten	nd				<b>M</b>		
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	1	nce Measurer			Cap. F	Port Sele	ect	S	tray (	Compe	nsation		open erej	SH1
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-	external		9	pF	p.	for	Factor	Offcet		Snan	Final Pecult	PI	mbined Er	
2.03	external Name	Result	9 ts F	pF		fpp	Factor	Offset	200	Span 100	Final Result	PI Mean ∯50	mbined Er	TTOT
0	external Name C0/Cref	Result 08000	9 ts F 005E n	Filter	5	<b>1</b> € -27	10p	0		10p	10p	<b>PI</b> Mean ∯50 10p	mbined Er	SNR (b)
)	Name C0/Cref C1/Cref	Result	9 ts F 005E n FCC n	pF	3	-27 -27	10p 10p	1000000000	AC	10p 10p	10p 74,209p	PI Mean∯50 10p 74,204p	mbined Er Std Dev 0 7,172f	SNR (b 10,45
) 1 2	Name C0/Cref C1/Cref C2/Cref	Result 08000 3B5DF	9 ts F 905E n FCC n HD70 n	Filter		<ul> <li>27</li> <li>27</li> <li>27</li> <li>27</li> <li>27</li> <li>27</li> </ul>	10p 10p 10p	0	40 40	10p 10p 10p	10p 74,209p 22,8237p	Mean ∯50 10p 74,204p 22,8228p	Std Dev           0           7,172f           3,324f	SNR (b Inf 10,45 11,55
D 1 2 3	Name C0/Cref C1/Cref	Result 08000 385DF 12424	9 1055 n FCC n D70 n 060A n	Filter		-27 -27 -27 -27 -27	10p 10p	0	40 40	10p 10p	10p 74,209p	PI Mean∯50 10p 74,204p	mbined Er Std Dev 0 7,172f	SNR (b Inf 10,45 11,55
D 1 2 3	external Name C0/Cref C1/Cref C2/Cref C3/Cref	Result 08000 385DF 12424 127AD	9 155 F 1055 n 1070 n 1060A n 1060A n	Filter	<b>3</b> <b>3</b> <b>3</b> <b>5</b> <b>5</b> <b>5</b> <b>5</b> <b>5</b>	-27 -27 -27 -27 -27 -27 -27	10p 10p 10p 10p	0 0 0 0	40 40	10p 10p 10p 10p 10p	10p 74,209p 22,8237p 23,0998p	Mean ∯50 10p 74,204p 22,8228p 23,0987p	0 7,172f 3,324f 3,384f	Tror SNR [b] Inf 10,45 11,55 11,53
# 0 1 2 3 4 5 6	Name C0/Cref C1/Cref C2/Cref C3/Cref C3/Cref C4/Cref	Result 08000 385DF 12424 127AD 00000	9 2055 n FCC n 2060A n 2060A n 2000 n	Filter tone   tone   tone	<b>3</b> <b>3</b> <b>3</b> <b>5</b> <b>5</b> <b>5</b> <b>5</b> <b>5</b>	-27 -27 -27 -27 -27 -27 -27 -27 -27	10p 10p 10p 10p 10p	0 0 0 0 0	40 40 40	10p 10p 10p 10p 10p	10p 74,209p 22,8237p 23,0998p 0	Mean ∯50 10p 74,204p 22,8228p 23,0987p 0	Std Dev           0           7,172f           3,324f           3,384f           0	Tror SNR [b] Inf 10,45 11,55 11,53 Inf

Figure 12 CDC Frontend page



Options on 'CDC Frontend page:

Capacitance Measurement Scheme	<b>Grounded   Single</b> – Single capacitive sensor connected between a port and ground.
	<b>Grounded   Differential</b> – Differential capacitive sensor connected between 2 ports with the middle tap of the sensor connected to ground.
	Floating   Single – Single capacitive sensor connected between 2 ports.
	<b>Floating   Differential</b> – Differential capacitive sensor connected between 2 ports with the middle tap of the sensor connected to another 2 ports.
Cap. Port Select	Select which capacitive ports have to be measured (Ports 0-5), i.e. at which ports the sensors have been connected in hardware.
Stray Compensation	None – No compensation
	<b>Internal</b> – One additional measurement performed through only the chip- internal stray capacitance with respect to ground.
	<b>External</b> – One additional measurement per port pair, performed through a parallel connection of the capacitance at the two ports with respect to ground.
	Both – Both internal and external compensation together.
Discharge Resistance Port 03	Selects the value of the internal resistance (180k, 90k, 30k, 10k) for measurements on port PC0 to PC3 through which the discharge cycles during measurement are to be performed. This value has to be selected in accordance with the capacitance value of the sensor.
Discharge Resistance Port 45	Selects the value of the internal resistance (180k, 90k, 30k, 10k) for measurements on port PC4 to PC5 through which the discharge cycles during measurement are to be performed. This value has to be selected in accordance with the capacitance value of the sensor.
Charge Resistance	Choice of one out of 4 on-chip charging resistors (180k, 10k) for the CDC. Permitting to limit the charging current and avoiding transients.
C Reference Select	Switching between external and internal reference capacitance.
Internal Cap	Selection of internal reference capacitance value. (031pF)

# 4.2.1.3 CDC Page

	emory Tools	Interfa	ce Help										
Setup	CDC Frontend	CDC	RDC	PDM/F	WM	DSP/G	PIO	Misc	Exp	ert		m	
	Capacita	nce to	Digital C	onver	sion Se	etting	6			10	V		
Cycle (	Control											Open Gra	ala
P	recharge Time		Fullcharge	Time		Disch	arge Tim	e			6	opendia	ph .
	0 🚖 <sub>s</sub> x 3	BFF	20u	🚖 s 🗴	0		20u 🌲	s × C			Sta	nt Measure	ement
	4	-	4									Write Con	fin
Vdd	- 221		-					11000		C_FAKE			
										0		Vrite Comp	lete
						1				C_AVRG	P	ower On R	eset
			10	ycle						(Sample Size)		Init Rese	et 📄
	7						1		1000	32	28		
0V L							Ti	me					
Сус	le Clock Select												
50	,0kHz   Low Pow	er	-				Conve	rsion	Durat	ion 6,40ms			
											14		
100000000000000000000000000000000000000													
Conver	sion Control												
				ext. Tri	eger-Pi	n					ñ I		
Ca	p. Tr <mark>igger</mark> Select			ext. Tri		- I	Co	nvers	sion Ti	me 80,0ms		Pur	nhit 🦱
Ca			• 2	ext. Tri DSP_II		-	Co	nver	sion Ti	me 80,0ms			nbit 🥘
Ca Ti	p. Trigger Select mer Triggered nversion Time		• 2			- I					Cc	Rur ombined E	
Ca Ti Co	p. Trigger Select mer Triggered		2			- I				me 80,0ms ate 12,5Hz		ombined E	rror 🖲
Ca Ti Co	p. Trigger Select mer Triggered nversion Time		• 2			- I							rror 🖲
Ca Ti Co 20	p. Trigger Select mer Triggered nversion Time 100				10 💌	0	N		uring R	ate 12,5Hz	PI	ombined E	
Ca Ti Co 20	p. Trigger Select mer Triggered nversion Time 200 😭	Jİts	Filter	DSP_II	fpp	Factor	N Offset	leasu	uring R	ate 12,5Hz Final Result	PI Mean # 50	ombined E	TROF
Ca Ti Co 20 # Nam 0 C0/C	p. Trigger Select mer Triggered nversion Time 200 💭 e Resu ref 0806		Filter	DSP_II	10 ×	0 Factor 10p	N	least AO	Span	Final Result 10p	Mean \$50	ombined E	SNR (bi
Ca Ti Co 20 # Nam 0 C0/C 1 C1/C	p. Trigger Select mer Triggered nversion Time 200 💭 e Resu ref 0800 ref 3850	JITS 3005E	Filter	DSP_II	10 ×	Factor 10p 10p	N Offset 0	A0	Span 10p 10p	Final Result 10p 74,2086p	Mean # 50 10p 74,2064p	ombined E CO( Std Dev 0 6,71f	SNR [bi 10,54
Ca Ti Co 20 # Nam 0 CO/C 1 C1/C	p. Trigger Select mer Triggered nversion Time 200 💭 e Resu ref 0800 ref 3850 ref 1243	JIts 3005E DEA4B	Filter none none	DSP_II	fpp -27 -27 -27	0 Factor 10p	N Offset 0 0	40 40	Span	Final Result 10p 74,2086p 22,82p	Mean #50 10p 74,2064p 22,8232p	ombined E Std Dev 0 6,71f 3,616f	SNR (bi Inf 10,54 11,43
Ca Ti Co 20 # Nam 0 C0/C 1 C1/C 2 C2/C	p. Trigger Select mer Triggered nversion Time 200 💭 ee Resur- ref 0800 ref 3851 ref 1241 ref 127/	ults 3005E DEA4B 18816	Filter none none	DSP_II	fpp   -27 : -27 : -27 : -27 :	Factor 10p 10p	N Offset 0 0 0	40 40 40	Span 10p 10p	Final Result 10p 74,2086p	Mean # 50 10p 74,2064p	ombined E CO( Std Dev 0 6,71f	SNR (bi Inf 10,54
Ca Ti Co 20 # Nam 0 C0/C 1 C1/C 2 C2/C 3 C3/C	p. Trigger Select mer Triggered nversion Time 100 e Resur- ref 0800 ref 3851 ref 1241 ref 1277 ref 0000	JIts 0005E DEA4B 18816 A20FD	Filter none none none none	DSP_II	<pre>fpp fpp fpp fpp fpp for fpp for fpp for for fpp for for for for for for for for for for</pre>	Factor 10p 10p 10p	V Offset 0 0 0 0	40 40 40 40	Span 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p	Mean (50) 10p 74,2064p 22,8232p 23,0993p	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Tror CAF SNR (b) Inf 10,54 11,43 11,45
Ca Ti Co 20 # Nam 0 CO/C 1 C1/C 2 C2/C 3 C3/C 4 C4/C	p. Trigger Select mer Triggered nversion Time 100 e Resur- ref 0800 ref 3851 ref 1241 ref 1277 ref 0000 ref 0000	JIts 2005E DEA4B 18816 A20FD 20000	Filter none none none none	DSP_IT	fpp -27 -27 -27 -27 -27 -27 -27 -27	0 Factor 10p 10p 10p 10p	V Offset 0 0 0 0 0	40 40 40	Span 10p 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p 0	Mean ∯[50 10p 74,2064p 22,8232p 23,0993p 0	0 5td Dev 0 6,71f 3,616f 3,582f 0	SNR (bi Inf 10,54 11,43 11,45 Inf

#### Figure 13 CDC page

Options on 'CDC page:

#### Cycle Control

Precharge Time	Time to charge via resistor for current limitation, can be set in multiples of the cycle clock
Fullcharge Time	Time for final charge without current limitation, can be set in multiples of the cycle clock
Discharge Time	Time to discharge the capacitor, can be set in multiples of the cycle clock
C_FAKE	Number of fake measurements per measurement cycle. Performing fake measurements may help in reducing noise.



C_AVRG	Enables averaging the measurement results over multiple measurement cycles. Setting to $1 \rightarrow No$ averaging, Setting to any number N, will result in averaging over N measurement cycles for generating one measurement result. (08191)
Cycle Clock Select	<ul> <li>50,0kHz   Low Power – Single capacitive sensor connected between a port and ground.</li> <li>500kHz   High Speed/4 – Differential capacitive sensor connected between 2 ports with the middle tap of the sensor connected to ground.</li> <li>2,00MHz   High Speed – Single capacitive sensor connected between 2 ports.</li> </ul>
Conversion Duration	Displays the entire conversion duration per cycles for averaging and fake measurements.
C_TRIG_SEL	<ul> <li>Selects the source that triggers the start of a capacitance measurement</li> <li>Continuous – Continuous measurement, self-triggering. Recommended when no temperature measurement is made in parallel.</li> <li>Read Triggered – Triggered by read out</li> <li>Timer Triggered – Depending on the setting the 'Conversion Time'. Generally recommended setting → less prone to error conditions.</li> <li>Timer Triggered (Stretched) – Depending on the setting the CONV_TIME. The parameter is used as sequence period.</li> <li>Pin triggered – Triggered by external Pin, selectable from option ext.Trigger-Pin</li> <li>Opcode Triggered   Off – Started by SPI Command 0x8C</li> <li>Continuous (exp.) – (not recommended)</li> </ul>
Ext. Trigger-Pin	Used to select the pin to be used as the source of trigger for the capacitance measurement. NOTE: In the delivered EVA board, the pins DSP_IN0 and DSP_IN1 are part of the SPI communication interface, hence only DSP_IN2 and DSP_IN3 selections are relevant.

#### **Conversion Control**

CONV_TIME	Sets the conversion time in multiples of twice the period of the low-frequency clock
Conversion Time	Displays the entire conversion time per measurement.
Measuring rate	Displays the frequency at which capacitive measurement data is transferred from the DSP to the interface (SPI or I2C).

# 4.2.1.4 RDC Page

	ams PCap04 e Memory	Tools Interfa	ce Help									
S	etup CDC F	rontend CDC	RDC PDM	/PWM	DSP/C	SPIO	Misc	Exp	pert	C	in	
	Res	istance to Dig	itial Conversio	on for	Temper	ature	Mea	surem	ent			
		87		ŕ	2						0	32 C
				35	11					0	Open Gra	pn
		PT	TOUT	1			$\searrow$			St	art Measur	ement
	Γ	070	/055	٦ <sub>-</sub>	1	4					Write Cor	fin
	+		/REF	ALU		Poly-S	i/					
		PT1000	PT1	1	J. L						Write Comp	plete
	2523					/					Power On R	eset
	10n		in r		REFE	RENCE					Init Res	et 🛛
	20us Fulicharge 20us Discharge 7 20us	2	0 ersion Duration	<u></u>	DC asyni		DSP_		1	P	Rui Combined E	nbit ) rror ) CAF
#	Name	Results	Filter	fpp	Factor	Offset	-	Span	Final Result	Mean 🗍 50	Std Dev	SNR [bit
0	CO/Cref	0800005E	none 💌 S		10p	0		10p	10p	10p	0	Inf
1	C1/Cref	3B5DEA4B	none 💌 S	<b>∳</b> -27	10p	0	AO		74,2086p	74,2064p	and the second second	10,54
2	C2/Cref	12418816	Concession of the local division of the loca	<b>-</b> 27	10p	0	AO		22,82p	22,8232p		
3	C3/Cref	127A20FD		-27	10p	0	AO	1	23,0963p	23,0993p		
4	C4/Cref	00000000		-27	10p	0	AO		0	0	0	Inf
5	C5/Cref	00000000	And Address of Concession, Name	-27	10p	0	AO	10000	0	0	0	Inf
6 7	PT1/Ref Alu/Ref	00000000 01DD2CBE	and the second se	-25	1	0	AO AO		0 931,982m	0 931,937m	0 30,36u	Inf

#### Figure 14 RDC page

Options on 'RDC' page:

Temp.Sensor0	To select a thermistor connected to port PT0/REF for temperature measurement. This could be e.g. an external PT1000.
Temp.Sensor1	To select a thermistor connected to port PT1 for temperature measurement.
Temp.Sensor2	To select either the internal aluminum (ALU) thermistor for temperature measurement.
Reference	To select either the internal Poly-Si thermistor or an external reference resistor at port PT0/REF for temperature measurement.

### **Cycle Control**

Precharge Time	Displays the precharge time. It depends on R_OLF_DIV.
Fullcharge Time	Displays the fullcharge time It depends on R_OLF_DIV.
Discharge Time	Set the discharge time. It depends on R_OLF_DIV.
R_AVRG	Set averaging for temperature measurement.
R_FAKE	Set number of fake measurements per temperature measurement cycle.
Conversion Duration	Displays the entire conversion duration per cycles for averaging and fake measurements.

#### **Conversion Control**

Temp. Trigger Select	Selects the source that triggers the start of a temperature measurement
	Off: Default setting when no temperature measurement is wanted. In this case,
	a temperature measurement can still be started by SPI Command 0x8E.
	OLF_CLK: Triggered by Low-frequency oscillator.
	Pin-Triggered: Triggered by external Pin, selectable from option ext.Trigger-Pin
	<b>CDC asynchronous</b> : Depending on the setting in the 'T_TRIG_PREDIV' counter on the RDC page. The DSP is triggered by the RDC end of conversion. If RDC rate is less than CDC rate the DSP is triggered directly from the CDC for inactive RDC conversions.
	<b>CDC synchronous</b> : Depending on the setting in the 'T_TRIG_PREDIV' counter on the RDC page. The DSP is triggered by the RDC end of conversion. Assuming that RDC rate is less than the CDC rate, the inactive RDC conversions are replaced by a delay.
R_TRIG_PREDIV	For CDC and OLF options the RDC measure rate can be reduced by setting a divider.
Conversion Time	Displays the entire conversion time per measurement.
Measuring Rate	Displays the frequency at which capacitive measurement data is transferred from the DSP to the interface (SPI or I2C).
Ext. Trigger-Pin	Used to select the pin to be used as the source of trigger for the capacitance measurement.
	NOTE: In the evaluation board, the pins DSP_IN0 and DSP_IN1 are part of the SPI communication interface, hence only DSP_IN2 and DSP_IN3 selections can be used.

## 4.2.1.5 PDM / PWM Page

	ns PCap04													x
File	Memory T	ools Inte	erface	Help										
Setu	p CDC Fro	ntend (	CDC	RDC	PDM/P	WM	DSP/C	SPIO	Misc	Exp	pert		m	
Pu	ulse Interface	e 0			Pul	se In	terface 1	Ľ						
	Clock Se	elect					Clock Se	elect					Open Gra	ph
	OHF / 1		5				OHF / 1		•	5		Sta	nt Measure	ement
	Resolut	ion					Resolut	tion					Write Con	fig
	14 bits		10 bits	esence R	•	0			Write Complete					
	Pulse In	nterface Se	elect				Pulse Ir	nterface	Sele	ect			ower On R	
	PDM		- 1				PDM		-	1			Init Rese	et
	Toggi	le Enable					Togg	le Enabi	-					
	Pulse Se						Pulse S		C.					
	C1/Cref	5655555	Ìm				1	200222						
	UL/UEI	2					Alu/Re	t i	•	17				
	C1/GE		1				Alu/Re	1	•	7				
			1				Alu/Re	1		7				
		<u>. I</u>	1				Alu/Re	1	•	7				
			1				Alu/Re	Ţ		7			Rur	ıbit 🥘
			1				Alu/Re	T		7		Co	Rur ombined E	2
			1				Alu/Re	T		7				2
			1				Alu/Re			·		PI		2
# Na	ame	Results		lter		fpp	Alu/Re Factor			Span	Final Result	PI		TROF
0 00	ame )/Cref	Results 0800005	Fi 5E no	one [		-27	Factor 10p	Offset 0	AO	Span 10p	10p	PI Mean∯50 10p	ombined E	SNR (bi
0 CO 1 C1	ame )/Cref	Results 0800005 385DEA4	Fi 5E no 4B no	one [	- 5	-27 -27	Factor 10p 10p	Offset 0 0	40	Span 10p 10p	10p 74,2086p	PI Mean ∯ 50 10p 74,2064p	ombined E CO Std Dev 0 6,71f	SNR (b) Inf 10,54
0 C0 1 C1 2 C2	ame D/Cref L/Cref 2/Cref	Results 0800005	Fi 5E no 4B no	one [	•	-27 -27 -27	Factor 10p 10p 10p	Offset 0	40 40	Span 10p 10p 10p	10p 74,2086p 22,82p	Mean∯50 10p 74,2064p 22,8232p	ombined E Std Dev 0 6,71f 3,616f	SNR [b Inf 10,54 11,43
0 C0 1 C1 2 C2 3 C3	ame )/Cref L/Cref 2/Cref 8/Cref	Results 0800005 385DEA4	Fi 5E no 4B no 16 no	one [ one [ one [	• • •	-27 -27 -27 -27	Factor 10p 10p	Offset 0 0	40 40 40	Span 10p 10p 10p 10p	10p 74,2086p	PI Mean ∯ 50 10p 74,2064p	ombined E Std Dev 0 6,71f 3,616f	SNR [b Inf 10,54 11,43
0 C0 1 C1 2 C2 3 C3	ame D/Cref L/Cref 2/Cref	Results 0800005 385DEA4 1241881	Fi 5E no 4B no 16 no 7D no	one [ one [ one [	•	-27 -27 -27 -27	Factor 10p 10p 10p	Offset 0 0 0	40 40	Span 10p 10p 10p 10p	10p 74,2086p 22,82p	Mean∯50 10p 74,2064p 22,8232p	ombined E Std Dev 0 6,71f 3,616f	SNR [b Inf 10,54 11,43
0 C0 1 C1 2 C2 3 C3 4 C4	ame )/Cref L/Cref 2/Cref 8/Cref	Results 0800005 385DEA4 1241881 127A20F	Fi 5E no 4B no 16 no 7D no 30 no	one [ one [ one [ one [	• • •	-27 -27 -27 -27 -27	Factor 10p 10p 10p	Offset 0 0 0 0	40 40 40 40 40	Span 10p 10p 10p 10p	10p 74,2086p 22,82p 23,0963p	Mean (50 10p 74,2064p 22,8232p 23,0993p	ombined E Std Dev 0 6,71f 3,616f 3,582f	rror CAP SNR (b Inf 10,54 11,43 11,45
0 C0 1 C1 2 C2 3 C3 4 C4 5 C5	ame D/Cref L/Cref 2/Cref 3/Cref 4/Cref	Results 0800005 385DEA4 1241881 127A20F 0000000	Fi 5E no 4B no 16 no 5D no 30 no 30 no	one [ one [ one [ one [ one [ one [		-27 -27 -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p	Offset 0 0 0 0 0 0 0	40 40 40 40 40	Span 10p 10p 10p 10p 10p 10p	10p 74,2086p 22,82p 23,0963p 0	Mean ∯50 10p 74,2064p 22,8232p 23,0993p 0	Ombined E           Std Dev           0           6,71f           3,616f           3,582f           0	rror CAI SNR (b Inf 10,54 11,43 11,45 Inf

Figure 15 PDM/PWM page

Options on 'PDM / PWM' Page:

Clock Select	Selects the clock frequency to be used for the PWM/PDM generation.
Resolution	Resolution of the output in bits. This resolution also determines the pulsed output range.
Pulse Interface Select	Select the pulse interface – Pulse Width Modulated Output (PWM) or Pulse Density Modulated (PDM) Output. Of the two, the PDM is the recommended interface. With PWM option, 100 kHz clock and 10-bit resolution the resulting PWM output frequency = (100 kHz / 1024) ~ 100 Hz.



Toggle Enable	activates toggle flip flop at Pulse Interface Output, especially for PDM to create 1:1 duty factor
Pulse Select	Select the measurement result which has to be given out as pulsed output – any of the capacitance or temperature measurement results.

### 4.2.1.6 DSP/GPIO Page

01	III ams PCap04												
Fil	e Memory T	ools Interfa	ce Help										
	etup CDC From	ntend CDC	RDC	PDM/P	WM	DSP/G	iPIO M	Nisc	Exp	pert:	Q	m	
	DSP_SPEED Stow 2 DSP_START_EN			DSP_FF_IN DSP_MOFLO_EN							Open Graph Start Measurement Write Config Write Complete		
	INT_TRIG_EN TIMER_TRIG_EN RDC_TRIG_EN CDC_TRIG_EN				DSP_STARTONPIN 공표공공							ower On R Init Rese	
G	PIO												
	PG_DIR_IN       PG_PU       PG0xPG2         이 이 이 이 이 이 이 이 이 이 이 이 이 이 이 이 이 이 이							rror ě					
#	Name	Results	Filter		fpp	Factor	Offset		Span	Final Result	Mean \$ 50	Std Dev	SNR [bit]
0	CO/Cref	0800005E	none .		-27	10p	0	AO	10p	10p	10p	0	Inf
1	C1/Cref	3B5DEA4B	1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	. 5		10p	0	AO		74,2086p	74,2064p	6,71f	10,54
2	C2/Cref	12418816	none .	5		10p	0	AO		22,82p	22,8232p	3,616f	11,43
3	C3/Cref	127A20FD	none 💽	5		10p	0	AO		23,0963p	23,0993p	3,582f	11,45
4	C4/Cref	00000000	none .	5		10p	0	AO		0	0	0	Inf
5	C5/Cref	00000000	none 💽	. 5		10p	0	AO	10p	0	0	0	Inf
6	PT1/Ref	00000000	none 💽	- 5	-25	1	0	AO	1	0	0	0	Inf
7	Alu/Ref	01DD2CBE	Median 5 🔒	- 5	-25	1	0	AO	1	931,982m	931,937m	30,36u	15,01

Figure 16 DSP/GPIO page



Options on 'DSP/GPIO' Page:

#### DSP

DSP_SPEED	Select the DSP Speed. Choose between Fastest, Fast, Slow and Slowest.
DSP_FF_IN	Pin mask for latching flip-flop activation (PG0 to PG3)
DSP_MOFLO_EN	Activates anti-bouncing filter in PG0 and PG1 lines
DSP_STARTONPIN	Not supported by standard firmware The DSP can be started externally by a signal on a pin; these buttons select the pin that has to be sensed for detecting the start signal.
DSP_START_EN	Mask for activating various trigger sources for starting the DSP

GPIO

PG_DIR_IN	To configure the ports PG0-PG3 as input (otherwise output)
PG_UP	To enable the internal pull up on the ports PG0-PG3
PG0_X_PG2	Possible only when the selected interface for communication is IIC. Interchange PortG0 with PortG2. This is useful when the Pulsed output is needed on Port PG0 instead of PG2.
PG1_X_PG3	Possible only when the selected interface for communication is IIC. Interchange PortG1 with PortG3. This is useful when the Pulsed output is needed on Port PG1 instead of PG3.
PG4_INTN_EN	Map the Interrupt output from chip, INTN to Port PG4. This setting is useful for 24 pin QFN package, because the dedicated INTN pin is absent in this version.
PG5_INTN_EN	Map the Interrupt output from chip, INTN to Port PG5. This setting is useful for 24 pin QFN package, because the dedicated INTN pin is absent in this version.

# 4.2.1.7 Misc. Page

100	etup CDC Fr	rontend CD	C RDC	PDM/P	WM D	OSP/GPIO	Misc	Exp	pert			
				and the second s	11		-	-	111		Im	
LF	Clock				HF Cloc	k					and the second second	
	10				OX_	RUN					Open Gra	ph
	OLF_CTUNE	• 0L	F_FTUNE		Pe	rmanent	8	-	1	St	art Measur	ement
	Laconia E	<u> </u>	LEG			OX DIS		100	OX_STOP		Write Con	fig
						OX AUTO	STOP D	9	n an <del>T</del> errere		Write Comp	lete
						UN_AUTO	5101_0		OX_DIV4		Power On Reset	
											Init Rese	
					ļ						Init Rese	et j
	0 1 2 3 C_G_OP_RU	и	200	P EXT		2,0	G_OP_A	3				
						2,0 C_0		] J		PI	Rur ombined E	nbit () rror () CAI
	C_G_OP_RU	и	200		fpp Fa	2,0 C_0	0 pF ▼ S_OP_V ,00 ▼	] J	Final Result	PI	ombined E	
	C_G_OP_RU pulsed	NI NI	<b>□</b> c_e_c	OP_EXT	-27 10	C_C C_C x 1	0 pF ▼ 5_0P_VI 5,00 ▼ set	J J O Span	Final Result 10p	PI Mean #50 10p	ombined E	
	C_G_OP_RL pulsed Name C0/Cref C1/Cref	JN Results	Filter	DP_EXT	-27 10 -27 10	C_C C_C x 1 ector Offs p 0	D pF ▼ S_OP_VI ,,00 ▼ set AC	3 J 0 Span 10p	10p 74,2086p	PI Mean∯50 10p 74,2064p	ombined E	SNR (b Inf 10,54
	C_G_OP_RL pulsed Name C0/Cref C1/Cref C2/Cref	JN	Filter none none	DP_EXT	-27 10 -27 10 -27 10	2,0 C_( x.1 p 0 p 0 p 0 p 0	5_OP_VI 5_OP_VI 1,00 ▼ 5et Ac	3 0 Span 10p 10p	10p 74,2086p 22,82p	PI Mean ∰50 10p 74,2064p 22,8232p	ombined E Std Dev 0 6,71f 3,616f	SNR [b Inf 10,54
NAME OF COMPANY	C_G_OP_RU pulsed Name C0/Cref C1/Cref C2/Cref C3/Cref	JN	Filter none none none	DP_EXT	-27 10 -27 10 -27 10 -27 10 -27 10	ctor Offs p 0 p 0 p 0 p 0 p 0	S_OP_V S_OP_V ,000 ▼ set AC AC AC	3 0 5pan 10p 10p 10p	10p 74,2086p 22,82p 23,0963p	PI Mean ∯50 10p 74,2064p 22,8232p 23,0993p	ombined E Std Dev 0 6,71f 3,616f 3,582f	rror CAI SNR [b Inf 10,54 11,43 11,45
	C_G_OP_RU pulsed Name C0/Cref C1/Cref C2/Cref C3/Cref C3/Cref C4/Cref	JN Results 0800005E 3B5DEA4B 12418816 127A20FD 00000000	Filter none none none none		-27 10 -27 10 -27 10 -27 10 -27 10 -24 10	ctor Offs p 0 p 0 p 0 p 0 p 0 p 0 p 0	S_OP_V S_OP_V ,000 ▼ set AC AC AC	3 0 5pan 10p 10p 10p 10p	10p 74,2086p 22,82p 23,0963p 0	PI Mean #50 10p 74,2064p 22,8232p 23,0993p 0	ombined E Std Dev 0 6,71f 3,616f 3,582f 0	rror CAI SNR [b Inf 10,54 11,43 11,45 Inf
	C_G_OP_RU pulsed Name C0/Cref C1/Cref C2/Cref C3/Cref C3/Cref C4/Cref C5/Cref	JN Results 0800005E 3B5DEA4B 12418816 127A20FD 00000000 00000000	Filter none none none none none		-27 10 -27 10 -27 10 -27 10 -27 10 -24 10 -24 10	ccor         Offs           p         0           p         0           p         0           p         0           p         0           p         0           p         0           p         0           p         0           p         0           p         0           p         0           p         0	S_OP_V S_OP_V (,00 ▼ Set AC AC AC AC	3 0 5pan 10p 10p 10p 10p 10p	10p 74,2086p 22,82p 23,0963p 0 0	Mean ∯50 10p 74,2064p 22,8232p 23,0993p 0 0	Std Dev           0           6,71f           3,616f           3,582f           0	rror SNR (b SNR (b Inf 10,54 11,43 11,45 Inf Inf
	C_G_OP_RU pulsed Name C0/Cref C1/Cref C2/Cref C3/Cref C3/Cref C4/Cref	JN Results 0800005E 3B5DEA4B 12418816 127A20FD 00000000	Filter none none none none		-27 10 -27 10 -27 10 -27 10 -27 10 -24 10 -24 10	ctor Offs p 0 p 0 p 0 p 0 p 0 p 0 p 0	S_OP_V S_OP_V ,000 ▼ set AC AC AC	3 0 0 5pan 10p 10p 10p 10p 10p	10p 74,2086p 22,82p 23,0963p 0	PI Mean #50 10p 74,2064p 22,8232p 23,0993p 0	Std Dev           0           6,71f           3,616f           3,582f           0           0	SNR [t] SNR [t] Inf 10,54 11,45 Inf Inf Inf

Figure 17 Misc. page

Options on 'Misc.' Page:

#### LF Clock

OLF_CTUNE	Coarse-tune the low frequency clock. (10kHz, 50kHz, 100kHz, 200kHz)
OLF_FTUNE	Fine-tune the low frequency clock. (015)

#### HF Clock

OX_RUN	Controls the permanency or the latency of the OX generator. Latency means an
	oscillator settling time before a measurement starts.

OX_DIS	Disable the OX clock.
OX_AUTOSTOP_DIS	Disables the automatic stop function of the OX generator between the individual measure sequences.
OX_STOP	Stop the OX-generator
OX_DIV4	OX clock frequency := raw freq./4

#### Guarding

Guarding Port Select	Individual Guard enable to each Port PC0PC5
C_G_OP_RUN	<ul> <li>permanent – Guarding OP is permanent activated</li> <li>(additional power consumption)</li> <li>pulsed – Guarding OP set to sleep mode between CDC conversions</li> </ul>
C_G_TIME	Controls the pre-charge phase
C_G_OP_EXT	Switch between internal guarding OP and an optional external OP
C_G_OP_TR	Trim power consumption of guarding OP.
C_G_OP_ATTN	Capacitive attenuation of Guarding OP.
C_G_OP_VU	OP Gain (from Sense Port to Guard).

### 4.2.1.8 Expert Page

Please modify the settings on the Expert page only in consultation with acam Support team.

#### 4.2.2 Front Panel Menus

#### 4.2.2.1 File Menu

File	Memory	Tools	Interface
0	pen Project	Ctrl+0	bc
Sa	ave Project	Ctrl+S	DC
In	nport		•
Ð	port		•
C	lose	Ctrl+W	tion

Figure 18 File Menu

Open Project	Open project file *.prj that subsumed the firmware and configuration filenames and the settings and Calibration data
Save Project	Here you can save your own project file.
Import	Import configuration (*.cfg), calibration data (*.dat) or firmware. Note: Any import will modify the active project file! Save the project file under a new name.
Export	Here you can export Config (*.cfg), Calibration (*.dat), Memory (*.dat) or Firmware (*.hex), separately
Close	Close the evaluation software

### 4.2.2.2 Memory Menu

File	Memory	Tools	Interface	Help	
Scti	Firmwa Calibra Read C	ition	om NVRAM	Ctrl+M	i/PV

#### Figure 19 Memory Menu

Figure 1-10: Memory Menu

Firmware	Opens the window to download the firmware. (section 4.2.3.1)
Calibration	Opens the Calibration window (section 4.2.3.2)
Read Config from NVRAM	Reads back the configuration information from the NVRAM and overwrites those of the GUI.

### 4.2.2.3 Tools Menu

File M	emory	Tools	Interface He	elp		
Setup	CDC I	Run	Measurement	Ctrl+R	WN	
		Grap	ph	Ctrl+G	Г	
		Reg	isters	Ctrl+F	De	
		Line	arize	Ctrl+L	4a	
		Asse	embler	Ctrl+A	w	

#### Figure 20 Tools Menu

Run Measurement	Start the measurement
Graph	Opens the window for graphical display of the various measurement results (section 4.2.3.4)
Registers	Opens the Register window (section 4.2.3.5)
Linearize	Opens the Linearize window
Assembler	Opens the assembler

#### 4.2.2.4 Interface Menu

File M	lemory	Tools	Interface	Help		
Setup	CDC F	rontenc	Bus USB C	rl+U		

#### Figure 21 Interface Menu

Bus	Select between SPI and I2C interface
USB	Opens the USB Communications window with PicoProg V3.0 Settings and the possibility to send opcodes

### 4.2.2.5 Help Menu

File M	emory Tools I	nterface	Help			
Setup	CDC Frontend	Hel Che	s F1	SP		
			Abo	out	F12	1

Figure 22 Help Menu

Help Contents	Opens the help window
Check Errors	Opens the error message window if there is an inconsistency after plausibility check.
About	Version

After each change in settings, the evaluation software automatically performs a plausibility check in the background. If a setting is not allowed or doesn't fit with the setting of the other parameters, the faulty setting is highlighted in red color.

### 4.2.3 Special Windows

#### 4.2.3.1 Firmware Window

In the 'Firmware' Window the write data can be edited.

If the NVRAM is read ('Read' button), the content is automatically compared with the 'Write Data' window content. If contents are equal this will be indicated by a green illuminated LED.

Firmware	Calibratio	n	Mi	sc. C	alik	orati	on	C	omp	lete	Me	mor	v					
		Wri	te D	ata		PCa	p04	sta	nda	rd v	XX.h	ex						
Oper	File	24	05	AO	01				5C			07	92	02	20	13	02	
		20	93	02	B2	02	78	20	54	B3	06	91	00	7F	20	86	20	
Reloa	d File	54	B6	03	72	62	20	54	B7	00	00	42	5C	A1	00	49	BO	
		00	49	40	AB	5D	92	10	90	02	7F	20	86	66	67	76	77	
Remove	'FF' at End	66	7A	CF	CD	E6	43	F1	44	29	EO	7A	DC	E7	41	32	AA	Ξ
		01	99	FD	7B	01	7A	CF	EB	E6	43	F1	44	29	EO	7A	C1	
		E7	41	32	6A	DE	44	7A	CF	EA	E6	43	F1	44	29	EO	6A	
		DF	44	7A	C4	E7	41	32	AB	05	7A	C1	E1	43	EO	3A	7A	1
		CO	E1	43	EO	3A	02	7A	CF	E6	E6	43	F1	44	29	EO	7A	
Address	Length	EF	44	02	20	9D	84	01	21	2E	21	74	20	37	C8	7A	E7	
dO	d 1024	43	49	11	6A	D4	44	7A	C1	D8	E6	43	E9	44	10	43	13	
		AB	63	6A	DE	41	AB	0B	46	46	46	7A	DF	FF	FF	FF	FF	
	1	E3	41	32	10	44	E9	13	6A	D4	13	41	AA	DF	7A	C5	E1	
Wr	ite	43	49	EO	34	7A	CF	E3	E6	43	F1	44	29	EO	DB	CO	27	
		E5	6A	DF	43	7A	C8	E7	41	30	AB	03	86	01	92	37	7A	
Re	ad	C6	E7	41	7A	FA	E7	43	EA	44	7A	C1	E1	E6	43	E9	44	
		Rea	d D	ata											Da	ta e	qual	
		24	05	AO	01	20	55	42	5C	48	B1	07	92	02	20	13	02	
		20	93	02	B2	02	78	20	54	B3	06	91	00	75	20		20	E
		5.5	B6	10.00	72	62	20		B7	00	00	42	5C	A1	00	49		
		00	2.23	40	AB	50	92	10	90	02	7F	20	86	1000	67	1222	77	1
		66	7A	CF	CD	EG	43	F1	44	29	EO	7A	DC	E7	41	1993	AA	
Firmware \	/ersion	01	99	FD	7B	01	7A	CF	EB	E6	43	F1	44	29	EO	7A	C1	
Contractor Colleges		E7	41	32	6A	1.11	44	177	CF	12.2	E6	43	F1	44	29	EO	6A	
Product G	roup	DF	44	7A	1000	E7	41	32	AB	05	7A	C1	E1	43	EO	3A	7A	
1		CO	E1	172	EO	3A	02	1.7.5.1	CF	E6	E6	43	F1	44	29	EO	7A	
		EF	44	02	20	9D	84	01	21	2E	21	74	20	37	C8	7A	E7	
Program 1	ype	43	49	11	6A	D4	44	7A	C1	D8	E6	43	E9	44	10	43	13	
		AB	63	6A	DE	41	AB	OB	46	46	46		DF	FF	FF	FF	FF	
		E3	41	32	10	44	E9	13	6A	D4	13	41	AA	DF	7A	C5	E1	
Version		43	49	EO	34	7A	CF	E3	E6	43	F1	44	29	EO	DB	CO	27	
0		E5	6A	DF	43	7A	C8	E7	41	30	AB	03	86	01	92	37	7A	
And the second sec		CG		41										E6				

Figure 23 Firmware Window

Open File	Select and open a firmware file (.hex) or import firmware from a project file. The content is shown in the 'Write Data' window.
Reload File	Reload the last opened firmware file (.hex). The content is shown in the 'Write Date' window again.
Read	Pressing this button, the content of the NVRAM is read and shown in the 'Read Data' window. In 'Address' and 'Length' you can specify how many bytes you want read, starting at which address.
Write	Writes the firmware into the chip's NVRAM. The status of the write process is indicated by the green bar. The successful end is indicated by a pop-up window. For verification we recommend to read back the NVRAM afterwards and compare it with the source.
Firmware Version	In the firmware, a specific address is reserved to save 3 byte information about the application and the version of the software. The coding is specified in the header file of the supported PICOCAP device, for example: <i>pcap_standard.h</i> . The header file is found in the library directory of the assembler.

### 4.2.3.2 Calibration Window

The NVRAM provides the possibility to store data like linearization coefficients, division steps, alert levels etc.. This way, one and the same firmware can be used for various types of sensors.

The Calibration data are part of the project file. After opening a project, the Calibration data need to be written manually. Therefore please open the "Memory / Calibration" menu and then press "Write" or use the 'Write Complete' button.

Firmw	are Calibration	Misc. Calibrat	tion	Comp	lete Mem	югу		
Calil	oration N	o. of Calibration	n Values	55	Si	tart Addre:	ss d 800	
#	Name	Value	fpp	s/u	Length	Address	Value (hex)	
0	pi0_result0	0	8	5	4	800	00000000	
1	pi0_result1	100	8	5	4	804	00006400	
2	pi0_pulse0	0	0	u	2	808	0000	
3	pi0_pulse1	16,383k	0	u	2	810	3FFF	
4	pi1_result0	-40	8	s	4	812	FFFFD800	=
5	pi1_result1	125	8	s	4	816	00007D00	1
6	pi1_pulse0	0	0	u	2	820	0000	
7	pi1_pulse1	16,383k	0	u	2	822	3FFF	
8	xi_at_ccp1	0	26	s	4	824	00000000	
9	xi_at_ccp2	1	26	s	4	828	04000000	4
10	ci_at_ccp1	0	26	u	4	832	00000000	
11	ci_at_ccp2	1	26	u	4	836	04000000	
12	cc32	0	0	5	4	840	00000000	
13	cn_div32	0	0	u	1	844	00	
14	cc22	0	0	5	4	845	00000000	
15	cn_div22	0	0	u	1	849	00	
16	cc12	0	0	5	4	850	00000000	
17	cn_div12	0	0	u	1	854	00	
18	cc02	0	0	s	4	855	00000000	
19	cn_shift2	0	0	s	1	859	00	
20	cc31	0	0	5	4	860	00000000	
21	cn_div31	0	0	u	1	864	00	
22	cc21	0	0	s	4	865	00000000	
23	cn_div21	0	0	u	1	869	00	-

Figure 24 Calibration Window

Import Linearization Data	Imports Linearization Data from "Linearize / Pulse" window
Write	Writes the data into the chip's NVRAM.
Read	Pressing this button, the Linearization Data are read from the NVRAM and shown in the tab.



### 4.2.3.3 Misc. Calibration Window

This window shows miscellaneous calibration bits at address d'956-d'959 (4 byte). The meaning of the content strongly depends on the firmware.

ware	Calibration	Misc. C	alibra	tion	Con	npl	ete Me	mor
scella	ineous Calibrati	on Bits a	t Ado	ress	956	].	<mark>d 9</mark> 59	
‡ N;	ame		#	Name		200	t.	1
а		0	16					0
Ú.		0	17					0
2		0	18					0
3		0	19					0
1		0	20					0
5		0	21					0
5		0	22					0
7		0	23					0
3		0	24					0
9		O	25					0
10		0	26					0
11		0	27					0
12		0	28					0
13		O	29					0
14		0	30					0
15		0	31					0
						×	000000	000
							Write	
							Read	

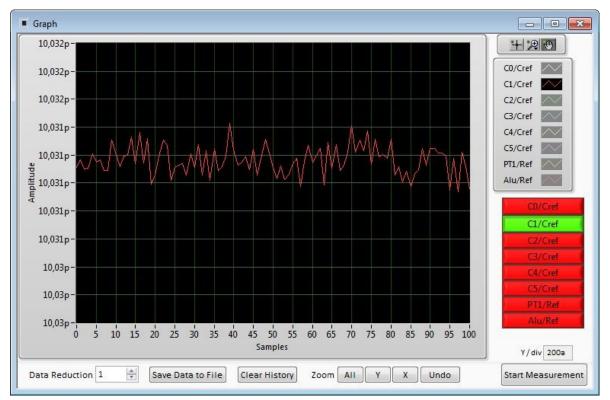
Figure 25 Misc. Calibration Window

Write	Writes the data into the chip's NVRAM.
Read	Pressing this button, the bits are read from the NVRAM and shown in the tab.

			n N	IISC.	calib	oratio	on	Com	plete	Men	nory					6				
Write	Men	nory																		
24	05	AØ	01	20	55	42	5C	48	B1	07	92	02	20	13	02					
20	93	02	B2	02	78	20	54	<b>B</b> 3	06	91	00	7F	20	86	20					
54	<b>B6</b>	03	72	62	20	54	B7	00	00	42	5C	A1	00	49	BØ	1				
00	49	40	AB	5D	92	1C	90	02	7F	20	86	66	67	76	77					
66	7A	CF	CD	E6	43	F1	44	29	EØ	<b>7</b> A	DC	E7	41	32	AA					
01	99	FD	7B	01	<b>7</b> A	CF	EB	E6	43	F1	44	29	EØ	7A	C1					
E7	41	32	6A	DE	44	7A	CF	EA	E6	43	F1	44	29	EØ	6A					
DF	44	7A	C4	E7	41	32	AB	05	7A	C1	E1	43	EØ	ЗA	7A	Ŧ				
Read	Mem	ory											Da	ta ec	ual	C				
-	-		00	-		10		10	Da	07	00									
	1 2 2 2					2.7			100.00			1.55.50		1.55.50		C				
		_																		
								1												
							-					-		-		1				
								10						1000		1				
-																				
		74	C4	E7	41	32	AB	05	7A	C1	E1	43	EØ	3A	7A					
	24 20 54 00 66 01 E7 DF	24         05           20         93           54         86           00         49           66         7A           01         99           E7         41           DF         44           Read         Mem           24         05           20         93           54         86           00         49           66         7A           01         99	20         93         02           54         86         03           00         49         40           66         7A         CF           01         99         FD           E7         41         32           DF         44         7A           Colspan="2">Colspan="2"           Colspan="2">Colspan="2"           Colspan="2">Colspan="2"           Colspan="2"           Colspan="2" <td>24         05         A0         01           20         93         02         B2           54         B6         03         72           00         49         40         AB           66         7A         CF         CD           01         99         FD         7B           E7         41         32         6A           DF         44         7A         C4</td> <td>24       05       A0       01       20         20       93       02       B2       02         54       B6       03       72       62         00       49       40       AB       5D         66       7A       CF       CD       E6         01       99       FD       7B       01         E7       41       32       6A       DE         DF       44       7A       C4       E7</td> <td>24         05         A0         01         20         55           20         93         02         B2         02         78           54         B6         03         72         62         20           00         49         40         AB         5D         92           66         7A         CF         CD         E6         43           01         99         FD         7B         01         7A           E7         41         32         6A         DE         44           DF         44         7A         C4         E7         41           Sead Memory         Write         Write         55         20         93         02         B2         02         78           54         B6         03         72         62         20         78           54         B6         03         72         62         20         78           54         B6         03         72         62         20         78         51         20         92         66         7A         CF         CD         E6         43         61         52         <td< td=""><td>24         05         A0         01         20         55         42           20         93         02         B2         02         78         20           54         B6         03         72         62         20         54           00         49         40         AB         5D         92         1C           66         7A         CF         CD         E6         43         F1           01         99         FD         7B         01         7A         CF           E7         41         32         6A         DE         44         7A           DF         44         7A         C4         E7         41         32</td><td>24       05       A0       01       20       55       42       5C         20       93       02       B2       02       78       20       54         54       B6       03       72       62       20       54       B7         00       49       40       AB       5D       92       1C       90         66       7A       CF       CD       E6       43       F1       44         01       99       FD       7B       01       7A       CF       EB         E7       41       32       6A       DE       44       7A       CF         DF       44       7A       C4       E7       41       32       AB         Write</td><td>24         05         A0         01         20         55         42         5C         48           20         93         02         B2         02         78         20         54         B3           54         B6         03         72         62         20         54         B7         00           00         49         40         AB         5D         92         1C         90         02           66         7A         CF         CD         E6         43         F1         44         29           01         99         FD         7B         01         7A         CF         EB         E6           E7         41         32         6A         DE         44         7A         CF         EA           DF         44         7A         C4         E7         41         32         AB         05</td><td>24       05       A0       01       20       55       42       5C       48       B1         20       93       02       B2       02       78       20       54       B3       06         54       B6       03       72       62       20       54       B7       00       00         00       49       40       AB       5D       92       1C       90       02       7F         66       7A       CF       CD       E6       43       F1       44       29       E0         01       99       FD       7B       01       7A       CF       EB       E6       43         E7       41       32       6A       DE       44       7A       CF       EA       E6         DF       44       7A       C4       E7       41       32       AB       05       7A         Write       Store         Write       Store         Store         Q2       65       42       5C       48       B1         20       93       02       B2       02</td><td>24         05         A0         01         20         55         42         5C         48         B1         07           20         93         02         B2         02         78         20         54         B3         06         91           54         B6         03         72         62         20         54         B7         00         00         42           00         49         40         AB         5D         92         1C         90         02         7F         20           66         7A         CF         CD         E6         43         F1         44         29         E0         7A           01         99         FD         7B         01         7A         CF         EB         E6         43         F1           E7         41         32         6A         DE         44         7A         CF         EA         E6         43           DF         44         7A         C4         E7         41         32         AB         05         7A         C1           Write         Store         Store           <td <="" colspan="4" td=""><td>24         05         A0         01         20         55         42         5C         48         B1         07         92           20         93         02         B2         02         78         20         54         B3         06         91         00           54         B6         03         72         62         20         54         B7         00         00         42         5C           00         49         40         AB         5D         92         1C         90         02         7F         20         86           66         7A         CF         CD         E6         43         F1         44         29         E0         7A         DC           01         99         FD         7B         01         7A         CF         EB         E6         43         F1         44           F7         41         32         6A         DE         44         7A         CF         EB         E6         43         F1         44           F7         44         7A         C4         E7         41         32         AB         05         7A</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0         E7       41       32       6A       DE       44       7A       CF       EB       E6       43       F1       44       29       E0         DF       44       7A       C4       E7       41</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20       13         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29       E0       7A</td><td>24       95       A0       01       20       55       42       5C       48       B1       07       92       02       20       13       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49       B0         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76       77         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32       AA         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A       C1         E7       41       32       AB       05       7A       C1       E1       43       E0</td></td></td></td<></td>	24         05         A0         01           20         93         02         B2           54         B6         03         72           00         49         40         AB           66         7A         CF         CD           01         99         FD         7B           E7         41         32         6A           DF         44         7A         C4	24       05       A0       01       20         20       93       02       B2       02         54       B6       03       72       62         00       49       40       AB       5D         66       7A       CF       CD       E6         01       99       FD       7B       01         E7       41       32       6A       DE         DF       44       7A       C4       E7	24         05         A0         01         20         55           20         93         02         B2         02         78           54         B6         03         72         62         20           00         49         40         AB         5D         92           66         7A         CF         CD         E6         43           01         99         FD         7B         01         7A           E7         41         32         6A         DE         44           DF         44         7A         C4         E7         41           Sead Memory         Write         Write         55         20         93         02         B2         02         78           54         B6         03         72         62         20         78           54         B6         03         72         62         20         78           54         B6         03         72         62         20         78         51         20         92         66         7A         CF         CD         E6         43         61         52 <td< td=""><td>24         05         A0         01         20         55         42           20         93         02         B2         02         78         20           54         B6         03         72         62         20         54           00         49         40         AB         5D         92         1C           66         7A         CF         CD         E6         43         F1           01         99         FD         7B         01         7A         CF           E7         41         32         6A         DE         44         7A           DF         44         7A         C4         E7         41         32</td><td>24       05       A0       01       20       55       42       5C         20       93       02       B2       02       78       20       54         54       B6       03       72       62       20       54       B7         00       49       40       AB       5D       92       1C       90         66       7A       CF       CD       E6       43       F1       44         01       99       FD       7B       01       7A       CF       EB         E7       41       32       6A       DE       44       7A       CF         DF       44       7A       C4       E7       41       32       AB         Write</td><td>24         05         A0         01         20         55         42         5C         48           20         93         02         B2         02         78         20         54         B3           54         B6         03         72         62         20         54         B7         00           00         49         40         AB         5D         92         1C         90         02           66         7A         CF         CD         E6         43         F1         44         29           01         99         FD         7B         01         7A         CF         EB         E6           E7         41         32         6A         DE         44         7A         CF         EA           DF         44         7A         C4         E7         41         32         AB         05</td><td>24       05       A0       01       20       55       42       5C       48       B1         20       93       02       B2       02       78       20       54       B3       06         54       B6       03       72       62       20       54       B7       00       00         00       49       40       AB       5D       92       1C       90       02       7F         66       7A       CF       CD       E6       43       F1       44       29       E0         01       99       FD       7B       01       7A       CF       EB       E6       43         E7       41       32       6A       DE       44       7A       CF       EA       E6         DF       44       7A       C4       E7       41       32       AB       05       7A         Write       Store         Write       Store         Store         Q2       65       42       5C       48       B1         20       93       02       B2       02</td><td>24         05         A0         01         20         55         42         5C         48         B1         07           20         93         02         B2         02         78         20         54         B3         06         91           54         B6         03         72         62         20         54         B7         00         00         42           00         49         40         AB         5D         92         1C         90         02         7F         20           66         7A         CF         CD         E6         43         F1         44         29         E0         7A           01         99         FD         7B         01         7A         CF         EB         E6         43         F1           E7         41         32         6A         DE         44         7A         CF         EA         E6         43           DF         44         7A         C4         E7         41         32         AB         05         7A         C1           Write         Store         Store           <td <="" colspan="4" td=""><td>24         05         A0         01         20         55         42         5C         48         B1         07         92           20         93         02         B2         02         78         20         54         B3         06         91         00           54         B6         03         72         62         20         54         B7         00         00         42         5C           00         49         40         AB         5D         92         1C         90         02         7F         20         86           66         7A         CF         CD         E6         43         F1         44         29         E0         7A         DC           01         99         FD         7B         01         7A         CF         EB         E6         43         F1         44           F7         41         32         6A         DE         44         7A         CF         EB         E6         43         F1         44           F7         44         7A         C4         E7         41         32         AB         05         7A</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0         E7       41       32       6A       DE       44       7A       CF       EB       E6       43       F1       44       29       E0         DF       44       7A       C4       E7       41</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20       13         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29       E0       7A</td><td>24       95       A0       01       20       55       42       5C       48       B1       07       92       02       20       13       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49       B0         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76       77         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32       AA         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A       C1         E7       41       32       AB       05       7A       C1       E1       43       E0</td></td></td></td<>	24         05         A0         01         20         55         42           20         93         02         B2         02         78         20           54         B6         03         72         62         20         54           00         49         40         AB         5D         92         1C           66         7A         CF         CD         E6         43         F1           01         99         FD         7B         01         7A         CF           E7         41         32         6A         DE         44         7A           DF         44         7A         C4         E7         41         32	24       05       A0       01       20       55       42       5C         20       93       02       B2       02       78       20       54         54       B6       03       72       62       20       54       B7         00       49       40       AB       5D       92       1C       90         66       7A       CF       CD       E6       43       F1       44         01       99       FD       7B       01       7A       CF       EB         E7       41       32       6A       DE       44       7A       CF         DF       44       7A       C4       E7       41       32       AB         Write	24         05         A0         01         20         55         42         5C         48           20         93         02         B2         02         78         20         54         B3           54         B6         03         72         62         20         54         B7         00           00         49         40         AB         5D         92         1C         90         02           66         7A         CF         CD         E6         43         F1         44         29           01         99         FD         7B         01         7A         CF         EB         E6           E7         41         32         6A         DE         44         7A         CF         EA           DF         44         7A         C4         E7         41         32         AB         05	24       05       A0       01       20       55       42       5C       48       B1         20       93       02       B2       02       78       20       54       B3       06         54       B6       03       72       62       20       54       B7       00       00         00       49       40       AB       5D       92       1C       90       02       7F         66       7A       CF       CD       E6       43       F1       44       29       E0         01       99       FD       7B       01       7A       CF       EB       E6       43         E7       41       32       6A       DE       44       7A       CF       EA       E6         DF       44       7A       C4       E7       41       32       AB       05       7A         Write       Store         Write       Store         Store         Q2       65       42       5C       48       B1         20       93       02       B2       02	24         05         A0         01         20         55         42         5C         48         B1         07           20         93         02         B2         02         78         20         54         B3         06         91           54         B6         03         72         62         20         54         B7         00         00         42           00         49         40         AB         5D         92         1C         90         02         7F         20           66         7A         CF         CD         E6         43         F1         44         29         E0         7A           01         99         FD         7B         01         7A         CF         EB         E6         43         F1           E7         41         32         6A         DE         44         7A         CF         EA         E6         43           DF         44         7A         C4         E7         41         32         AB         05         7A         C1           Write         Store         Store <td <="" colspan="4" td=""><td>24         05         A0         01         20         55         42         5C         48         B1         07         92           20         93         02         B2         02         78         20         54         B3         06         91         00           54         B6         03         72         62         20         54         B7         00         00         42         5C           00         49         40         AB         5D         92         1C         90         02         7F         20         86           66         7A         CF         CD         E6         43         F1         44         29         E0         7A         DC           01         99         FD         7B         01         7A         CF         EB         E6         43         F1         44           F7         41         32         6A         DE         44         7A         CF         EB         E6         43         F1         44           F7         44         7A         C4         E7         41         32         AB         05         7A</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0         E7       41       32       6A       DE       44       7A       CF       EB       E6       43       F1       44       29       E0         DF       44       7A       C4       E7       41</td><td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20       13         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29       E0       7A</td><td>24       95       A0       01       20       55       42       5C       48       B1       07       92       02       20       13       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49       B0         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76       77         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32       AA         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A       C1         E7       41       32       AB       05       7A       C1       E1       43       E0</td></td>	<td>24         05         A0         01         20         55         42         5C         48         B1         07         92           20         93         02         B2         02         78         20         54         B3         06         91         00           54         B6         03         72         62         20         54         B7         00         00         42         5C           00         49         40         AB         5D         92         1C         90         02         7F         20         86           66         7A         CF         CD         E6         43         F1         44         29         E0         7A         DC           01         99         FD         7B         01         7A         CF         EB         E6         43         F1         44           F7         41         32         6A         DE         44         7A         CF         EB         E6         43         F1         44           F7         44         7A         C4         E7         41         32         AB         05         7A</td> <td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44</td> <td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0         E7       41       32       6A       DE       44       7A       CF       EB       E6       43       F1       44       29       E0         DF       44       7A       C4       E7       41</td> <td>24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20       13         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29       E0       7A</td> <td>24       95       A0       01       20       55       42       5C       48       B1       07       92       02       20       13       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49       B0         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76       77         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32       AA         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A       C1         E7       41       32       AB       05       7A       C1       E1       43       E0</td>				24         05         A0         01         20         55         42         5C         48         B1         07         92           20         93         02         B2         02         78         20         54         B3         06         91         00           54         B6         03         72         62         20         54         B7         00         00         42         5C           00         49         40         AB         5D         92         1C         90         02         7F         20         86           66         7A         CF         CD         E6         43         F1         44         29         E0         7A         DC           01         99         FD         7B         01         7A         CF         EB         E6         43         F1         44           F7         41         32         6A         DE         44         7A         CF         EB         E6         43         F1         44           F7         44         7A         C4         E7         41         32         AB         05         7A	24       05       A0       01       20       55       42       5C       48       B1       07       92       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44	24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0         E7       41       32       6A       DE       44       7A       CF       EB       E6       43       F1       44       29       E0         DF       44       7A       C4       E7       41	24       05       A0       01       20       55       42       5C       48       B1       07       92       02       20       13         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A         E7       41       32       6A       DE       44       7A       CF       EA       E6       43       F1       44       29       E0       7A	24       95       A0       01       20       55       42       5C       48       B1       07       92       02       20       13       02         20       93       02       B2       02       78       20       54       B3       06       91       00       7F       20       86       20         54       B6       03       72       62       20       54       B7       00       00       42       5C       A1       00       49       B0         00       49       40       AB       5D       92       1C       90       02       7F       20       86       66       67       76       77         66       7A       CF       CD       E6       43       F1       44       29       E0       7A       DC       E7       41       32       AA         01       99       FD       7B       01       7A       CF       EB       E6       43       F1       44       29       E0       7A       C1         E7       41       32       AB       05       7A       C1       E1       43       E0

Figure 26 Complete Memory Window

Write	Writes the complete NVRAM.
Store	The complete data transfer from Memory (volatile) to FLASH (non-volatile) is performed by a STORE
Erase	During this ERASE procedure, first the complete NVRAM will erased (set to zero) and afterwards the MEM_LOCK bits will be cleared.
Read	Pressing this button, the complete NVRAM are read and shown in the tab.
Recall	This means that the complete Memory is copied from the FLASH (non-volatile) to the Memory (volatile). After a power-on reset, a recall is processed.



4.2.3.4 Graph Window

Figure 27 Graph Window

The data to be displayed are selected in the field at the bottom right. The labels in the buttons are the same as in the diagnostics window. To display data press the corresponding button so that it gets green. Top right of the 'Graph' Windows are various options for automatic zoom in/out, center or scale in other ways. Below the graph are various automatic zoom functions for the x-axis and the y-axis.

Y-Zoom will be chanced with the keys [+], [-] and X-Zoom with the keys [\*], [/]. With the cursor control keys  $[\leftarrow]$ ,  $[\rightarrow]$ ,  $[\uparrow]$ ,  $[\downarrow]$  is it possible to move the graph.

The data displayed can be stored into a text file. For long-term investigations it is possible to reduce the data displayed and stored. The field 'Data Reduction' allows to define the level of data reduction.

### 4.2.3.5 Registers Window

These windows display the configuration data in hexadecimal format as they are currently used. Also the result registers' content is shown in hexadecimal format, but updated only when the button is pressed. Finally, the various status bits are shown.

Write Registers Re	sults
	Register
Register 3, 2, 1, 0	× 1058001D
Register 7, 6, 5, 4	× 200F0010
Register 11, 10, 9, 8	× 0007D000
egister 15, 14, 13, 12	× 03FF0800
Register 19, 18, 17, 16	× 00002400
Register 23, 22, 21, 20	× 30500100
Register 27, 26, 25, 24	× 04520434
Register 31, 30, 29, 28	× 0882005A
Register 35, 34, 33, 32	× 00470008
Register 39, 38, 37, 36	× 71002800
Register 43, 42, 41, 40	× 00080000
Register 47, 46, 45, 44	× 01000000
Register 51, 50, 49, 48	× 00000000

Write Registers	Results			
	Results			
Res 0 <310>	× 08000014			
Res 1 <310>	× 08066338			
Res 2 <310>	× 080F08C4			
Res 3 <310>	× 081D6C44			
Res 4 <310>	× 00000000			
Res 5 <310>	× 00000000			
Res 6 <310>	× 00000000			
Res 7 <310>	× 01D120B8			
	Read Results			
Statusreg				
Port Error 🧕 🕲	0000			
😑 Runbit	COMB_ERR			
CDC active	ERR_OVFL			
TENDFLAG	MUP_ERROR			
Autoboot bus	y 🔘 RDC_ERR			
TESTMODE	SENSE_TESTO			

Figure 28 Write Registers and Results

# 4.2.4 Linearize

### 4.2.4.1 Sensor Characterization

The first step is the characterization of the sensor. Therefore, it is necessary to collect data at several measurement points and at several temperatures.

As mentioned earlier, the data collection should be made of minimum 12 measurements, taken at least at 3 different temperatures. The temperatures should cover the operating temperature range of interest of the final device. The number of calibration points is set at the top left. This is the first thing to be done. Then calibration can begin. Line by line the user can enter the reference values for Z and  $\Box$  at the various calibration points. Having the cursor in this line it is sufficient to press the acquire button to get the actual ci\_ratio result. But of course the value can be entered manually, too.

The graph on the bottom left shows the Z,  $\vartheta$  distribution of the calibration points. Ideally it should have dots on three different lines covering the operating range of the sensor.

The table on the left shows the calculated calibration coefficients and the graph below shows the deviation due to the mathematical approximation.

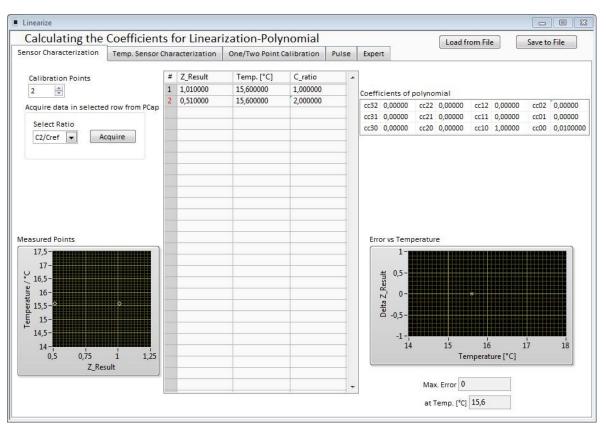


Figure 29 Sensor Characterization

# 4.2.4.2 Temperature Sensor Characterization

Together with the calibration of the capacitance sensor it is mandatory to calibrate the temperature, too. Whether the internal aluminum sensor is used or an external platinum sensor or any other sensor: they need to be calibrated to get the correct temperature information which is then used as input for the polynomial correction of the capacitance measurement.

The tab "Temperature Sensor Characterization" (Figure 1-18) offers a tool very similar to the capacitive sensor characterization. The resistance ratio has to be collected at several temperature points. For best approximation 4 calibration points are needed. In case of 2 or 3 calibration points a 2nd respectively a 3rd order polynomial is calculated.

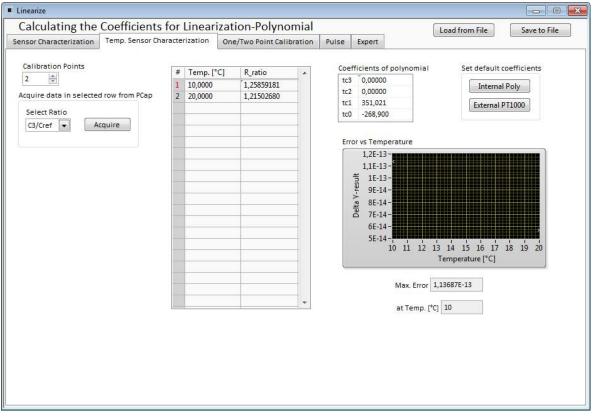


Figure 30 Temp. Sensor Characterization

On the right side of the tab "Temperature Sensor Characterization" there are two buttons to select default characteristic data for the internal aluminum sensor and a platinum sensor. The aluminum is assumed to be linear in a range of 10 °C to 70°C so only two coefficients are used.

In case the default values are used it is necessary to have at least a two point calibration of the temperature (see next section).

# 4.2.4.3 One/Two Point Calibration

Once a batch is characterized with respect to the capacitive sensor and the resistive temperature sensor it might be sufficient to perform two-point or even one-point calibration for the rest of the sensors in the batch.

The tab "One/Two Point Calibration" offers a simple GUI to do that. On this page the user enters the reference values for Z and  $\vartheta$ . CCP1 stands for capacitance calibration point 1 etc.. When the calibration conditions are reached pressing the acquire buttons will read the actual ratios while the theoretical ones are calculated on basis of the linearization coefficients. Together with programmable limits for minimum and maximum this gives an additional set of 12 parameters to be written into the EEPROM.

Linearize	e Coefficients for Linea	rization-Polynomial			
ensor Characterization	1		Pulse	Expert	Load from File Save to File
For Ic Cap CC CC Acq S		two calibration points pleas	e use thi at_CCP		x_hex_at_CCP
TC TC Acq S		r_hex_ 00000 02000	0000	y_at_CCP 0 1	y_hex_at_CCP 00000000 02000000

Figure 31 One/Two Point Calibration



### 4.2.4.4 Pulse

ensor Characterization	Coefficients for Linear	One/Two Point Calibratio		Expert	Load from File	Save to File
ensor characterization	Temp. Sensor characterization	One/1wo Point Calibratio	n ruise	expert		
Pulse Interface 0						
Acquire Results fro	m PCan					
Input of Result	in r cop	Coefficients				
C0/Cref			00000000			
	Acquire Result 1		00000000			
Input of Pulse	Acquire Result 2		00000000			
PT1/Ref		pi0_pulse1 0,00000	0000000			
Pulse Interface 1						
Assulta Desulas for						
Acquire Results fro	песар	Coefficients				
		pi1_result0 0,00000	00000000			
Input of Result		pil_resulto 0,00000				
C1/Cref 💌	Acquire Result 1	pi1_result1 0,00000	00000000			
C1/Cref  Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref 💌	Acquire Result 1 Acquire Result 2	pi1_result1 0,00000 pi1_pulse0 0,00000	Contract of Contract of Contract			
C1/Cref Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref  Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			
C1/Cref 💌 Input of Pulse		pi1_result1 0,00000 pi1_pulse0 0,00000	0000000			

Figure 32 Pulse

# 4.2.4.5 Expert

As indicated by the name this tab is for experts only. There you set the fixed point position of the result Z. It further displays the numbers of division steps respectively shift operation to achieve the maximum resolution over all calculations.

Those are stored in the NVRAM, too. But they are calculated by the DLL and for information purpose only.

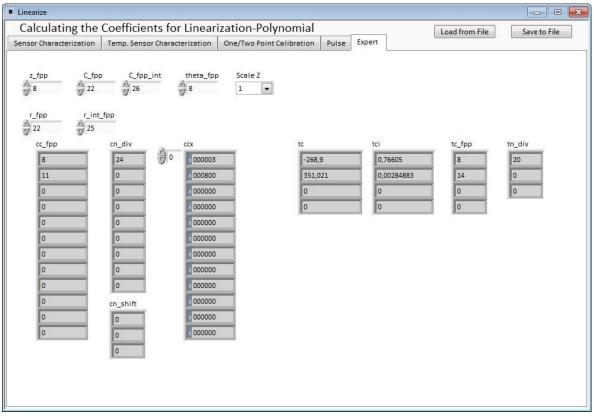


Figure 33 Expert

# 4.2.5 Assembler

	- L												The second second	-		Contraction and	1000	10.5 million 10.5	- 13 S			
		H H	×		\$	9	Ж		Ê	×		$\bigcirc$	Q	5					<sup>2</sup>			
Cap04	4 star	dard_v1	.asm																			
1																						
2		File:	PCan	a4 sta	andaro	V0.1	.asm															1
3		Descri			andand																	
4	;		8																			
5	;	This i	s the	e star	ndard	firm	are t	hat t	rans	Late	s the	TDC	Start	and	TDC S	top v	alues	into				
6		CDC an																				
7		Furthe																				
8																		ster RE		7.		
9	;	Pre-re	quist	ite :														L senso				
10	;								ernal	Rete	erenc	e. Ho	wever	, tor	this	s tirm	ware,	follow	ing			
11 12	3					d be		Senso		Ext	Icon	Dofo	nonco									
12								Senso			ernat	Rele	rence									
14											ce ou	oht t	o he	seled	ted i	n the	R POI	RT_EN_I	REE			
15								ation					U DC	SCICI	u 1	in the	A_10		nici i			
16	:	Output	5:				-8-															
17	-			5	: Car	acita	nce F	atios	for	Capi	acita	nce P	orts	PC0.	5							
18	;	RE	56		: Res	istan	ce Ra	atio f	or Ex	ter	nal S	ensor	at P	ort P	T1, v	.r.t.	Inter	nal or	Exter	nal ref	erence	
19	;	RE	57		: Res	istan	ce Ra	atio f	or In	nteri	nal s	ensor	, w.r	.t. ]	interr	nal or	Exter	nal re	ferenc	e		
20	;	PU	LSE0	& PUI	SE1 :	Pu	lse (	Output	5													
21	;				and sources				0.010.000													
22		Two of																		2.2		
23																		Pulse				
24	;	Revisi	ons	:(17.6	34.201													l signa	1 over	tlow		
25 26	3																	isters	Enont		before C	DC
20	1						ine i	leasur	emerit	L Vd.	tues	can b	e sni	rtea	LTBU	by 6		Sec In	Front	paner) i	before C	UL,
28																						
29																						
30	;	Author	: VK	OH																		
31	;																					
32																						
33	#dev	ice PC	ap04	-Z																		
34	1.00												10		1		15.7					
35	CONS	T FPP	CRATI	m			27		11			FPP	ot th	e Car	acita	ance R	atios	result				
tput																						- 6-

Figure 34 Assembler

This is a comfortable editor with syntax highlighting, search and replace, copy and paste functions.

Under menu item "Assembler" the user finds the compile and download options.

Whether the call of these functions was successful or not is indicated by the messages at the bottom of the assembler window.

Debugging is not supported in this software revision.

### 4.3 Scaling Results

PCap04 in general calculates capacitance ratios. The measured ratios include of course all effects from parasitic capacitances. Nonetheless, in many cases users might be interested in an intuitive understanding the displayed values without making a full calibration run.

The following shows by example how to set Factor and Offset to give a suitable display.

Starting point: 10 pF between PC0 and PC1, 12.2 pF between PC2 and PC3, 8pF between PC4 and PC5.

In grounded configuration, the chip measures 10pF reference against 10 pF at PC1, 12.2 pF at PC2 and PC3 and 8 pF at PC4 and PC5. In floating configuration 10pF reference is measured against 12.2 pF and 8pF.

#### a. Grounded single, no compensation

The capacitance seen includes the port parasitic capacitance as well as the internal "parasitic" capacitance (5 to 6 pF), which is dominated by the comparator delay (about 10 pF).

The base capacitance is then not 10 pF but 25 pF. Thereof 15 pF are Offset which can be subtracted.

#	Name	Results	Filter		fpp	Factor	Offset		Span	Final Result	Mean 50	Std Dev	SNR [bit]
0	CO/Cref	08000013	none [	- S	-27	25p	-15p	AO	10p	10p	10p	0	Inf
1	C1/Cref	0808B6B7	none	- S	-27	25p	-15p	AO	10p	10,1064p	10,1063p	234,5a	15,38
2	C2/Cref	08BF5F56	none	- S	-27	25p	-15p	AO	10p	12,3361p	12,336p	225,2a	15,44
3	C3/Cref	08BA5E49	none	- S	-27	25p	-15p	AO	10p	12,275p	12,2748p	316,8a	14,95
4	C4/Cref	075FA4B4	none	- 5	-27	25p	-15p	AO	10p	8,04252p	8,04221p	291,4a	15,07
5	C5/Cref	07688199	none	- 5	-27	25p	-15p	AO	10p	8,15071p	8,15064p	257,6a	15,24
6	DT1/Dof	00000000			25	1	0	10	1	0	0	0	Tof

b. Floating single, no compensation

The influence of parasitic capacitances is the same and therefore the setting for Factor and Offset are the same.

#	Name	Results	Filter		fpp	Factor	Offset		Span	Final Result	Mean 50	Std Dev	SNR [bit]
0	C0/Cref	08000009	none 🖉	5	-27	25p	-15p	AO	10p	10p	10p	0	Inf
1	C1/Cref	08B81EAB	none 🖉	5	-27	25p	-15p	AO	10p	12,2476p	12,2474p	273,1a	15,16
2	C2/Cref	076008D8	none 🖉	5	-27	25p	-15p	AO	10p	8,0473p	8,04729p	167,9a	15,86

#### c. Ground single, internal compensation

Now the chip sees only the port parasitic capacitance, not the internal one. This is in the order of 5 to 6 pF. Accordingly, the total base capacitance is 15 pF (Factor) with an offset of 5 pF.

#	Name	Results	Filter		fpp	Factor	Offset		Span	Final Result	Mean 50	Std Dev	SNR [bit]
0	CO/Cref	08000021	none [	<b>→</b> S ‡	-27	15p	-5p	AO	10p	10p	10p	0	Inf
1	C1/Cref	080E6BCE	none [	🖵 S 🛊	-27	15p	-5p	AO	10p	10,1056p	10,1059p	219,2a	15,48
2	C2/Cref	0946D492	none [	🖵 S 🛔	-27	15p	-5p	AO	10p	12,3938p	12,3935p	283a	15,11
3	C3/Cref	093E1B82	none [	🖵 S 🛢	-27	15p	-5p	AO	10p	12,3299p	12,3295p	353,1a	14,79
4	C4/Cref	06ECA6E1	none [	- S	-27	15p	-5p	AO	10p	7,98329p	7,98315p	274,7a	15,15
5	C5/Cref	06FBDDE2	none [	<b>→</b> S 🛔	-27	15p	-5p	AO	10p	8,09473p	8,09469p	214,2a	15,51

d. Floating single, internal compensation

Again, the chip sees only the port parasitic capacitance. But due to the different port pattern the correction factors are slightly higher.

#	Name	Results	Filter	fpp	Factor	Offset		Span	Final Result	Mean 50	Std Dev	SNR [bit]
0	CO/Cref	080000C	none 🖵 S	-27	20p	-10p	AO	10p	10p	10p	1,632E-	52,44
1	C1/Cref	08E7E36C	none 🗨 S	-27	20p	-10p	AO	10p	12,2645p	12,2646p	301,6a	15,02
2	C2/Cref	0735B673	none 🗨 S	-27	20p	-10p	AO	10p	8,02454p	8,02458p	252,1a	15,28
	02/06	00000000		07	4	<u>^</u>	100	10-	•	0	0	TE

Using floating in combination with an internal reference there is a deviation as we have internally only a single grounded capacitor. This is measured twice and the factor needs to be doubled.

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### e. Floating, both compensation

Now all parasitic capacitances are compensated. The initial base capacitance without offset can be used.

F	ŧ	Name	Results	Filter	fpp	Factor	Offset		Span	Final Result	Mean 50	Std Dev	SNR [bit]
0	כ	C0/Cref	0800001A	none 🗶 S	-27	10p	0	AO	10p	10p	10p	0	Inf
1	1	C1/Cref	09E81FB7	none 🗨 S	-27	10p	0	AO	10p	12,3834p	12,1831p	1,414p	2,822
2	2	C2/Cref	066773EF	none 🗨 S	-27	10p	0	AO	10p	8,00514p	6,40549p	3,703p	1,433
	•	collesse	00000000		A 97	4	^		10-	0	0	0	Traf

### 4.4 Scaling PDM Output

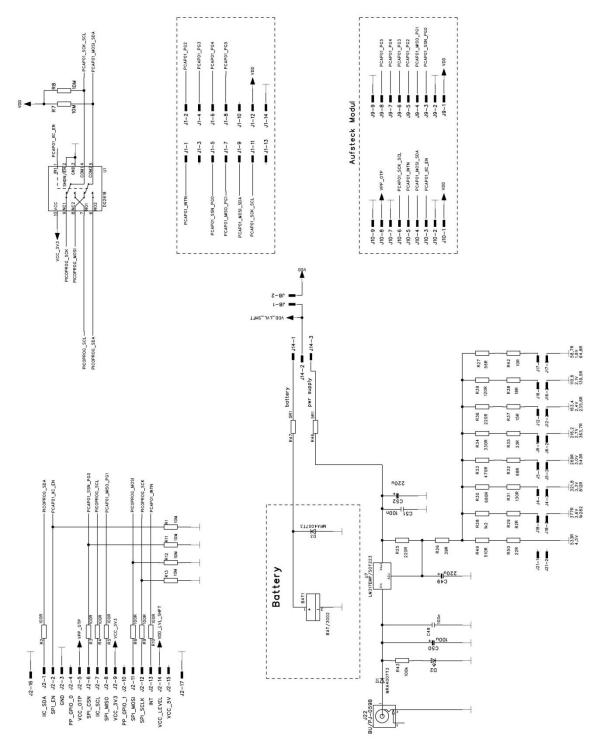
Here we describe how to scale the PDM output when working with the standard firmware. Open the Memory window and select tab calibration:

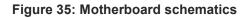
irmw	are Calibration	Misc. Calibr	ation	Comp	lete Men	югу		(
Cali	bration No	o. of Calibrati	on Value	es 8	S	tart Addres	ss d 800	
#	Name	Value	fpp	s/u	Length	Address	Value (hex)	
0	pi0_result0	1,089	27	5	4	800	08B645A2	
1	pi0_result1	1,24	27	5	4	804	09EB851F	
2	pi0_pulse0 (min)	1	0	u	2	808	0001	
3	pi0_pulse1 (max)	1,022k	0	u	2	810	03FE	
4	pi1_result0	900m	27	u	4	812	07333333	
5	pi1_result1	1,1	27	u	4	816	08CCCCCD	
6	pi1_pulse0 (min)	1	0	័ម	2	820	0001	
7	pi1_pulse1 (max)	1,022k	0	u	2	822	03FE	
	Import Linea	is vites serving		Write		Rei		

Set fpp to 27 and s/u to S for signed. Enter the capacitance ratios at minimum and maximum sensor signal. Set pix\_pulse1 (max) to the value according to the set resolution of the PDM. This is 1023 at 10 bit and 65535 at 16 bit.

Press "write" to write the data into the chip.

## 5 Schematics, Layers and BOM





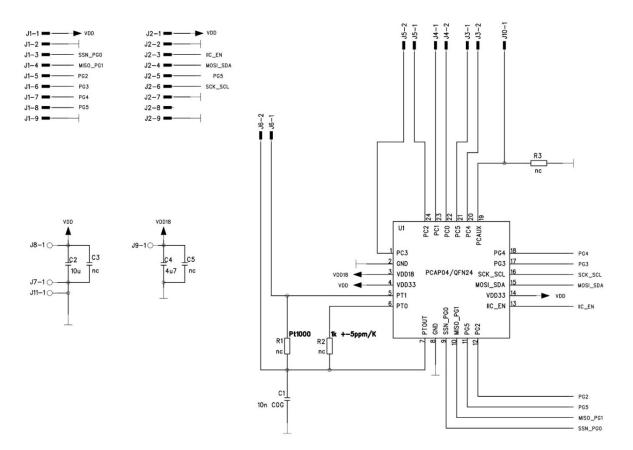


Figure 36: PCa04 AD board schematics

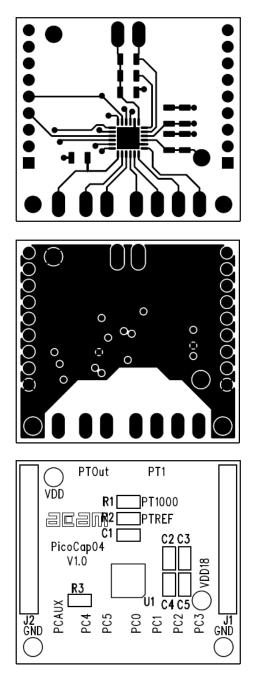
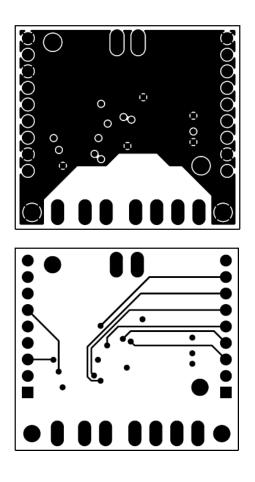


Figure 37: PCa04 AD board layout



ltem	Qty	Reference	Part Name	Description
2	1	C2		C805, 10u
3	1	C4		C805, 4u7
5	1	U1		PCAP04/QFN24
6	3	R1 R2 R3	R805, nc	
4	2	C3 C5	C805, nc	
1	1	C1	C805, nc	CHIP-CAPACITOR

### Bill of Materials for PCap04 plug-in board

am

## 6 Ordering & Contact Information

Ordering Code	Description
PCAP04-EVA-KIT	PCap04 Eval Kit Standard Board
PCAP04-EVA-BOARD	

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### 8 Revision Information

Changes from previous version to current revision 1-02 (2017-Oct-20)	Page
Adding section "4.3 Scaling Results"	42
Adding section "4.4 Scaling PDM Output"	43
Updated screenshots and photos	

**Note:** Page numbers for the previous version may differ from page numbers in the current revision. Correction of typographical errors is not explicitly mentioned.

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