LMC6035/LMC6035-Q1/LMC6036 Low Power 2.7V Single Supply CMOS Operational Amplifiers

Check for Samples: LMC6035, LMC6036

FEATURES

- (Typical Unless Otherwise Noted)
- LMC6035 in DSBGA Package
- Ensured 2.7V, 3V, 5V and 15V Performance
- Specified for 2 kΩ and 600Ω Loads
- Wide Operating Range: 2.0V to 15.5V
- Ultra Low Input Current: 20fA
- Rail-to-Rail Output Swing
  - @ 600Ω: 200mV from Either Rail at 2.7V
  - @ 100kΩ: 5mV from Either Rail at 2.7V
- High Voltage Gain: 126dB
- Wide Input Common-Mode Voltage Range
  - -0.1V to 2.3V at V_S = 2.7V
- Low Distortion: 0.01% at 10kHz
- LMC6035 Dual LMC6036 Quad
- See AN-1112 (Literature Number SNVA009) for DSBGA Considerations
- AEC-Q100 Grade 3 Qualified (LMC6035-Q1)

APPLICATIONS

- Filters
- High Impedance Buffer or Preamplifier
- Battery Powered Electronics
- Medical Instrumentation
- Automotive Applications

DESCRIPTION

The LMC6035/6 is an economical, low voltage op amp capable of rail-to-rail output swing into loads of 600Ω. LMC6035 is available in a chip sized package (8-Bump DSBGA) using micro SMD package technology. Both allow for single supply operation and are ensured for 2.7V, 3V, 5V and 15V supply voltage. The 2.7 supply voltage corresponds to the End-of-Life voltage (0.9V/cell) for three NiCd or NiMH batteries in series, making the LMC6035/6 well suited for portable and rechargeable systems. It also features a well behaved decrease in its specifications at supply voltages below its ensured 2.7V operation. This provides a "comfort zone" for adequate operation at voltages significantly below 2.7V. Its ultra low input currents (I_{IN}) makes it well suited for low power active filter application, because it allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035/6 gives these op amps a broad range of applications for low voltage systems.

Connection Diagram

Top View

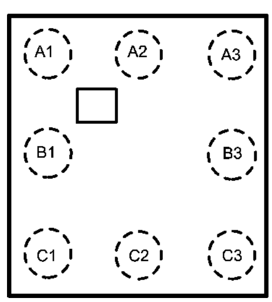

Figure 1. 8-Bump DSBGA Package (Bump Side Down) See Package Number YZR0008

Table 1. DSBGA Connection Table

Bump Number	LM6035IBP LMC6035IBPX	LMC6035ITL LMC6035ITLX
A1	OUTPUT A	OUTPUT B
B1	IN A^-	V^+
C1	IN A^+	OUTPUT A
C2	V^-	IN A^-
C3	IN B^+	IN A^+
B3	IN B^-	V^-
A3	OUTPUT B	IN B^+
A2	V^+	IN B^-

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

ESD Tolerance[3]	Human Body Model (LMC6035, LMC6036)	3000V
	Human Body Model (LMC6035-Q1)	2000V
	Machine Model	300V
Differential Input Voltage		± Supply Voltage
Supply Voltage ($V^+ - V^-$)		16V
Output Short Circuit to V^+		See[4]
Output Short Circuit to V^-		See[5]
Lead Temperature (soldering, 10 sec.)		260°C
Current at Output Pin		±18mA
Current at Input Pin		±5mA
Current at Power Supply Pin		35mA
Storage Temperature Range		−65°C to +150°C
Junction Temperature[6]		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Do not short circuit output to V^+ when V^+ is greater than 13V or reliability will be adversely affected.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 30mA over long term may adversely affect reliability.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board with no air flow.

Operating Ratings[1]

Supply Voltage		2.0V to 15.5V
Temperature Range	LMC6035I and LMC6036I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	8-pin VSSOP	230°C/W
	8-pin SOIC	175°C/W
	14-pin SOIC	127°C/W
	14-pin TSSOP	137°C/W
	8-Bump (6 mil) DSBGA	220°C/W
	8-Bump (12 mil) Thin DSBGA	220°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		LMC6035I/LMC6036I			Units
				Min[1]	Typ[2]	Max[1]	
V_{OS}	Input Offset Voltage				0.5	5 **6**	mV
TCV_{OS}	Input Offset Voltage Average Drift				2.3		μV/°C
I_{IN}	Input Current	See[3]			0.02	**90**	pA
I_{OS}	Input Offset Current	See[3]			0.01	**45**	PA
R_{IN}	Input Resistance				> 10		Tera Ω
CMRR	Common Mode Rejection Ratio	0.7V ≤ V_{CM} ≤ 12.7V, V^+ = 15V		63 **60**	96		dB
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V, V_O = 2.5V		63 **60**	93		dB
−PSRR	Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V, V_O = 2.5V, V^+ = 5V		74 **70**	97		dB
V_{CM}	Input Common-Mode Voltage Range	V^+ = 2.7V For CMRR ≥ 40dB			−0.1	0.3 **0.5**	V
				2.0 **1.7**	2.3		
		V^+ = 3V For CMRR ≥ 40dB			−0.3	0.1 **0.3**	V
				2.3 **2.0**	2.6		
		V^+ = 5V For CMRR ≥ 50dB			−0.5	−0.2 **0.0**	V
				4.2 **3.9**	4.5		
		V^+ = 15V For CMRR ≥ 50dB			−0.5	−0.2 **0.0**	V
				14.0 **13.7**	14.4		
A_V	Large Signal Voltage Gain[4]	R_L = 600Ω	Sourcing	100 **75**	1000		V/mV
			Sinking	25 **20**	250		V/mV
		R_L = 2kΩ	Sourcing		2000		V/mV
			Sinking		500		V/mV

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm or one sigma value.
(3) Ensured by design.
(4) V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		LMC6035I/LMC6036I			Units
				Min (1)	Typ (2)	Max (1)	
V_O	Output Swing	V^+ = 2.7V R_L = 600Ω to 1.35V		2.0 **1.8**	2.5		V
					0.2	0.5 **0.7**	
		V^+ = 2.7V R_L = 2kΩ to 1.35V		2.4 **2.2**	2.62		V
					0.07	0.2 **0.4**	
		V^+ = 15V R_L = 600Ω to 7.5V		13.5 **13.0**	14.5		V
					0.36	1.25 **1.50**	
		V^+ = 15V, R_L = 2 kΩ to 7.5V		14.2 **13.5**	14.8		V
					0.12	0.4 **0.5**	
I_O	Output Current	V_O = 0V	Sourcing	4 **3**	8		mA
		V_O = 2.7V	Sinking	3 **2**	5		
I_S	Supply Current	LMC6035 for Both Amplifiers V_O = 1.35V			0.65	1.6 **1.9**	mA
		LMC6036 for All Four Amplifiers V_O = 1.35V			1.3	2.7 **3.0**	

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ (1)	Units
SR	Slew Rate	See (2)	1.5	V/μs
GBW	Gain Bandwidth Product	V^+ = 15V	1.4	MHz
θ_m	Phase Margin		48	°
G_m	Gain Margin		17	dB
	Amp-to-Amp Isolation	See (3)	130	dB
e_n	Input-Referred Voltage Noise	f = 1kHz V_{CM} = 1V	27	$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise	f = 1kHz	0.2	$fA/\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 10kHz, A_V = −10 R_L = 2kΩ, V_O = 8 V_{PP} V^+ = 10V	0.01	%

(1) Typical Values represent the most likely parametric norm or one sigma value.
(2) V^+ = 15V. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(3) Input referred, V^+ = 15V and R_L = 100kΩ connected to 7.5V. Each amp excited in turn with 1kHz to produce V_O = 12 V_{PP}.

Typical Performance Characteristics

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25°C

Supply Current vs. Supply Voltage (Per Amplifier)

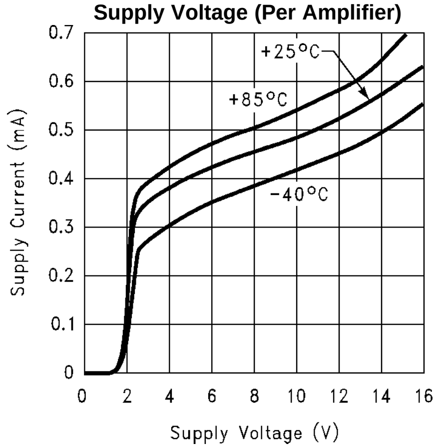

Figure 2.

Input Current vs. Temperature

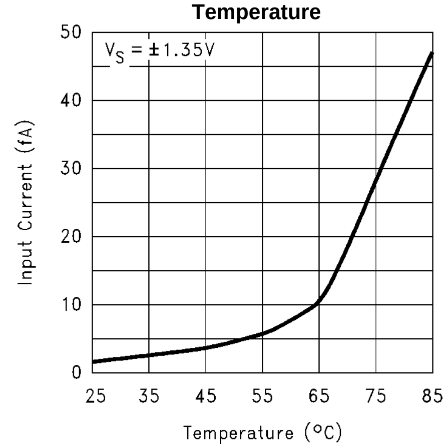

Figure 3.

Sourcing Current vs. Output Voltage

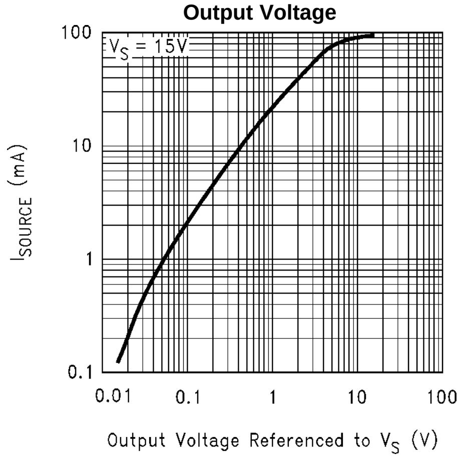

Figure 4.

Sourcing Current vs. Output Voltage

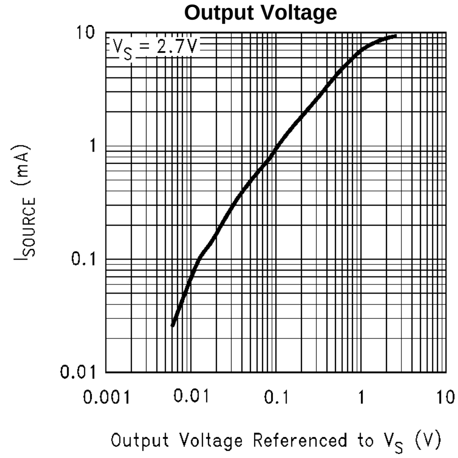

Figure 5.

Sinking Current vs. Output Voltage

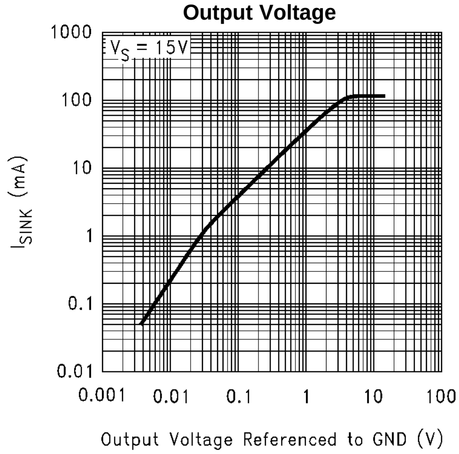

Figure 6.

Sinking Current vs. Output Voltage

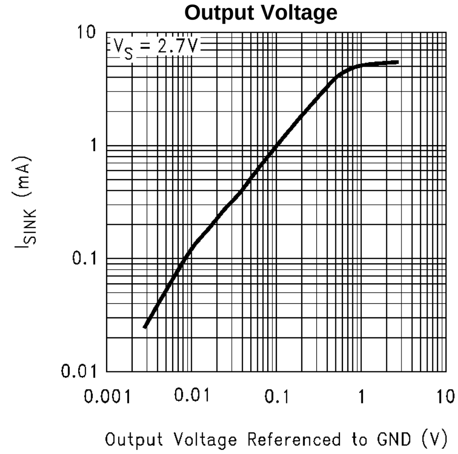

Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25°C

Output Voltage Swing vs. Supply Voltage

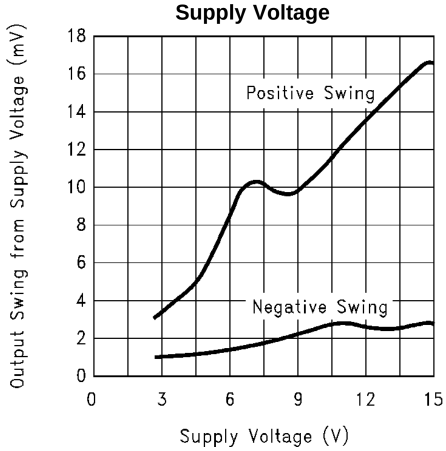

Figure 8.

Input Noise vs. Frequency

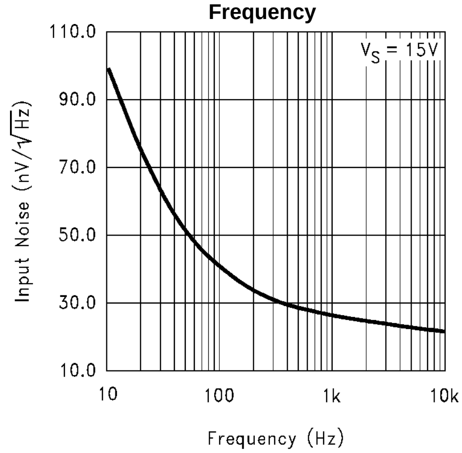

Figure 9.

Input Noise vs. Frequency

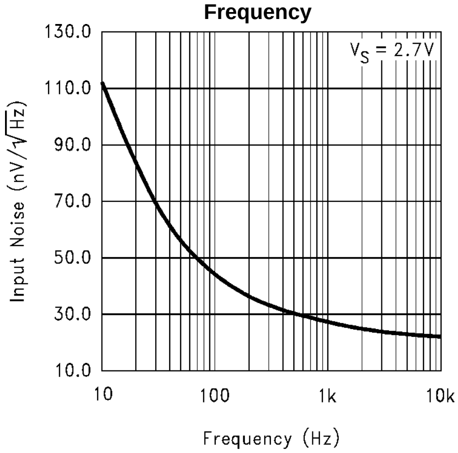

Figure 10.

Amp to Amp Isolation vs. Frequency

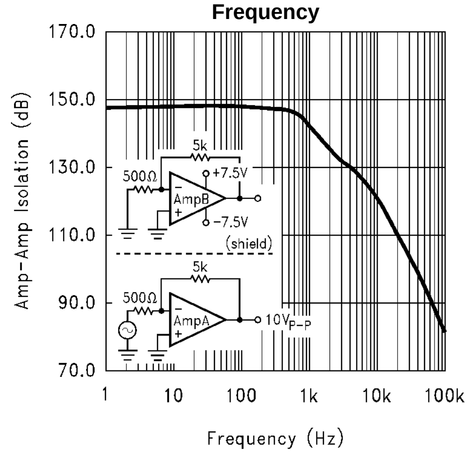

Figure 11.

Amp to Amp Isolation vs. Frequency

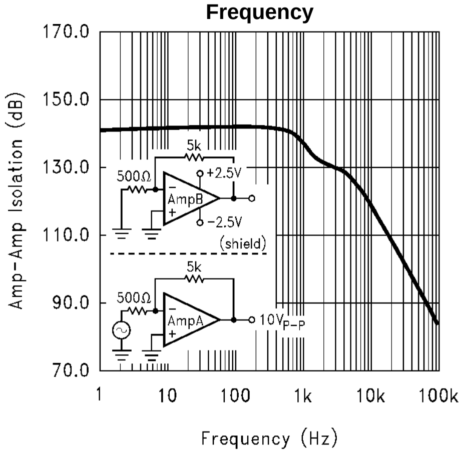

Figure 12.

+PSRR vs. Frequency

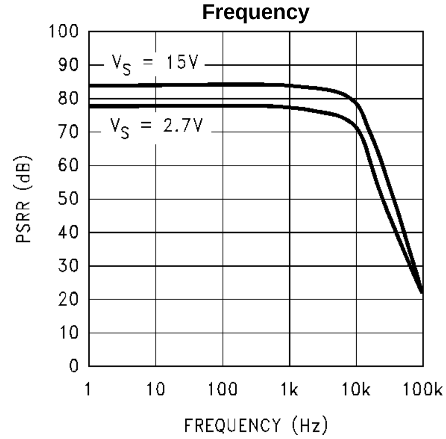

Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25°C

−PSRR vs. Frequency

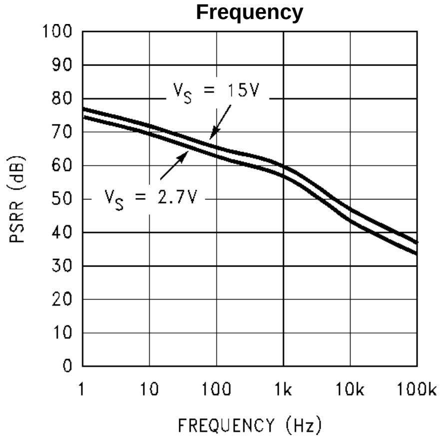

Figure 14.

CMRR vs. Frequency

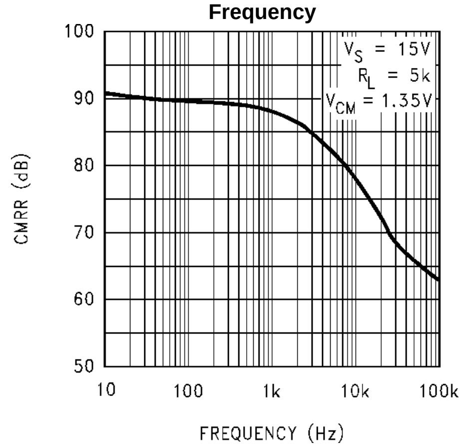

Figure 15.

CMRR vs. Input Voltage

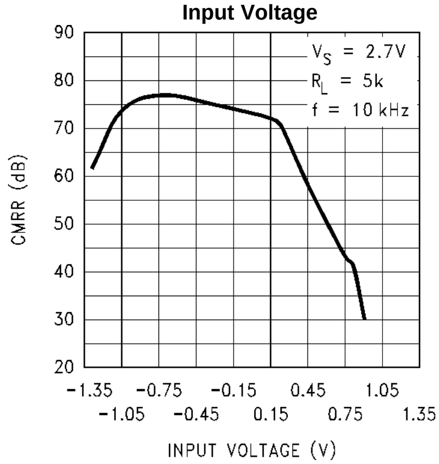

Figure 16.

CMRR vs. Input Voltage

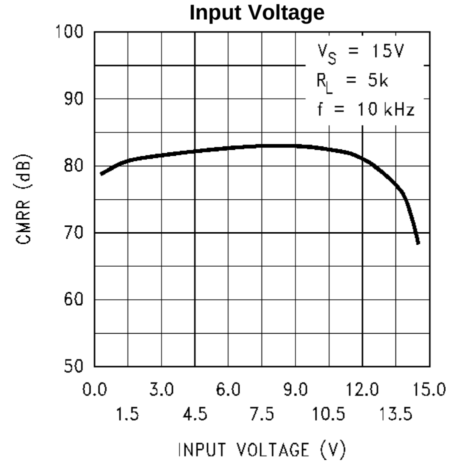

Figure 17.

Input Voltage vs. Output Voltage

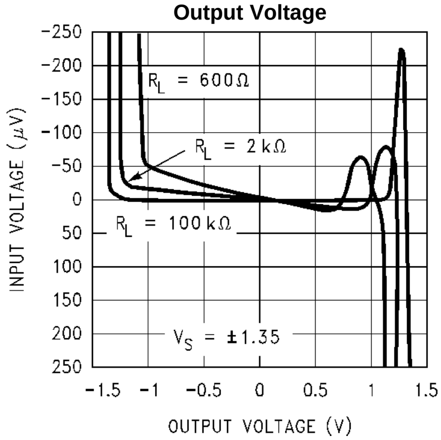

Figure 18.

Input Voltage vs. Output Voltage

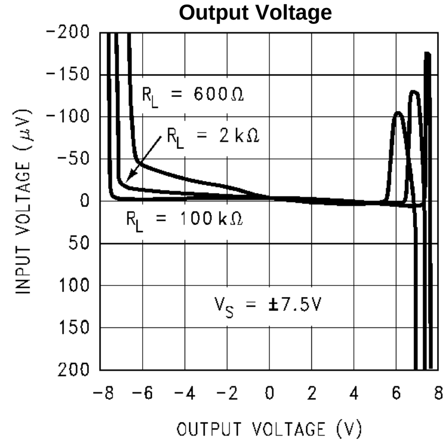

Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25°C

Frequency Response vs. Temperature

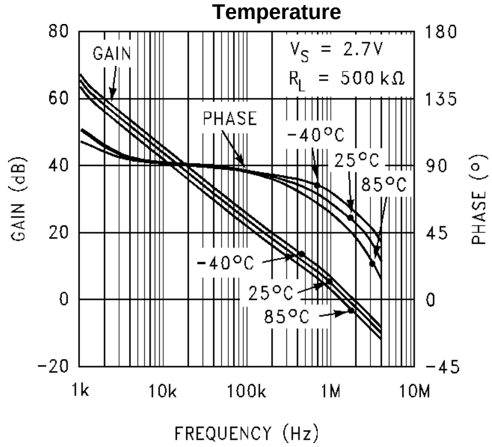

Figure 20.

Frequency Response vs. Temperature

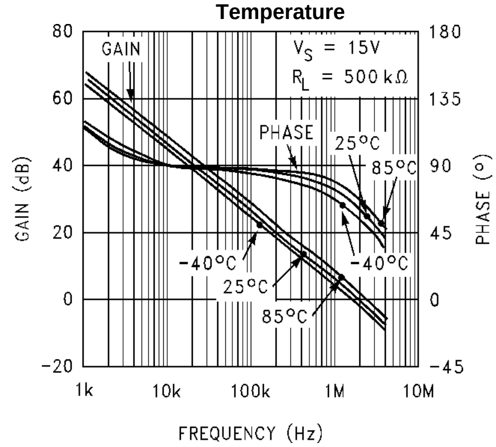

Figure 21.

Gain and Phase vs. Capacitive Load

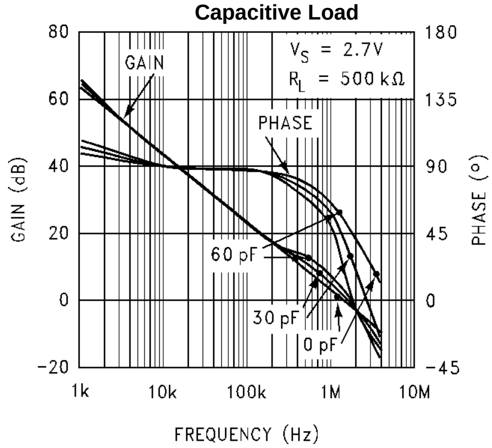

Figure 22.

Gain and Phase vs. Capacitive Load

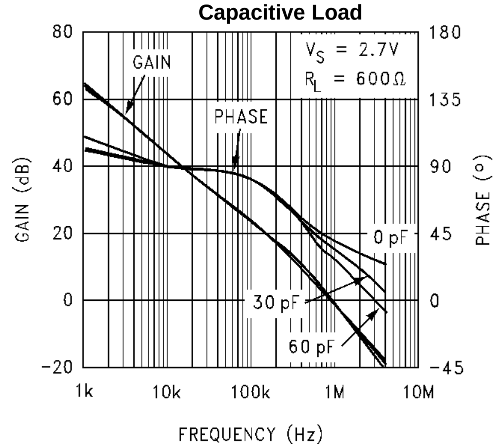

Figure 23.

Slew Rate vs. Supply Voltage

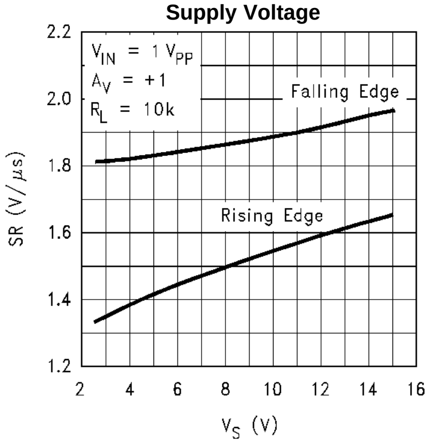

Figure 24.

Non-Inverting Large Signal Response

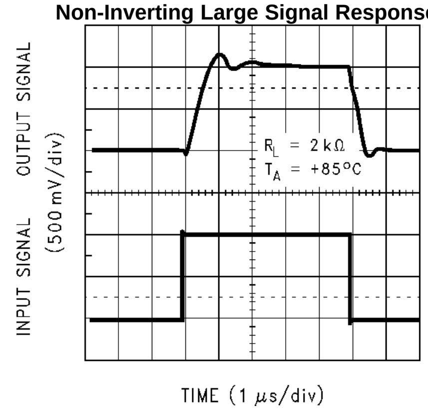

Figure 25.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25°C

Non-Inverting Large Signal Response

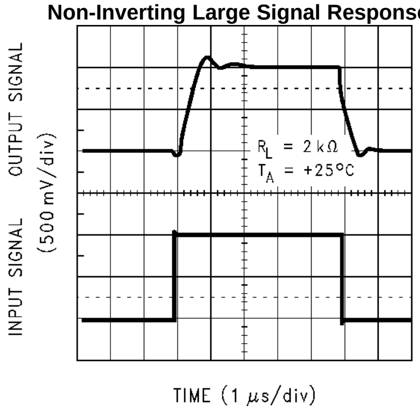

Figure 26.

Non-Inverting Large Signal Response

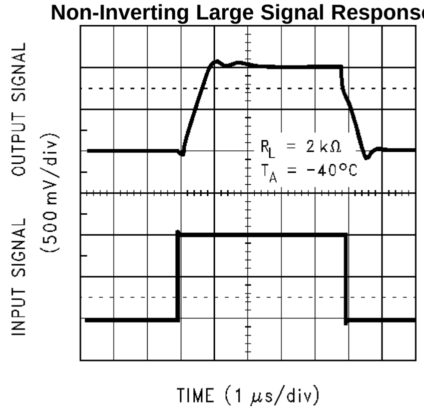

Figure 27.

Non-Inverting Small Signal Response

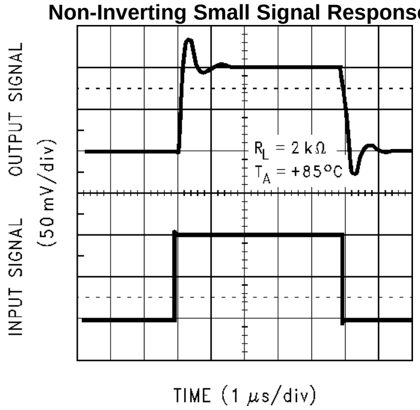

Figure 28.

Non-Inverting Small Signal Response

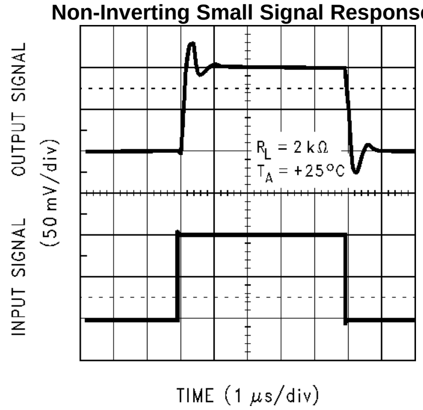

Figure 29.

Non-Inverting Large Signal Response

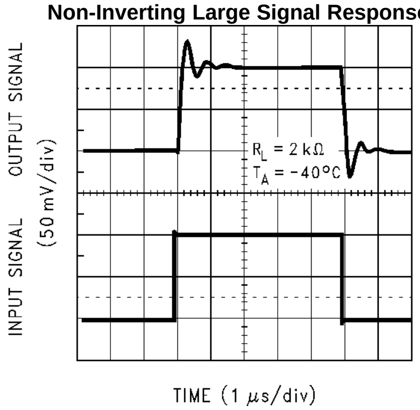

Figure 30.

Inverting Large Signal Response

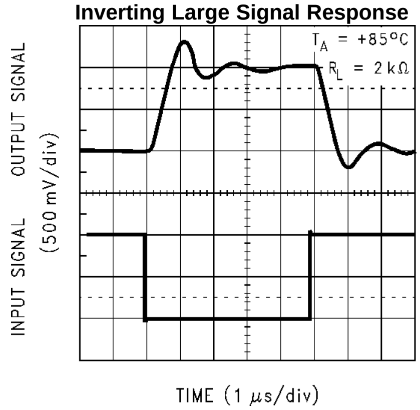

Figure 31.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25°C

Inverting Large Signal Response

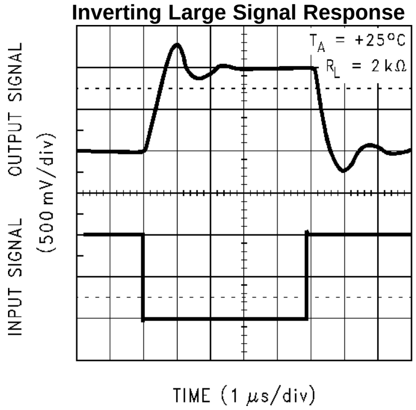

Figure 32.

Inverting Large Signal Response

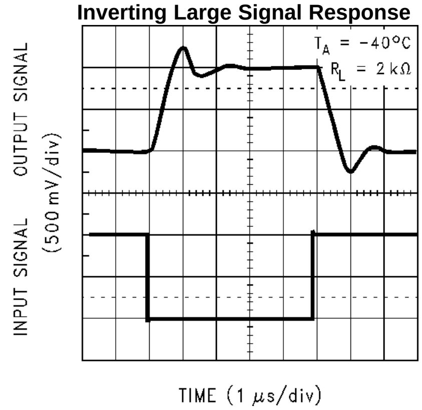

Figure 33.

Inverting Small Signal Response

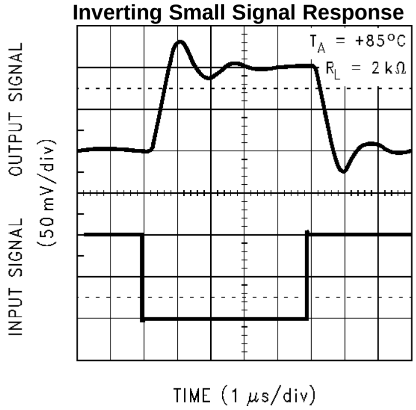

Figure 34.

Inverting Small Signal Response

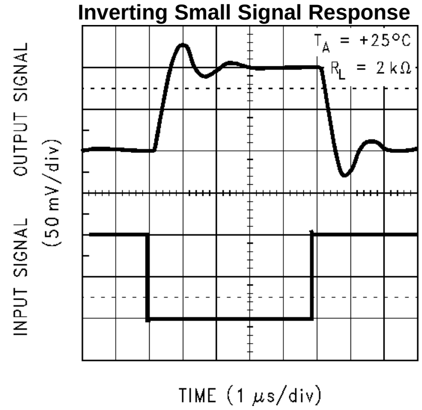

Figure 35.

Inverting Small Signal Response

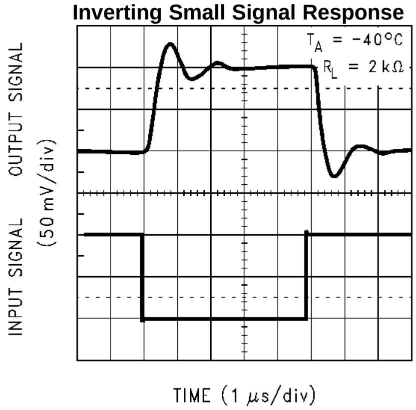

Figure 36.

Stability vs. Capacitive Load

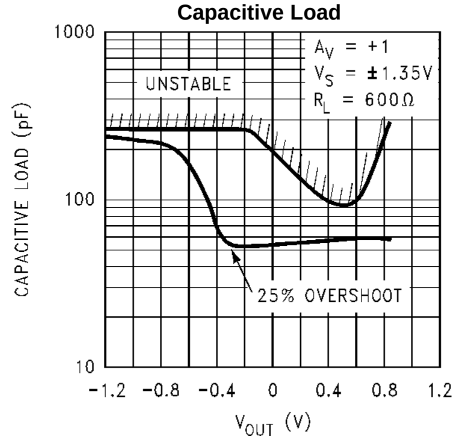

Figure 37.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25°C

Stability vs. Capacitive Load

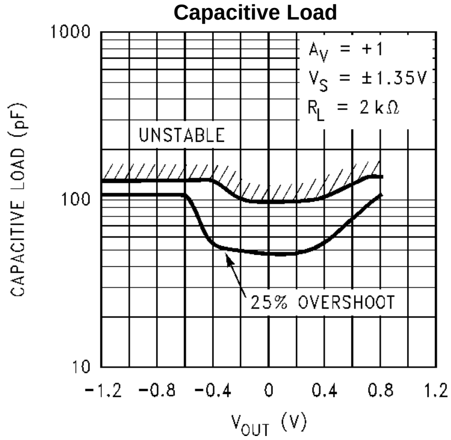

Figure 38.

Stability vs. Capacitive Load

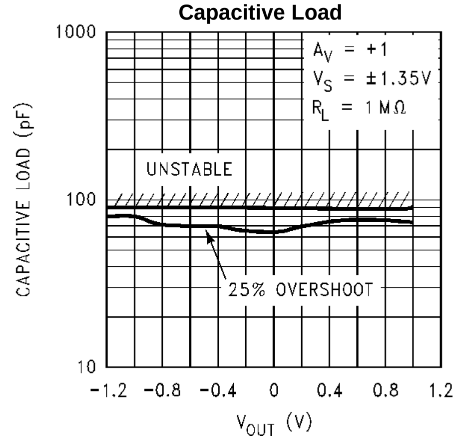

Figure 39.

Stability vs. Capacitive Load

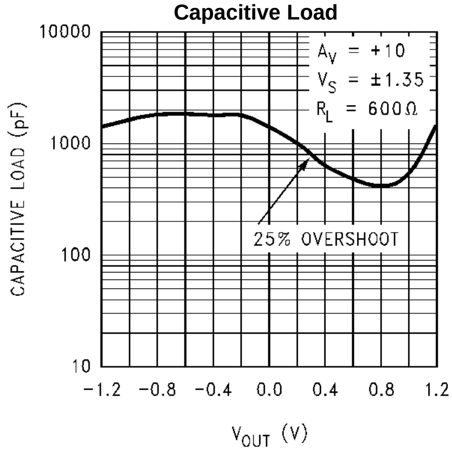

Figure 40.

Stability vs. Capacitive Load

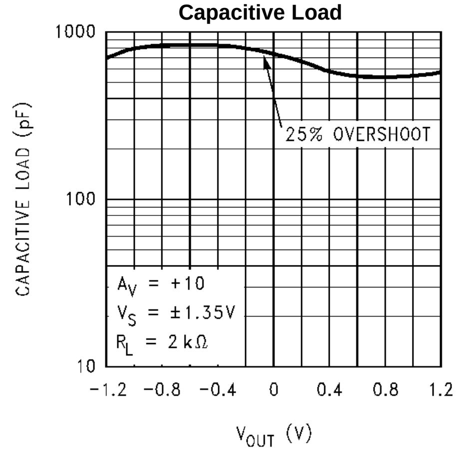

Figure 41.

Stability vs. Capacitive Load

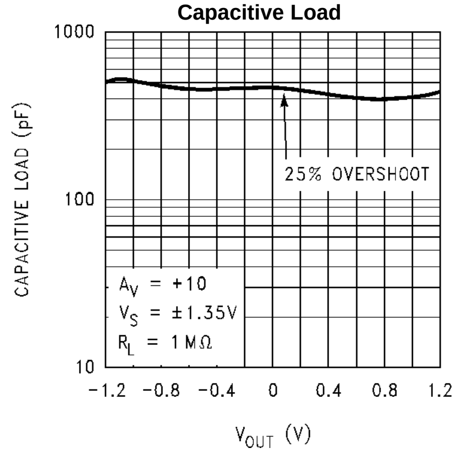

Figure 42.

APPLICATION NOTES

Background

The LMC6035/6 is exceptionally well suited for low voltage applications. A desirable feature that the LMC6035/6 brings to low voltage applications is its output drive capability—a hallmark for TI's CMOS amplifiers. The circuit of Figure 43 illustrates the drive capability of the LMC6035/6 at 3V of supply. It is a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about 600Ω of AC load, at 1 kHz. Capacitor C1 functions to block DC from the low winding resistance of T1. Although the value of C1 is relatively high, its load reactance (Xc) is negligible compared to inductive reactance (X_l) of T1.

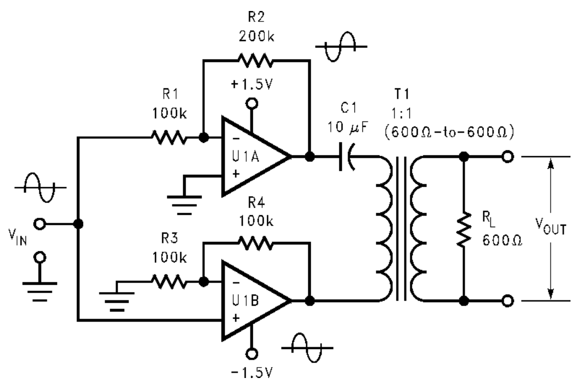

Figure 43. Differential Driver

The circuit in Figure 43 consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of −2, while the U1B amplifies the input with a non-inverting gain of +2. Since the two outputs are 180° out of phase with each other, the gain across the differential output is 4. As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.

How good a CMOS op amp can sink or source a current is an important factor in determining its output swing capability. The output stage of the LMC6035/6—like many op amps—sources and sinks output current through two complementary transistors in series. This “totem pole” arrangement translates to a channel resistance (R_{dson}) at each supply rail which acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails—except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035/6 exhibits exceptional output swing capability under these conditions.

The scope photos of Figure 44 and Figure 45 represent measurements taken directly at the output (relative to GND) of U1A, in Figure 43. Figure 44 illustrates the output swing capability of the LMC6035, while Figure 45 provides a benchmark comparison. (The benchmark op amp is another low voltage (3V) op amp manufactured by one of our reputable competitors.)

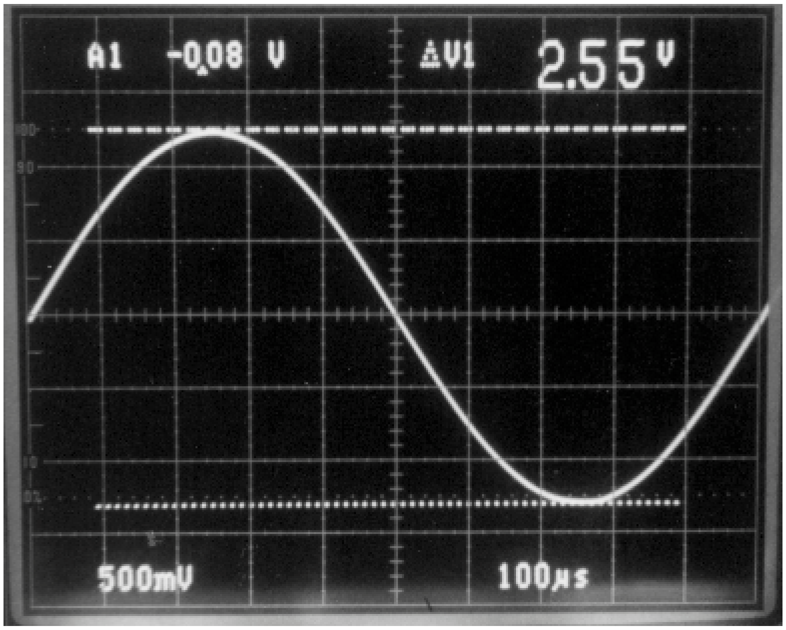

Figure 44. Output Swing Performance of the LMC6035 per the Circuit of Figure 43

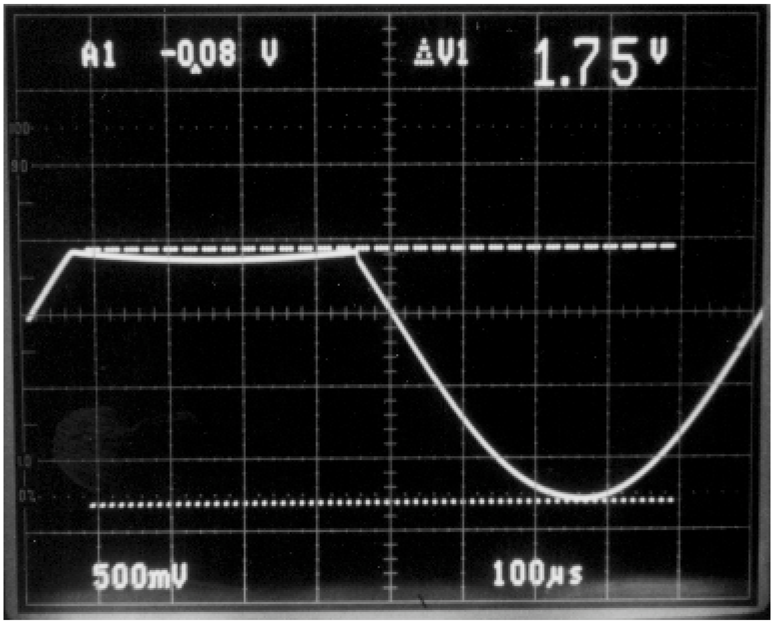

Figure 45. Output Swing Performance of Benchmark Op Amp per the Circuit of Figure 43

Notice the superior drive capability of LMC6035 when compared with the benchmark measurement—even though the benchmark op amp uses twice the supply current.

Not only does the LMC6035/6 provide excellent output swing capability at low supply voltages, it also maintains high open loop gain (A_{VOL}) with heavy loads. To illustrate this, the LMC6035 and the benchmark op amp were compared for their distortion performance in the circuit of Figure 43. The graph of Figure 46 shows this comparison. The y-axis represents percent Total Harmonic Distortion (THD plus noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1 kHz sine wave. (Note that T1 loses about 20% of the voltage to the voltage divider of R_L (600Ω) and T1's winding resistances—a performance deficiency of the transformer.)

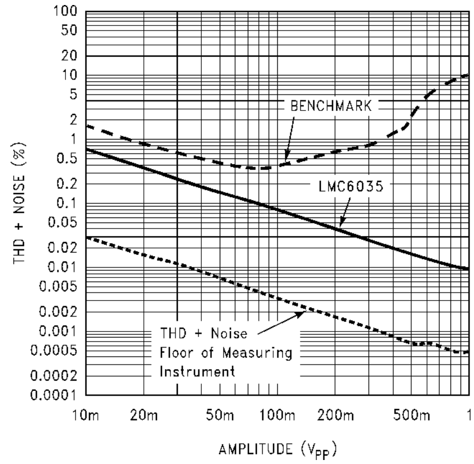

Figure 46. THD+Noise Performance of LMC6035 and "Benchmark" per Circuit of Figure 43

Figure 46 shows the superior distortion performance of LMC6035/6 over that of the benchmark op amp. The heavy loading of the circuit causes the A_{VOL} of the benchmark part to drop significantly which causes increased distortion.

APPLICATION CIRCUITS

Low-Pass Active Filter

A common application for low voltage systems would be active filters, in cordless and cellular phones for example. The ultra low input currents (I_{IN}) of the LMC6035/6 makes it well suited for low power active filter applications, because it allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.

Figure 47 shows a low pass, active filter with a Butterworth (maximally flat) frequency response. Its topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1Hz cutoff frequency, but they can be easily scaled for a desired cutoff frequency (f_c). The bold component values of Figure 47 provide a cutoff frequency of 3kHz. An example of the scaling procedure follows Figure 47.

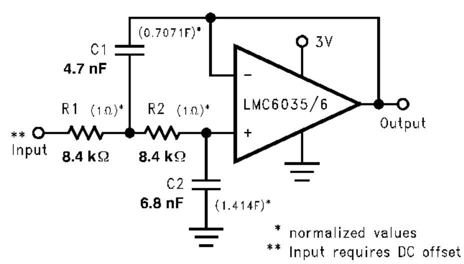

Figure 47. 2-Pole, 3kHz, Active, Sallen and Key, Lowpass Filter with Butterworth Response

Low-Pass Frequency Scaling Procedure

The actual component values represented in bold of Figure 47 were obtained with the following scaling procedure:

1. First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing f_c at 3kHz, provides the following FSF computation:
   – FSF = 2π x 3kHz $_{\text{(desired cutoff freq.)}}$ = 18.84 x 10 ^{3}
2. Then divide all of the normalized capacitor values by the FSF as follows: C1' = $C_{(Normalized)}$/FSF C1' = 0.707/18.84 x 10^3 = 37.93 x 10^{-6} C2' = 1.414/18.84 x 10^3 = 75.05 x 10^{-6} (C1' and C2': prior to impedance scaling)
3. Last, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C2. Then Z can be used to determine the remaining component values as follows:

Z = C2'/$C2_{(chosen)}$ = 75.05 x 10 $^{-6}$/**6.8nF** = 8.4k

C1 = C1'/Z = 37.93 x 10^{-6} /8.4k = 4.52nF

(Standard capacitor value chosen for C1 is **4.7nF**) R1 = $R1_{(normalized)}$ x Z = 1Ω x 8.4k = 8.4kΩ R2 = $R2_{(normalized)}$ x Z = 1Ω x 8.4k = 8.4kΩ

(Standard value chosen for R1 and R2 is **8.45kΩ**)

High Pass Active Filter

The previous low-pass filter circuit of Figure 47 converts to a high-pass active filter per Figure 48.

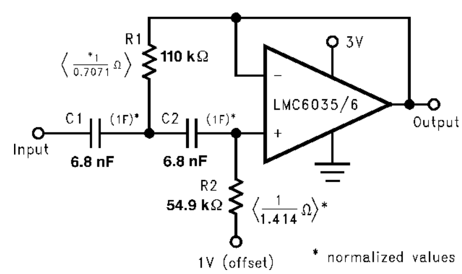

Figure 48. 2 Pole, 300Hz, Sallen and Key, High-Pass Filter

High-Pass Frequency Scaling Procedure

Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency (300Hz) as follows: C = C1 = C2 Z = 1 Farad/$C_{(chosen)}$ x 2π x (desired cutoff freq.) = 1 Farad/**6.8nF** x 2π x 300 Hz = 78.05k

R1 = Z x $R1_{(normalized)}$ = 78.05k x (1/0.707) = 110.4kΩ

(Standard value chosen for R1 is **110kΩ**)

R2 = Z x $R2_{(normalized)}$ = 78.05k x (1/1.414) = 55.2kΩ

(Standard value chosen for R1 is **54.9kΩ**)

Dual Amplifier Bandpass Filter

The dual amplifier bandpass (DABP) filter features the ability to independently adjust f_c and Q. In most other bandpass topologies, the f_c and Q adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and high Qs. The following application of Figure 49, provides a 1kHz center frequency and a Q of 100.

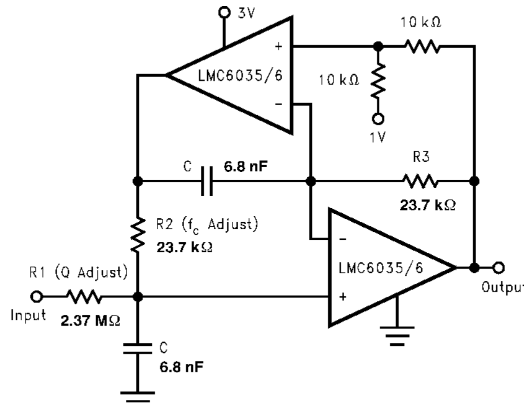

Figure 49. 2 Pole, 1kHz Active, Bandpass Filter

DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:

1. First choose a center frequency (f_c). Figure 49 represents component values that were obtained from the following computation for a center frequency of 1kHz. R2 = R3 = 1/(2 πf $_c$C) Given: f_c = 1kHz and C $_{(chosen)}$ = **6.8nF** R2 = R3 = 1/(2π x 3kHz x 6.8nF) = 23.4kΩ
   – (Chosen standard value is **23.7kΩ**)
2. Then compute R1 for a desired Q (f_c/BW) as follows: R1 = Q x R2. Choosing a Q of 100, R1 = 100 x 23.7kΩ = **2.37MΩ.**

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with < 1000pA of leakage current requires special layout of the PC board. If one wishes to take advantage of the ultra-low bias current of the LMC6035/6, typically < 0.04pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may at times appear acceptably low. Under conditions of high humidity, dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035 or LMC6036 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See Figure 50. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12}Ω, which is normally considered a very large resistance, could leak 5pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the amplifiers actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of 10^{11}Ω would cause only 0.05pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 51(a) through Figure 51(c) for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 51(d).

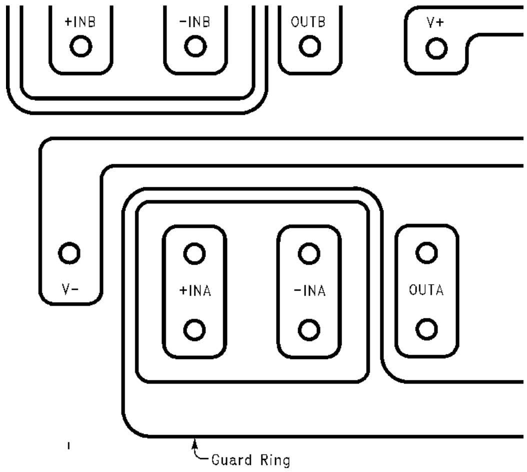

Figure 50. Example, using the LMC6036 of Guard Ring in PC Board Layout

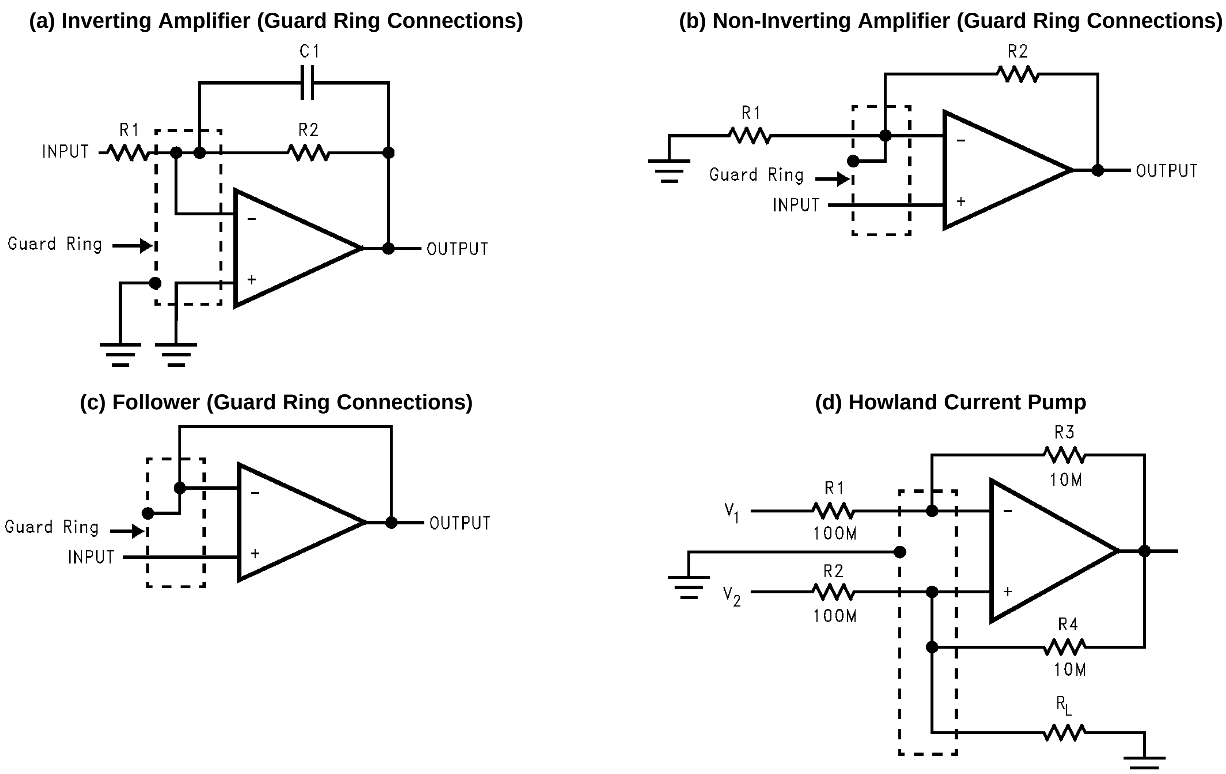

Figure 51. Guard Ring Connections

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6035/6 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 52, the addition of a small resistor (50Ω–100Ω) in series with the op amp's output, and a capacitor (5pF–10pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

DSBGA Considerations

Contrary to what might be guessed, the DSBGA package does not follow the trend of smaller packages having higher thermal resistance. LMC6035 in DSBGA has thermal resistance of 220°C/W compared to 230°C/W in VSSOP. Even when driving a 600Ω load and operating from ±7.5V supplies, the maximum temperature rise will be under 4.5°C. For application information specific to DSBGA, see Application note AN-1112 (Literature Number SNVA009).

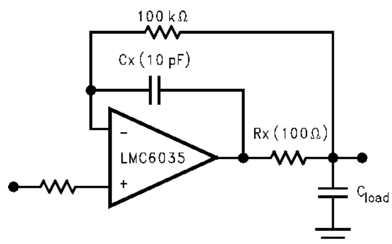

Figure 52. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 53). Typically a pull up resistor conducting 500μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

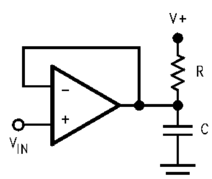

Figure 53. Compensating for Large Capacitive Loads with a Pull Up Resistor

Connection Diagrams

Top View

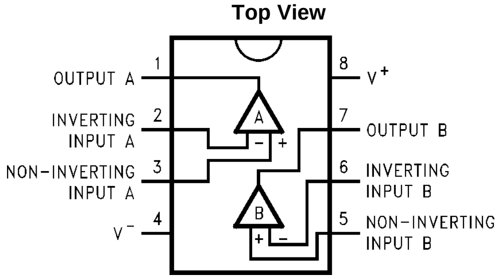

Figure 54. 8-Pin SOIC or VSSOP Package See Package Number D0008A or DGK0008A

Top View

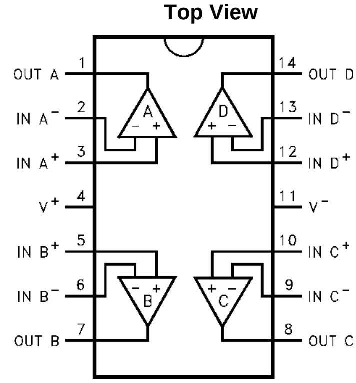

Figure 55. 14-Pin SOIC or TSSOP Package See Package Number D0014A or PW0014A

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6035IM	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LMC60 35IM	Samples
LMC6035IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 35IM	Samples
LMC6035IMM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A06B	Samples
LMC6035IMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A06B	Samples
LMC6035IMMX	ACTIVE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 85	A06B	Samples
LMC6035IMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A06B	Samples
LMC6035IMQ1	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 35IMQ	Samples
LMC6035IMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC60 35IM	Samples
LMC6035IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 35IM	Samples
LMC6035IMXQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 35IMQ	Samples
LMC6035ITL/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 80	Samples
LMC6035ITLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A 80	Samples
LMC6036IM	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMC6036IM	Samples
LMC6036IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6036IM	Samples
LMC6036IMT	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LMC603 6IMT	Samples
LMC6036IMT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC603 6IMT	Samples
LMC6036IMTX	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LMC603 6IMT	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6036IMTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC603 6IMT	Samples
LMC6036IMX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMC6036IM	Samples
LMC6036IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6036IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMC6035, LMC6035-Q1 :

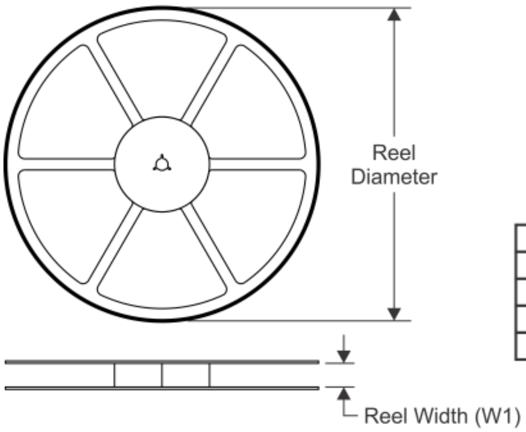
- Catalog: LMC6035
- Automotive: LMC6035-Q1

NOTE: Qualified Version Definitions:

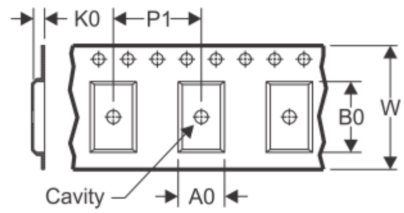
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

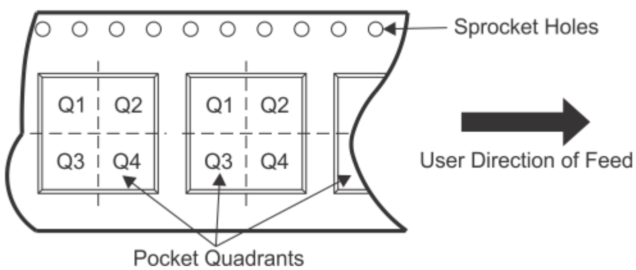


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

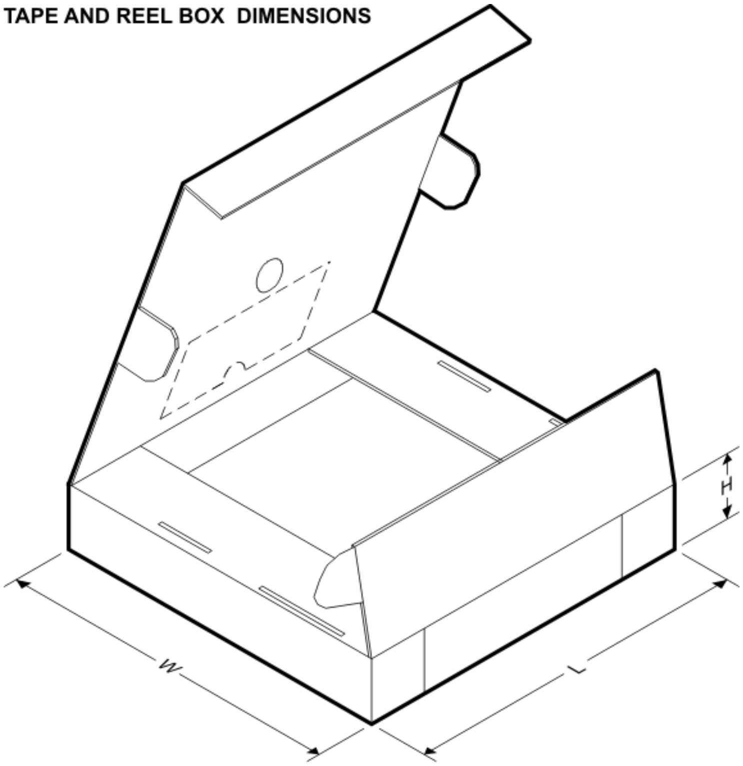
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6035IMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6035IMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6035IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6035IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6035IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6035IMXQ1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6035ITL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LMC6035ITLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LMC6036IMTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMC6036IMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6036IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

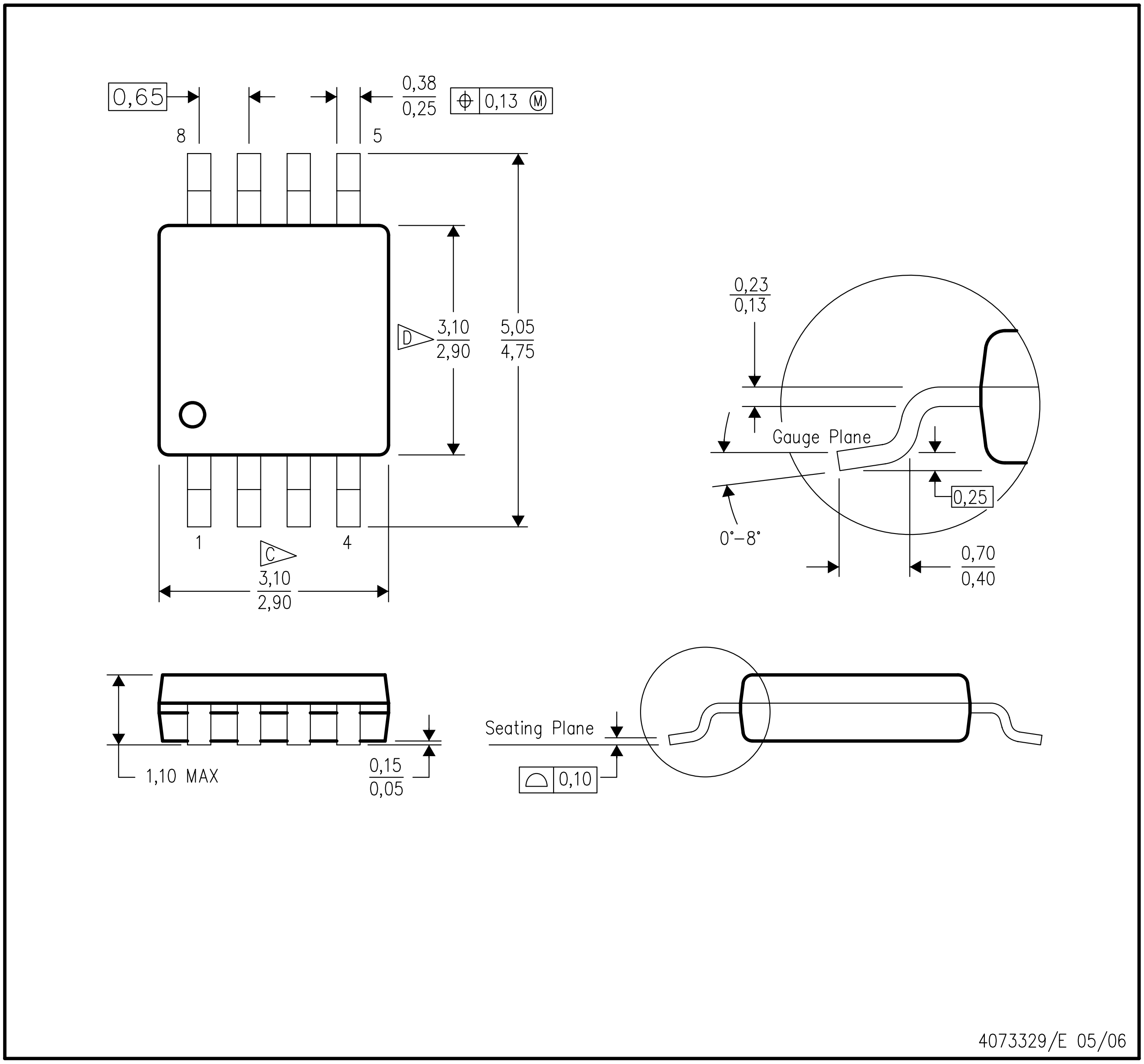
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

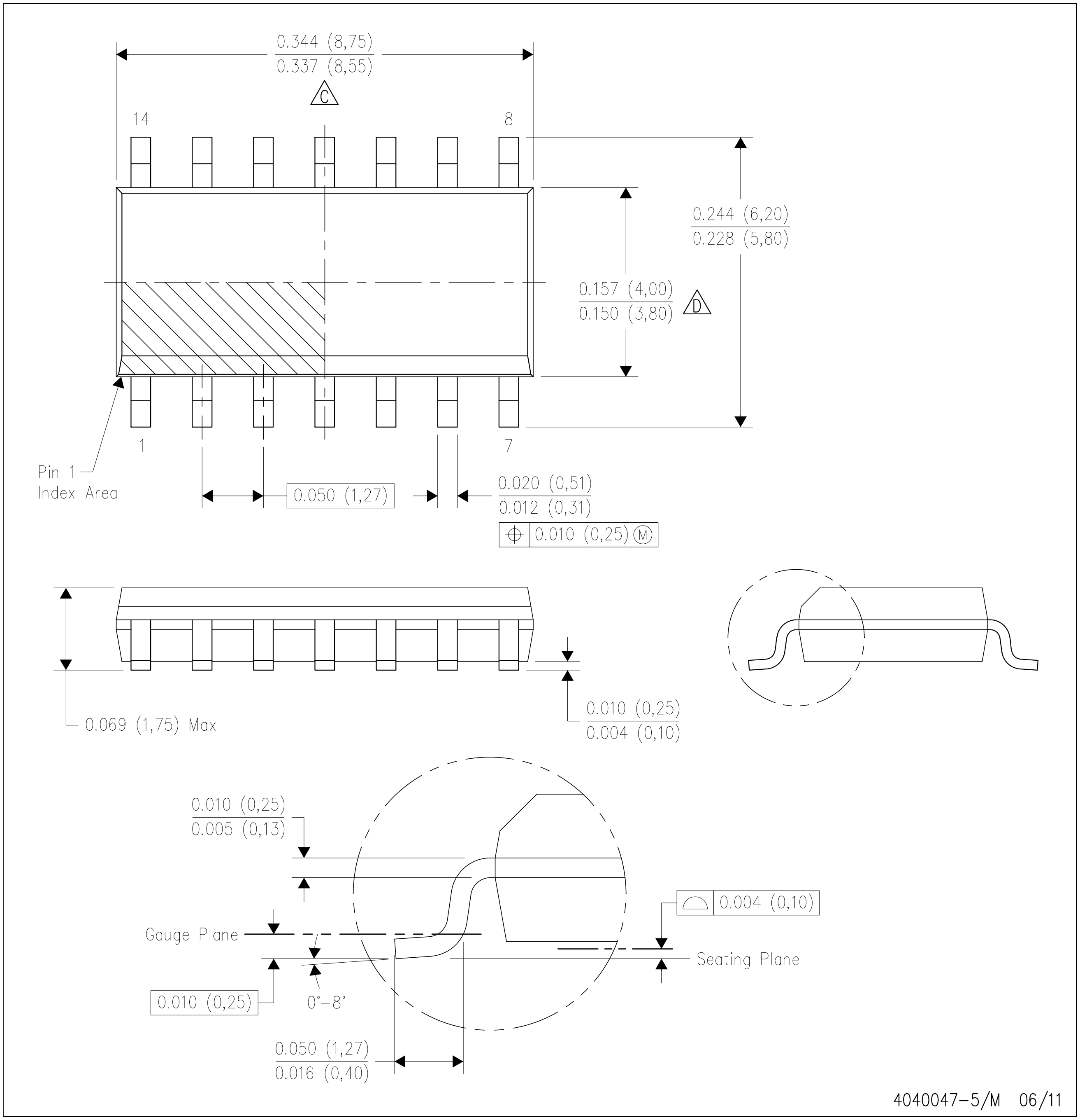
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6035IMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6035IMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6035IMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6035IMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6035IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6035IMXQ1	SOIC	D	8	2500	367.0	367.0	35.0
LMC6035ITL/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LMC6035ITLX/NOPB	DSBGA	YZR	8	3000	210.0	185.0	35.0
LMC6036IMTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMC6036IMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC6036IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



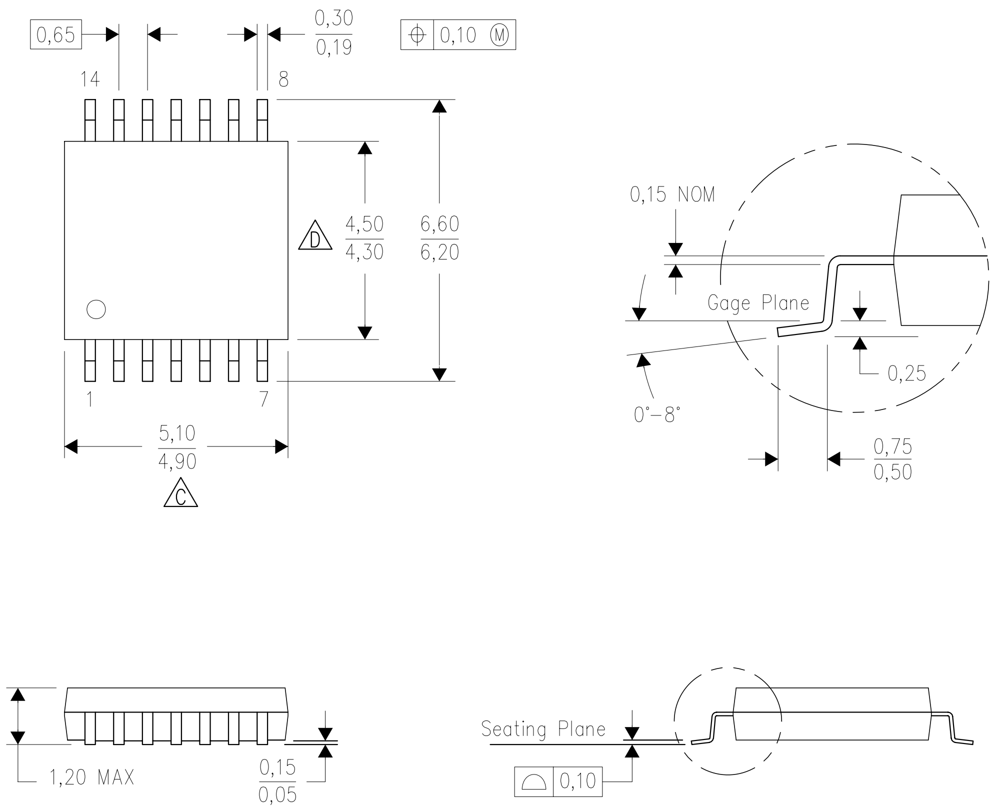
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

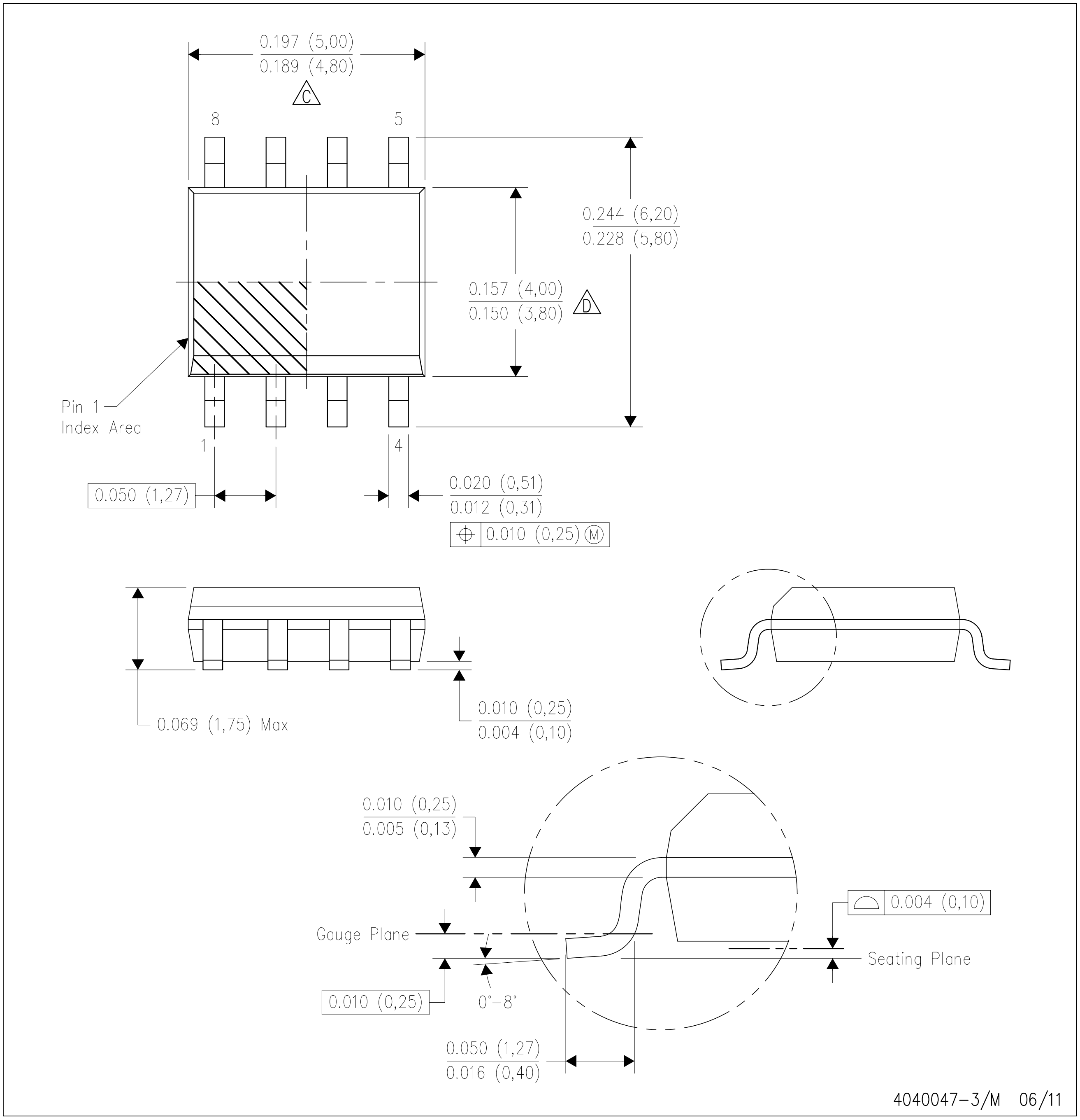
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



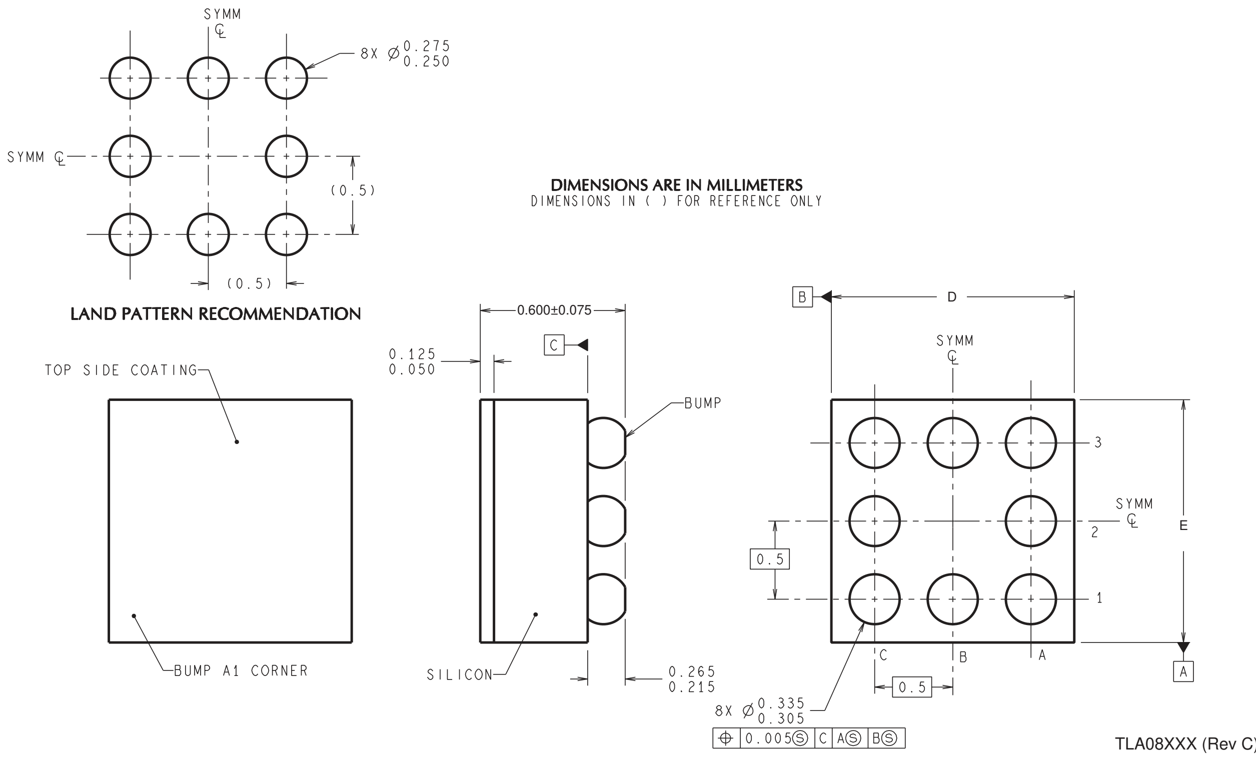
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D: Max = 1.921 mm, Min = 1.86 mm

E: Max = 1.768 mm, Min =1.708 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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