



P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary (Typ.	$@V_{GS} = -4.5V, T_A = +25^{\circ}C)$
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VDSS	RDS(ON)	Qg	Qgd	ID
-12V	65mΩ	2.5nC	0.6nC	-3.3A

Description

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance. making it ideal for high efficiency power management applications.

Applications

- Battery managements
- Load switches
- Battery protections

Features

- LD-MOS Technology with the Lowest Figure of Merit: $R_{DS(ON)} = 65m\Omega$ to Minimize On-State Losses Qg = 2.5nC for Ultra-Fast Switching
- VGS(TH) = -0.6V typ. for a Low Turn-On Potential
- CSP with Footprint 1.0mm × 1.0mm
- Height = 0.62mm for Low Profile
- ESD = 3kV HBM Protection of Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at

https://www.diodes.com/products/automotive/automotiveproducts/.

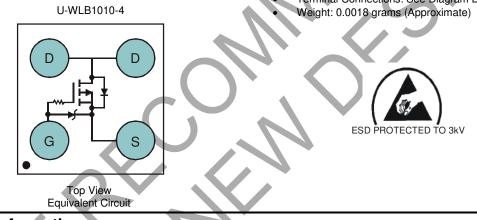
This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.

https://www.diodes.com/quality/product-definitions/

Mechanical Data

Package: U-WLB1010-4

Terminal Connections: See Diagram Below



Ordering Information (Note 4)

Part Number		Package		Packaging			
Part Number	art Number	Fackage	Qty.	Carrier			
DMP1080UCB4-7		U-WLB1010-4	3,000	Tape & Reel			

No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. Notes: 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

Date Code Key	BW = YM = Y = Y	/LB1010-4 BW = Product Type Marking Code YM = Date Code Marking Y = Year (ex: J = 2022) M = Month (ex: 9 = September)										
Year	2011		2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	Y		J	K	L	М	N	0	Р	R	S	Т
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	VDSS	-12	V
Gate-Source Voltage	Vgss	-6	V
Continuous Drain Current (Note 5) V _{GS} = -4.5V	lo	-3.3 -2.7	А
Continuous Drain Current (Note 5) $V_{GS} = -2.5V$	ID	-3.0 -2.4	А
Pulsed Drain Current (Note 6)	ldм	-20	А

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 7)	PD	0.82	W
Thermal Resistance, Junction to Ambient $@T_A = +25^{\circ}C$ (Note 7)	Reja	150	°C/W
Thermal Resistance, Junction to Case $@T_C = +25^{\circ}C$ (Note 7)	Rejc	42.66	°C/W
Power Dissipation (Note 5)	PD	1.59	W
Thermal Resistance, Junction to Ambient $@T_A = +25^{\circ}C$ (Note 5)	Reja	80.29	°C/W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Complexit	Min	Turn	Max	Unit	Test Condition
	Symbol	MIN	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)		10				
Drain-Source Breakdown Voltage	BVDSS	-12	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
Gate-Source Breakdown Voltage	BV _{GSS}	-6.0		—	V	$V_{DS} = 0V, I_G = -250\mu A$
Zero Gate Voltage Drain Current TJ = +25°C	IDSS			-1	μA	$V_{DS} = -9.6V, V_{GS} = 0V$
Gate-Source Leakage	Igss	—	—	-100	nA	$V_{GS} = -6V, \ V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	VGS(TH)	-0.4	-0.6	-1.0	V	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$
			65	80	$V_{GS} = -4.5V, I_D = -500mA$	
Static Drain-Source On-Resistance	RDS(ON)		77	93	mΩ	V _{GS} = -2.5V, I _D = -500mA
			108	130		V _{GS} = -1.5V, I _D = -500mA
Forward Transfer Admittance	Y _{fs}	_	4	_	S	$V_{DS} = -6V, I_{D} = -500mA$
Diode Forward Voltage	Vsd		-0.6	-1.0	V	$V_{GS} = 0V, I_{S} = -500mA$
Reverse Recovery Charge	QRR	—	2.0	—	nC	$V_{dd} = -4.0V, I_F = -0.5A,$
Reverse Recovery Time	trr	—	9.5	—	ns	di/dt = 100A/µs
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	Ciss	_	213	350		
Output Capacitance	Coss	—	119	250	pF	$V_{DS} = -6V$, $V_{GS} = 0V$, f = 1.0MHz
Reverse Transfer Capacitance	Crss	_	54.4	90		
Total Gate Charge	Qg	—	2.5	5		
Gate-Source Charge	Qgs		0.3	_	nC	$V_{GS} = -4.5V, V_{DS} = -6V,$
Gate-Drain Charge	Qgd		0.6	_	nC	I _D = -500mA
Gate Charge at Vth	Q _g (th)		0.15	_		
Turn-On Delay Time	tD(ON)	_	16.7	—		
Turn-On Rise Time	tR		20.6	_	I	VDS = -6V, VGS = -2.5V,
Turn-Off Delay Time	t _{D(OFF)}		38.4	_	ns	$R_{G} = 20\Omega, I_{D} = -500 \text{mA}$
Turn-Off Fall Time	tF	_	28.4	—		

Notes: 5. Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

6. Repetitive rating, pulse width limited by junction temperature.

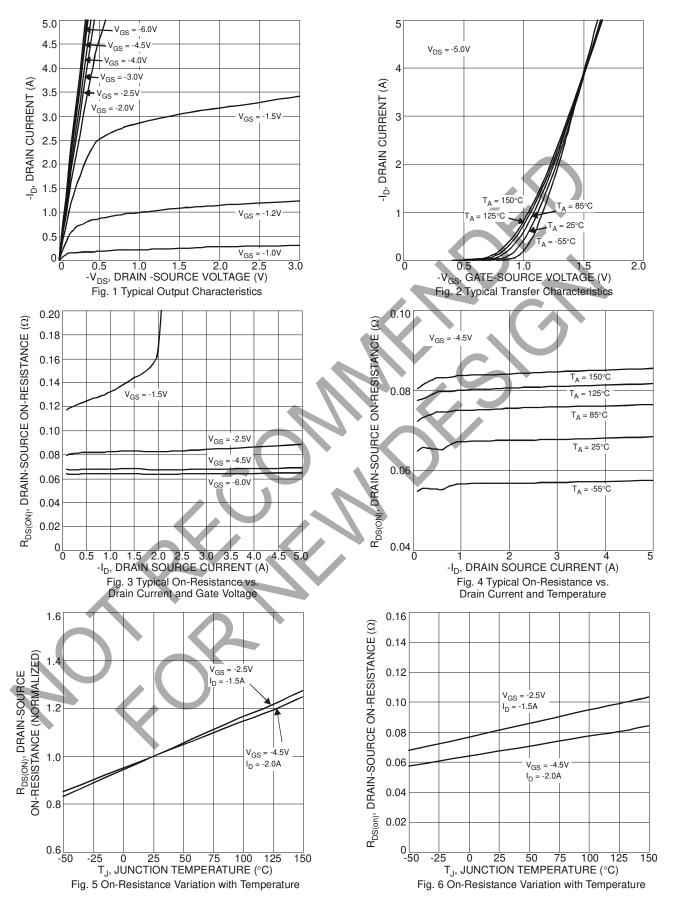
7. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.

8. Short duration pulse test used to minimize self-heating effect.

9. Guaranteed by design. Not subject to production testing.

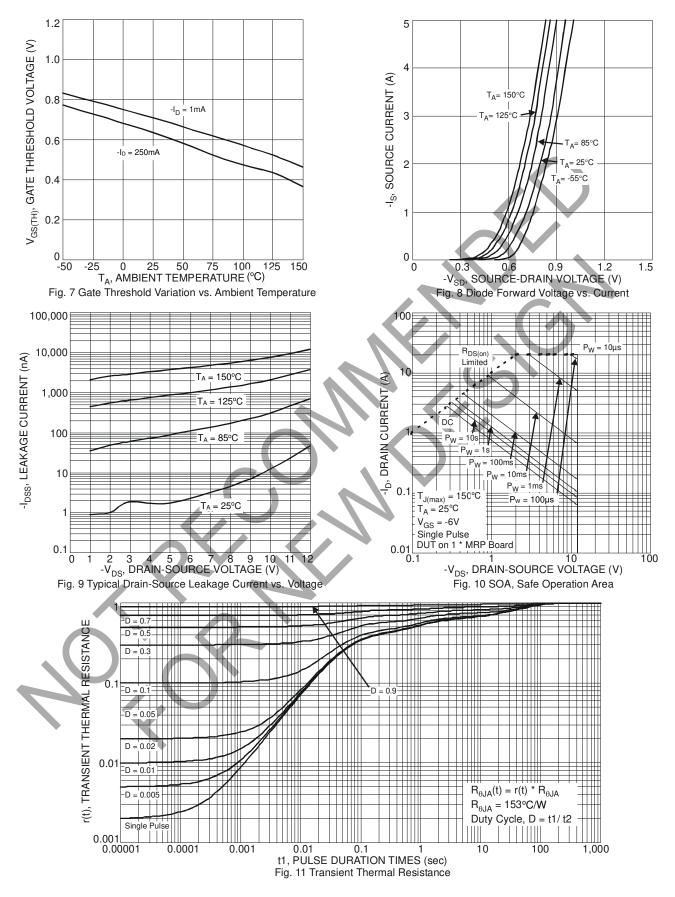


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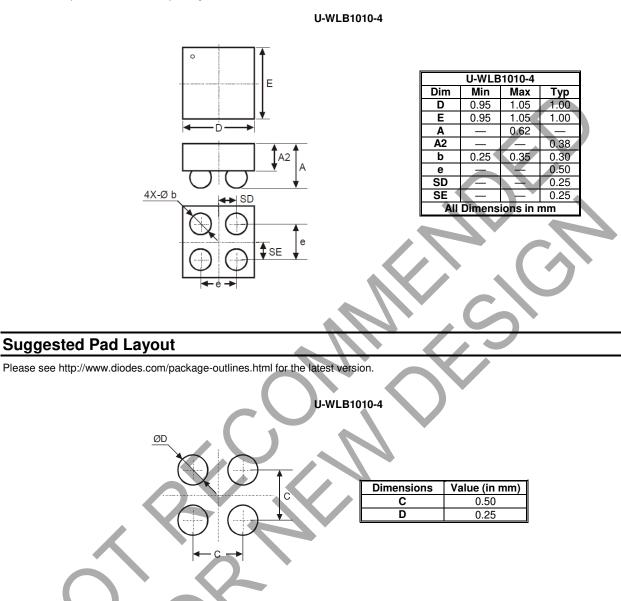
DMP1080UCB4





Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.





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