75 V/2 A Peak, Low Cost, High Frequency Half Bridge Driver

DESCRIPTION

SiP41111 is the MOSFET driver, which is designed to simplify the converter design for the topologies, which requires the high-side switch such as half bridge, two switch forward and active clamping forward. The high-side and low-side drivers can be configured to meet different driving requirement for these topologies because the high-side and low side drivers are independent controlled. The built-in bootstrap diode eliminates the external diode to improve the flexibility PCB layout. The V_{DD} undervoltage lockout prevents the abnormal operation.

FEATURES

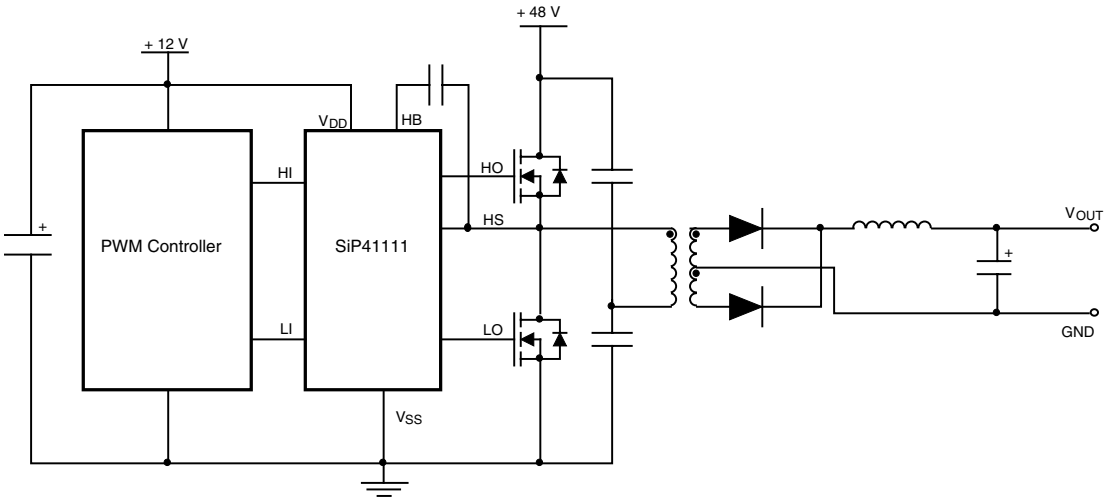
- Drives N-Channel MOSFET Half Bridge Topology
- SOIC, SOIC (PowerPAK®) Package Options
- Lead (Pb)-free Product Available (RoHS Compliant)
- Bootstrap Supply Maximum Voltage to 75 VDC
- Built-In Bootstrap Diode
- Fast Propagation Times Meet High Frequency Converter Circuits
- Drives 1000 pF Load with Rise and Fall Times Typical 15 ns to meet 400 kHz typical Switching Requirement
- Independent Driver Channel for Two Switch Forward and Active Clamp Forward Topologies
- Low Power Consumption
- Supply Under Voltage Lockout
- 2.0 A Peak Sink and Source Gate Driver Current

Pb-free
RoHS COMPLIANT

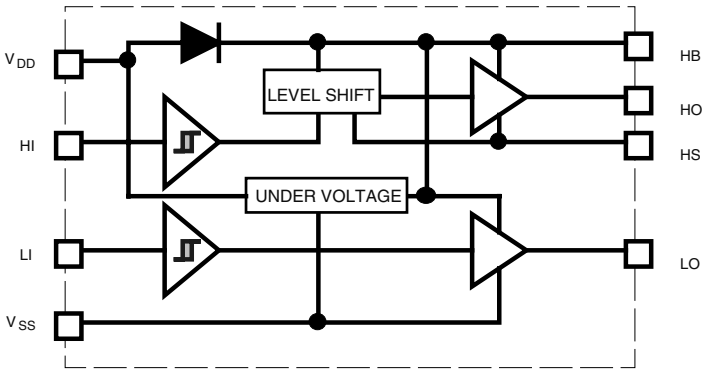
APPLICATIONS

- Half Bridge Converter
- Two-Switch Forward Converters
- Active Clamp Forward Converters
- Bus Converters
- Motor Control

TYPICAL APPLICATION CIRCUIT



BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Supply Voltage, V_{DD}, V_{HB}-V_{HS}[a]		- 0.3 to 14	V
LI and HI Voltage[a]		- 0.3 to V_{DD} + 0.3	
Voltage on LO[a]		- 0.3 to V_{DD} + 0.3	
Voltage on HO[a]		V_{HS} - 0.3 to V_{HB} + 0.3	
Voltage on HS[a]	Continuous	- 1 to + 89	
Voltage on HB[a]	V_{DD} = 12 V	+ 89	
Average Current in V_{DD} to HB diode		100	mA
ESD Classification	Class 1	1	kV

THERMAL INFORMATION

Parameter		Limit	Unit
Thermal Resistance (Typical) θJA	SOIC[b]	153	°C/W
	SOIC (PowerPak)[b]	40	
Max Power Dissipation	at 70 °C in Free Air (SOIC)[c]	522	mW
	at 70 °C in Free Air (SOIC PowerPAK)[d]	2.0	W
Junction Temperature Range		- 65 to 150	°C
Storage Temperature Range		- 55 to 150	

Notes:
a. All voltages are referenced to ground unless otherwise specified.
b. Device mounted with all leads soldered or welded to PC board.
c. Derate 6.5 mW/°C above + 70 °C.
d. Derate 25 mW/°C above + 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

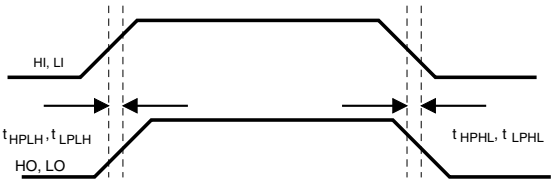
Parameter		Limit	Unit
Supply Voltage	V_{DD}	+ 9 to 13.2	V
Voltage on HS		- 1 to 75	
Voltage on HB		V_{HS} + 8 to V_{HS} + 13.2 and V_{DD} - 1 to V_{DD} + 75	

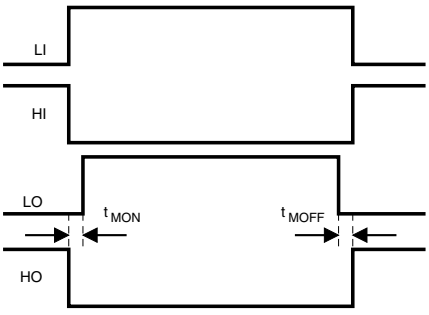
ELECTRICAL SPECIFICATIONS $V_{DD} = V_{HB} = 12$ V, $V_{SS} = V_{HS} = 0$ V, no load on LO or HO, unless otherwise specified

Parameter	Symbol	Test Conditions	T_J = 25 °C			T_J = 40 °C to 125 °C		Unit
			Min	Typ	Max	Min	Max	
Supply Currents								
V_{DD} Quiescent Current	I_{DD}	LI = HI = 0 V	-	0.18	0.24	-	0.27	mA
V_{DD} Operating Current	I_{DDO}	f = 500 kHz	-	1.7	2.5	-	3	
Total HB Quiescent Current	I_{HB}	LI = HI = 0 V	-	0.02	0.10	-	0.15	
Total HB Operating Current	I_{HBO}	f = 500 kHz	-	1.5	2.5	-	3	
HB to V_{SS} Quiescent Current	I_{HBS}	$V_{HS} = V_{HB} = 89$ V	-	7	12	-	15	µA
HB to V_{SS} Operating Current	I_{HBSO}	f = 500 kHz	-	0.6	-	-	-	mA
Input Pins								
Low Level Input Voltage Thresold	V_{IL}		4	4.5	-	3	-	V
High Level Input Voltage Threshold	V_{IH}		-	5.5	7	-	8	
Input Voltage Hysteresis	V_{IHYS}		-	1.0	-	-	-	
Input Pulldown Resistance	R_I		-	300	-	100	600	kΩ
Supply Undervoltage Protection								
V_{DD} Rising Threshold	V_{DDR}		6.6	7.1	7.6	6.4	7.8	V
V_{DD} Threshold Hysteresis	V_{DDH}		-	1.3	-	-	-	
Bootstrap Diode								
Low-Current Forward Drop Out Voltage	V_{DL}	$I_{VDD-HB} = 100$ µA	-	1.25	1.4	-	1.8	V
High-Current Forward Drop Out Voltage	V_{DH}	$I_{VDD-HB} = 100$ mA	-	1.8	2.0	-	2.2	
Dynamic Resistance	R_D	$I_{VDD-HB} = 100$ mA	-	1.5	-	-	-	Ω
LO Gate Driver								
Low Level Output Voltage	V_{OLL}	$I_{LO} = 100$ mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHL}	I_{LO} - 100 mA, $V_{OHL} = V_{DD} - V_{LO}$	-	0.25	0.3	-	0.4	
Peak Sourcing Current	I_{OHL}	$V_{LO} = 0$ V	-	2	-	-	-	A
Peak Sinking Current	I_{OLL}	$V_{LO} = 12$ V	-	2	-	-	-	
HO Gate Driver								
Low Level Output Voltage	V_{OLH}	$I_{HO} = 100$ mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHH}	$I_{HO} = -100$ mA $V_{OHH} = V_{HB} - V_{HO}$	-	0.25	0.3	-	0.4	V
Peak Sourcing Current	I_{OHH}	$V_{HO} = 0$ V	-	2	-	-	-	A
Peak Sinking Current	I_{OLH}	$V_{HO} = 12$ V	-	2	-	-	-	A

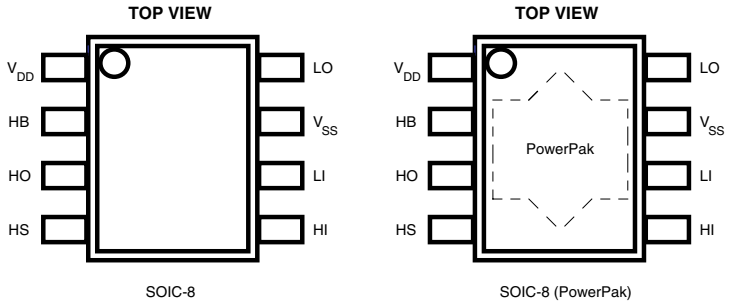
ELECTRICAL SPECIFICATIONS $V_{DD} = V_{HB} = 12$ V, $V_{SS} = V_{HS} = 0$ V, no load on LO or HO, unless otherwise specified						
			$T_J = 25$ °C			
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	18	-	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	18	-	
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	23	-	
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	23	-	
Delay Matching: Lower Turn-On and Upper Turn-Off	t_{MON}		-	5.5	-	
Delay Matching: Lower Turn-Off and Upper Turn-On	t_{MOFF}		-	6.5	-	
Low-side Output Rise Time	t_{RCL}	C_L = 1000 pF	-	14	-	
High-side Output Rise Time	t_{RCH}		-	13	-	
Low-side Output Fall Time	t_{FCL}		-	15	-	
High-side Output Fall Time	t_{FCH}		-	15	-	
Either Output Rise Time Driving DMOS	t_{RD}	C_L = Si7456DP C_{iss} = 3100 pF	-	27	-	
Either Output Fall Time Driving DMOS	t_{FD}	C_L = Si7456DP C_{iss} = 3100 pF	-	30	-	
Minimum Input Pulse Width that Changes the Output	t_{PW}		-	-	65	
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	

TIMING DIAGRAMS





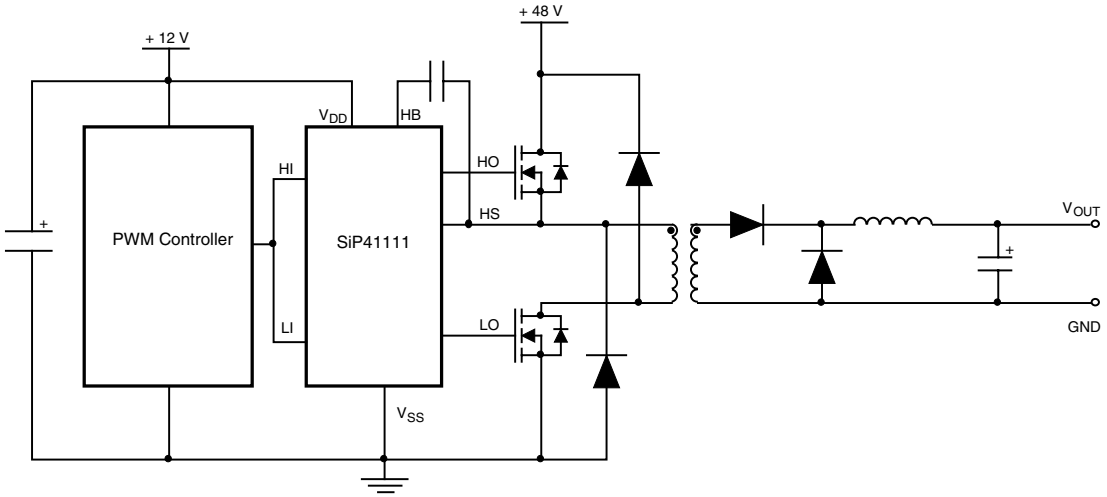
PIN CONFIGURATION



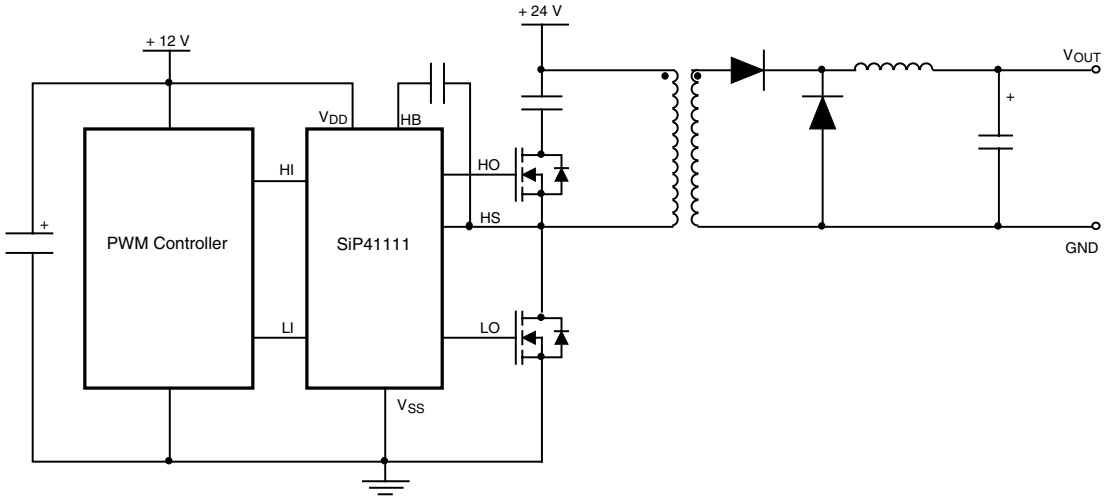
PIN DESCRIPTIONS	
Symbol	**Descriptions**
V_{DD}	Input power supply to IC and lower gate drivers
HB	Floating boostrap supply for the upper MOSFET. External bootstrap capacitor is required
HO	Output drive for upper MOSFET. Connect to gate of upper power MOSFET
HS	Floating GND for the upper MOSFET. Connect to source of upper power MOSFET
HI	Input for upper drive
LI	Input for lower drive
V_{SS}	Ground supply
LO	Output drive for lower MOSFET. Connect to gate of lower power MOSFET
PowerPAK	Exposed PowerPAK is for heat dissipation. Exposed PowerPAK is floating or grounded. The PowerPad is not guaranteed electrically isolated from all other pins

ORDERING INFORMATION			
Part Number	**Marking**	**Temperature Range**	**Package**
SiP41111DY-T1-E3	41111	- 40 to 85 °C	SOIC-8
SiP41111DYP-T1-E3	41111	- 40 to 85 °C	SOIC-8 PowerPAK

TYPICAL APPLICATION CIRCUITS

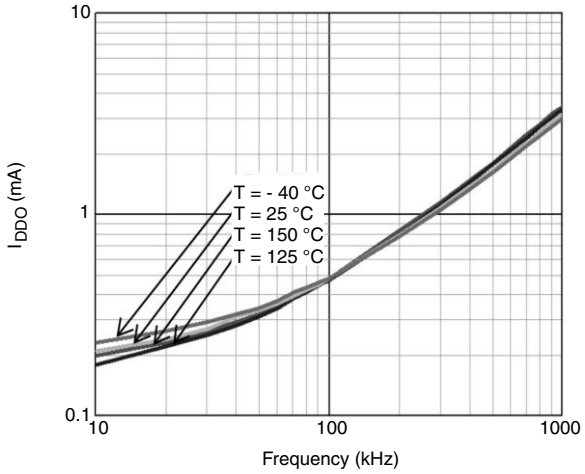


Two Switch Forward Application Circuit

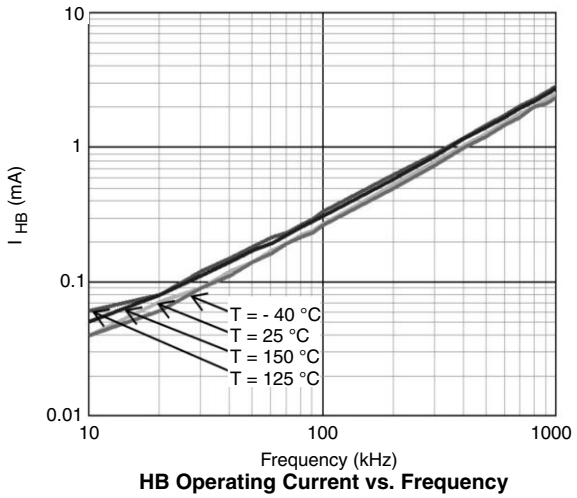


Active Clamp Forward Application Circuit

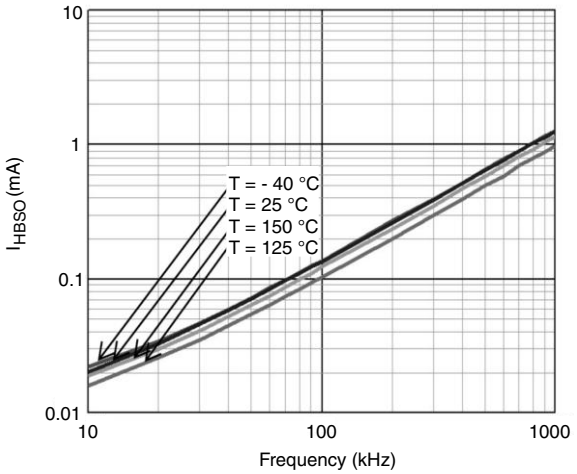
TYPICAL CHARACTERISTICS



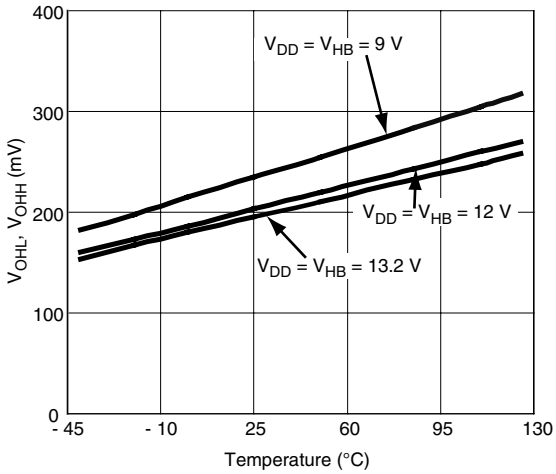
Operating Current vs. Frequency



HB Operating Current vs. Frequency

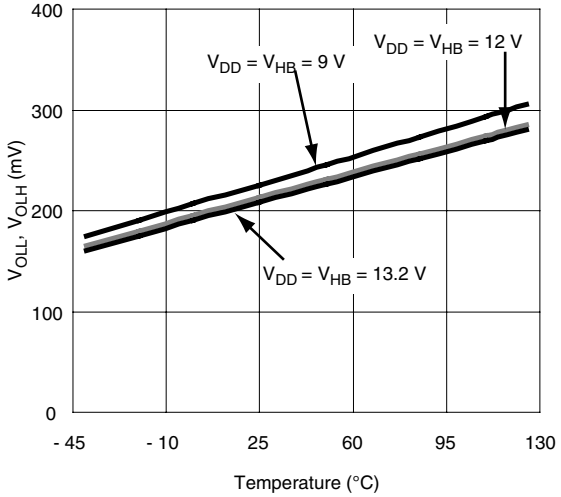


HB to V_{ss} Operating Current vs. Frequency

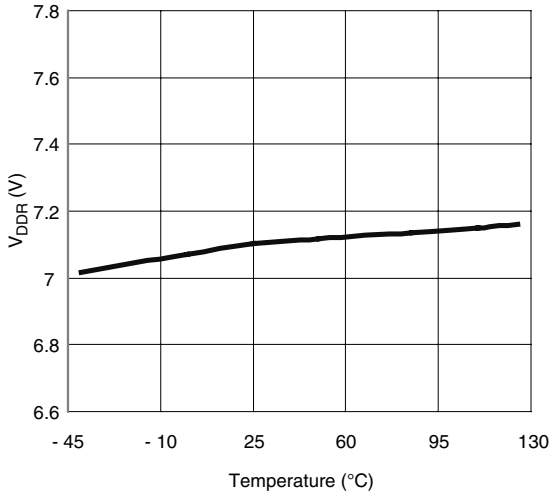


High Level Output Voltage vs. Temperature

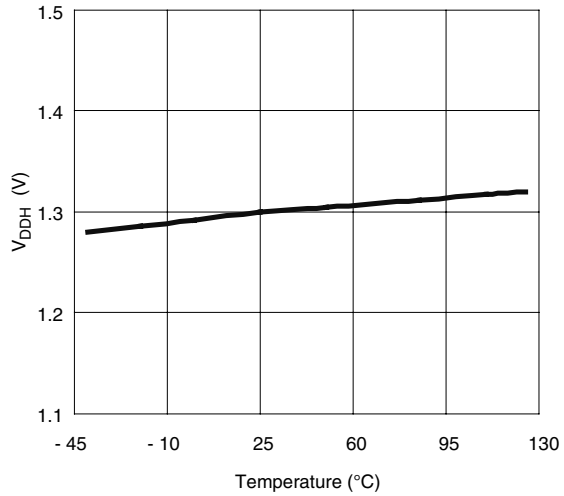
TYPICAL CHARACTERISTICS



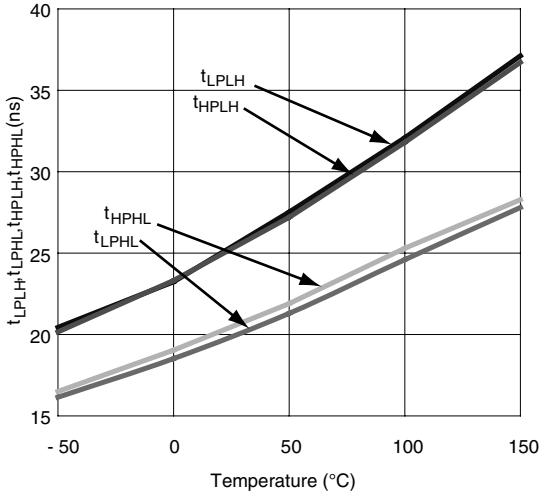
Low Level Output Voltage vs. Temperature



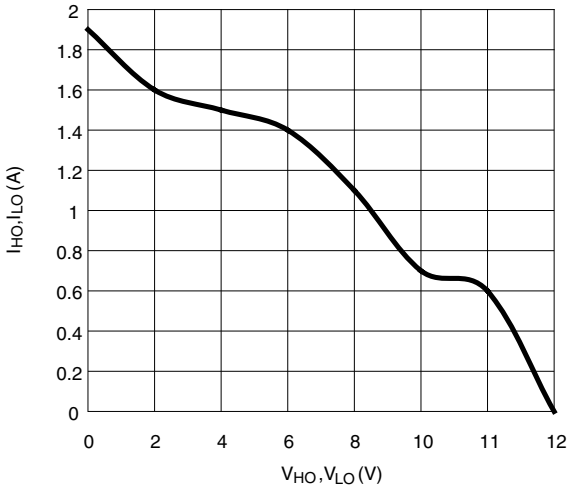
Undervoltage Lockout Threshold vs. Temperature



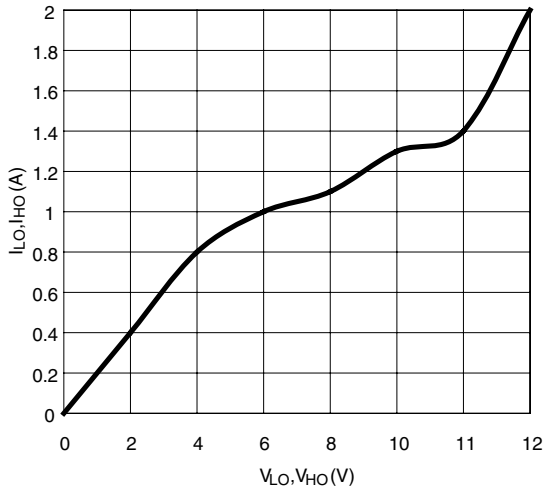
Undervoltage Lockout Hysteresis vs. Temperature



Propagation Delay vs. Temperature

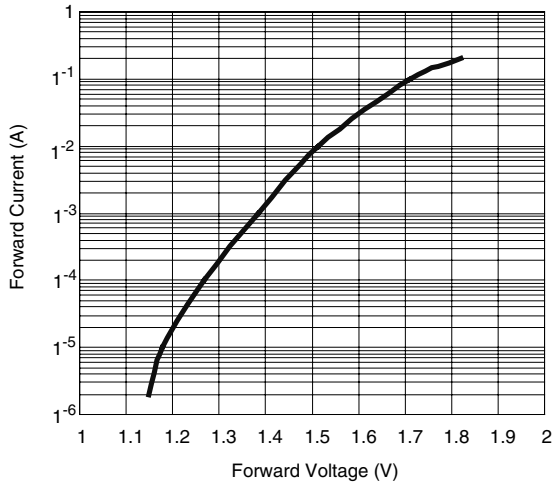


Peak Source Current vs. Output Voltage

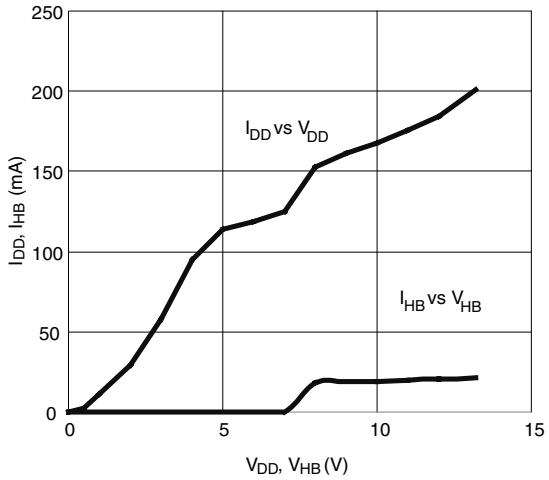


Peak Sink Current vs. Output Voltage

TYPICAL CHARACTERISTICS



Bootstrap Diode I-V Characteristics



Quiescent Current vs. Voltage

DETAIL DESCRIPTION

The SiP41111 IC is the high-speed 2 A half bridge MOSFET drivers, which operating between 9 V to 13.2 V. The drivers are designed to drive the upper MOSFET switch directly without any isolation devices for half bridge topology and other topologies, which require the upper switch MOSFET.

The thermally enhanced PowerPak SOIC package can dissipate more heat to meet the aggressive 400 kHz switching frequency while driving 1000 pf total gate capacitance MOSFET with typical 15 ns rise and fall time.

Bootstrap Supply Operation

The power to drive the high-side MOSFET gate comesfrom the external bootstrap capacitor. This capacitor charges through built-in diode during the time when the low-side MOSFET is on (HS is at GND potential), and then provides the necessary charge to turn on the high-side MOSFET.

Bootstrap Capacitor Selection

The capacitance of bootstrap capacitor should be carefully selected to avoid the unexpected oscillations at HO pin. The typical capacitance value for the bootstrap capacitor should be at least 0.1 uf to 1 uf or at least 20 time of the total gate capacitance of MOSFET. The energy in the bootstrap capacitor should large enough to supply the driving current for the upper MOSFET during the on time of the upper MOSFET without significant voltage drop on the bootstrap capacitor. Low ESR ceramic capacitor is recommended for this application.

Built-in Bootstrap Diode

A built-in bootstrap diode eliminates the external discrete diode to improve flexibility of PCB layout in field application. The bootstrap diode is connected between Pin V_{DD} and HB. The diode is used to charge up the external bootstrap capacitor while the lower MOSFET is on, and isolated V_{DD} while the lower MOSFET is off. The voltage rating of the built-in diode is 89 V. This voltage rating enables the half bridge and two switch forward design for 48 V input converter and 24 V input active clamp forward converter. The typical forward drop out voltage is 1.8 V and the reverse time is 10 ns to meet 400 kHz-switching requirement.

Under Voltage Lockout Function

The SiP41111 has an internal under-voltage lockout feature to prevent driving the MOSFET gates when the supply voltage (at V_{DD}) is less than the under-voltage lockout specification (V_{DDR}). This prevents the output MOSFET from being turned on without sufficient gate voltage to ensure they are fully on.

Thermal Consideration

The thermal issue of the IC cannot be ignored because the driver IC is the power conversion device. The IC can generate unexpected amount of heat to have high temperature if the thermal issue is not carefully considered at begin of the system level design. The additional heat sink for the IC will increase the cost of materials. The best solution to settle the thermal issue to improve the reliability of the system design is to increase the trace copper area as much as possible for heat dissipation. The PCB traces are not only for electrical connection. It is also used for heat dissipation.

The PowerPAK SOIC package is designed to meet the higher ambient environment operation. A heat dissipation pad is built under the body of the SOIC package. Availability of heat dissipation pad under the body of the package doesn't means the thermal issue can be ignored because the PowerPAK is designed to mount the body of the package on the PCB trace for heat dissipation. The PowerPAK cannot dissipate enough heat to provide a cool environment for the IC because the surface area of PowerPAK is small. Large trace area is the best way to control the temperature of the IC in the high ambient environment.

Layout Consideration

Careful PCB layout design is absolutely necessary for any high frequency switching device to avoid circuit function and EMI issues. The following guideline should be carefully followed to optimize the performance of SiP41111 driver.

1. It is strongly recommended to place a 0.1 uf lower ESR decoupling ceramic capacitor right next to the IC from V_{DD} to V_{SS}.
2. The loops formed between device and the gate of the MOSFET should be as small as possible. It is strongly recommended to place the IC right next to the gate of the MOSFET to form small driving loop between pin HO, HS, LO and Vss because high frequency, huge instantaneous current is being sunk and sourced in these loop to drive the gate of the MOSFET, which look like a large capacitive load to the device. If the physical distance can not be minimized due to PCB layout mechanical specification, the width of the loop traces should be increased as much as possible to reduce the impedance of the loop traces.

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