

**NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ICL3222E**

ISL83384E

±15kV ESD Protected, +3V to +5.5V, 1 Microamp, 250Kbps, RS-232 Transmitter/Receiver

FN6017
Rev 3.00
March 15, 2005

The Intersil ISL83384E contains 3.0V to 5.5V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at $V_{CC} = 3.0V$. Targeted applications are PDAs, Palmtops, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with a manual powerdown function reduces the standby supply current to a 1 μ A trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250Kbps are guaranteed at worst case load conditions. This device is fully compatible with 3.3V only systems, mixed 3.3V and 5.0V systems, and 5.0V only systems.

The single pin powerdown function ($\overline{SHDN} = 0$) disables all the transmitters and receivers, while shutting down the charge pump to minimize supply current drain.

Table 1 summarizes the features of the ISL83384E, while Application Note AN9863 summarizes the features of each device comprising the ICL32XX 3V family.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL83384ECA	0 to 70	20 Ld SSOP	M20.209
ISL83384ECAZA (See Note)	0 to 70	20 Ld SSOP (Pb-free)	M20.209
ISL83384ECA-T	0 to 70	Tape and Reel	M20.209
ISL83384ECAZA-T (See Note)	0 to 70	Tape and Reel (Pb-free)	M20.209

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF Tx.	NO. OF Rx.	NO. OF MONITOR Rx. (R _{OUTB})	DATA RATE (Kbps)	Rx. ENABLE FUNCTION?	READY OUTPUT?	MANUAL POWER-DOWN?	AUTOMATIC POWERDOWN FUNCTION?
ISL83384E	2	2	0	250	NO	NO	YES	NO

Features

- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Drop In Replacement for MAX3384E, SP385E
- Low Power, Pin Compatible Upgrade for 5V MAX222, SP310E, ADM222, and LT1780
- Single \overline{SHDN} Pin Disables Transmitters and Receivers
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- RS-232 Compatible with $V_{CC} = 2.7V$
- Latch-Up Free
- On-Chip Voltage Converters Require Only Four External 0.1 μ F Capacitors
- Receiver Hysteresis For Improved Noise Immunity
- Very Low Supply Current 0.3mA
- Guaranteed Minimum Data Rate 250Kbps
- Guaranteed Minimum Slew Rate 6V/ μ s
- Wide Power Supply Range Single +3V to +5.5V
- Low Supply Current in Powerdown State. <1 μ A
- Pb-Free Available (RoHS Compliant)

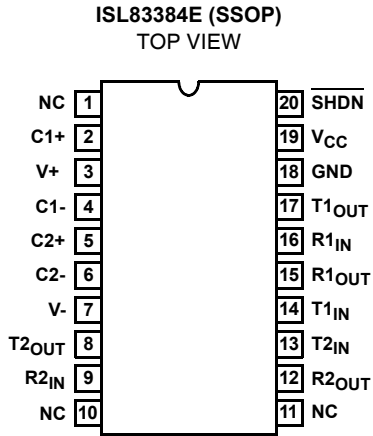
Applications

- Any System Requiring RS-232 Communication Ports
 - Battery Powered, Hand-Held, and Portable Equipment
 - Laptop Computers, Notebooks, Palmtops
 - Modems, Printers and other Peripherals
 - Digital Cameras
 - Cellular/Mobile Phones

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- AN9863, "3V to +5.5V, 250k-1Mbps, RS-232 Transmitters/Receivers"

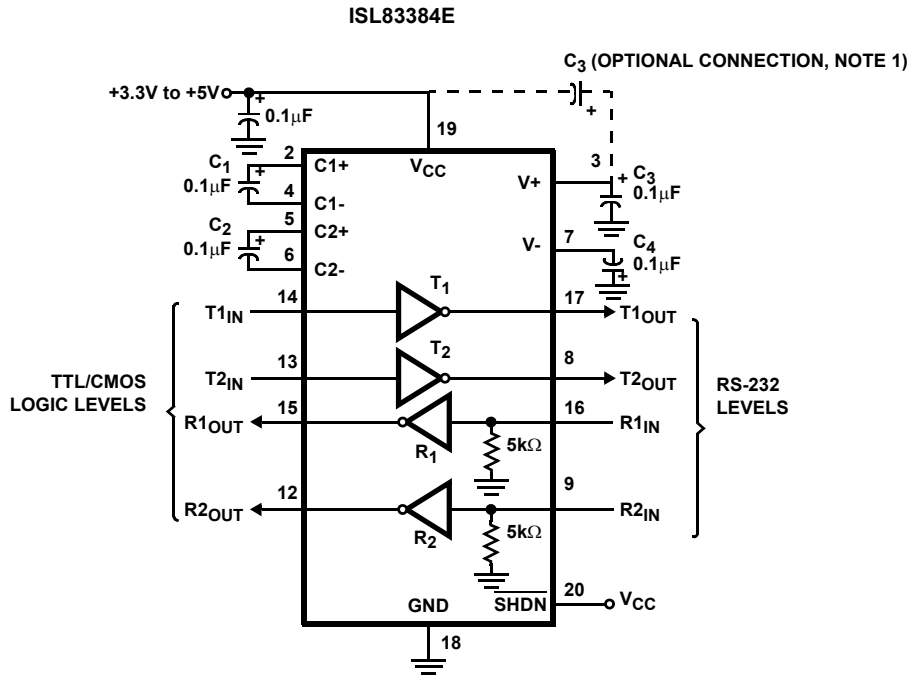
Pinout



Pin Descriptions

PIN	FUNCTION
V _{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T _{IN}	TTL/CMOS compatible transmitter Inputs.
T _{OUT}	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R _{IN}	±15kV ESD Protected, RS-232 compatible receiver inputs.
R _{OUT}	TTL/CMOS level receiver outputs.
SHDN	Active low input to shut down transmitters, receivers, and on-board power supply, to place device in low power mode.

Typical Operating Circuit



NOTES:

1. The negative terminal of C₃ can be connected to either V_{CC} or GND.

Absolute Maximum Ratings

V_{CC} to Ground	-0.3V to 6V
$V+$ to Ground	-0.3V to 7V
$V-$ to Ground	+0.3V to -7V
$V+$ to $V-$	14V
Input Voltages	
T_{IN}, \overline{SHDN}	-0.3V to 6V
R_{IN}	$\pm 25V$
Output Voltages	
T_{OUT}	$\pm 13.2V$
R_{OUT}	-0.3V to $V_{CC} + 0.3V$
Short Circuit Duration	
T_{OUT}	Continuous
ESD Rating	
	See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{\circ}C/W$)
20 Ld SSOP Package	125
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) (Lead Tips Only)	300 $^{\circ}C$

Operating Conditions

Temperature Range	
ISL83384ECX	0 $^{\circ}C$ to 70 $^{\circ}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications Test Conditions: $V_{CC} = 3V$ to 5.5V, $C_1 - C_4 = 0.1\mu F$; Unless Otherwise Specified.
Typicals are at $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	TEMP ($^{\circ}C$)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Current, Powerdown	$\overline{SHDN} = GND$	25	-	0.1	5	μA
		Full	-	1	50	μA
Supply Current, Enabled	All Outputs Unloaded, $\overline{SHDN} = V_{CC}$	Full	-	0.3	3.0	mA
LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T_{IN}, \overline{SHDN}	Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, \overline{SHDN}	Full	2.4	-	-	V
Input Leakage Current	T_{IN}, \overline{SHDN}	Full	-	± 0.01	± 1.0	μA
Output Leakage Current	$\overline{SHDN} = GND$	Full	-	± 0.05	± 10	μA
Output Voltage Low	$I_{OUT} = 3.2mA$	Full	-	-	0.4	V
Output Voltage High	$I_{OUT} = -1.0mA$	Full	$V_{CC} - 0.6$	$V_{CC} - 0.1$	-	V
RECEIVER INPUTS						
Input Voltage Range		Full	-25	-	25	V
Input Threshold Low	$V_{CC} = 3.3V$	25	0.6	1.2	-	V
	$V_{CC} = 5.0V$	Full	0.8	1.5	-	V
Input Threshold High	$V_{CC} = 3.3V$	25	-	1.5	2.4	V
	$V_{CC} = 5.0V$	Full	-	1.8	2.4	V
Input Hysteresis		Full	0.2	0.5	1	V
Input Resistance		Full	3	5	7	k Ω
TRANSMITTER OUTPUTS						
Output Voltage Swing	All Transmitter Outputs Loaded with 3k Ω to Ground	Full	± 5.0	± 5.4	-	V
Output Resistance	$V_{CC} = V+ = V- = 0V$, Transmitter Output = $\pm 2V$	Full	300	10M	-	Ω
Output Short-Circuit Current		Full	± 7	± 35	-	mA
Output Leakage Current	$V_{OUT} = \pm 12V$, $V_{CC} = 0V$ or 3V to 5.5V, $\overline{SHDN} = GND$	Full	-	-	± 10	μA
TIMING CHARACTERISTICS						
Maximum Data Rate	$R_L = 3k\Omega$, $C_L = 1000pF$, One Transmitter Switching	Full	250	500	-	Kbps

Electrical Specifications Test Conditions: $V_{CC} = 3V$ to $5.5V$, $C_1 - C_4 = 0.1\mu F$; Unless Otherwise Specified.
Typicals are at $T_A = 25^\circ C$ (Continued)

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
Transmitter Propagation Delay	Transmitter Input to Transmitter Output, $C_L = 1000pF$	t_{PHL}	Full	-	0.6	3.5	μs
		t_{PLH}	Full	-	0.7	3.5	μs
Receiver Propagation Delay	Receiver Input to Receiver Output, $C_L = 150pF$	t_{PHL}	Full	-	0.2	1	μs
		t_{PLH}	Full	-	0.3	1	μs
Transmitter Output Enable Time	From \overline{SHDN} Rising Edge to $T_{OUT} = \pm 3V$		25	-	50	-	μs
Transmitter Output Disable Time	From \overline{SHDN} Falling Edge to $T_{OUT} = \pm 5V$		25	-	600	-	ns
Transmitter Skew	$t_{PHL} - t_{PLH}$ (Note 3)		25	-	100	-	ns
Receiver Skew	$t_{PHL} - t_{PLH}$		25	-	100	-	ns
Transition Region Slew Rate	$R_L = 3k\Omega$ to $7k\Omega$, Measured From $3V$ to $-3V$ or $-3V$ to $3V$	$V_{CC} = 3.3V$, $C_L = 150pF$ to $2500pF$	25	4	-	-	$V/\mu s$
		$V_{CC} = 4.5V$, $C_L = 150pF$ to $2500pF$	25	6	-	-	$V/\mu s$
ESD PERFORMANCE							
RS-232 Pins (T_{OUT} , R_{IN})	Human Body Model		25	-	± 15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	± 8	-	kV
	IEC61000-4-2 Air Gap Discharge		25	-	± 15	-	kV
All Other Pins	Human Body Model		25	-	± 3	-	kV

NOTE:

3. Transmitter skew is measured at the transmitter zero crossing points.

Detailed Description

The ISL83384E operates from a single +3V to +5.5V supply, guarantees a 250Kbps minimum data rate, requires only four small external 0.1 μF capacitors, features low power consumption, and meets all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: The charge pump, the transmitters, and the receivers.

Charge-Pump

Intersil's new ISL83384E utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate $\pm 5.5V$ transmitter supplies from a V_{CC} supply as low as 3.0V. This allows these devices to maintain RS-232 compliant output levels over the $\pm 10\%$ tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1 μF capacitors for the voltage doubler and inverter functions over the full V_{CC} range. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip $\pm 5.5V$ supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

All transmitter outputs disable and assume a high impedance state when the device enters the powerdown mode (see Table 2). These outputs may be driven to $\pm 12V$ when disabled.

All devices guarantee a 250Kbps data rate for full load conditions (3k Ω and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, $R_L = 3k\Omega$, and $C_L = 250pF$, one transmitter easily operates at 900Kbps.

Transmitter inputs float if left unconnected (there are no pull-up resistors), and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

TABLE 2. POWERDOWN AND ENABLE LOGIC TRUTH TABLE

SHDN INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	MODE OF OPERATION
H	Active	Active	Normal Operation
L	High-Z	High-Z	Manual Powerdown

Receivers

The ISL83384E contains standard inverting receivers that three-state via the \overline{SHDN} control line. Receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 2 and 3).

All the receivers convert RS-232 signals to CMOS output levels and accept inputs up to $\pm 30V$ while presenting the required $3k\Omega$ to $7k\Omega$ input impedance (see Figure 1) even if the power is off ($V_{CC} = 0V$). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

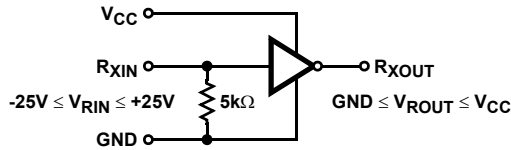


FIGURE 1. INVERTING RECEIVER CONNECTIONS

Low Power Operation

This 3V device requires a nominal supply current of 0.3mA, even at $V_{CC} = 5.5V$, during normal operation (not in powerdown mode). This is considerably less than the 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by replacing the old style device with the ISL83384E.

Low Power, Pin Compatible Replacement

Pin compatibility with existing 5V products (e.g., MAX222), coupled with the wide operating supply range, make the ISL83384E a potential lower power, higher performance drop-in replacement for existing 5V applications. As long as the $\pm 5V$ RS-232 output swings are acceptable, and transmitter pull-up resistors aren't required, the ISL83384E should work in most 5V applications.

When replacing a device in an existing 5V application, it is acceptable to terminate C_3 to V_{CC} as shown on the "Typical Operating Circuit". Nevertheless, terminate C_3 to GND if possible, as slightly better performance results from this configuration.

Powerdown Functionality

The already low current requirement drops significantly when the device enters powerdown mode. In powerdown, supply current drops to $1\mu A$, because the on-chip charge pump turns off ($V+$ collapses to V_{CC} , $V-$ collapses to GND), and the transmitter and receiver outputs three-state. This micro-power mode makes these devices ideal for battery powered and portable applications.

Software Controlled (Manual) Powerdown

The ISL83384E may be forced into its low power, standby state via a simple shutdown (\overline{SHDN}) pin (see Figure 4). Driving this pin high enables normal operation, while driving it low forces the IC into its powerdown state. The time required to exit powerdown, and resume transmission is less than $50\mu s$. Connect \overline{SHDN} to V_{CC} if the powerdown function isn't needed.

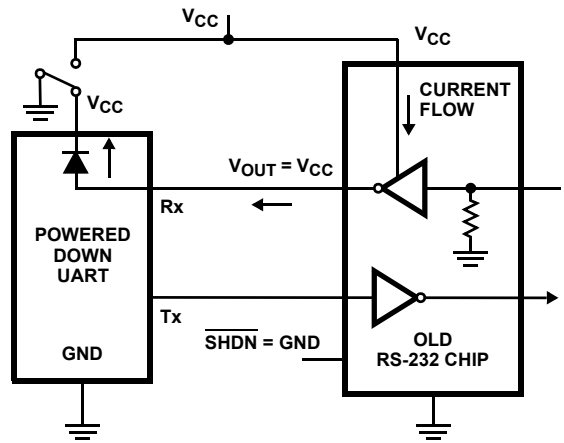


FIGURE 2. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

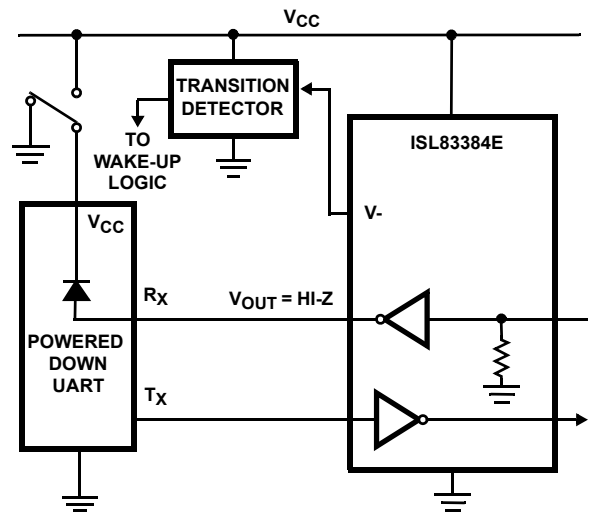


FIGURE 3. DISABLED RECEIVERS PREVENT POWER DRAIN

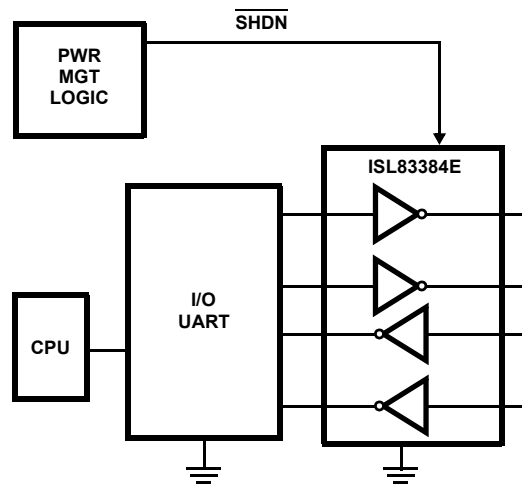


FIGURE 4. CONNECTIONS FOR MANUAL POWERDOWN

Capacitor Selection

The charge pumps require 0.1µF or greater capacitors for operation with $3.3V \leq V_{CC} \leq 5.5V$. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2 , C_3 , and C_4 can be increased without increasing C_1 's value, however, do not increase C_1 without also increasing C_2 , C_3 , and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on $V+$ and $V-$.

Operation Down to 2.7V

ISL83384E transmitter outputs meet RS-562 levels ($\pm 3.7V$), at the full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1 . Connect the bypass capacitor as close as possible to the IC.

Transmitter Outputs when Exiting Powerdown

Figure 5 shows the response of two transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

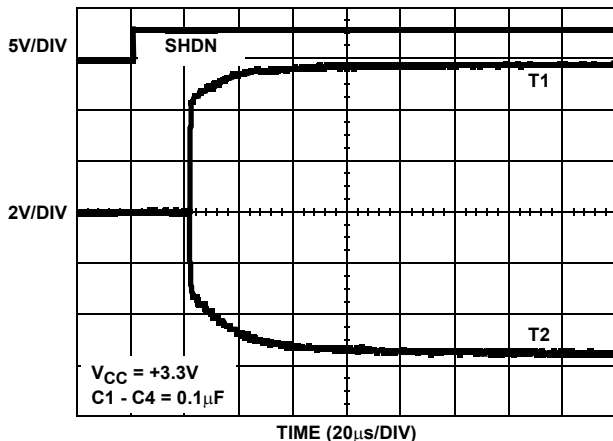


FIGURE 5. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN

High Data Rates

The ISL83384E maintains the RS-232 $\pm 5V$ minimum transmitter output voltages even at high data rates. Figure 6 details a transmitter loopback test circuit, and Figure 7 illustrates the loopback test result at 120Kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120Kbps. Figure 8 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250Kbps. The static transmitter was also loaded with an RS-232 receiver.

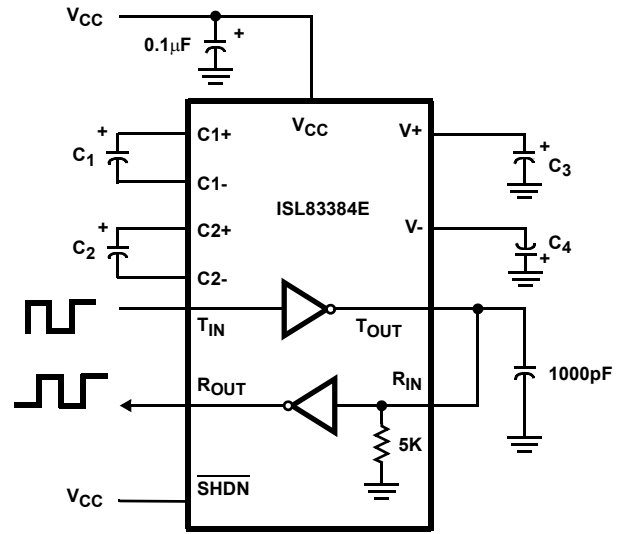


FIGURE 6. TRANSMITTER LOOPBACK TEST CIRCUIT

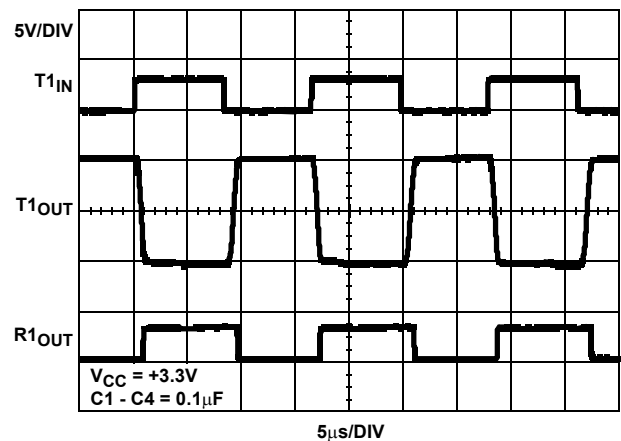


FIGURE 7. LOOPBACK TEST AT 120Kbps

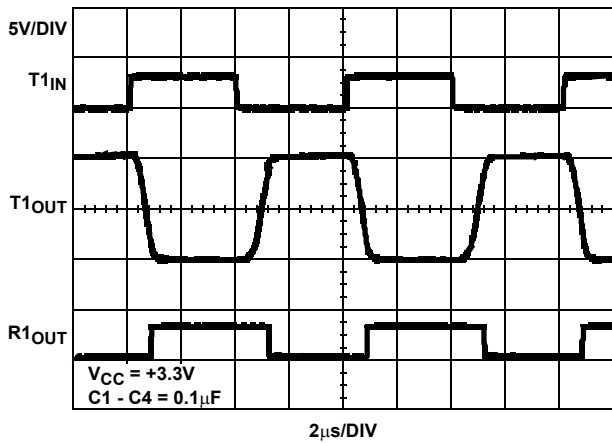


FIGURE 8. LOOPBACK TEST AT 250Kbps

Interconnection with 3V and 5V Logic

The ISL83384E directly interfaces with 5V CMOS and TTL logic families. Nevertheless, with the device at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ISL83384E inputs, but ISL83384E outputs do not reach the minimum V_{IH} for these logic families. See Table 3 for more information.

TABLE 3. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V _{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ISL83384E outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

±15kV ESD Protection

All pins on ISL83XXX devices include ESD protection structures, but the ISL83384E incorporates advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC16000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves $V_{CC} = 3.3V, T_A = 25^\circ C$

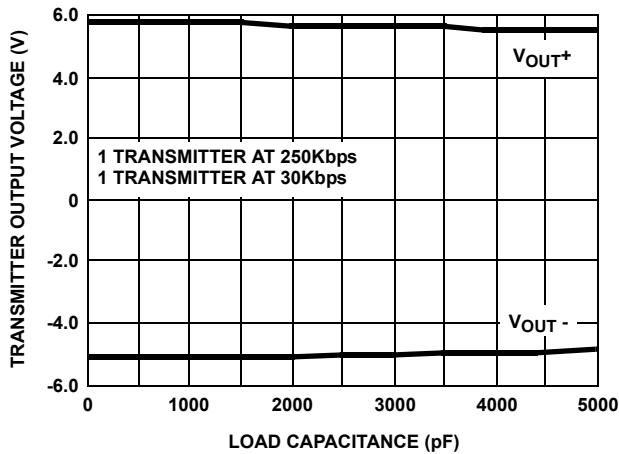


FIGURE 9. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

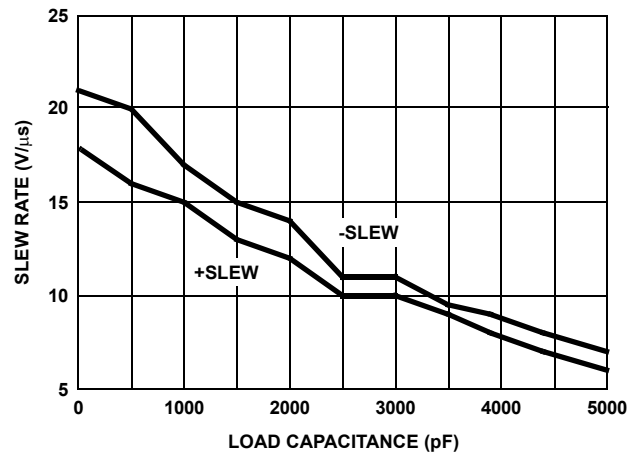


FIGURE 10. SLEW RATE vs LOAD CAPACITANCE

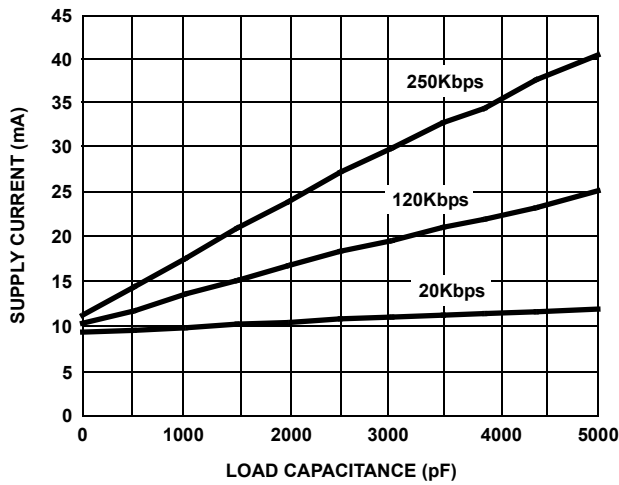


FIGURE 11. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

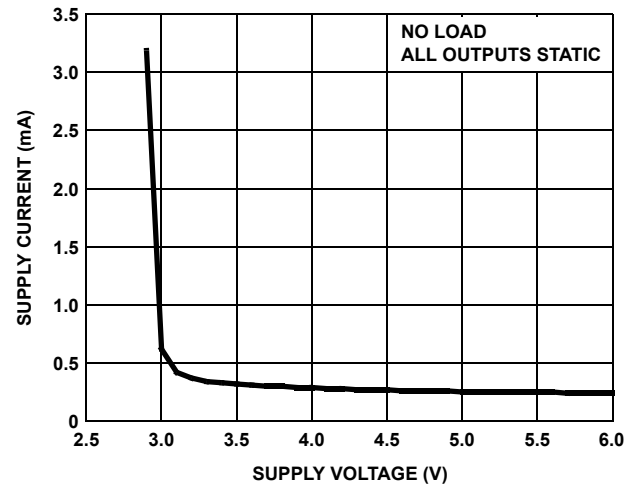


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP)

GND

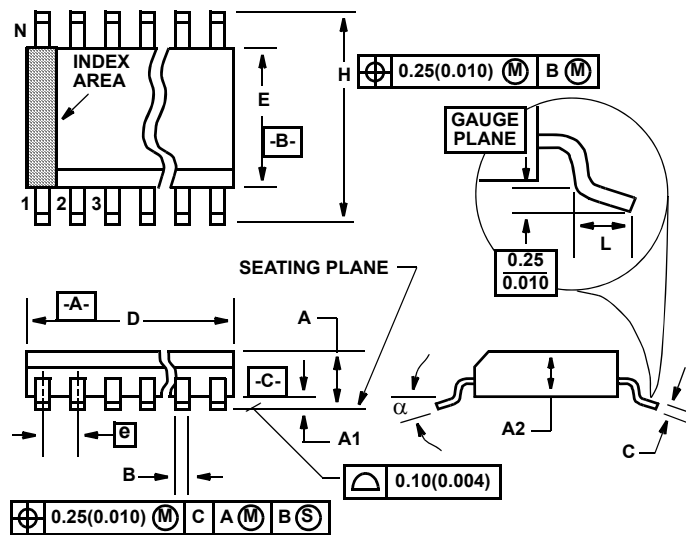
TRANSISTOR COUNT

338

PROCESS

Si Gate CMOS

Shrink Small Outline Plastic Packages (SSOP)



**M20.209 (JEDEC MO-150-AE ISSUE B)
20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008'	0.05	0.21	
A2	0.066	0.070'	1.68	1.78	
B	0.010'	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20'	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20'	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90'	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 3 11/02

© Copyright Intersil Americas LLC 2001-2005. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com