

SN74ALS992, SN74ALS993 9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

D2836, APRIL 1984—REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
'ALS992 . . . True Outputs
'ALS993 . . . Inverting Outputs
- Designed with 9 Bits for Parity Applications
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

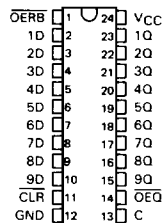
These 9-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily implemented in parity applications.

The nine latches of the 'ALS992 and 'ALS993 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS992 will follow the data (D) inputs. For the 'ALS993, the \bar{Q} outputs will provide the complement of what is applied to its data (D) inputs. On both devices, the Q or \bar{Q} outputs will be in the 3-state condition when output enable \overline{OEQ} is high.

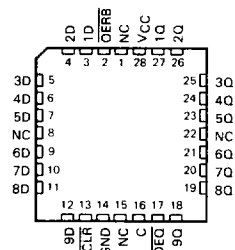
Read-back is provided through the read-back control input (\overline{OERB}). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS992 and SN74ALS993 are characterized for operation from 0°C to 70°C.

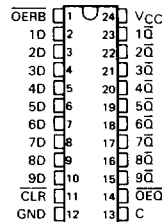
SN74ALS992 . . . DW OR NT PACKAGE
(TOP VIEW)



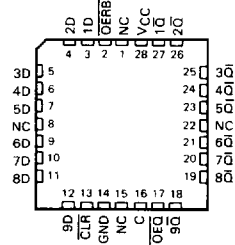
SN74ALS992 . . . FN PACKAGE
(TOP VIEW)



SN74ALS993 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS993 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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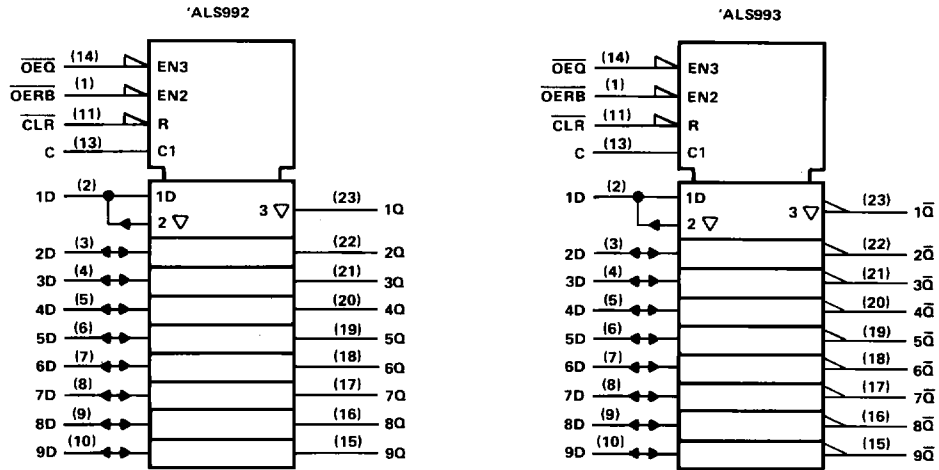
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SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

logic symbols†



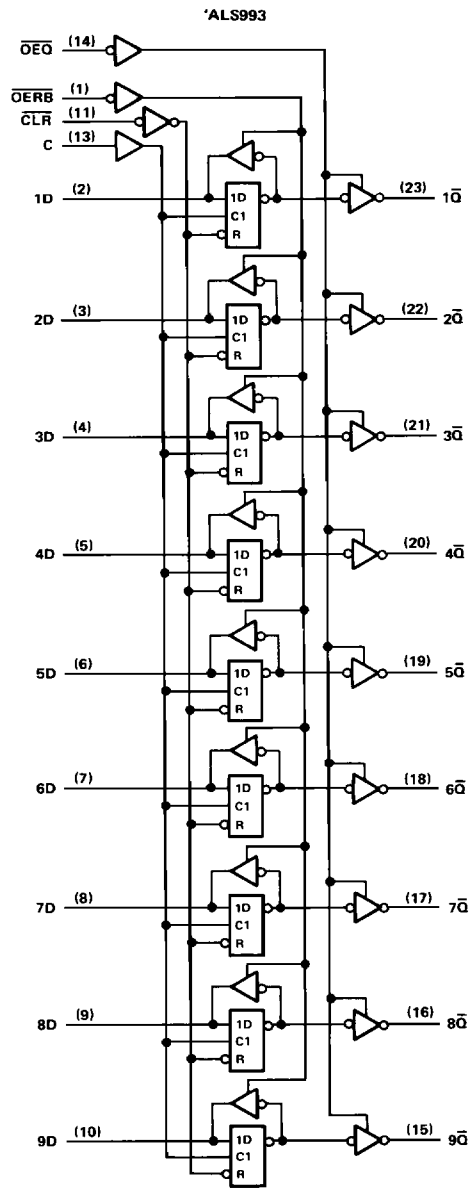
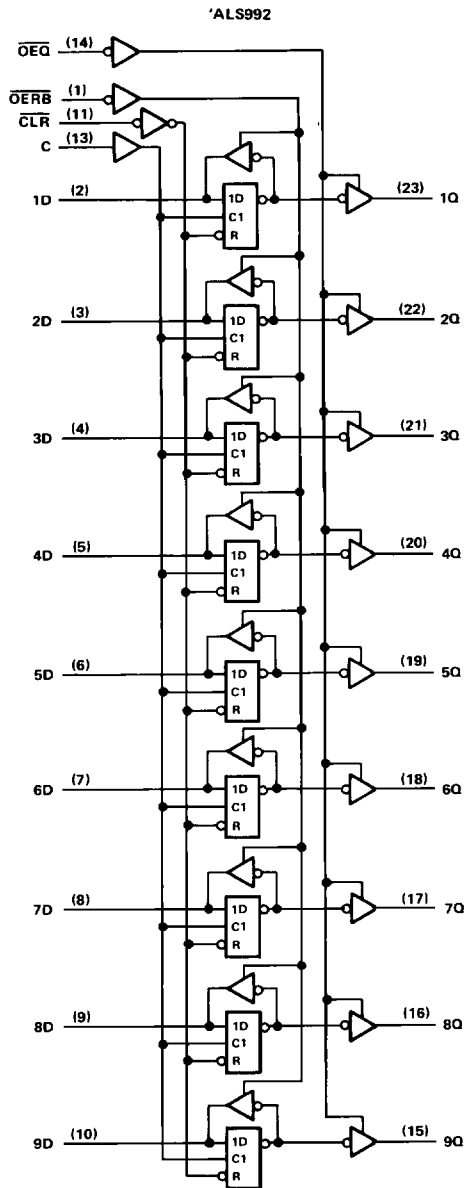
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†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers are for DW and NT packages.

SN74ALS992, SN74ALS993
9-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
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logic diagrams (positive logic)

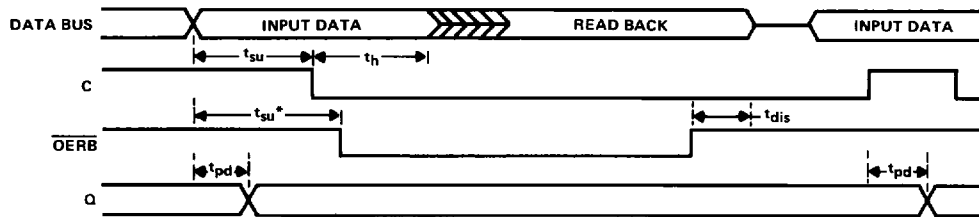


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Pin numbers are for DW and NT packages.

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timing diagram



$\overline{CLR} = H, \overline{OEQ} = L$

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage, (\overline{OERB} , \overline{OE} , \overline{CLR} , and C inputs)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature	0°C to 70°C
Storage temperature range	-65°C to 150°C

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q or \overline{Q}		-2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q or \overline{Q}		24	mA
		D		8	
t_w	Pulse duration	Enable C high	10		ns
		\overline{CLR} low	10		
t_{su}	Setup time	Data before C \downarrow	10		ns
		Data before $\overline{OERB}\downarrow$	10		
t_h	Hold time	5			ns
T_A	Operating free-air temperature	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	All outputs Q or \bar{Q}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$,	$I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			V
		$V_{CC} = 4.5 \text{ V}$,	$I_{OH} = -2.6 \text{ mA}$	2.4	3.2		
V_{OL}	D	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 8 \text{ mA}$		0.35	0.5	
	Q or \bar{Q}	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4	
		$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 24 \text{ mA}$		0.35	0.5	
I_{OZH}	Q or \bar{Q}	$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.7 \text{ V}$			20	μA
I_{OZL}		$V_{CC} = 5.5 \text{ V}$,	$V_O = 0.4 \text{ V}$			-20	
I_I	D inputs	$V_{CC} = 5.5 \text{ V}$,	$V_I = 5.5 \text{ V}$			0.1	mA
	All other	$V_{CC} = 5.5 \text{ V}$,	$V_I = 7 \text{ V}$			0.1	
I_{IH}	D inputs‡	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$			20	μA
	All other					20	
I_{IL}	D inputs‡	$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.4 \text{ V}$			-0.1	mA
	All other					-0.1	
I_O^{\S}		$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.25 \text{ V}$	-30		-112	mA
I_{CC}	'ALS992	$V_{CC} = 5.5 \text{ V}$, \overline{OERB} high	Q outputs high		30	50	mA
			Q outputs low		50	80	
			Q outputs disabled		35	55	
	'ALS993		\bar{Q} outputs high		30	50	mA
			\bar{Q} outputs low		52	82	
			\bar{Q} outputs disabled		40	60	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS} .

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***ALS992 switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0 °C to 70 °C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q	7	10	3	14	ns	
t _{PHL}			9	13	4	16		
t _{PLH}			12	15	6	20		
t _{PHL}	C	Q	15	19	8	25	ns	
t _{PHL}			12	16	6	20		
t _{PHL}			15	22	8	26		
t _{en}	OE \bar{B}	D	11	17	4	21	ns	
t _{dis}		D	6	11	2	14		
t _{en}	OE \bar{Q}	Q	11	16	4	18	ns	
t _{dis}			6	10	1	14		

***ALS993 switching characteristics (see Figure 1)**

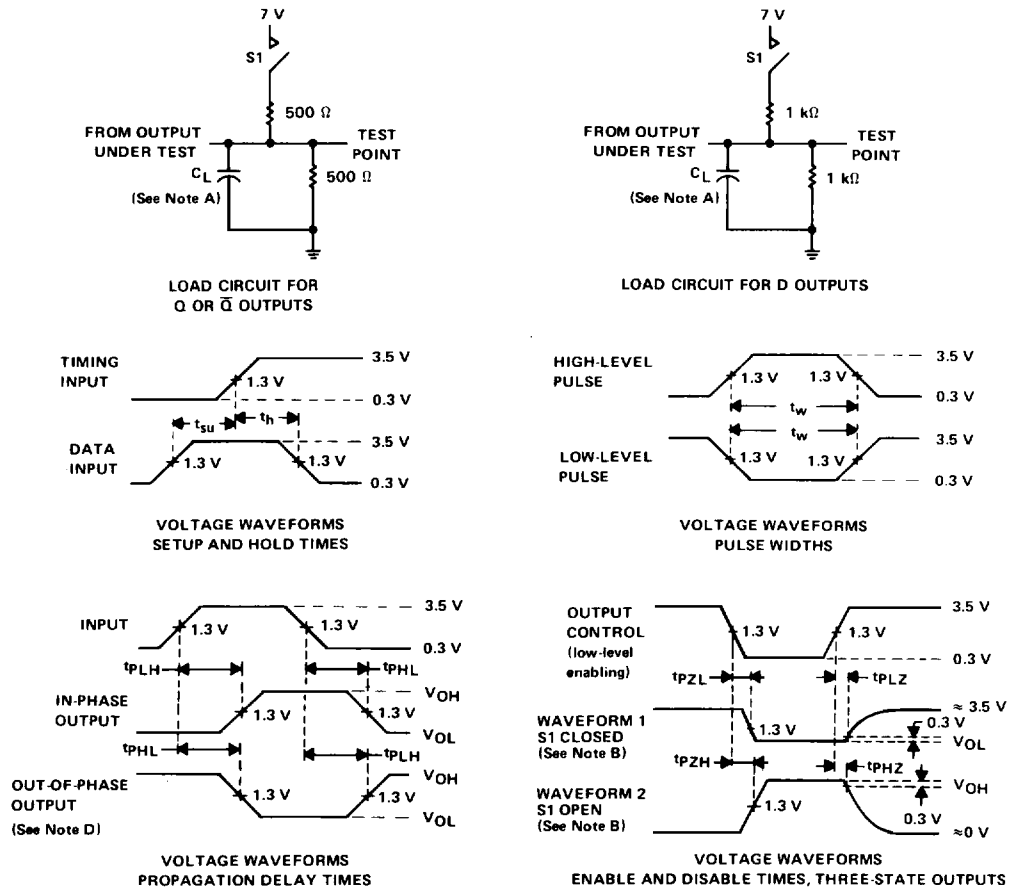
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0 °C to 70 °C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q	11	14	6	20	ns	
t _{PHL}			8	11	4	15		
t _{PLH}			16	20	9	28		
t _{PHL}	C	Q	13	16	7	22	ns	
t _{PHL}			10	13	5	17		
t _{PHL}			15	22	8	26		
t _{en}	OE \bar{B}	D	11	17	4	21	ns	
t _{dis}		D	6	11	2	14		
t _{en}	OE \bar{Q}	Q	11	16	4	20	ns	
t _{dis}			6	10	1	12		

t_{en} = t_{pZH} or t_{pZL}

t_{dis} = t_{pHZ} or t_{pLZ}

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

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