19-3960; Rev 3; 6/06

Quad SPST CMOS Analog Switches

General Description

The DG202/DG212 are normally open, quad single-pole single-throw (SPST) analog switches. These CMOS switches can be continuously operated with power supplies ranging from ±4.5V to ±18V. Maxim guarantees that these switches will not latch up if the power supplies are disconnected with input signals still connected.

The DG202/DG212 are similar to the DG201/DG211 except for inverted control inputs. All devices have guaranteed break-before-make switching, as well as essentially constant on-resistance over the analog signal range. All switches conduct current in either direction and add no offset to the output signal.

Compared to the original manufacturer's products, Maxim's DG202/DG212 consume very little power, making them better suited for portable applications. Maxim has also eliminated the need for the third logic power supply (V_L) that is required for the operation of the original manufacturer's DG212 without sacrificing compatibility.

Applications

Analog Multiplexers

Programmable Gain Amplifiers

Communications Systems

Sample/Holds

Automatic Test Equipment

PBX, PABX

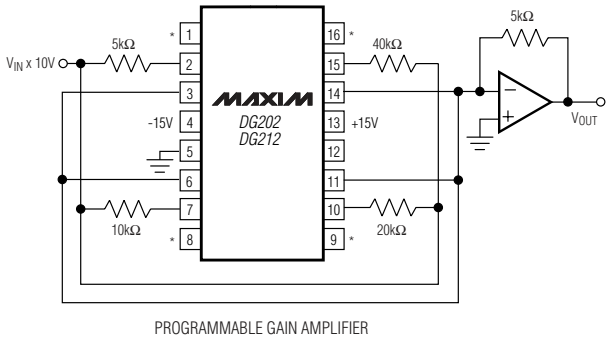
Features

- **Guaranteed ±4.5V to ±18V Operation**
- **No V_L Supply Required**
- **Nonlatching with Supplies Turned Off and Input Signals Present**
- **CMOS and TTL Logic Compatible**
- **Monolithic, Low-Power CMOS Design**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG202CUE	0°C to +70°C	16 TSSOP
DG202CSE	0°C to +70°C	16 SO
DG202CJ	0°C to +70°C	16 Plastic DIP
DG202C/D	0°C to +70°C	Dice
DG202AEGE	-40°C to +85°C	16 QFN (5mm x 5mm)
DG202AEUE	-40°C to +85°C	16 TSSOP
DG202ADY	-40°C to +85°C	16 SO
DG202ADJ	-40°C to +85°C	16 Plastic DIP
DG202AK	-55°C to +125°C	16 CERDIP
DG212CUE	0°C to +70°C	16 TSSOP
DG212CSE	0°C to +70°C	16 SO
DG212CJ	0°C to +70°C	16 Plastic DIP
DG212C/D	0°C to +70°C	Dice
DG212EGE	-40°C to +85°C	16 QFN (5mm x 5mm)
DG212EUE	-40°C to +85°C	16 TSSOP
DG212DY	-40°C to +85°C	16 SO
DG212DJ	-40°C to +85°C	16 Plastic DIP
DG212ETE	-40°C to +85°C	16 Thin QFN

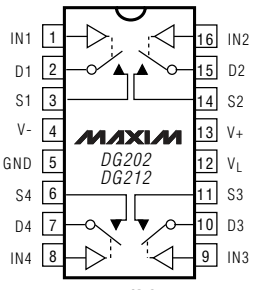
Typical Operating Circuit



PROGRAMMABLE GAIN AMPLIFIER

NOTE: *PINS 1, 8, 9, AND 16 ARE LOGIC CONTROL INPUTS

Pin Configurations



DIP/SO

LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS (DG212)

V+ to V-.....44V
V_{IN} to Ground.....V-, V+
V_L to Ground.....-0.3V, 25V
V_S or V_D to V+.....0, -40V
V_S or V_D to V-.....0, 40V
V+ to Ground.....25V
V- to Ground.....-25V
Current, Any Terminal Except S or D.....30mA
Continuous Current, S or D.....20mA
Peak Current, S or D
(pulsed at 1ms 10% duty cycle max).....70mA
Storage Temperature Range.....-65°C to +125°C

Operating Temperature Range
DG212C.....0°C to +70°C
DG212D/E.....-40°C to +85°C
Power Dissipation (T_A = +70°C) (Note 1)
16-Pin Plastic Dip (derate 10.5mW/°C above +70°C) ..842mW
16-Pin Narrow SO (derate 8.7mW/°C above+70°C). 696mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
16-Pin QFN (5mm x 5mm)
(derate 19.2mW/°C above +70°C).....1538mW
16-Pin Thin QFN
(derate 14.7mW/°C above +70°C).....1177mW

Note 1: Device mounted with all leads soldered to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG212)

(V+ = +15V, V- = -15V, GND = 0, T_A = +25°C, unless otherwise noted.) (For more information on TYP values see Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}			-15		+15	V
Drain-Source ON-Resistance	$R_{DS\ (ON)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA			115	175	Ω
Source OFF-Leakage Current	$I_{S\ (OFF)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	5.0	nA
			V_S = -14V, V_D = 14V	-5.0	-0.02		
Drain OFF-Leakage Current	$I_{D\ (OFF)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	5.0	
			V_S = -14V, V_D = 14V	-5.0	-0.02		
Drain ON-Leakage Current (Note 3)	$I_{D\ (ON)}$	V_S = V_D = 14V, V_{IN} = 2.4V			0.1	5.0	
		V_S = V_D = -14V, V_{IN} = 2.4V		-5.0	-0.15		
INPUT							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		µA
		V_{IN} = 15V			0.003	1.0	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0		-1.0	-0.0004		
DYNAMIC							
Turn-ON Time	t_{ON}	See Switching Time Test Circuit V_S = 2V, R_L = 1kΩ, C_L = 35pF			460	1000	ns
Turn-OFF Time	t_{OFF1}				360	500	
	t_{OFF2}				450		
Source OFF-Capacitance	$C_{S\ (OFF)}$	V_S = 0, V_{IN} = 0, f = 1MHz			5		pF
Drain OFF-Capacitance	$C_{D\ (OFF)}$	V_D = 0, V_{IN} = 0, f = 1MHz			5		
Channel ON-Capacitance	$C_{D\ +\ S\ (ON)}$	V_D = V_S = 0, V_{IN} = 5V, f = 1MHz			16		
OFF-Isolation (Note 4)	OIRR	V_{IN} = 0, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz			70		dB
Crosstalk (Channel to Channel)	CCRR				90		

ELECTRICAL CHARACTERISTICS (DG212) (continued)

(V+ = +15V, V- = -15V, GND = 0, T_A = +25°C, unless otherwise noted.) (For more information on TYP values see Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Positive Supply Current	I+	V_{IN} = 0 and 2.4V (all)		0.02	0.4	mA
Negative Supply Current	I-			0.01	0.4	
Logic Supply Current	I_L			0	0	
Power-Supply Range for Continous Operation	V_{OP}		±4.5		±18.0	V

Note 2: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 3: $I_{D(ON)}$ is leakage from driver into "ON" switch.
Note 4: OFF-Isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = output.

ABSOLUTE MAXIMUM RATINGS (DG202)

Voltages Reference to V-
V+.....44V
GND.....25V
Digital Inputs (Note 1), V_S, V_D.....-2V to (V+ + 2V)
or 20mA, whichever occurs first
Current, Any Terminal Except S or D.....30mA
Continuous Current, S or D.....20mA
Peak Current, S or D
(pulsed at 1ms 10% duty cycle max).....70mA

Operating Temperature Range
DG202C .....0°C to +70°C
DG202D/E.....-40°C to +85°C
DG202A .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Power Dissipation (Note 2)
16-Pin Plastic Dip (derate 10.5mW/°C above +70°C) ...842mW
16-Pin SO (derate 8.7mW/°C above +70°C) 696mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C).....755mW
16-Pin QFN (5 × 5)
(derate 19.2mW/°C above +70°C).....1538mW
16-Pin CERDIP (derate 10.0mW/°C above +70°C).....800mW

Note 1: Signals on S_, D_, or IN_ exceeding V+ or V- on Maxim's DG202 will be clamped by internal diodes, and are also internally current limited to 25mA.
Note 2: Device mounted with all leads soldered to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG202)

(V+ = +15V, V- = -15V, GND = 0, **T_A = +25°C**, unless otherwise noted.) (For more information on TYP values see Note 3.)

PARAMETER	SYMBOL	CONDITIONS		DG202A			DG202C, D, E			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
SWITCH										
Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
Drain-Source ON Resistance	$R_{DS (ON)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA			115	175		115	200	Ω
Source OFF-Leakage Current	$I_{S (OFF)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	nA
			V_S = -14V, V_D = 14V	-1.0	-0.02		-1.0	-0.02		
Drain OFF-Leakage Current	$I_{D (OFF)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	
			V_S = -14V, V_D = 14V	-1.0	-0.02		-1.0	-0.02		
Drain ON-Leakage Current (Note 4)	$I_{D (ON)}$	V_{IN} = 2.4V	V_S = -14V		0.1	1.0		0.1	1.0	
			V_S = 14V	-1.0			-5.0			

ELECTRICAL CHARACTERISTICS (DG202) (continued)

(V+ = +15V, V- = -15V, GND = 0, **T_A = +25°C**, unless otherwise noted.) (For more information on TYP values see Note 3.)

PARAMETER	SYMBOL	CONDITIONS	DG202A			DG202C, D, E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V	-1.0	-0.0004		-1.0	-0.0004		µA
		V_{IN} = 15V		0.003	1.0		0.003	1.0	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0	-1.0	-0.0004		-1.0	-0.0004		
DYNAMIC									
Turn-ON Time	t_{ON}	See Figure 1 Switching Time Test Circuit		480	600		480	600	ns
Turn-OFF Time	t_{OFF1}			370	450		370	450	
Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0, R_{GEN} = 0		20			20		pC
Source OFF-Capacitance	$C_{S\ (OFF)}$	V_S = 0, V_{IN} = 0, f = 140kHz		5			5		pF
Drain OFF-Capacitance	$C_{D\ (OFF)}$			5			5		
Channel ON-Capacitance	$C_{D\ (ON)}$ + $C_{S\ (ON)}$	V_D = V_S = 0, V_{IN} = 5V, f = 140kHz		16			16		
OFF-Isolation		V_{IN} = 0, Z_L = 75Ω		70			70		dB
Crosstalk (Channel to Channel)		V_S = 2.0V, f = 100kHz		90			90		
SUPPLY									
Positive Supply Current	I+	All channels ON or OFF		0.02	0.1		0.02	0.1	mA
Negative Supply Current	I-	All channels ON or OFF	-0.1	-0.01		-0.1	-0.01		
Power-Supply Range for Continuous Operation	V_{OP}		±4.5		±18	±4.5		±18.0	V

Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 4: $I_{D\ (ON)}$ is leakage from driver into "ON" switch.

ELECTRICAL CHARACTERISTICS (DG202)

(V+ = +15V, V- = -15V, GND = 0, **T_A = full opearting temperature range**, unless otherwise noted.) (For more information on TYP values see Note 3.)

PARAMETER	SYMBOL	CONDITIONS		DG202A			DG202C, D, E			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
SWITCH										
Analog Signal Range	V_{ANALOG}			-15		+15	-15		+15	V
Drain-Source ON Resistance (Note 5)	$R_{DS\ (ON)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA				250			250	Ω
Source OFF-Leakage Current	$I_{S\ (OFF)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V			100			100	nA
			V_S = -14V, V_D = 14V	-100			-100			
Drain OFF-Leakage Current	$I_{D\ (OFF)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V			100			100	
			V_S = -14V, V_D = 14V	-100			-100			
Drain ON-Leakage Current (Note 6)	$I_{D\ (ON)}$	V_{IN} = 2.4V	V_S = -14V			200			200	
			V_D = 14V	-200			-200			
INPUT										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0			-1.0			µA
		V_{IN} = 15V				1.0			1.0	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0		-1.0			-1.0			

Note 5: Electrical characteristics, such as On-Resistance, will change when power supplies other than ±15V, are used.
Note 6: $I_{D\ (ON)}$ is leakage from driver into "ON" switch.

Pin Description

PIN		NAME	FUNCTION
DIP/SO/TSSOP	QFN/TQFN		
1, 16, 9, 8	15, 14, 7, 6	IN1–IN4	Input
2, 15, 10, 7	16, 13, 8, 5	D1–D4	Analog Switch Drain Terminal
3, 14, 11, 6	1, 12, 9, 4	S1–S4	Analog Switch Source Terminal
4	2	V-	Negative-Supply Voltage Input
5	3	GND	Ground
12	10	N.C.	No Connection
13	11	V+	Positive-Supply Voltage Input—Connected to Substrate
—	EP	EP	Exposed Pad. Connect exposed pad to V+ or leave EP unconnected.

Switching Time Test Circuit

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be +ve or -ve as per switching times test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

Protecting Against Fault Conditions

Fault conditions occur when power supplies are turned off when input signals are still present, or when over-voltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased and conduct current from the signal source. If

Quad SPST CMOS Analog Switches

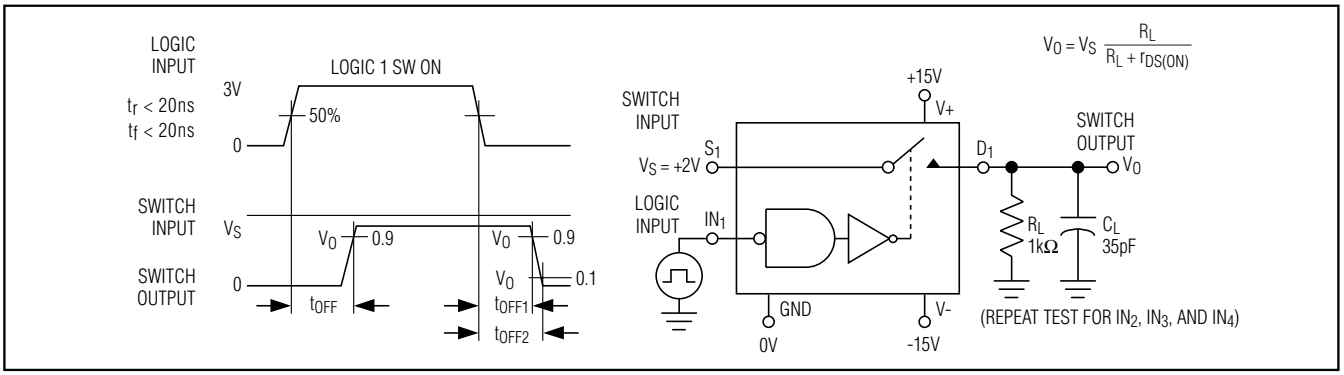


Figure 1. Switching Time

Typical $R_{DS(ON)}$ vs. Power Supplies for Maxim's DG202, and DG212

POWER SUPPLIES	$R_{DS(ON)}$ AT ANALOG SIGNAL LEVEL					
	-5V	+5V	-10V	+10V	-15V	+15V
±5V	350Ω	380Ω	—	—	—	—
±10V	—	—	165Ω	250Ω	—	—
±15V	—	—	125Ω	160Ω	135Ω	155Ω

this current is required to be kept to low (µA) levels then the addition of external protection diodes is recommended.

To provide protection for overvoltages up to 20V above the supplies, a 1N4001 or 1N914 type diode should be placed in series with the positive and negative supplies as shown in Figure 2. The addition of these diodes will reduce the analog signal range to 1V below the positive supply and 1V above the negative supply.

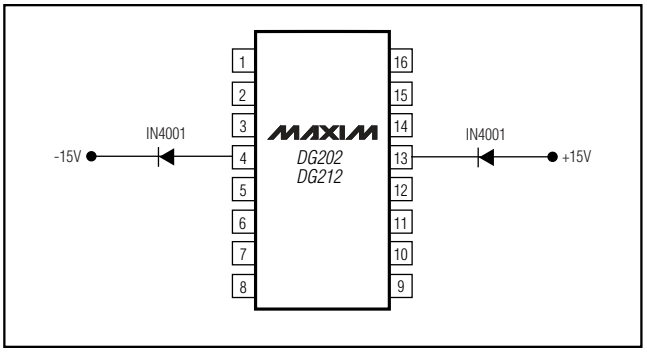
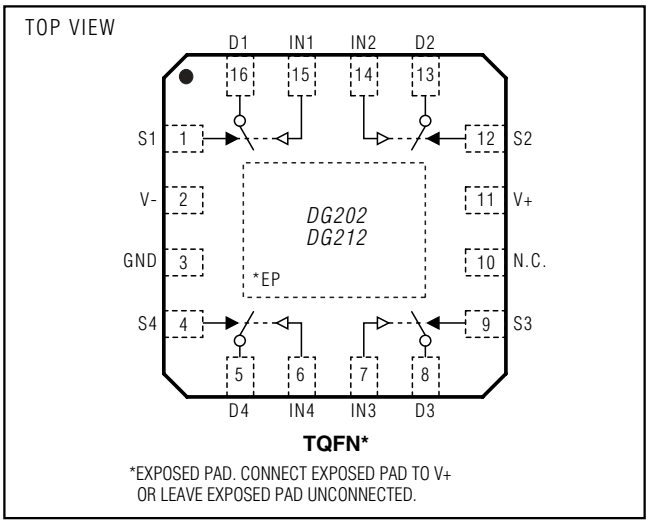


Figure 2. Protection against Fault Conditions

Pin Configurations (continued)



TQFN*

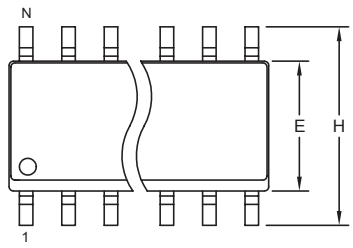
*EXPOSED PAD. CONNECT EXPOSED PAD TO V+ OR LEAVE EXPOSED PAD UNCONNECTED.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

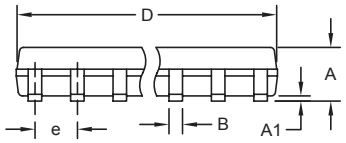
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



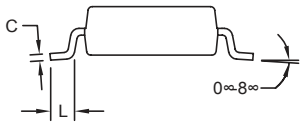
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

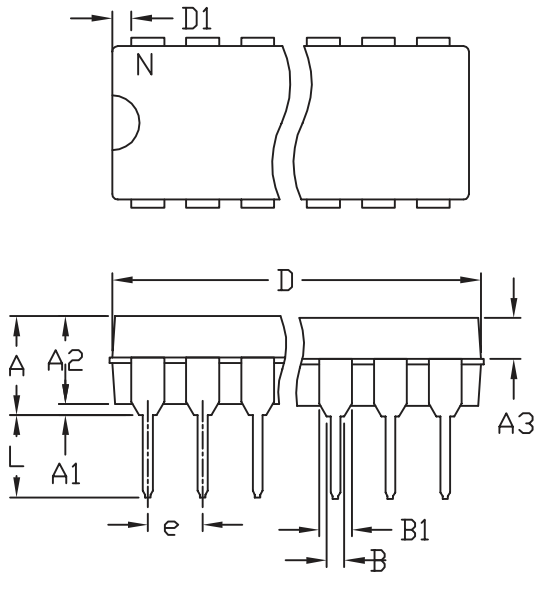
TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

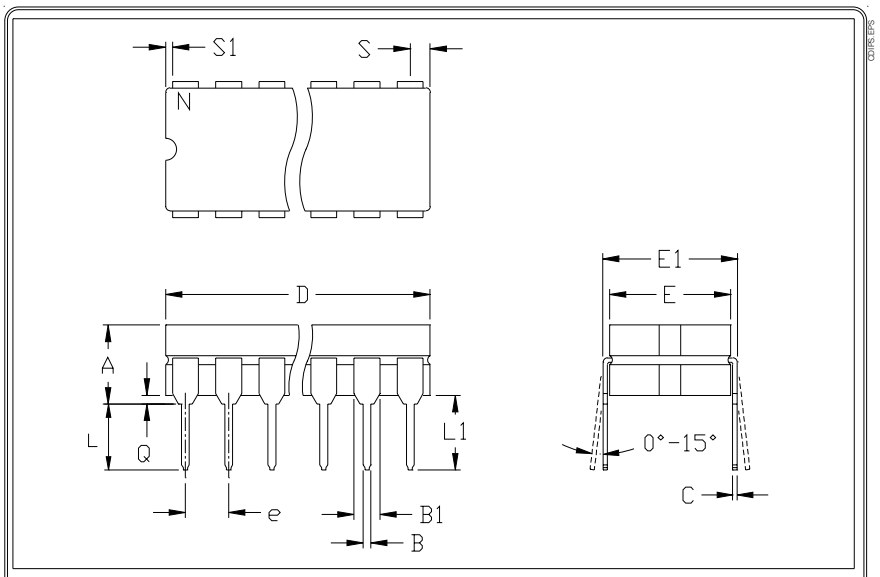
PACKAGE FAMILY OUTLINE: PDIP .300" (TITLE)

1/1

21-0043 D (DOCUMENT CONTROL NUMBER REV)

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

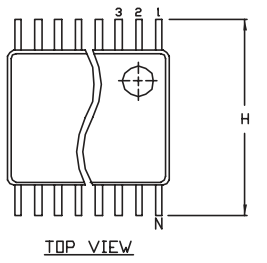
TITLE: PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A (DOCUMENT CONTROL NUMBER REV)

Quad SPST CMOS Analog Switches

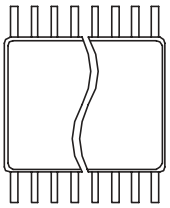
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

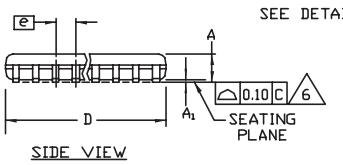
TSSOP4.40mm.EPS



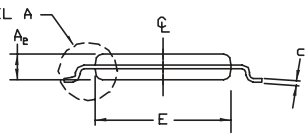
TOP VIEW



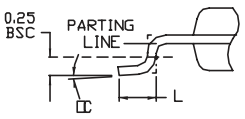
BOTTOM VIEW



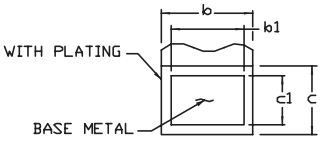
SIDE VIEW



END VIEW



DETAIL A



LEAD TIP DETAIL

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

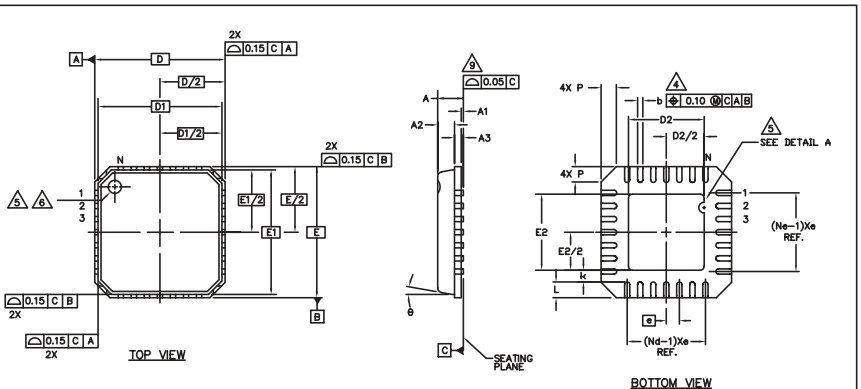
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	G	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L QFN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV. I | 1/2

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

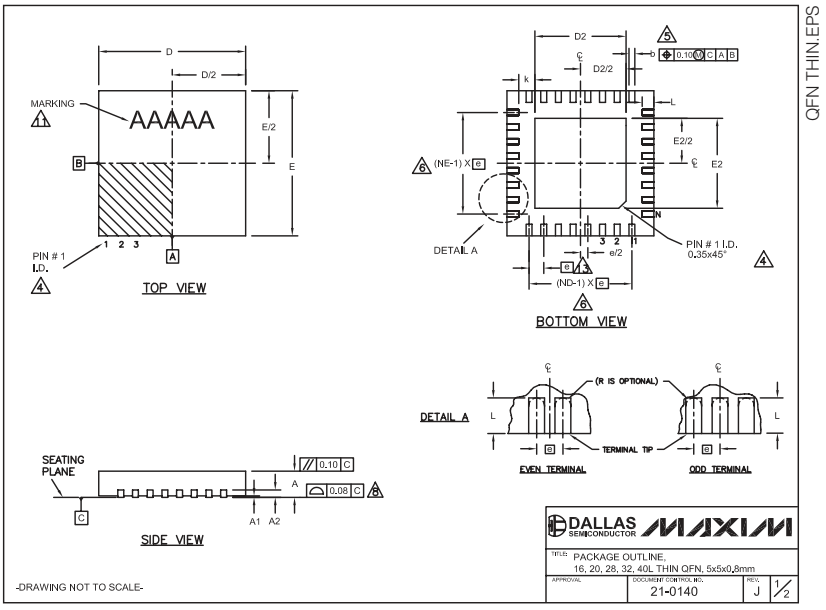
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV. I | 2/2

Quad SPST CMOS Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			---		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
21-0140
J
2/2

Revision History

Pages changed at Rev3: 1–6, 11

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.