ISL1533A

Dual Channel Differential DSL Line Driver

FN8648
Rev 2.00
Jan 31, 2019

The ISL1533A is a dual channel differential amplifier designed for driving high crest factor signals at very low distortion levels. The high drive capability of 450mA makes this driver ideal for DMT designs. It contains two pairs of wideband, high-voltage, current mode feedback amplifiers designed with the Renesas HS30 Bipolar SOI process for low power consumption in Asymmetric Digital Subscriber Line (ADSL) and Power Line Communications (PLC) systems. This process provides very rugged protection against lightning induced surges on the line.

The supply current can be set using a resistor on the I_{ADJ} pin. Pins C_0 and C_1 can adjust supply current to one of four preset modes (full-I_S, 3/4-I_S, 1/2-I_S, and full power-down). The ISL1533A integrates 50k pull-up resistors on Pins C_0 and C_1 to initially disable the device.

The ISL1533A operates on ±5V to ±15V supplies or a single supply up to 30V and retains its bandwidth and linearity across the complete full scale supply range.

The device is supplied in a thermally-enhanced small footprint (4mmx5mm) 24 Ld QFN package. The ISL1533A is specified for operation across the full -40°C to +85°C temperature range.

Features

- 450mA output drive capability
- 44.4V_{P-P} differential output drive into 100Ω
- ±5V to ±15V or single supply to 30V operation
- Operates down to a supply current of 4mA per port
- Current control pins
- Channel separation: 80dB at 500kHz
- Pb-free (RoHS compliant)

Applications

- Dual port ADSL2+ line drivers
- Power Line Communications (PLC)

Related Literature

For a full list of related documents, visit our website:

- ISL1533A device page

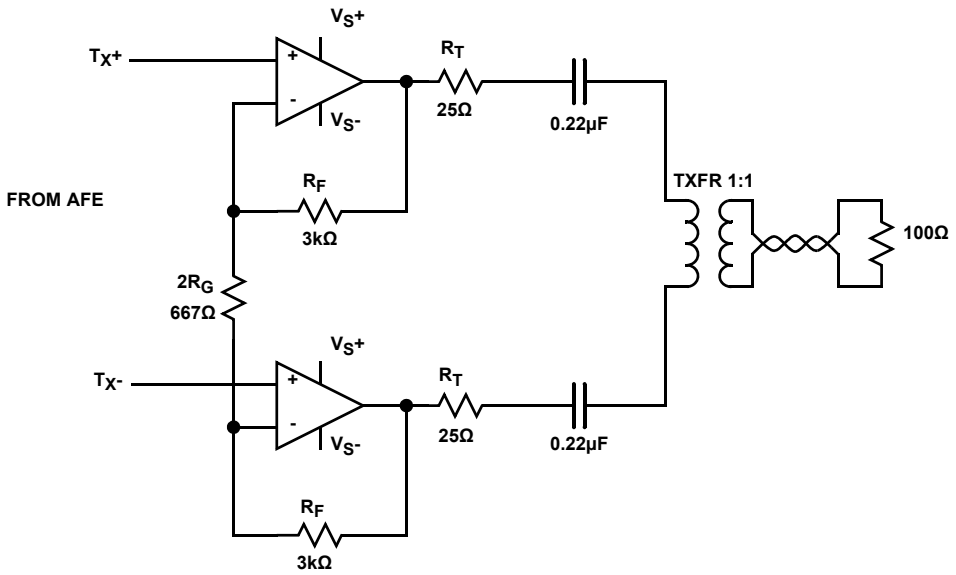


FIGURE 1. TYPICAL APPLICATION CIRCUIT

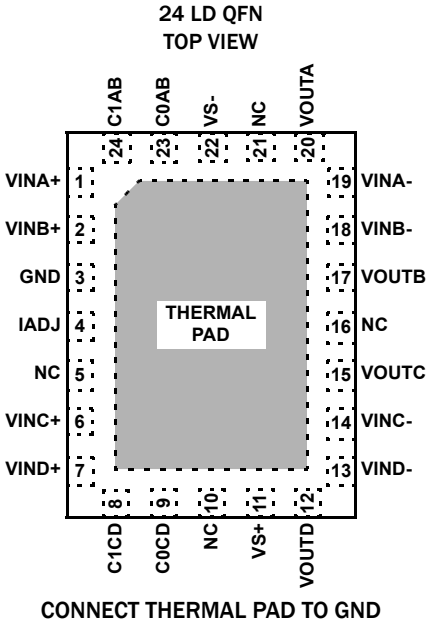
Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TAPE AND REEL (UNITS) (Note 1)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL1533AIRZ	1533A IRZ	-	-40°C to +85°C	24 Ld QFN	L24.4x5F
ISL1533AIRZ-T13	1533A IRZ	2.5k	-40°C to +85°C	24 Ld QFN	L24.4x5F

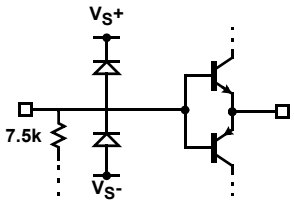
NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL1533A device page. For more information about MSL, see TB363.

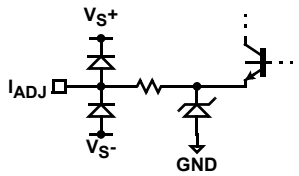
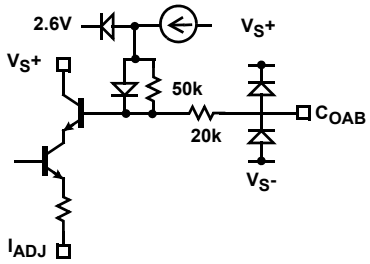
Pin Configuration



Pin Descriptions

24 Ld QFN	PIN NAME	FUNCTION	CIRCUIT
1	VINA+	Amplifier A non-inverting input	 CIRCUIT 1
2	VINB+	Amplifier B non-inverting input	(See Circuit 1)
3	GND	Ground connection	

Pin Descriptions

24 Ld QFN	PIN NAME	FUNCTION	CIRCUIT
4	IADJ (Note 4)	Supply current control pin for both DSL channels #1 and #2	 CIRCUIT 2
5, 10, 16, 21	NC	Not connected	
6	VINC+	Amplifier C non-inverting input	(See Circuit 1)
7	VIND+	Amplifier D non-inverting input	(See Circuit 1)
8	C1CD (Note 5)	DSL channel #2 current control pin	 CIRCUIT 3
9	C0CD (Note 5)	DSL channel #2 current control pin	(See Circuit 3)
11	VS+	Positive supply	
12	VOUTD	Amplifier D output	(See Circuit 1)
13	VIND-	Amplifier D inverting input	(See Circuit 1)
14	VINC-	Amplifier C inverting input	(See Circuit 1)
15	VOUTC	Amplifier C output	(See Circuit 1)
17	VOUTB	Amplifier B output	(See Circuit 1)
18	VINB-	Amplifier B inverting input	(See Circuit 1)
19	VINA-	Amplifier A inverting input	(See Circuit 1)
20	VOUTA	Amplifier A output	(See Circuit 1)
22	VS-	Negative supply	
23	C0AB (Note 6)	DSL channel #1 current control pin	(See Circuit 3)
24	C1AB (Note 6)	DSL channel #1 current control pin	(See Circuit 3)

NOTES:

4. IADJ controls bias current (IS) settings for both DSL channels.
5. Amplifiers C and D comprise DSL channel #2. C0CD and C1CD control I_S settings for DSL channel #2.
6. Amplifiers A and B comprise DSL channel #1. C0AB and C1AB control I_S settings for DSL channel #1.

Absolute Maximum Ratings

(T_A = +25°C)

V_S+ to V_S- Supply Voltage . . . . . -0.3V to 30V
V_S+ Voltage to GND . . . . . -0.3V to 30V
V_S- Voltage to GND . . . . . -30V to 0.3V
Driver V_{IN}+ Voltage . . . . . V_S- to V_S+
C_0, C_1 Voltage to GND . . . . . -0.3V to 6V
I_{ADJ} Voltage to GND . . . . . -0.3V to 4V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3kV
Machine Model (Per EIAJ ED-4701 Method C-111) 200V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Lead QFN Package (Notes 7, 8)	37	2.5

Current into any Input 8mA
Output Current from Driver (Static) 50mA
Power Dissipation . . . . . See Figure 37
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Junction Temperature . . . . . -40°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
8. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters with Min/Max specifications are assured. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Specifications

V_S = ±12V, R_F = 3kΩ, R_L= 50Ω, I_{ADJ} = C_0 = C_1 = 0V, T_A = +25°C. Amplifiers tested separately.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 9)	TYP	MAX Note 9	UNIT
SUPPLY CHARACTERISTICS						
Positive Supply Current per Amplifier	I_S+ (Full I_S)	All outputs at 0V, C_0 = C_1 = 0V, R_{ADJ} = 0	3.0	4.0	5.0	mA
Negative Supply Current per Amplifier	I_S- (Full I_S)	All outputs at 0V, C_0 = C_1 = 0V, R_{ADJ} = 0	-4.88	-3.88	-2.88	mA
Positive Supply Current per Amplifier	I_S+ (3/4 I_S)	All outputs at 0V, C_0 = 5V, C_1 = 0V, R_{ADJ} = 0		3.0		mA
Negative Supply Current per Amplifier	I_S- (3/4 I_S)	All outputs at 0V, C_0 = 5V, C_1 = 0V, R_{ADJ} = 0		-2.8		mA
Positive Supply Current per Amplifier	I_S+ (1/2 I_S)	All outputs at 0V, C_0 = 0V, C_1 = 5V, R_{ADJ} = 0	1.63	2.0	2.75	mA
Negative Supply Current per Amplifier	I_S- (1/2 I_S)	All outputs at 0V, C_0 = 0V, C_1 = 5V, R_{ADJ} = 0	-2.63	-1.88	-1.5	mA
Positive Supply Current per Amplifier	I_S+ (Power-down)	All outputs at 0V, C_0 = C_1 = 5V, R_{ADJ} = 0		0.12	0.5	mA
Negative Supply Current per Amplifier	I_S- (Power-down)	All outputs at 0V, C_0 = C_1 = 5V, R_{ADJ} = 0	-0.5	0		mA
GND Supply Current per Amplifier	I_{GND}	All outputs at 0V		0.25		mA
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}		-10	4	+10	mV
V_{OS} Mismatch	ΔV_{OS}		-2	0	+2	mV
Non-Inverting Input Bias Current	I_B+		-7.5		+7.5	µA
Inverting Input Bias Current	I_B-		-50		+50	µA
I_B- Mismatch	ΔI_B-		-10	0	+10	µA
Transimpedance	R_{OL}			15		MΩ
Input Noise Voltage	e_N			10		nV/√Hz
Input Noise Current	i_N			25		pA/√Hz
Input High Voltage	V_{IH}	C_0 and C_1 inputs	2.2			V
Input Low Voltage	V_{IL}	C_0 and C_1 inputs			0.8	V
Input High Current for C_0, C_1	I_{IH0}, I_{IH1}	C_0 = 5V, C_1 = 5V	5	33	60	µA

Electrical Specifications $V_S = \pm12V$, $R_F = 3k\Omega$, $R_L = 50\Omega$, $I_{ADJ} = C_0 = C_1 = 0V$, $T_A = +25°C$. Amplifiers tested separately. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 9)	TYP	MAX Note 9	UNIT
Input Low Current for C_0 or C_1	I_{IL}	$C_0 = 0V$, $C_1 = 0V$	-15	-3.5		µA
OUTPUT CHARACTERISTICS						
Loaded Output Swing (R_L Single-Ended to GND)	V_{OUT}	$R_L = 100\Omega$		±11.1		V
		$R_L = 50\Omega$ (+)		+10.8		V
		$R_L = 50\Omega$ (-)		-10.8		V
		$R_L = 25\Omega$ (+)	+9.4	+10.3		V
		$R_L = 25\Omega$ (-)		-10.5	-9.3	V
Linear Output Current	I_{OL}	$A_V = 5$, $R_L = 10\Omega$, f = 100kHz, THD = -60dBc (10Ω single-ended)		450		mA
Output Current	I_{OUT}	$V_{OUT} = 1V$, $R_L = 1\Omega$		1		A
DYNAMIC PERFORMANCE						
-3dB Bandwidth	BW	$A_V = 5$, $R_{L\text{-}DIFF} = 100\Omega$		60		MHz
2nd Harmonic Distortion	HD2	$f_C = 200kHz$, $R_{L\text{-}DIFF} = 100\Omega$, $V_{OUT} = 10.5V_{P\text{-}P\text{-}DIFF}$		-86		dBc
		$f_C = 2MHz$, $R_{L\text{-}DIFF} = 100\Omega$, $V_{OUT} = 2V_{P\text{-}P\text{-}DIFF}$		-65		dBc
		$f_C = 2MHz$, $R_{L\text{-}DIFF} = 100\Omega$ $V_{OUT} = 10.5V_{P\text{-}P\text{-}DIFF}$		-60		dBc
3rd Harmonic Distortion	HD3	$f_C = 200kHz$, $R_{L\text{-}DIFF} = 100\Omega$, $V_{OUT} = 10.5V_{P\text{-}P\text{-}DIFF}$		-92		dBc
		$f_C = 2MHz$, $R_{L\text{-}DIFF} = 100\Omega$, $V_{OUT} = 2V_{P\text{-}P\text{-}DIFF}$		-50		dBc
		$f_C = 2MHz$, $R_{L\text{-}DIFF} = 100\Omega$, $V_{OUT} = 10.5V_{P\text{-}P\text{-}DIFF}$		-58		dBc
Slewrate (Single-Ended)	SR	V_{OUT} from -8V to +8V measured at ±4V		400		V/µs

NOTE:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

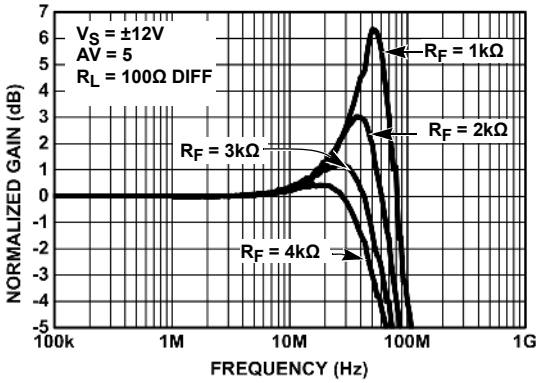


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (FULL I_S)

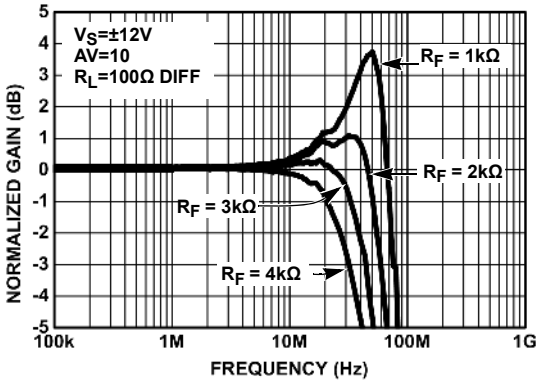


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (FULL I_S)

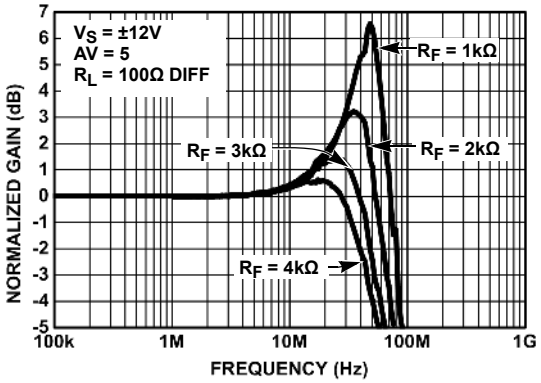


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (3/4 I_S)

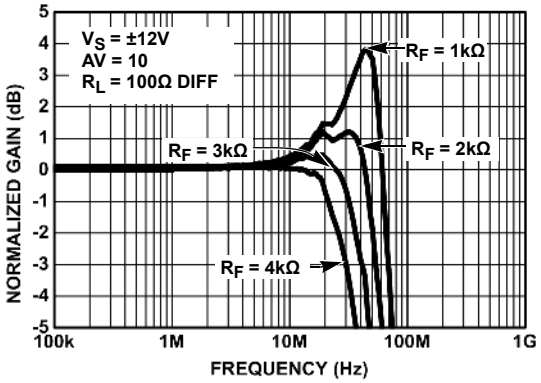


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (3/4 I_S)

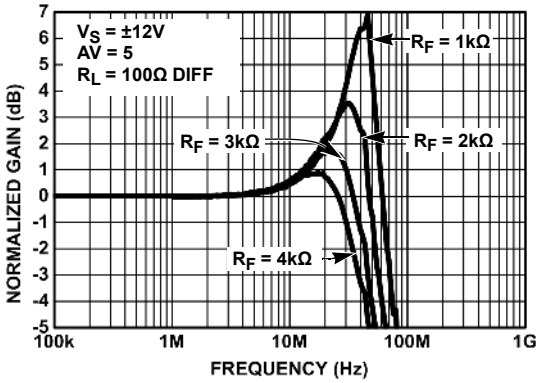


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (1/2 I_S)

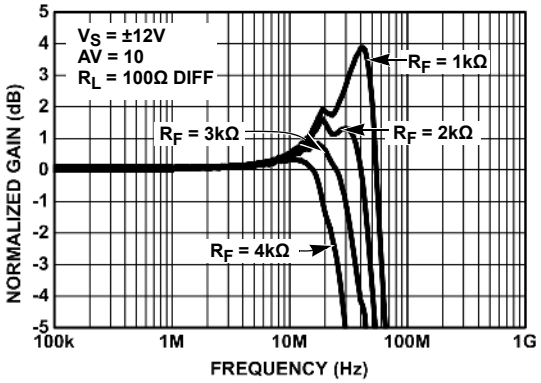


FIGURE 7. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (1/2 I_S)

Typical Performance Curves (Continued)

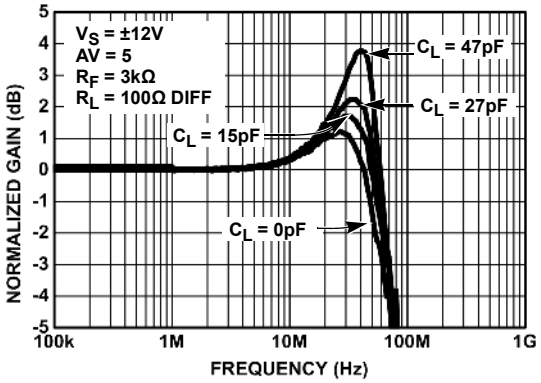


FIGURE 8. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (FULL I_S)

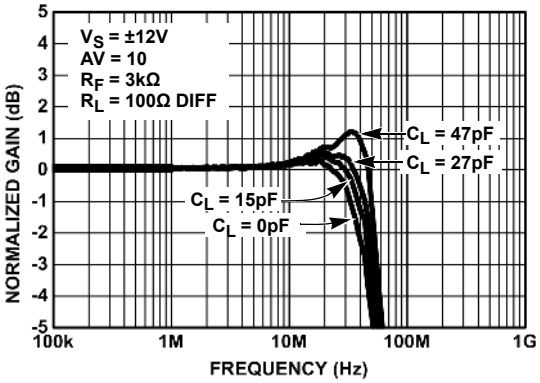


FIGURE 9. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (FULL I_S)

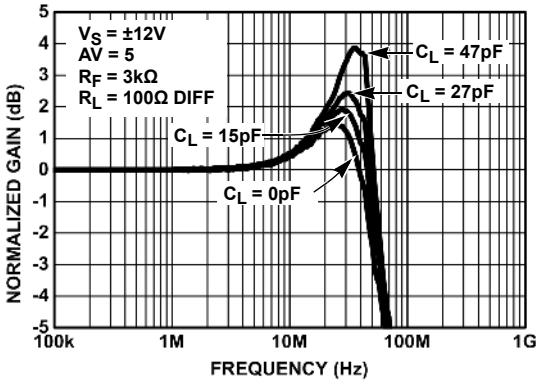


FIGURE 10. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (3/4 I_S)

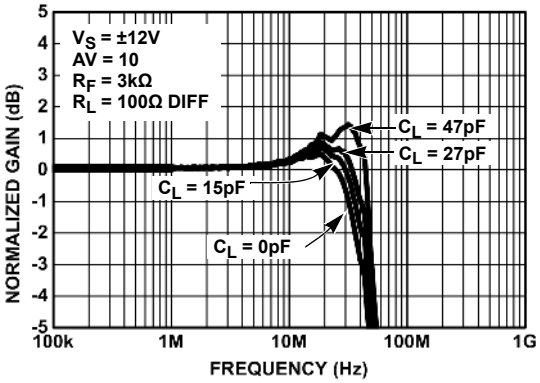


FIGURE 11. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (3/4 I_S)

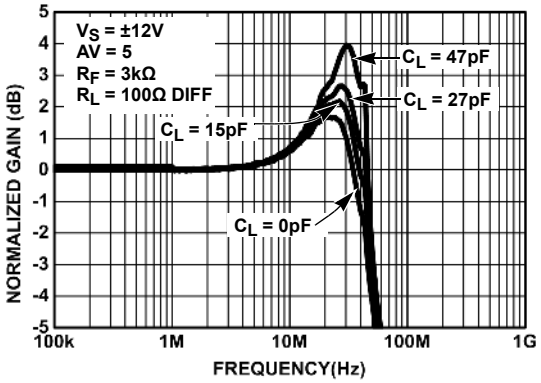


FIGURE 12. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (1/2 I_S)

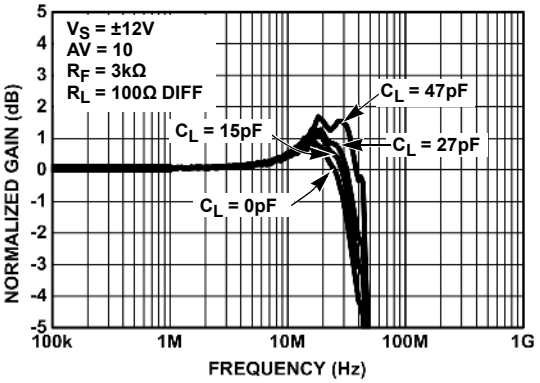


FIGURE 13. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (1/2 I_S)

Typical Performance Curves (Continued)

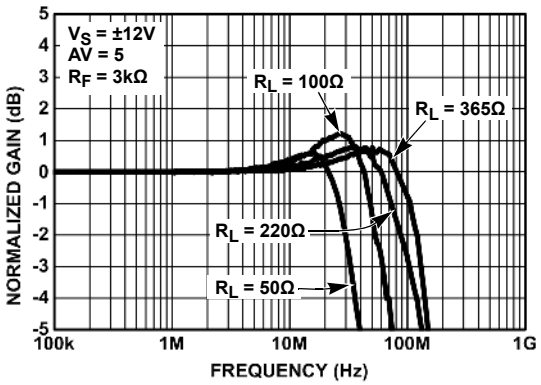


FIGURE 14. DIFFERENTIAL FREQUENCY RESPONSE vs R_L (FULL I_S)

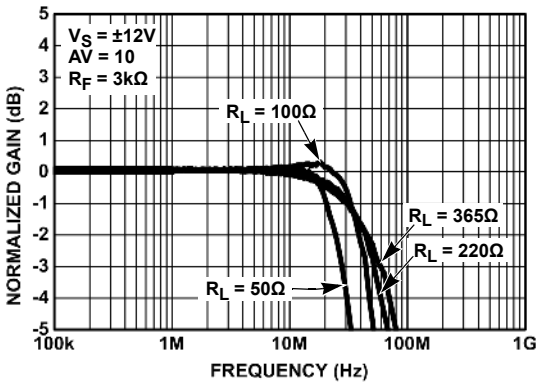


FIGURE 15. DIFFERENTIAL FREQUENCY RESPONSE vs R_L (FULL I_S)

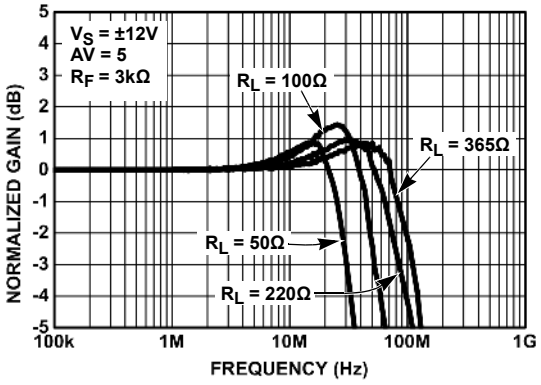


FIGURE 16. DIFFERENTIAL FREQUENCY RESPONSE vs R_L (3/4 I_S)

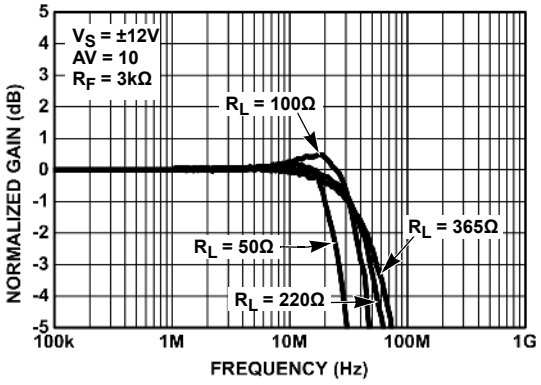


FIGURE 17. DIFFERENTIAL FREQUENCY RESPONSE vs R_L (3/4 I_S)

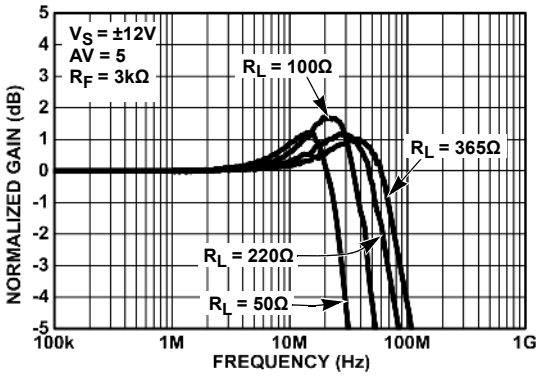


FIGURE 18. DIFFERENTIAL FREQUENCY RESPONSE vs R_L (1/2 I_S)

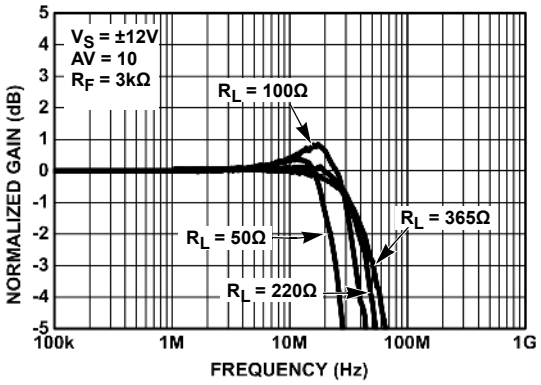


FIGURE 19. DIFFERENTIAL FREQUENCY RESPONSE vs R_L (1/2 I_S)

Typical Performance Curves (Continued)

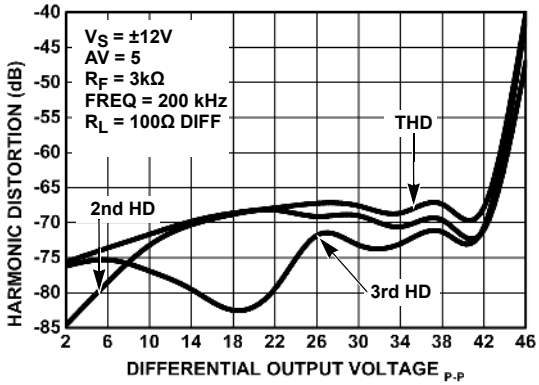


FIGURE 20. HARMONICS DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL I_S)

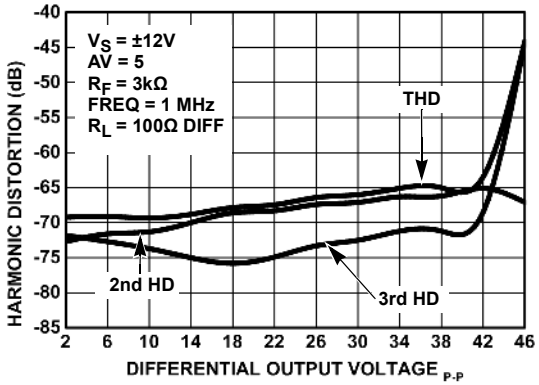


FIGURE 21. HARMONICS DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL I_S)

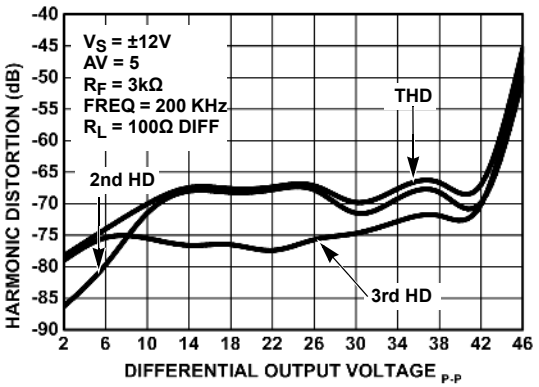


FIGURE 22. HARMONICS DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 I_S)

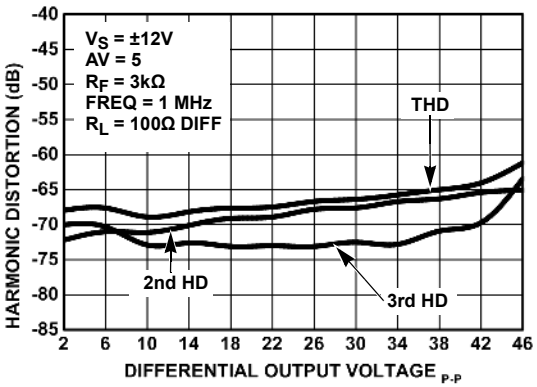


FIGURE 23. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 I_S)

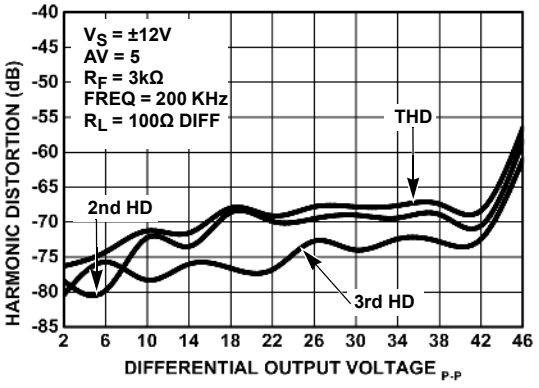


FIGURE 24. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 I_S)

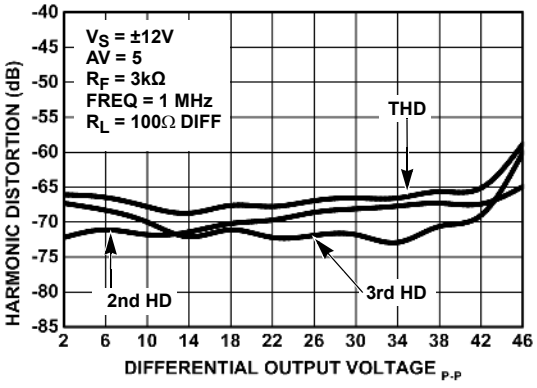


FIGURE 25. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 I_S)

Typical Performance Curves (Continued)

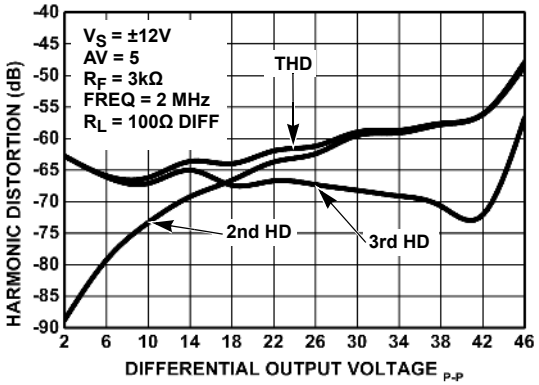


FIGURE 26. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL I_S)

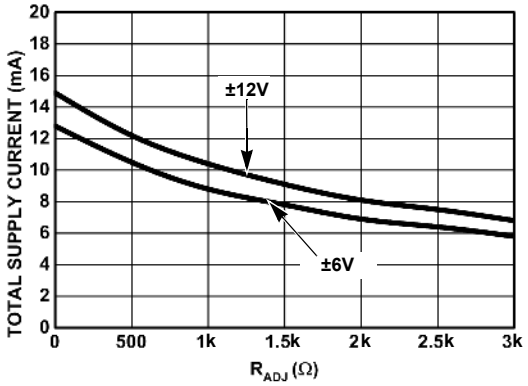


FIGURE 27. QUIESCENT SUPPLY CURRENT vs R_{ADJ}

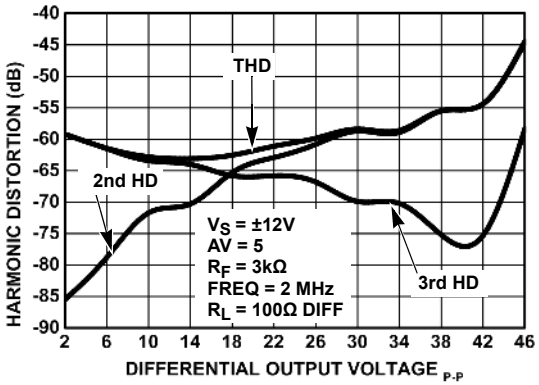


FIGURE 28. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 I_S)

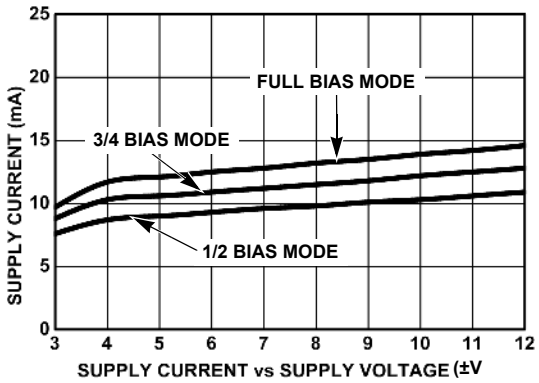


FIGURE 29. SUPPLY CURRENT vs SUPPLY VOLTAGE

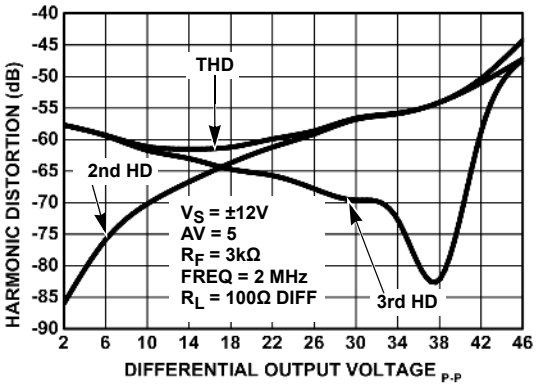


FIGURE 30. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 I_S)

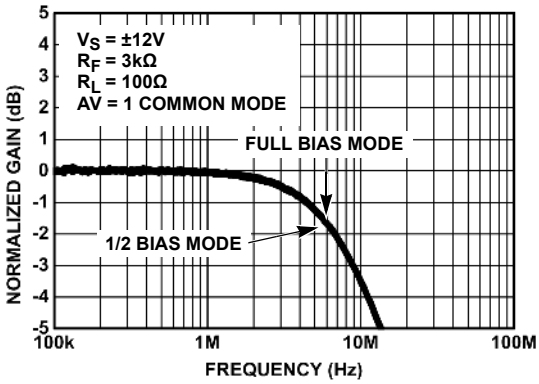


FIGURE 31. COMMON-MODE FREQUENCY RESPONSE

Typical Performance Curves (Continued)

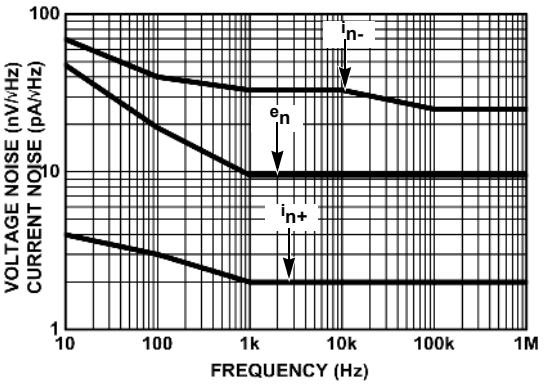


FIGURE 32. INPUT VOLTAGE & CURRENT NOISE vs FREQUENCY

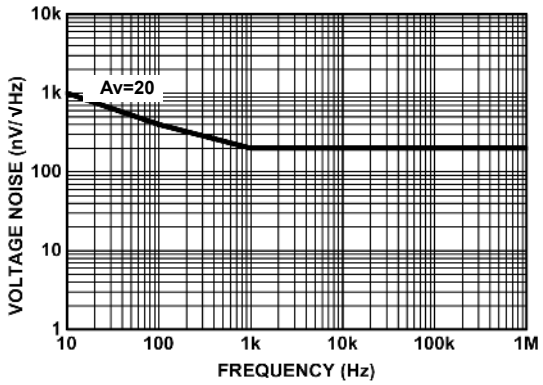


FIGURE 33. SINGLE-ENDED OUTPUT VOLTAGE NOISE vs FREQUENCY

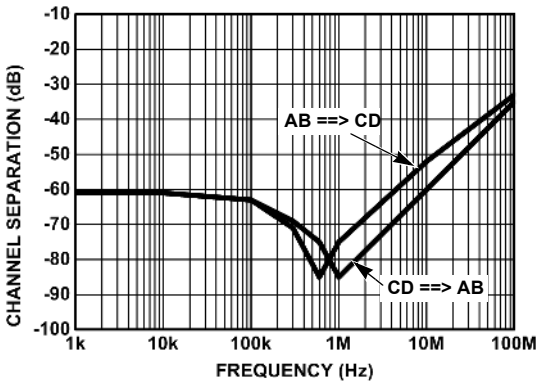


FIGURE 34. CHANNEL SEPARATION vs FREQUENCY

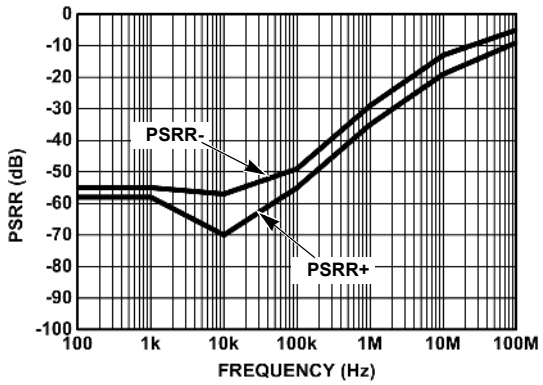


FIGURE 35. PSRR vs FREQUENCY

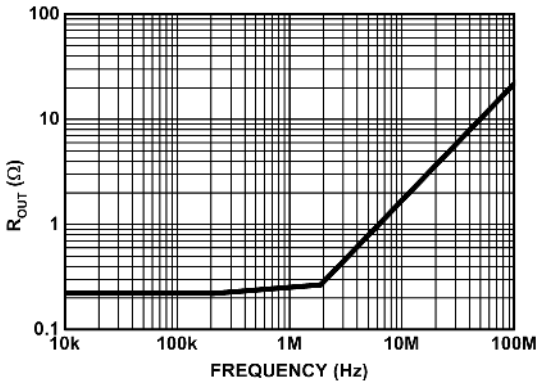


FIGURE 36. OUTPUT IMPEDANCE vs FREQUENCY

JEDEC JESD51-7 HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD - QFN EXPOSED DIEPAD SOLDERED TO PCB PER JESD51-5

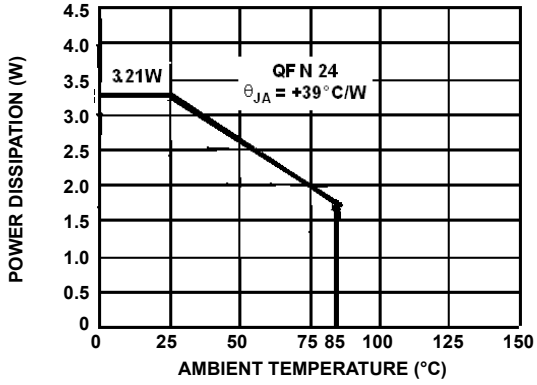


FIGURE 37. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Figure 38 shows a typical application circuit for the ISL1533A as an ADSL2+ CO line driver. The driver output stage is sized to provide the full ADSL2+ CO power level of 20dBm onto the telephone lines. The actual peak output voltages and currents depend on the transformer turn ratio. The ISL1533A is designed to support 450mA of output current, which exceeds the level required for 1:1 transformer ratio.

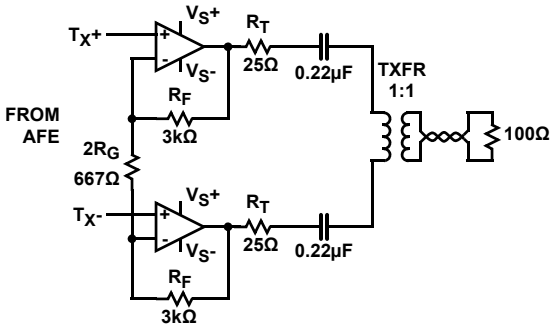


FIGURE 38. TYPICAL ADSL CO LINE DRIVER

Power Control Function

Two forms of power control operation are available:

- Digital input supply current control.
- Resistor from I_{ADJ} to ground

CONTROLLING THE SUPPLY CURRENT WITH THE DIGITAL INPUTS

Two digital inputs, C_0 and C_1, can control the supply current of the ISL1533A drive amplifiers. The C_0 and C_1 inputs are designed to pull high initially. Float these inputs to set the device in disable mode.

As the supply current is reduced, the ISL1533A starts to exhibit slightly higher levels of distortion and the frequency response is limited. The ISL1533A's four power modes are set up as shown in Table 1.

TABLE 1. ISL1533A POWER MODES

C_1	C_0	OPERATION
0	0	I_S Full Power Mode
0	1	3/4 I_S Power Mode
1	0	1/2 I_S Power Mode
1	1	Power-Down

CONTROLLING POWER CONSUMPTION WITH A RESISTOR

Another method for controlling the power consumption of the ISL1533A is to connect a resistor from the I_{ADJ} pin to ground.

When the I_{ADJ} pin is grounded (the normal state), the supply current per channel is as shown in the "SUPPLY CHARACTERISTICS" on page 4 of the "Electrical Specifications" table. When a resistor is inserted, the supply current is scaled according to Figure 27 on page 10 of the "Typical Performance Curves". Both methods of power control can be used simultaneously. In this case, positive and negative supply currents (per Ampere) are given by Equation 1.

$$I_S+ = 0.34mA + \frac{5.06mA}{1+(R_{SET}/1300)} \times (3/4\overline{C_1} + 1/2\overline{C_0} - \overline{C_1} \times \overline{C_0} \times 1/4)$$

$$I_S- = \frac{-5.06mA}{1+(R_{SET}/1300)} \times (3/4\overline{C_1} + 1/2\overline{C_0} - \overline{C_1} \times \overline{C_0} \times 1/4) \quad \text{(EQ. 1)}$$

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with feedback and gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Table 2 shows the recommended resistor values that produce an optimal driver frequency response (1dB of peaking).

TABLE 2. OPTIMUM DRIVER FEEDBACK RESISTOR FOR VARIOUS GAINS

SUPPLY VOLTAGE	DRIVER VOLTAGE GAIN	
	5	10
±12V	3k	2k

Single Supply Operation in PLC Modems

Powerline Communication (PLC) modems often commonly operate from a single 12V supply while using only one amplifier pair. Figure 39 shows the necessary circuit configuration for one amplifier pair operation.

To ensure symmetrical operation, all non-inverting amplifier inputs are DC-biased with $V_S/2$ using the four bias resistors, R_B. $V_S/2$ is generated from V_S from the voltage divider resistors, R_D. The Drive-Enable pin ($\overline{DE}$) of the local controller or Analog Front End (AFE) controls the bias control inputs, C0AB and C1AB, of the active differential pair, consisting of amplifiers A and B. The bias inputs, C0CD and C1CD, are left open to disable the amplifiers C and D.

Note: C0CD and C1CD are internally pulled high.

The outputs of amplifiers A and B are configured for the desired signal gain using R_F and R_G. The outputs of amplifiers C and D are configured for unity gain using only R_F. The external circuitry around amplifiers C and D defines a solid operating point that prevents the amplifiers from oscillating.

The single 12V supply represents a 50% reduction of the rated typical ±12V and causes the amplifier bias currents to drop. For best performance, increase these bias currents by applying a negative bias voltage (V_{Bias}) from the resistor, R_{ADJ}, to the IADJ input. See Figure 40.

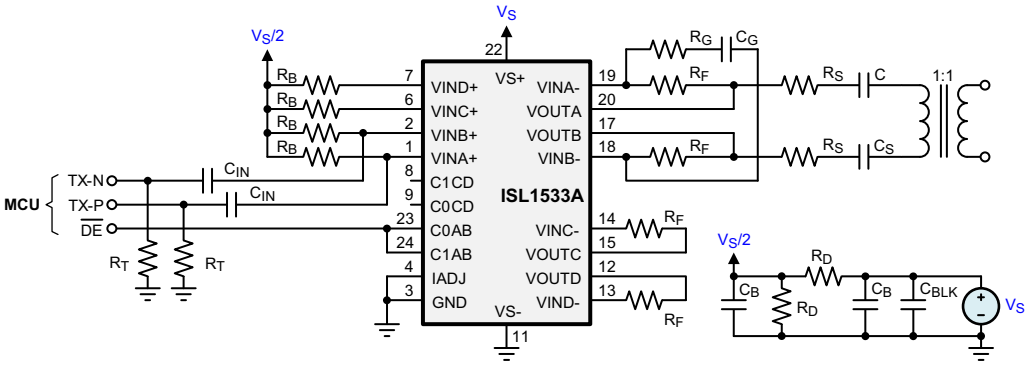


FIGURE 39. SINGLE SUPPLY OPERATION OF ONE AMPLIFIER PAIR

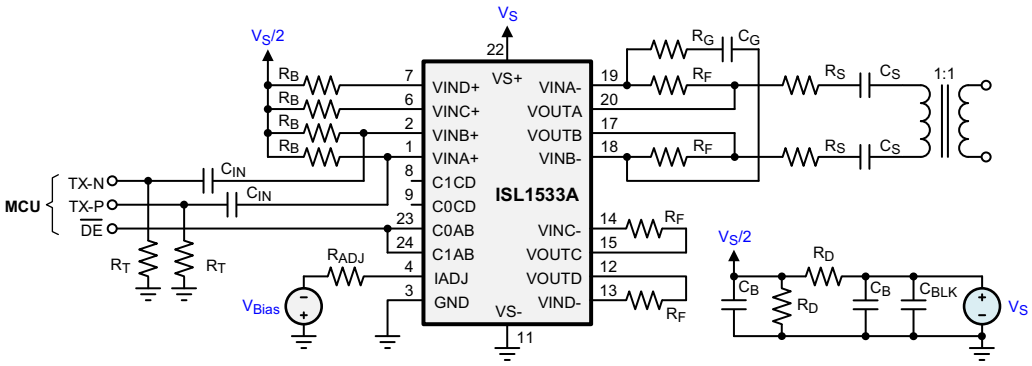


FIGURE 40. INCREASING BIAS CURRENTS FOR LOW SUPPLY VOLTAGE OPERATION

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Jan 31, 2019	FN8648.2	Added “Single Supply Operation in PLC Modems” section on page 13. Updated disclaimer.
Sep 17, 2018	FN8648.1	Added Related Literature section on page 1. Added Tape and Reel column to Ordering Information table on page 2. Changed θ_{JA} from 39 to 37 and θ_{JA} from 4.5 to 2.5 on page 4. Updated Power Control Function section on page 12. Changed package outline drawing from L24.4x5F-A to L24.4x5F. Updated new disclaimer. Removed About Intersil section.
May 9, 2014	FN8648.0	Initial Release

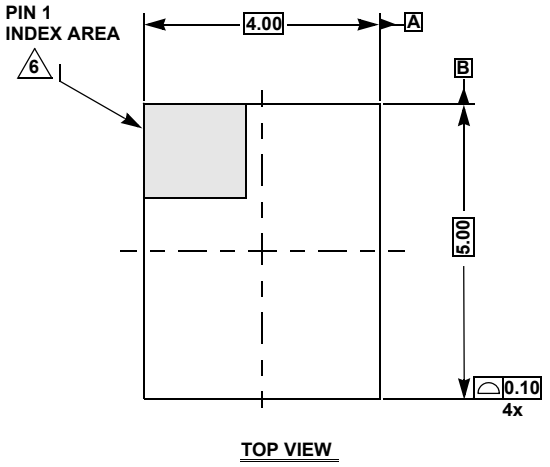
Package Outline Drawing

For the most recent package outline drawing, see L24.4x5F.

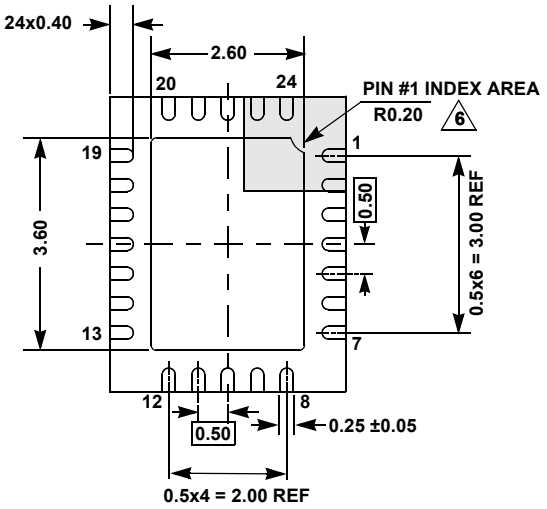
L24.4x5F

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

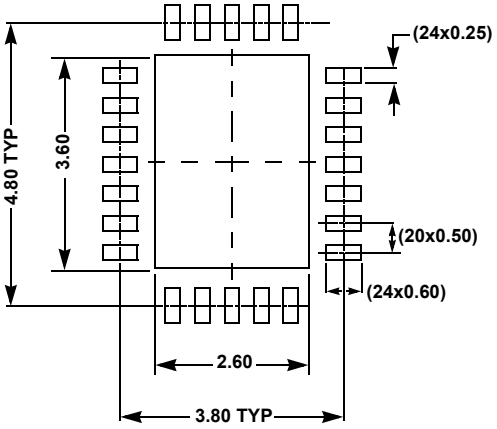
Rev 0, 5/14



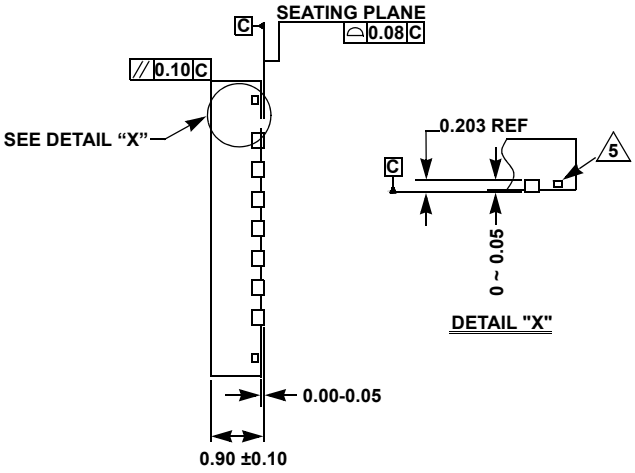
TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) are for Reference Only.
2. Dimensioning and tolerancing conform to ASMEY14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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