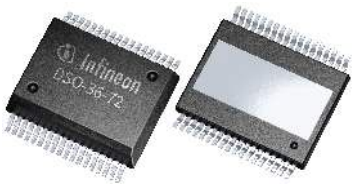
TLE92466ED

Six channel low-side solenoid driver IC

Quality Requirement Category: Automotive

Features



- Six independent low side channels with integrated MOSFETs (R_{DSon} = 115 mΩ)
- <1% current control accuracy
- Programmable setpoint from 0 mA to 1.5 A
- Load current including dither 1.8 A
- Current in parallel channel mode 2.7 A
- Integrated dither generator with programmable amplitude, frequency and waveform
- 15 bit current setpoint resolution
- Integrated sense resistor R_{SHUNT} = 140 mΩ
- Excellent immunity to large load supply voltage changes
- Operation down to 3.5 V at VDD pin
- 32 bit SPI with 8 bit CRC and SPI watchdog
- Sophisticated protection and diagnostic functions for each channel in on and off state
  - Independent thermal shutdown for each channel
  - Diagnostic Function (Open Load, Short Circuit Ground, Overcurrent)
  - Voltage monitoring
  - Overtemperature protection
- Two independent current feedback paths with fast measurement option
- Integrated system clock with clock watchdog
- Temperature range -40°C to 175 °C
- Small power package PG-DSO-36-72
- Green Product (RoHS compliant)
- Pb-free (RoHS compliant) package
- AEC-Q100 Grade 0 qualified
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL C

Potential applications

- Variable force solenoids (e.g. automatic transmission and e-Axle)
- Other constant current solenoids
  - Idle air control
  - Exhaust gas recirculation
  - Vapor management valve
  - Suspension control

Product validation

Qualified for automotive applications with higher temperature requirements. Product validation according to AEC-Q100, Grade 0.

Product type & package table

Product type	Package
TLE92466ED	PG-DSO-36 Dual-Gauge (300 mil)

Description

The TLE92466ED is a flexible, monolithic solenoid driver IC designed for the control of linear solenoids in automatic transmissions, electronic stability control and active suspension applications. The device includes the drive transistors and the current sensing resistors to minimize the number of external components.

The device controls the load current with less than 1% error. Target currents from 0 to 1500 mA can be programmed with a resolution of 15 bit. The device supports dither currents up to 1800 mA. The dither generator superimposes a triangular or trapezoidal waveform with programmable amplitude, frequency and shape on the programmed current setpoint. A 32 bit SPI interface is used to control the 6 channels and monitor the status of the diagnostic functions. The SPI communication is secured with an 8 bit CRC and a programmable timeout watchdog.

An active low reset input (RESN) is used to disable all channels and reset the internal registers to the default values. An active high enable pin (EN) enables or disables the output channels without disabling the SPI interface. A fault output pin (FAULTN) signal can be used as external interrupt to the microcontroller whenever a fault is detected.

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1 Block diagram

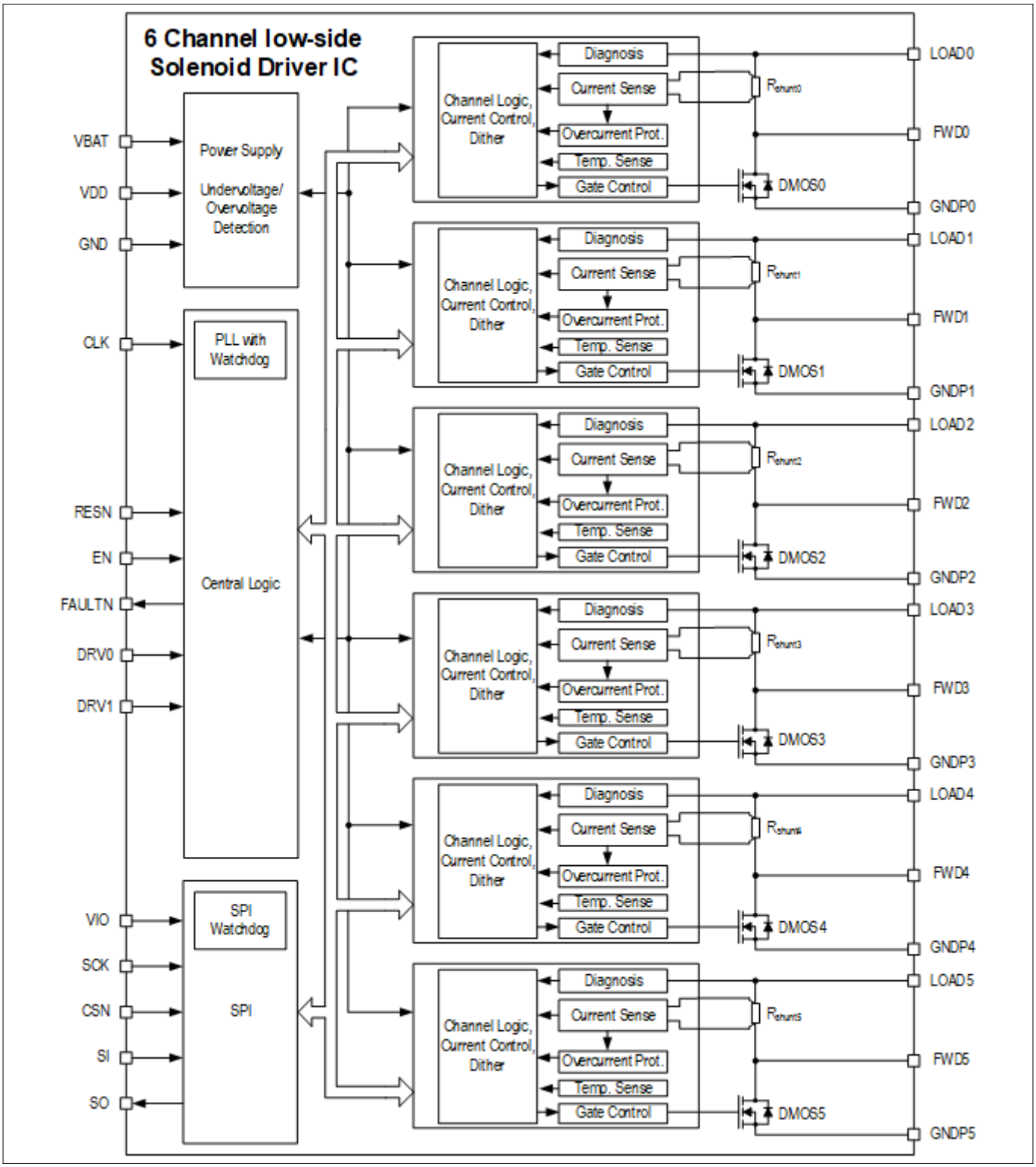


Figure 1 Block diagram

2 Pin configuration

Pin assignment

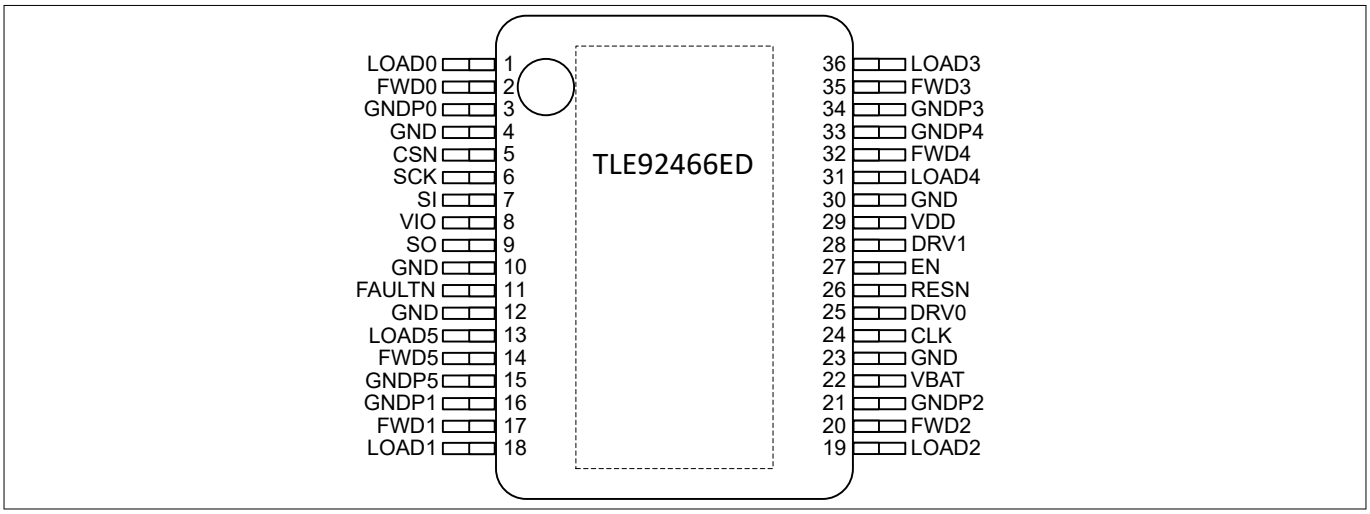


Figure 2 Pin assignment

Pin definitions and functions

Table 1 Pin definition and functions

Pin	Symbol	Function
1	LOAD0	Output; for channel 0.
2	FWD0	Free wheeling diode; for channel 0.
3	GNDP0	Ground; for channel 0 power stage.
4	GND	Ground; connect to GND.
5	CSN	SPI chip select input; digital input: 3.3 V or 5.0 V logic levels.
6	SCK	SPI clock input; digital input: 3.3 V or 5.0 V logic levels.
7	SI	SPI input; digital input: 3.3 V or 5.0 V logic levels.
8	VIO	Supply SPI Slave Out (SO) pin; connected to 3.3 V or 5.0 V supply.
9	SO	SPI output; push pull output compatible to 3.3 V or 5.0 V logic levels.
10	GND	Ground; signal ground. Internally connected to cooling tab.
11	FAULTN	Status output; open drain output. In case not used, keep open.
12	GND	Ground; signal ground. Internally connected to cooling tab.
13	LOAD5	Output; for channel 5.
14	FWD5	Free wheeling diode; for channel 5.
15	GNDP5	Ground; ground connection for channel 5 power stage.
16	GNDP1	Ground; ground connection for channel 1 power stage.
17	FWD1	Free wheeling diode; for channel 1.

(table continues...)

Table 1 (continued) Pin definition and functions

Pin	Symbol	Function
18	LOAD1	Output; for channel 1.
19	LOAD2	Output; for channel 2.
20	FWD2	Free wheeling diode; for channel 2.
21	GNDP2	Ground; ground connection for channel 2 power stage.
22	VBAT	Supply voltage; connected to battery voltage with reverse protection diode and filter against EMC.
23	GND	Ground; signal ground. Internally connected to cooling tab.
24	CLK	Clock input; Main system clock.
25	DRV0	Direct drive input: 3.3 V or 5.0 V logical levels.
26	RESN	Control input; digital input: 3.3 V or 5.0 V logic levels. Active low reset input.
27	EN	Control input; digital input: 3.3 V or 5.0 V logic levels. Active high enable input.
28	DRV1	Direct drive input: 3.3 V or 5.0 V logical levels.
29	VDD	Supply voltage; supplies digital circuits. Connected to 5.0 V supply voltage.
30	GND	Ground; signal ground. Internally connected to cooling tab.
31	LOAD4	Output; for channel 4.
32	FWD4	Free wheeling diode; for channel 4.
33	GNDP4	Ground; for channel 4 power stage.
34	GNDP3	Ground; for channel 3 power stage.
35	FWD3	Free wheeling diode; for channel 3.
36	LOAD3	Output; for channel 3.
37	Cooling Tap	Connect externally to GND and heat sink area

3 Electrial characteristics and parameters

3.1 Absolute maximum ratings

3.1.1 Absolute maximum voltage ratings

Table 2 Absolute maximum voltage ratings

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Max. supply voltage (VDD)	$V_{DD,max}$	-0.3	–	19	V	
Max. supply voltage (VBAT)	$V_{BAT,max}$	-0.3	–	40	V	
Max. supply voltage (VIO)	$V_{VIO,max}$	-0.3	–	19	V	
Max. digital input pin voltage (CLK, RESN, EN, DRVx, SCK, CSN, SI)	$V_{CLK,max}$ $V_{RESN,max}$ $V_{EN,max}$ $V_{DRVx,max}$ $V_{SCK,max}$ $V_{CSN,max}$ $V_{SI,max}$	-0.3	–	19	V	
Max. open drain output voltage (FAULTN)	$V_{FAULTN,max}$	-0.3	–	19	V	
Max. Push Pull Ouput (SO)	$V_{SO,max}$	-0.3	–	19	V	
Max. LOADx voltage	$V_{LOADx,max}$	-0.3[1)]	–	40	V	[1)] During negative pulses (V_{LOADx} < -0.3 V) the maximum energy of E_{LOADx} = |-V_{LOADx}*(I_{LOADx}+I_{FWDx})*t_{pulse}| <= 2 mJ shall not be violated.
Max. FWDx voltage	$V_{FWDx,max}$	-0.3[1)]	–	40	V	[1)] During negative pulses (V_{FWDx} < -0.3 V) the maximum energy of E_{FWDx} = |-V_{FWDx}*(I_{LOADx}+I_{FWDx})*t_{pulse}| <= 2 mJ shall not be violated.
Max. GNDPx voltage	$V_{GNDPx,max}$	-0.3	–	0.3	V	

3.1.2 Absolute maximum current ratings

Table 3 Absolute maximum current ratings

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Max. current range	$I_{FWDx,max}$ $I_{LOADx,max}$	-2	–	2	A	DC In the case of an active overcurrent shutdown the specification at the LOADx pin can be exceeded.
Max. Output Current (FAULTN)	$I_{FAULTN,max}$	-5	–	0	mA	
Max. output current (SO)	$I_{SO,max}$	-5	-	5	mA	DC
Max. input current (CLK, RESN, EN, DRVx, SCK, CSN, SI)	$I_{CLK,max}$ $I_{RESN,max}$ $I_{EN,max}$ $I_{DRVx,max}$ $I_{SCK,max}$ $I_{CSN,max}$ $I_{SI,max}$	-5	0	5	mA	Maximum allowed forward and reverse current through ESD structure.

3.1.2.1 TDS_max_rating

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.1.3 Absolute maximum temperature ratings

Table 4 Absolute maximum temperature ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction temperature (TJ)	T_J	-40	–	150	°C	
Extended junction temperature (TJ extended)	T_{Jext}	150	–	175	°C	parameter deviations are possible

(table continues...)

Table 4 (continued) Absolute maximum temperature ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Storage temperature (TSTG)	T_{STG}	-55	–	150	°C	

3.1.4 ESD Robustness

Table 5 ESD Robustness

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD robustness HBM (all pins)	V_{HBMall}	-2	–	2	kV	ESD robustness Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001.
ESD robustness HBM (VBAT, LOADx)	$V_{HBMglobal}$	-4	–	4	kV	VBAT, LOADx vs. all Grounds shorted ESD robustness Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001.
ESD robustness CDM (all pins)	V_{CDMall}	-500	–	500	V	ESD robustness Charged Device Model (CDM) according to JEDEC JESD22-C101
ESD robustness CDM (corner pins)	$V_{CDMcorner}$	-750	–	750	V	ESD robustness Charged Device Model (CDM) according to JEDEC JESD22-C101

3.2 Functional range

3.2.1 Functional range

Table 6 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Functional range (VDD)	V_{DD}	4.5	–	5.5	V	
Extended Functional range (VDD)	$V_{DD,ext}$	3.5	–	19	V	Outside of the normal Functional Range of V_{DD}: • $V_{DD} < V_{DD,UV,TH}$: SPI communication functional;Power-stage off • $V_{DD} > V_{DD,OV,TH}$: SPI communication functional; Power-stage off
Functional range (VBAT)	V_{BAT}	6	–	18	V	

(table continues...)

Table 6 (continued) Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Extended functional range (VBAT)	$V_{BAT,ext}$	4	–	38	V	Outside of the normal functional V_{BAT} range parameter deviations are possible: • V_{BATL} 4 V…6 V: Parameter deviation possible • V_{BATH} 18 V…38 V: Parameter deviation possible
Functional range (VIO)	V_{IO}	3.0	–	5.5	V	
Extended functional range (VIO)	$V_{IO,ext}$	5.5	–	19	V	Parameter deviation possible
Functional range (FWDx)	V_{FWDx}	-0.3[1)]	–	40	V	[1)] During negative pulses (V_{FWDx} < -0.3 V) the maximum energy of E_{FWDx} = |-V_{FWDx}*(I_{LOADx}+I_{FWDx})*t_{pulse}| <= 2 mJ shall not be violated.
Functional range (LOADx)	V_{LOADx}	-0.3[1)]	–	40	V	[1)] During negative pulses (V_{LOADx} < -0.3 V) the maximum energy of E_{LOADx} = |-V_{LOADx}*(I_{LOADx}+I_{FWDx})*t_{pulse}| <= 2 mJ shall not be violated.
Functional range clock frequency (CLK)	f_{CLK}	1	–	8	MHz	
System clock frequency	f_{SYS}	27.5	28	28.5	MHz	For use of external clock, clock divider must be set accordingly
System clock watchdog	$f_{SYS,WD}$	27	–	29	MHz	
Target PWM frequency	f_{PWM}	110	-	4000	Hz	PWM frequency control configuration range
Junction temperature	T_J	-40	–	150	°C	
Extended junction temperature	$T_{J,ext}$	150	–	175	°C	In the temperature range of 150 - 175°C parameter deviations are possible

3.2.1.1 TDS_functional_range

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given by the related "electrical characteristics" table.

3.2.2 Parameter above 150°C

Table 7 Parameter above 150°C

T_J = 150°C to 175°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Shunt resistance	R_{shunt}	-	-	190	mΩ	
ON resistance	R_{DSON}	-	-	215	mΩ	
Average current control error, absolut	$I_{err,absolut}$	-6	–	6	mA	I_{set} = 10 - 500mA V_{BAT} = 13V Single channel operation
Average current control error, absolut - parallel	$I_{err.absolut,par}$	-12	-	12	mA	$I_{set,par}$ = 20 - 1000 mA V_{BAT} = 13V Parallel channel operation
Average current control error, relative	$I_{err.relative}$	-1.2	–	1.2	%	I_{set} > 500mA; single channel operation $I_{set,par}$ > 1000mA; parallel channel operation V_{BAT} = 13V
Diagnosis Current 0	I_{HS} I_{LS}	-	-	130	µA	<I_DIAG> = 00_B

3.2.3 Thermal resistance

Table 8 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction to case	R_{thJC}	–	–	3	K/W	
Junction to ambient	R_{thJA}	–	18.5	–	K/W	Depending on the mounting conditions. Specified R_{thJA} value is according to JEDEC JESD51 -5, -7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm, 2 x 35 µm CU).

4 Functional description

4.1 Power supply

4.1.1 TDS_Power Supply

VDD pin

The VDD pin and GND pin are the supply and ground pins for the digital circuit blocks. The current through these pins contain high frequency components. Decoupling with ceramic capacitors and careful PCB layout are required to obtain good EMC performance.

VIO pin

The VIO pin supplies the SPI output pin (SO). It should be connected to the I/O supply of the microcontroller (3.3 V or 5.0 V). The VIO voltage level can be configured by the <VIO_SEL> bit in the GLOBAL_CONFIG register.

VBAT pin

The VBAT pin is an input pin used to measure and monitor the battery voltage and feed diagnosis current source. The pin should be connected to the reverse protected battery rail and decoupled with a ceramic capacitor.

GND/GNDP pin

GND pins are the ground pins for the logic while the GNDP pins are the power ground pins for the power stages. It is recommended to connect all GNDP pins to the GND net externally.

Power On Reset

An internal power on reset (POR) circuit holds the device in a reset state if the internal logic is not operational due to undervoltage. The power on reset is released after all supplies are within their functional range and the Reset Duration Time t_{POR} has elapsed. The SPI interface can be accessed after the power on reset time. Any power on reset will set the bit <POR_EVENT> in the GLOBAL_DIAG0 register to 1. This can be used to check whether a power on reset has happened since the bit was set to 0.

4.1.2 TDS_Voltage monitoring

The voltage levels of the supply pins V_{BAT}, V_{IO} and V_{DD} and all internal voltages (ADC reference voltages, internal supply voltages) are monitored. A voltage fault is detected if a voltage exceeds the corresponding overvoltage (OV) threshold or falls below the respective undervoltage (UV) threshold. Apart from a VBAT OV/UV, an under/overvoltage fault disables the output stages by setting all <EN_CH> bits to "0". Apart from a V_{BAT} and internal pre-regulator (<VPRE_OV>) fault, an OV/UV fault condition causes the device to enter the Operation State Config Mode.

External supply voltage (V_{BAT}, V_{IO}, V_{DD}) faults are indicated by setting the corresponding indication bit in the GLOBAL_DIAG0 register to 1 while IC internal voltage faults are listed in the GLOBAL_DIAG1 register. Voltage fault indication bits are cleared on write only. The bit <SUP_NOK_INT> and < SUP_NOK_EXT> in the FB_STAT register provide a summarized indication if any internal or external voltage fault has been detected.

The under and overvoltage thresholds of V_{BAT} can be adapted and be set in the VBAT_TH register.

$$V_{BAT,UV,TH} = < VBAT\_UV\_TH > \cdot 0.16208\text{V}$$
$$V_{BAT,OV,TH} = < VBAT\_OV\_TH > \cdot 0.16208\text{V}$$

Equation 1

The measured voltages of V_{IO} and V_{DD} are provided in the FB_VOLTAGE1 register. The V_{BAT} voltage level can be readout from the FB_VOLTAGE2 register.

The voltage monitoring mechanism of external and internal voltages can be tested by setting the <UV_OV_SWAP> bit in the GLOBAL_CONFIG register to "1". If the test is successful, the OV/UV detection bits <VDD_OV/UV>, <VIO_OV/UV>, <VBAT_OV/UV>, <VDD2V5_OV/UV>, <VR_IREF_OV/UV>, <VPRE_OV> and

<REF_OV/UV> are set. The power on reset (POR) due to an under or overvoltage can be tested by setting the bits <V1V5_OV_TEST> or <V1V5_UV_TEST> in the GLOBAL_CONFIG register to "1".

4.1.3 Electrical characteristics power supply

Table 9 Electrical characteristics power supply

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VBAT current consumption normal mode	I_{VBAT}	–	–	1	mA	V_{BAT} = 18 V Diagnosis off
VBAT current consumption inactive mode	$I_{VBAT,inactive}$	–	–	10	µA	V_{BAT} = 18 V V_{DD} = 0 V = V_{IO}
VDD current consumption	I_{VDD}	-	30	40	mA	V_{DD} = 5.5 V
VIO current consumption	I_{VIO}	–	–	1	mA	V_{DD} = 5.5 V $V_{CSN} > V_{CSN,high}$
VBAT undervoltage threshold	$V_{BAT,UV,TH}$	(x*8-17)*0.01965	x * 0.16208	(x*8+17)*0.02087	V	x = <VBAT_UV_TH> V_{BAT} voltage is falling.
VBAT overvoltage threshold	$V_{BAT,OV,TH}$	(x*8-17)*0.01965	x*0.16208	(x*8+17)*0.02087	V	x = <V_BAT_OV_TH> V_{BAT} voltage rising.
VDD undervoltage threshold	$V_{DD,UV,TH}$	3.7	–	4.5	V	V_{DD} falling
VDD overvoltage threshold	$V_{DD,OV,TH}$	5.5	–	6.4	V	V_{DD} rising
VIO undervoltage threshold 3.3 V	$V_{IO,UV,3V3,TH}$	2.6	–	3	V	V_{IO} falling
VIO overvoltage threshold 3.3 V	$V_{IO,OV,3V3,TH}$	3.6	–	4.1	V	V_{IO} rising
VIO undervoltage threshold 5 V	$V_{IO,UV,5V,TH}$	3.7	–	4.5	V	V_{IO} falling
VIO overvoltage threshold 5 V	$V_{IO,OV,5V,TH}$	5.5	–	6.4	V	V_{IO} rising
Power on reset time initialized with RESN	t_{RESN}	–	–	0.1	ms	Logic circuits are functional after t_{RESN}

(table continues...)

Table 9 (continued) Electrical characteristics power supply

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power on reset time initialized with undervoltage reset	t_{POR}	–	–	10	ms	Logic circuits are functional after t_{POR}

4.2 Input / Output

4.2.1 TDS_Clock

The chip system clock f_{SYS} is generated by an integrated PLL (phase locked loop) and is used to clock the internal analog to digital converters and logic. The PLL can be either sourced by an internal oscillator or an external rectangular clock signal applied on the CLK-pin. The PLL clock source f_{CLK} can be selected by programming the <EXT_CLK> bit in the CLK_DIV register. Changing the clock source can only be done in Operation State Config Mode. During a change of the clock source, the clock watchdog is disabled and the <INIT_DONE> bit is cleared. After a successful transition of the clock source, the <INIT_DONE> bit in the FB_STAT register is set to 1 and the clock watchdog is enabled.

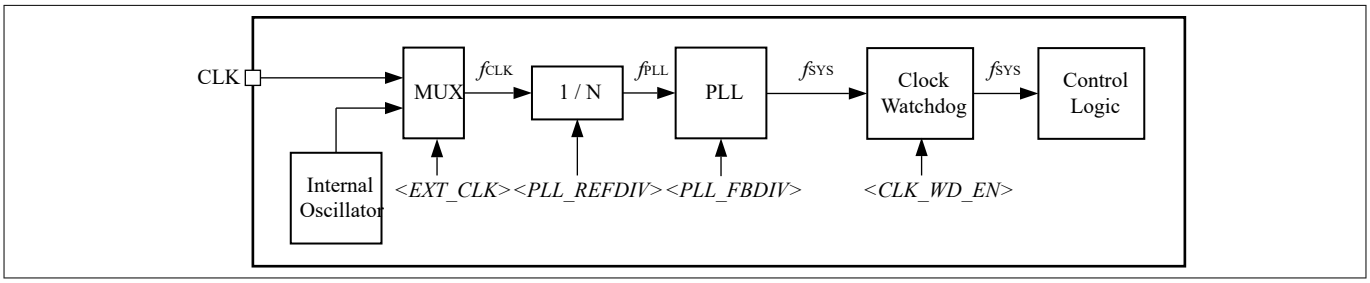


Figure 3 Clock Generation

The system clock frequency f_{SYS} is given by

$$f_{SYS} = f_{CLK} \cdot \frac{< PLL\_FBDIV >}{2 \cdot < PLL\_REFDIV >}$$

Equation 2

By selecting an external clock input, the PLL divider must be set to meet the system clock frequency f_{SYS} (see table "Clock control register settings"). If the internal clock oscillator is used, the contents of the divider bit fields are ignored. The values of PLL reference divider <PLL_REFDIV> and PLL feedback divider <PLL_FBDIV> are located in the CLK_DIV register.

$$< PLL\_REFDIV > = round\left(\frac{f_{CLK}}{1\text{MHz}}\right)$$

$$< PLL\_FBDIV > = \frac{56\text{MHz} \cdot < PLL\_REFDIV >}{f_{CLK}}$$

Equation 3

Table 10 Clock control register settings

f_{CLK} (MHz)	<PLL_REFDIV>	<PLL_FBDIV>	f_{SYS} (MHz)	Error (%)
1	1	56	28	0.00
1.5	1	37	27.75	-0.89
2	2	56	28	0.00
2.5	2	45	28.13	0.45
3	3	56	28	0.00
3.5	3	48	28	0.00
4	4	56	28	0.00
4.5	4	50	28.13	0.45
5	5	56	28	0.00
5.5	5	51	28.05	0.18
6	6	56	28	0.00
6.5	6	52	28.17	0.60
7	7	56	28	0.00
7.5	7	52	27.86	-0.51
8	8	56	28	0.00

4.2.2 TDS_Clock Watchdog

The internal system clock f_{SYS} can be supervised by a separate clock watchdog. The clock watchdog can be disabled by setting the <CLK_WD_EN> bit in the GLOBAL_CONFIG register to 0. A change of the clock watchdog configuration is only possible in Config Mode and if the <INIT_DONE> bit in the FB_STAT register is 1. If the system clock f_{SYS} is outside of the allowed frequency range $f_{SYS,WD}$, a clock watchdog fault is indicated by setting <CLK_NOK> in the GLOBAL_DIAG0 register to 1, all power stages are disabled and device enters the Config Mode. In case the clock watchdog detects a too fast clock, the device immediately enters the Critical Fault State.

4.2.3 TDS_I/O Pins

RESN pin

The RESN pin is an active low pin. If this pin is low, all channels are off, the device is in Reset State and all registers are set to their default values. The bit <RES_EVENT> in the GLOBAL_DIAG0 register indicates a reset triggered via the RESN pin. The RESN input pin is internally pulled low (GND).

EN pin

The EN pin is an active high pin. When this pin is low, all channels are turned off. The EN input pin is internally pulled low (GND).

FAULTN pin

The FAULTN pin is an open drain output. The FAULTN pin is initally high, if no fault is present after power up. The FAULTN pin is pulled low when the device transitions to the Critical Fault State, the RESN pin is low or an unmasked fault is detected. Fault inidication on the FAULTN pin can be masked by setting the appropriate mask bit in the FAULT_MASK registers.

- Channel specific:
  - CHx ICC regulation warning

  - CHx PWM regulation warning
  - CHx overtemperature warning
  - CHx open load
  - CHx short circuit battery
  - CHx short circuit ground
- Central overtemperature warning
- Central overtemperature error
- SPI watchdog error
- Clock too slow error
- Data error
- EN pin status indication
- Internal/External supply fault

CLK pin

A digital input clock signal f_{CLK} must be applied on the CLK pin if an external clock input is used. Using the internal clock, the pin should be connected to GND. The CLK input pin is internally pulled low (GND).

DRV pins

The DRV pins enable a direct control of the output stages, if the channel is configured to Direct Drive Mode via DRV pin. The DRV input pins are internally pulled low (GND). Unused DRV pins should be connected to GND.

SI, SO, CSN, SCK pin

The SI, SO, CSN, and SCK pins comprise the SPI interface. See SPI chapter for details.

4.2.4 Electrical characteristics I/O

4.2.4.1 Control inputs EN, RESN, CLK, DRVx

Table 11 Control inputs EN, RESN, CLK, DRVx

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital high threshold voltage (EN, RESN, CLK, DRVx)	$V_{EN,high}$ $V_{RESN,high}$ $V_{CLK,high}$ $V_{DRVx,high}$	2	–	-	V	
Digital low threshold voltage (EN, RESN, CLK, DRVx)	$V_{EN,low}$ $V_{RESN,low}$ $V_{CLK,low}$ $V_{DRVx,low}$	-	–	0.8	V	
Digital input hysteresis (EN, RESN, CLK, DRVx)	$V_{IN\_HYS,EN}$ $V_{IN\_HYS,RESN}$ $V_{IN\_HYS,CLK}$ $V_{IN\_HYS,DRVx}$	-	50	-	mV	
Pull down current (EN,	$I_{PD,EN}$ $I_{PD,RESN}$ $I_{PD,CLK}$	10	–	50	µA	V_{IN} = 0.8 V

(table continues...)

Table 11 (continued) Control inputs EN, RESN, CLK, DRVx

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RESN, CLK, DRVx)	$I_{PD,DRVx}$					

4.2.4.2 FAULTN

Table 12 FAULTN

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output low threshold voltage (FAULTN)	$V_{FAULTN,LOW}$	0	–	0.4	V	I_{FAULTN} = 2 mA
Output leakage current (FAULTN)	$I_{FAULTN,LGK}$	-100	–	100	µA	No fault present 0 V < V_{FAULTN} < V_{IO}

4.3 IC Operation states

4.3.1 TDS_IC Operation states

Reset state:

- The answer to an SPI command is the 16 bit reply frame.
- All SPI register values are being reset to default when the product leaves the Reset State.

Config Mode:

- All channels are disabled. <EN_CH> bits are 0 and cannot be set.
- Channel diagnostic is disabled (HS and LS current source are disabled).
- The Channel Mode, the global configuration, the parallel channel operation and the PLL divider can only be configured in Config Mode.

Mission Mode:

- The channels and their respective diagnosis are only functional in Mission Mode.

Critical Fault state:

- The IC will reply all SPI interactions with the Critical Fault frame.
- The FAULTN pin is pulled low.

The following State Diagram gives an overview on the transition conditions.

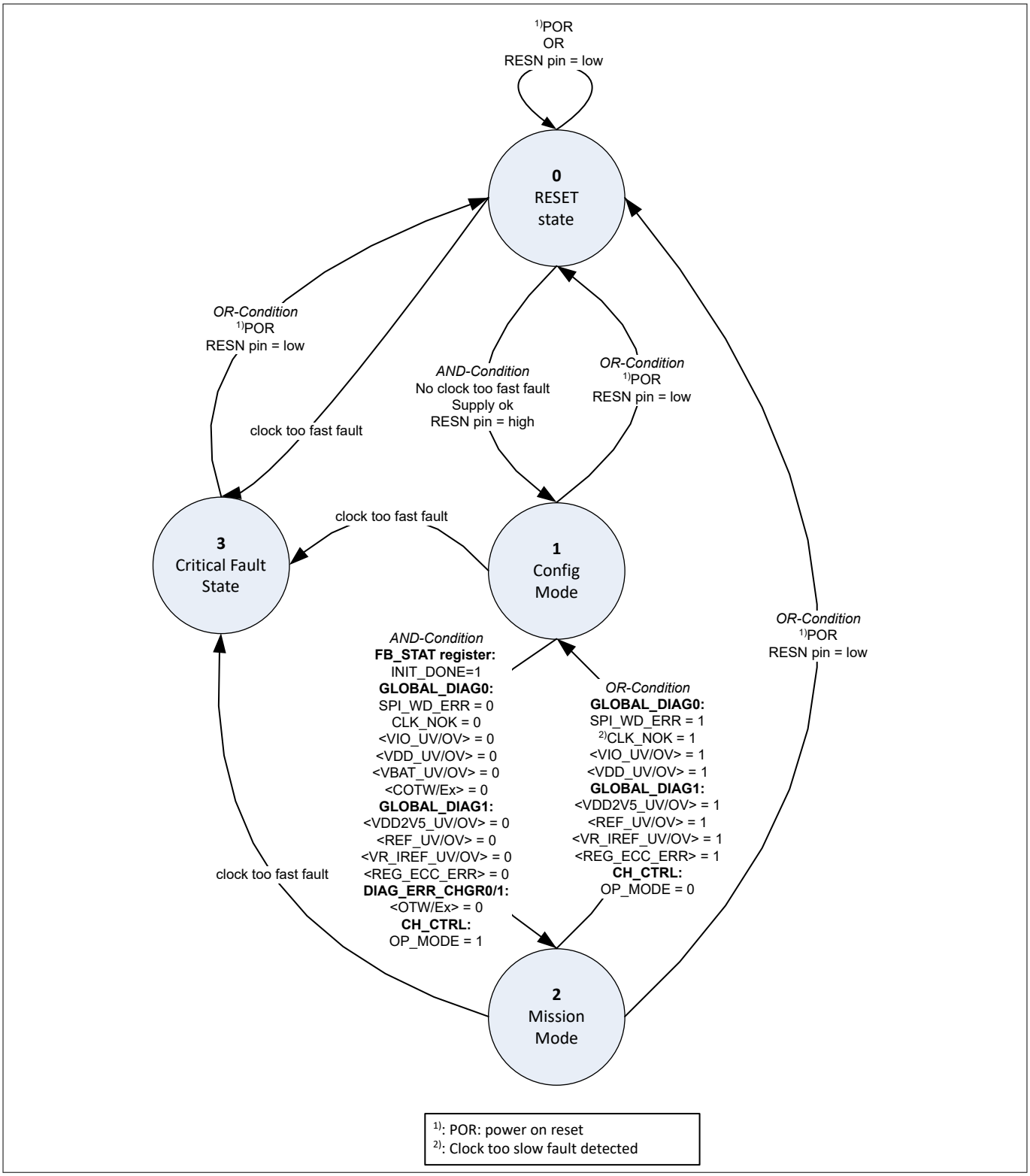


Figure 4 Operation States and Transitions

4.4 Channel modes

4.4.1 TDS_Channel Modes

The IC offers different modes to control the output stage of a channel. The channel mode can be selected by programming the MODE register. A change of the channel mode is only possible in Config Mode. The measurment period T_{meas} for averaged feedback values depends on the selected channel mode (see chapter "current supervision").

4.4.2 Channel Modes

Channel Mode	Measurement Period T_{meas} for Feedback Values
Channel off	No measurement active
Current Control ICC	Dither Period T_{Dither}
Direct Drive via on-time (TON register)	Dither Period T_{Dither}
Direct Drive via DRV pin	• If configured Dither Period T_{Dither}, else • Time between two rising edges at DRV pin
Measurement Mode*	Dither Period T_{Dither}

4.4.3 TDS_Measurement Mode - (4/6CHx)

Note: The current measurement over the shunt can be used for high-precision current measurement applications. In measurement mode the internal low-side switch is non-conductive.

4.4.4 TDS_Additional Information Channel Modes

Note: For more details on the "Current Control" and "Direct Drive" Mode please refer to the respective chapters.

4.5 Power stages

4.5.1 TDS_Channel overview - (6CHx)

There are six independent output channels implemented in this device. The output powerstage of each channel consists of a low side n-channel DMOS transistor and a current sensing resistor. The switch and shunt resistor are protected from external failures by built in overcurrent and overtemperature detection circuits. A high-side load can be connected to the LOADx pin. For inductive loads a diode must be applied at the FWDx pin for external freewheeling. The output current slew rate of the power stages can be programmed in the CH_CONFIG register.

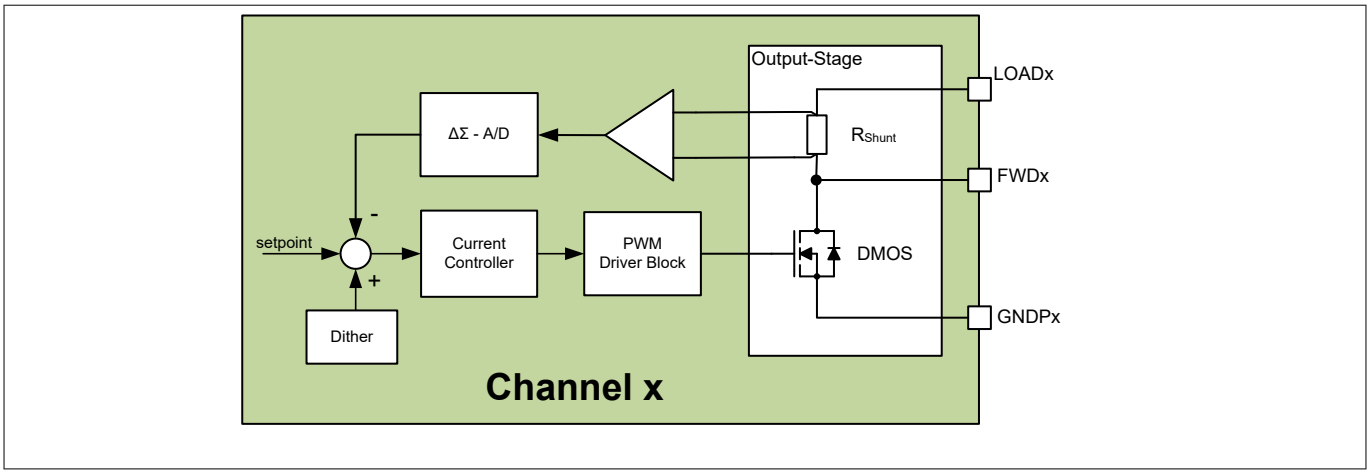


Figure 5 Channel Block Diagram

4.5.2 TDS_Parallel channel operation - (6CHx)

The IC features a parallel mode of output stages to increase the maximum current capability of the device. The channels 0/3, 1/2 and 4/5 can be connected in parallel. Channel 0, 1 and 4 are the master channels and channel 2, 3 and 5 are the slave channels. Only the master channels can be configured via SPI. The parallel channel mode can be enabled or disabled in the CH_CTRL register when the device is in Config Mode.

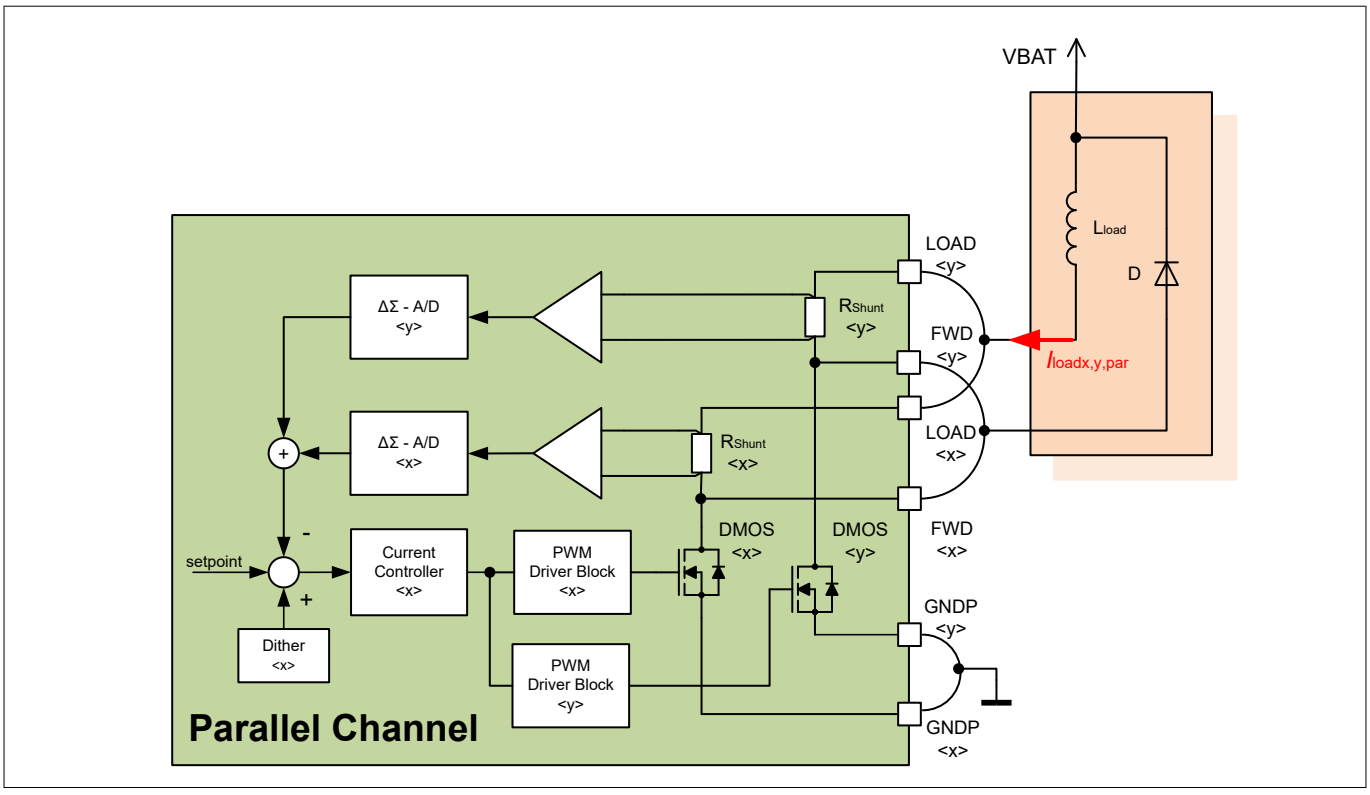


Figure 6 Parallel Channel Configuration

Slave channel

The current controller and the OFF-state diagnosis of the slave channel are disabled. A write access to the MODE register of the slave channel is ignored and reads back zero. The slave channel´s SETPOINT register cannot be set and is read back as zero. All feedback registers of the slave channel have to be disregarded. A write to a slave <EN_CH> bit is ignored and 0 is read back. After disabling the parallel channel mode the slave channel must be re-configured to the desired channel behaviour.

Setpoint

In parallel channel mode, the programmed setpoint of the master channel is used. Hence the LSB (least significant bit) of the setpoint is doubled.

Diagnostic functions

The LSB of the fixed OLSG (open load/short to GND) threshold is scaled by a factor of two. The OC (overcurrent) protection feature is active on the master as well as on the slave channel. If either the master or the slave channel detects an OC fault, both channels are disabled.

Feedback functions

The current feedback in the FB_I_AVG register represent the summed up current over the shunt resistors of the master and slave channel. The duty cycle feedback can be read from the master channel.

4.5.3 Electrical characteristics power stages

Table 13 Electrical characteristics power stages

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Shunt resistance	R_{shunt}	–	140	185	mΩ	
ON resistance	R_{DSON}	-	115	200[1)]	mΩ	[1)] T_J = 150°C, I_{LOADx} = 2.0 A
Leakage current (LOADx, FWDx)	$I_{LOADx,LKG}$ $I_{FWDx,LKG}$	-100	–	100	µA	V_{BAT} = 18 V; Setpoint = 0 mA; Diagnosis off
Slew rate 0	SR0	0.5	1	2	V/µs	V_{BAT}=14V; R_{LOAD}=10Ω 20% to 80% of applied load voltage <SLEWR> = 00_B
Slew rate 1	SR1	1.25	2.5	5	V/µs	V_{BAT}=14V; R_{LOAD}=10Ω 20% to 80% of applied load voltage <SLEWR> = 01_B
Slew rate 2	SR2	2.5	5	10	V/µs	V_{BAT}=14V; R_{LOAD}=10Ω 20% to 80% of applied load voltage <SLEWR> = 10_B
Slew rate 3	SR3	5	10	20	V/µs	V_{BAT}=14V; R_{LOAD}=10Ω 20% to 80% of applied load voltage <SLEWR> = 11_B

4.6 Current control

4.6.1 TDS_Average current setpoint

The average current setpoint is determined by the contents of <TARGET> in the SETPOINT register. The accuracy band of the current regulation is shown in the figure below. The accuracy is specified over the normal operating range of the device (including the normal operating junction temperature range).

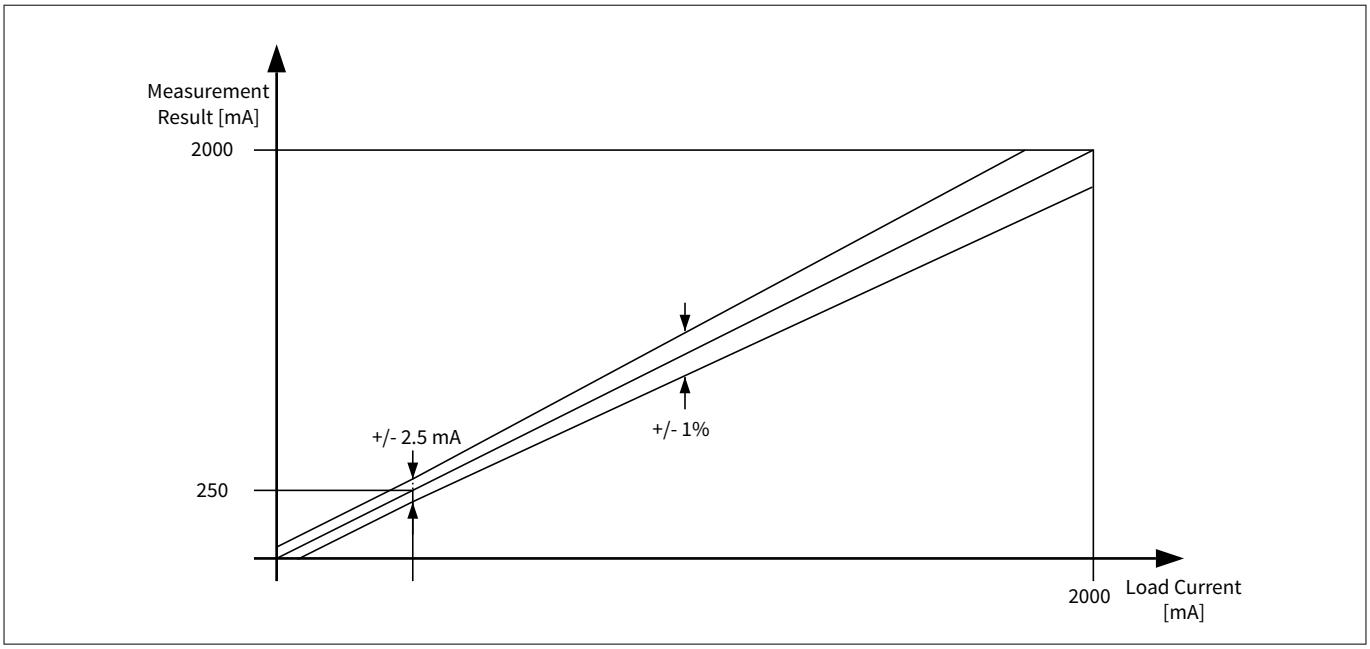


Figure 7 Current Accuracy

4.6.2 Integrating Current Controller (ICC)

4.6.2.1 TDS_Integrating Current Controller (ICC)

The current controller regulates the load current automatically to a user defined setpoint by turning on and off the internal transistor. If the internal transistor is switched on, the current through the inductive load will increase. If the internal transistor is turned off, the current will continue to flow through the recirculation diode gradually decay.

The Integrating Current Controller (ICC) is based on the requirement that the integrated current error over one PWM cycle is zero. This means that the average current after one PWM cycle exactly equals the targeted current. The controller integrates the current deviation (difference between load current and the setpoint) and switches the output stage accordingly: While the integrated current deviation is below a configurable integrator threshold, the power stage is turned on. In this phase the load current will increase. When the integrated current error exceeds the determined integrator threshold the power stage is turned off and the current recirculates through the freewheeling diode. The average current is reached when the integrated current deviation crosses zero which determines the start of a new PWM cycle. The ICC switching characteristic provides the physically fastest current response which makes it very robust against load voltage dips.

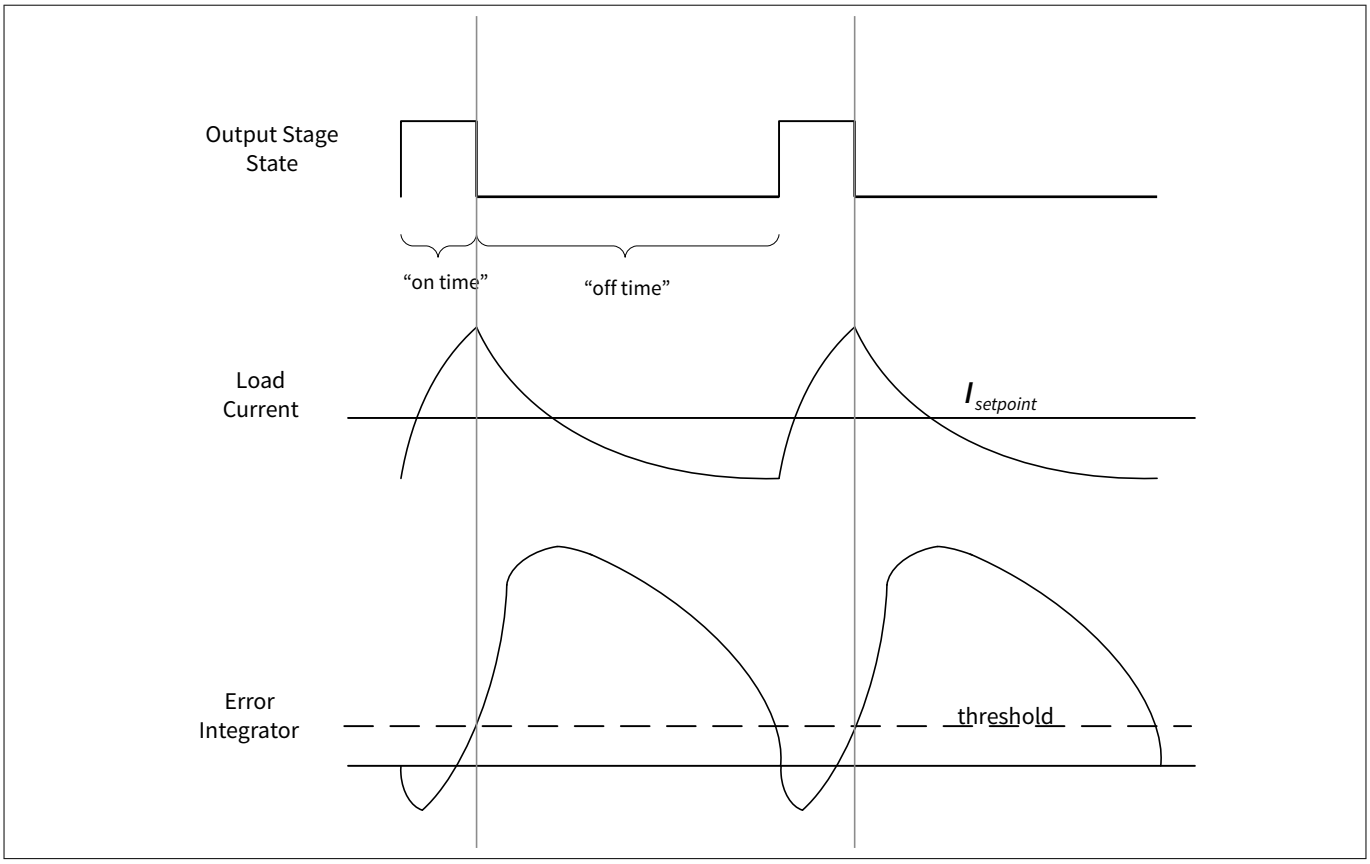


Figure 8 Current Control Waveform

4.6.2.2 TDS_Integrator Limits

The ICC integrator can be saturated in order to avoid an integrator windup. The integrator limits are configurable via +/-<LIM_VALUE_ABS> in the INTEGRATOR_LIMIT register.

In order to avoid current overshoots after setpoint changes the Autolimit feature is introduced. The device limits the integrator value to +/-<AUTO_LIM_VALUE_ABS> (INTEGRATOR_LIMIT register) for a maximum of two PWM cycles after a setpoint change. After the completion of Autolimit, the ICC automatically revert back to the normal integrator limit values +/-<LIM_VALUE_ABS>. The Autolimit feature is disabled by writing a 1 to the <AUTO_LIMIT_DIS> bit in the SETPOINT register.

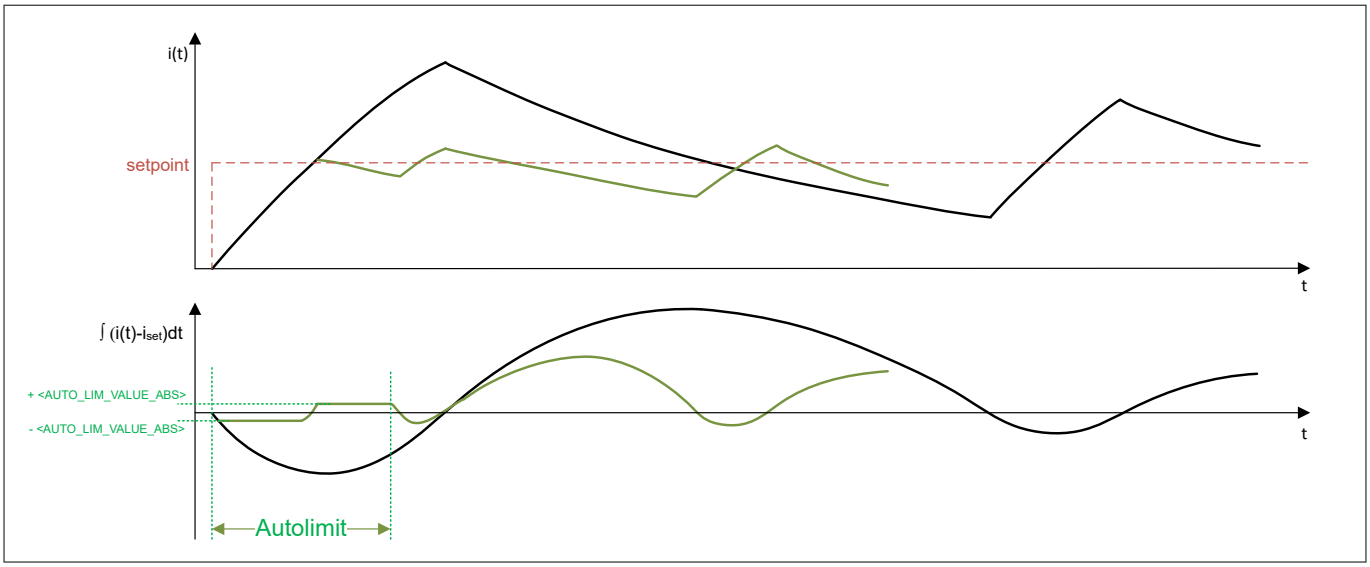


Figure 9 Autolimit feature

4.6.2.3 TDS_PWM Frequency Control

The load characteristic and load supply voltage affecting the PWM output frequency of the ICC controller. The on-time of the LS-FET and therefore the PWM cycle can be adjusted by modifying the integrator threshold value. A greater integrator threshold ends up in a longer on-time. Although the configured integrator threshold value is positive, the actual threshold can get negative since it is referenced to the lowest current deviation integral value captured during the on-phase. This means very short on-time configurations are possible. The shortest on-time is determined by limiting the integrator threshold to a minimum value configurable via <MIN_INT_THRESH> in the CTRL register.

There are two options to set the integrator threshold to adjust the PWM frequency.

Manual setting of On-time

The driver on-time and therefore a target PWM period can be set manually by programming a fixed integrator threshold <INT_THRESH> in the CTRL_INT_THRESH register. The PWM frequency controller has to be disabled by setting <PERIOD_MANT> in the PERIOD register to 0.

Automatic PWM control

The PWM frequency controller regulates the PWM frequency using an “Integral” control loop with a programmable gain, KI. This control loop monitors the actual PWM period and compares substracts it from the PWM period target setting in the PWM period register. The error in the PWM period is multiplied by the gain KI and then integrated at each PWM cycle. The output of the controller adjusts the on-time of the PWM signal until the actual PWM period matches the programmed PWM period. The internal PWM frequency controller can be activated by setting a target PWM period T_{period} in the PERIOD register.

$$T_{period} = \frac{< PERIOD\_MANT > \cdot 2^{< PERIOD\_EXP >}}{f_{SYS}}$$

Equation 4

By setting the bit <LOW_FREQ_RANGE_EN> the range of the configurable target PWM frequency is lower and can be calculated as follow.

$$T_{period} = \frac{< PERIOD\_MANT > \cdot 8 \cdot 2^{< PERIOD\_EXP >}}{f_{SYS}}$$

Equation 5

The bitfield <INT_THRESH> in the CTRL_INT_THRESH register determines the integrator threshold used after setpoint changes or activation of the PWM controller. The <INT_THRESH> value must be configured before applying the new setpoint. The resulting threshold calculated by the PWM frequency controller can be retrieved from the FB_INT_THRESH register. The threshold calculated by the PWM frequency controller can be read back from the FB_INT_THRESH register. The threshold value can be used to program <INT_THRESH> to reduce the settling time of the PWM frequency controller e.g. after a setpoint change.

Note: The Autolimit threshold must be greater than the lower threshold limit configuration for a correct ICC functioning (<AUTO_LIM_VALUE_ABS> > <MIN_INT_THRESH>+0x3).

The PWM frequency control parameter KI can be set by <PWM_CTRL_PARAM> in the PERIOD register. The integrator parameter KI determines the gain and therefore the speed of the PWM frequency control loop. A KI value of 0 results in a slower but more stable PWM control.

During steep dither settings, long off-times can appear which end up in high frequencies in the next rising dither slope. The frequency controller does not consider falling dither slopes by setting the <PWM_PERIOD_CALC_MODE> in the CTRL register.

4.6.2.4 TDS_PWM regulation warning

An ICC PWM regulation warning is issued if the ICC integrator value drops below the minimum integral value, which was captured during the on-phase. This can happen i.e. if a negative absolute integrator threshold is calculated from the PWM control and the inertia of the load is too large. This means the integrated current deviation could not exceed the zero level and therefore the power stage would not switch on anymore.
A negative integrator threshold can be avoided by programming <MIN_INT_THRESH> in the CTRL register to a value greater than 1. A recovery process maintains the current regulation by triggering the Autolimit feature. After finishing Autolimit, the integrator threshold configured in <INT_THRESH> bitfield is used. The PWM regulation warning is signaled by asserting the <PWM_REG_WARN> bit in the DIAG_WARN_CHGR register.

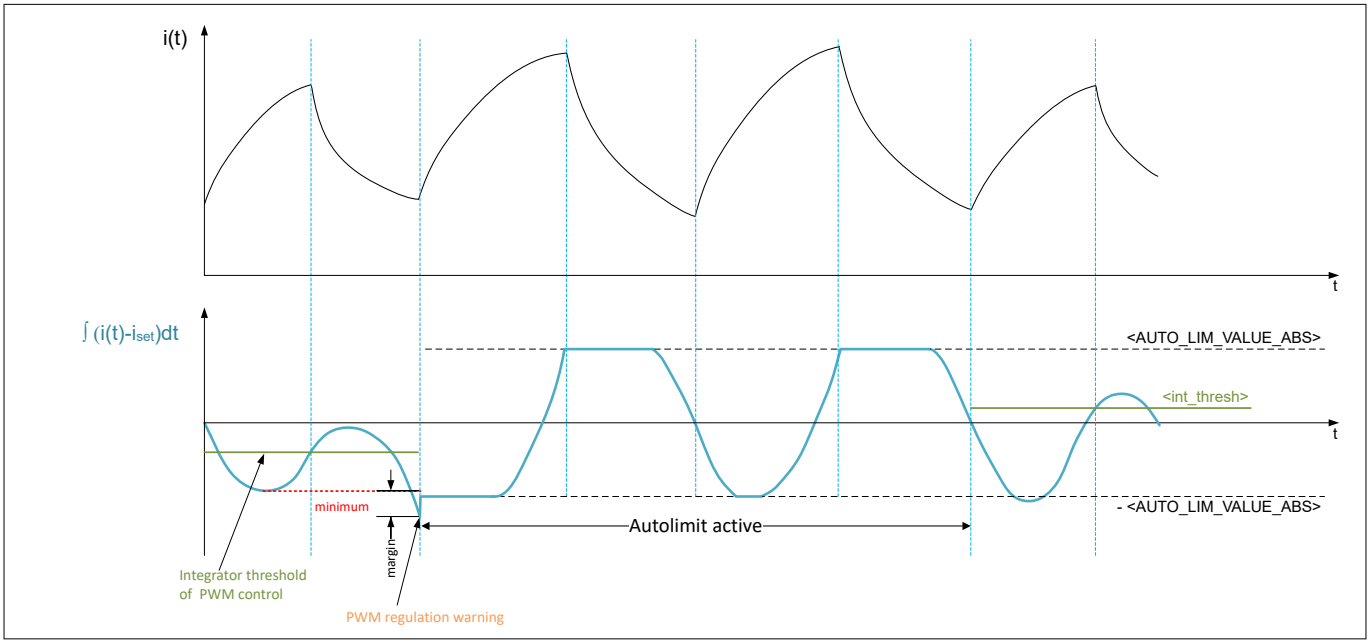


Figure 10 ICC PWM regulation warning

4.6.2.5 TDS_Current regulation warning

An ICC current regulation warning occurs if the ICC integrator value reaches the absolute integrator limit <LIM_VALUE_ABS> located in the INTEGRATOR_LIMIT register. This can happen for example during a voltage supply dip. A recovery process maintains the current regulation by triggering the Autolimit feature. The integrator threshold will be reset to <INT_THRESH> located in the CTRL_INT_THRESH register. The warning is signaled by asserting the respective <I_REG_WARN> bit in the DIAG_WARN_CHGR register.

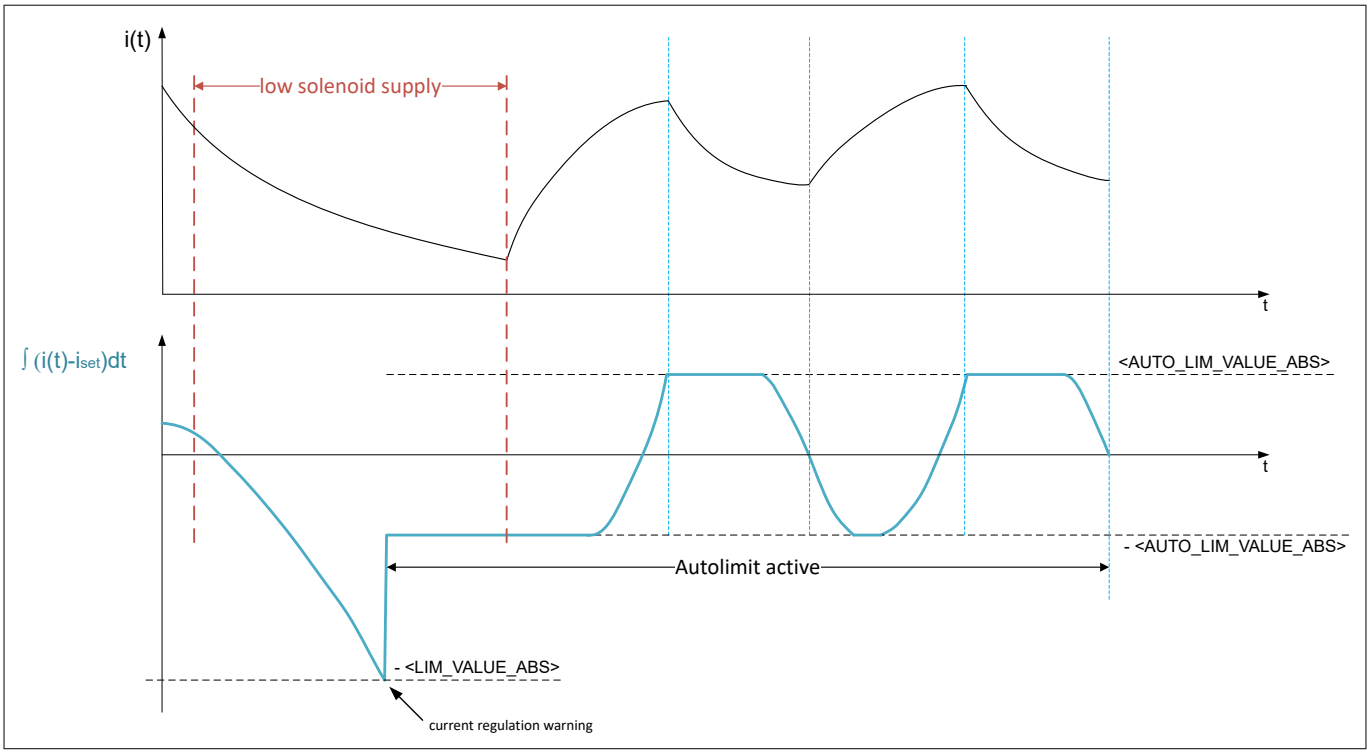


Figure 11 ICC current regulation warning

4.6.3 Electrical characteristics current control

Table 14 Electrical characteristics current control

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Average current control error, absolut	$I_{err.absolut}$	-2.5	–	2.5	mA	I_{set} = 10 - 250mA Single channel operation
Average current control error, absolut - parallel	$I_{err.absolut,par}$	-5	-	5	mA	$I_{set,par}$ = 20 - 500 mA Parallel channel operation
Average current control error, relative	$I_{err.relative}$	-1	–	1	%	I_{set} > 250mA; single channel operation $I_{set,par}$ > 500mA; parallel channel operation
Load current	I_{set}	0	–	1500	mA	DC setpoint current Single channel operation
Dither current	I_{set}+ I_{Dither}	0	–	1800	mA	DC setpoint current incl. dither current amplitude Single channel operation
Measurement current	I_{LOADx}	0	–	2000	mA	DC setpoint incl. dither current amplitude and overshoot Single channel operation

(table continues...)

Table 14 (continued) Electrical characteristics current control

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
						The user must take care that the maximum value is not exceeded
Measurement current - parallel	$I_{LOADx,y,par}$	0	-	2700	mA	DC setpoint current incl. dither current amplitude and overshoot Parallel channel operation Single channel measurement range I_{LOADx} of each Channel shall not be violated

4.7 Dither

4.7.1 TDS_Dither configuration

A configurable dither waveform can be added to the average current setpoint in order to reduce the hysteresis of a driven solenoid valve. The dither operation is an overlay of a triangular or trapezoidal waveform over the current setpoint. The dither waveform is generated by permanently changing the setpoint according to the programmed shape.

The dither shape can be configured by setting the <STEPS>, <STEP_SIZE> and <FLAT> values in the DITHER_STEP and DITHER_CTRL register. The <STEP_SIZE> value scales the height of each dither step where the LSB is equal to <TARGET> in the setpoint register. The value of <STEPS> determines the number of steps for the rising and falling edge of each half cycle of the dither waveform. The value of <FLAT> determines the number of flat steps at the minimum and maximum plateau of the dither waveform.

The amplitude of the dither waveform overlay I_{Dither} can be calculated as follows.

$$I_{Dither} = < \text{STEPS} > \cdot < \text{STEP\_SIZE} > \cdot \frac{2\text{A}}{2^{15} - 1}$$

Equation 6

Care should be taken that no negative dither amplitude (I_{set} - I_{Dither} > 0) is configured and possible overshoots are not violating the specified measurement current range I_{LOADx} or $I_{LOADx,par}$ (parallel channel operation). The dither overlay I_{Dither} is deactivated if the target setpoint is set to 0.

The Dither period T_{Dither} is a muliple of the Dither reference clock determined by the values of <MANT>, <EXP> of the DITHER_CLK_DIV register. The dither period T_{Dither} and dither reference clock t_{ref_clk} can be calculated as follows.

$$T_{Dither} = (4 \cdot < STEPS > + 2 \cdot < FLAT >) \cdot t_{ref\_clk}$$

Equation 7

$$t_{ref\_clk} = \frac{< MANT > \cdot 2^{< EXP >}}{f_{SYS}}$$

Equation 8

$$t_{flat} = < FLAT > \cdot t_{ref\_clk}$$

Equation 9

Note: If <STEPS> = 0 and <FLAT> = 0, the dither period T_{Dither} = t_{ref_clk}

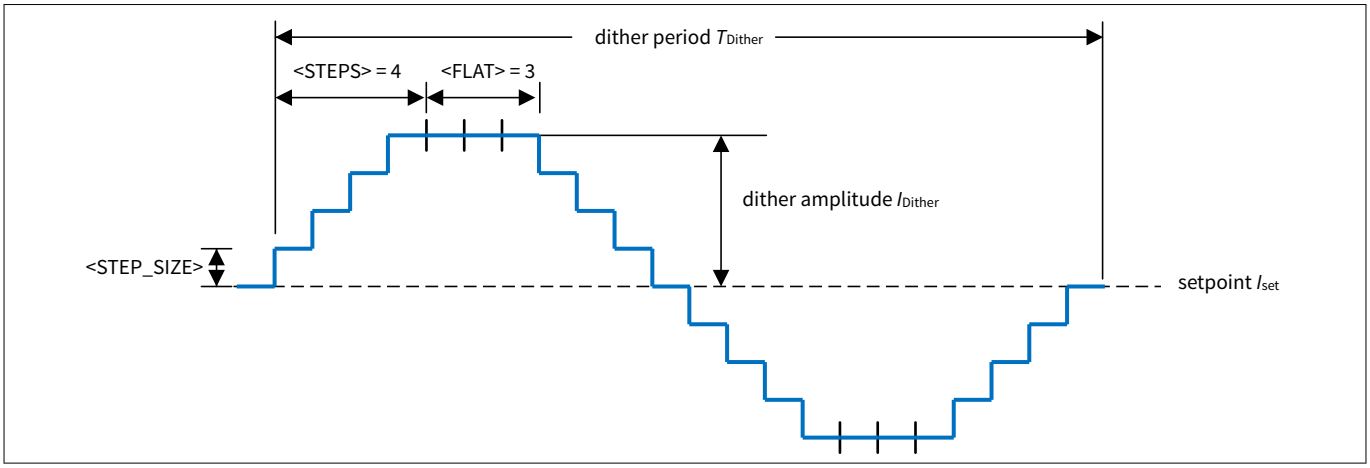


Figure 12 Dither Waveform Configuration

4.7.2 TDS_Dither parameter update

All dither parameters located in registers DITHER_STEP and DITHER_CTRL become active at the start of the next dither period after writing to the DITHER_CTRL register. After triggering an update event (write to DITHER_CTRL) within the active dither period, the dither configuration (DITHER_STEP/ DITHER_CTRL) that was transmitted last within the active dither period is taken over. An update of the reference clock t_{ref_clk} controlled by the DITHER_CLK_DIV register takes immediate effect. If the dither amplitude is disabled by clearing <STEP_SIZE>, the active dither period will be completed. The configured dither period and overlay is immediately (re)-started if the <EN_CH> bit transitions to 1.

4.7.3 TDS_Dither PWM synchronization

The dither-PWM synchronization starts a new dither period synchron with the start of the next PWM cycle to enable the same starting conditions for each dither period. The start of a PWM cycle period is defined as a turn on of the output stage. The start of a dither period is defined to be when the dither increases one step above zero on this rising slope of the dither waveform. The dither-PWM synchronization can be enabled by setting the <DITHER_PWM_SYNC_EN> bit in the DITHER_CLK_DIV register. When the <DITHER_PWM_SYNC_EN> bit is set to 0, the dither waveform is free-running and asynchronous to the PWM frequency.

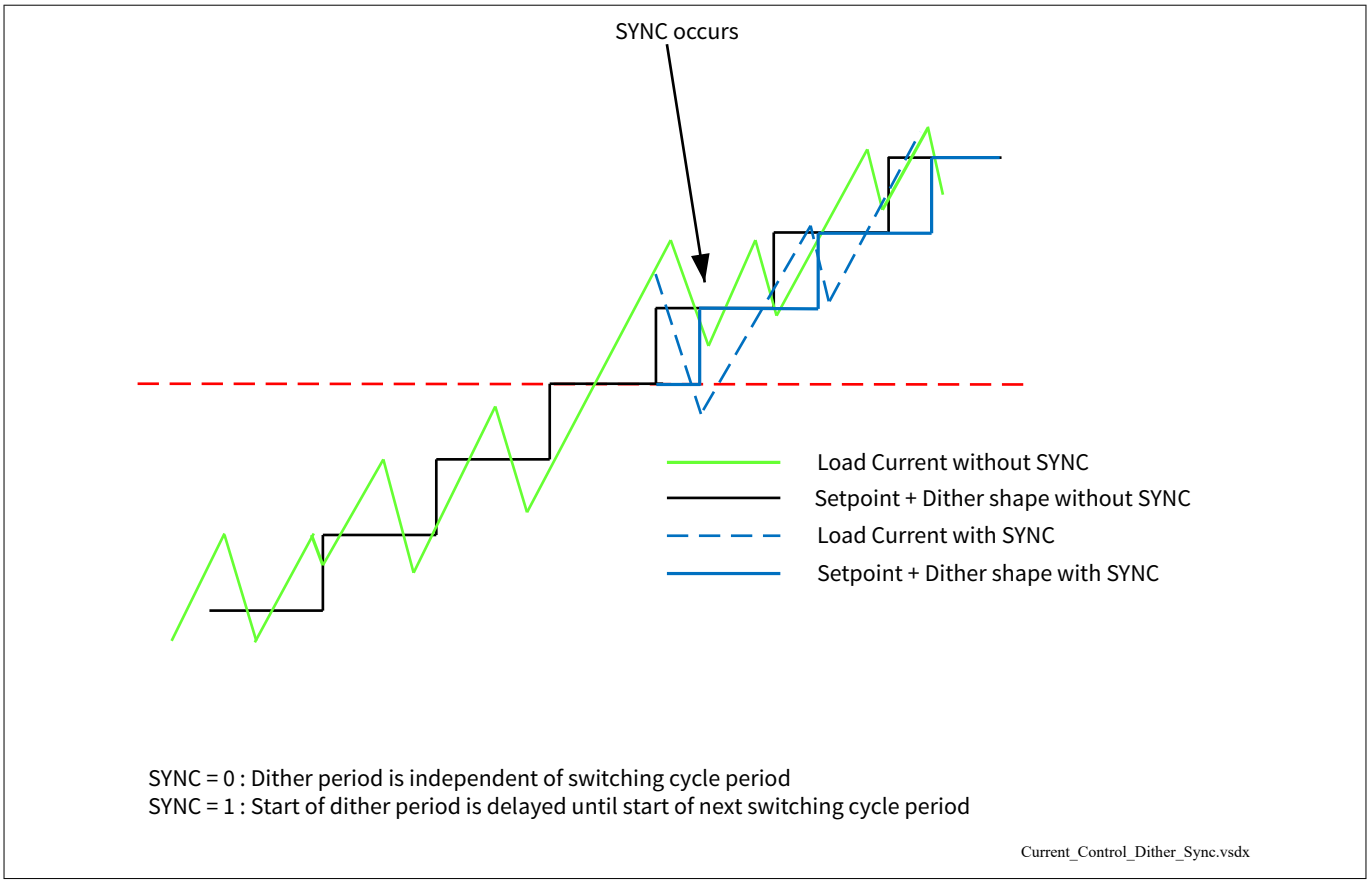


Figure 13 Dither sync

4.7.4 TDS_Only ICC

Note: This feature is only available in ICC Channel Mode.

4.7.5 TDS_Dither setpoint synchronization

The dither-setpoint synchronization feature updates the averaged feedback values of a channel (FB_DC, FB_I_AVG, FB_VBAT) after a change in setpoint in the shortest possible time. The dither-setpoint synchronization restarts the dither period when the newly applied setpoint has been reached. Therefore, the measurement period T_{meas} (dither period) for the feedback values is always in lockstep with a setpoint change and no latency of the averaged feedback values (FB_DC, FB_I_AVG, FB_VBAT) is present. The synchronization of the dither period to a setpoint change can be enabled by programming the <DITHER_SETPOINT_SYNC_EN> bit in the DITHER_CLK_DIV register. An enabled setpoint synchronization freezes the average feedback registers (FB_DC, FB_I_AVG, FB_VBAT) with the last valid measurement result if the channel is disabled with setpoint "0".

4.7.6 TDS_Only ICC

Note: This feature is only available in ICC Channel Mode.

4.7.7 TDS_Deep dither

A steep and deep dither command is comparable to great changes of setpoint. The deep dither function reduces the over- and undershoot of very steep dither overlays by permanently enabling the Autolimit feature. The deep dither feature can be enabled by setting the <DEEP_DITHER> bit in DITHER_CTRL register.

4.7.8 TDS_ICC only

Note: This feature is only available in ICC Channel Mode.

4.8 Direct Drive

4.8.1 TDS_Direct Drive

In Direct Drive, the channel's output stage is controlled directly by the user. To enable a output stage switching, the respective channel must be activated by setting <EN_CH> bit to 1 and a target current setpoint value different to zero. The Direct Drive mode must be selected by programming the MODE register.

Direct Drive mode via DRV pin

In Direct Drive mode via DRV pin the channel's output stage is switched according to the logic level at the corresponding DRV pin. The channel is turned on if the DRV pin is high and is switched off if the DRV pin is low.

Direct Drive mode via SPI on-Time

In Direct Drive mode via SPI on-Time, the channel's output stage is switched according to a configurable period. The period T_{period} is set in the DITHER_CLK_DIV register by the bit fields <MANT> and <EXP>. The on-time t_{on} during a period can be configured with the <TON_MANT> bit field in the TON register.

$$T_{period} = \frac{< MANT > \cdot 2^{< EXP >}}{f_{SYS}}$$

$$t_{on} = \frac{< TON\_MANT > \cdot 2^{< EXP >}}{f_{SYS}}$$

Equation 10

4.9 Diagnostic functions

4.9.1 TDS_Overview

Each IC channel has an independend open load (OL), overcurrent (OC) and short circuit to ground (SG) diagnosis.

The following points should be considered:

- All failure modes are only considered to occur on the off board routed LOAD-pin.
- The diagnosis indication bits are clear on write.
- The diagnosis is only enabled if the device is in Mission Mode

The diagnosis consists of an ON-state diagnosis and an OFF-state diagnosis. Both diagnosis states shall be used to enable a full fault analysis coverage.

ON-state diagnosis

A channel is in ON-state if the <EN_CH> bit is set and the setpoint value is different to 0 mA. All diagnostic functions in ON-state rely on measuring the current through the shunt resistor. The ON-state diagnosis cannot distinguish between a short circuit to ground (SG) and an open load (OL) fault. Those faults are summarized to an Open Load/Short to Ground fault (OLSG) in the ON-state. A distinction whether an OL or SG is present needs to be done by the OFF-state diagnosis.

OFF-state diagnosis

A channel is in OFF-state if

1. the setpoint is 0 and the <EN_CH> bit is set to 1 (EN-pin must be high for use of OFF-state diagnosis state machine)
2. the setpoint is non-zero and the <EN_CH> bit is set to 0.

The first condition can be used to initially test the application circuit. The second condition is present after the ON-state diagnosis has detected a fault .

In OFF-state, the internal high and low side current sources I_{HS} and I_{LS} at the LOADx pin are active. The switching configuration and current strength of I_{HS} and I_{LS} can configured in the CH_CONFIG register.

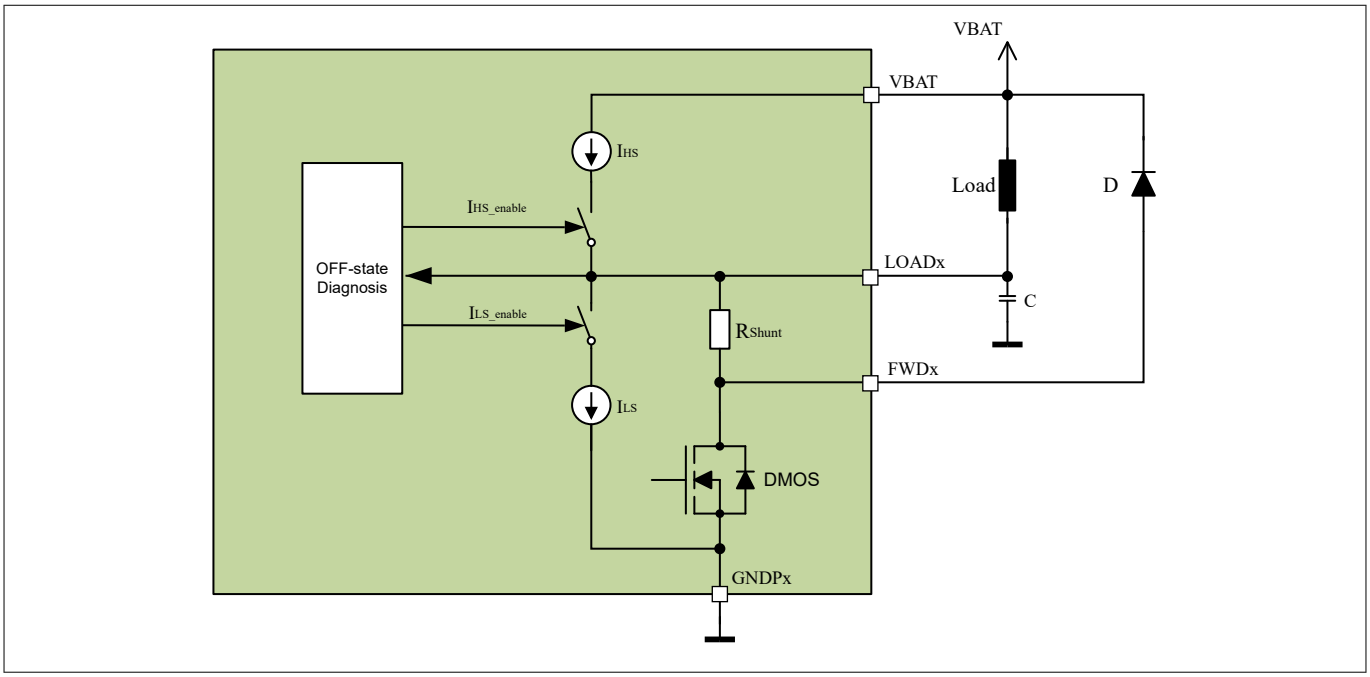


Figure 14 OFF-state diagnosis circuit

Setting <OFF_DIAG_CH> bit in the CH_CONFIG register to "0", activates the OFF-state diagnosis. The OFF-state diagnosis detects and indicates open load (OL) or short circuit to ground (SG) faults by performing following LOAD pin voltage checks.

1. The low side diagnostic current I_{LS} is enabled and the high side diagnostic current I_{HS} is disabled.
- If $V_{LOAD} > V_{TH\_BAT/2}$ no fault is detected.
- If $V_{LOAD} < V_{TH\_BAT/2}$ the sequence continues.

2. The high side diagnostic current I_{HS} is enabled and the low side diagnostic current I_{LS} is disabled.
- If $V_{LOAD} > V_{TH\_BAT/2}$ an OL is detected and indicated in the DIAG_ERR_CHGR register.
- If $V_{LOAD} < V_{TH\_BAT/2}$ a SG is detected and indicated in the DIAG_ERR_CHGR register.

The OFF-state diagnosis handles all channels sequentially. The OFF-state diagnosis sequence takes $T_{off,sequence}$.

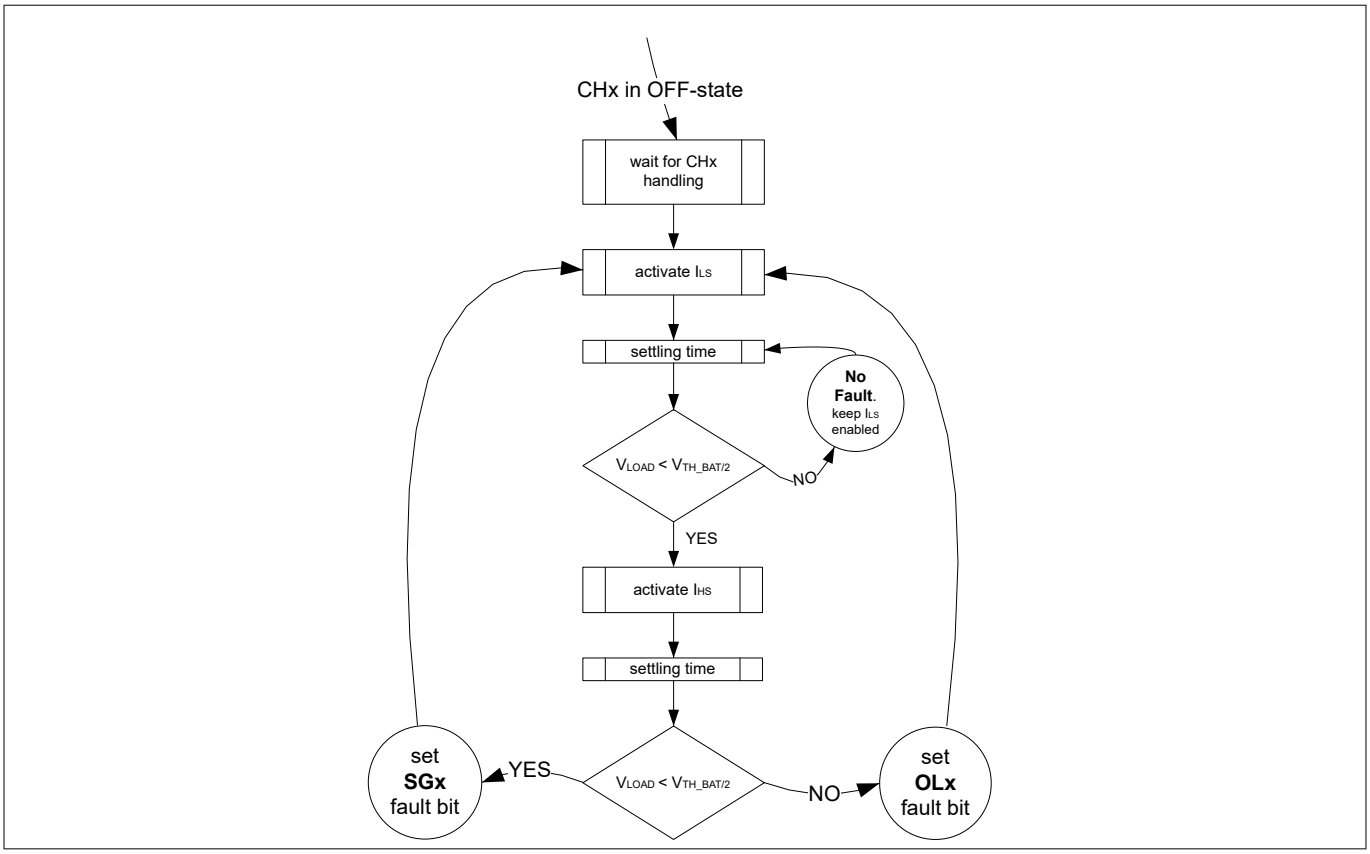


Figure 15 OFF-state diagnosis sequence

4.9.2 TDS_Open Load/Short to Ground (OLSG)

An open load (OL) and a short circuit to ground (SG) are both reducing the current flowing through the shunt resistor. Therefore the faults cannot be distinguished in ON-state and are summarized as OLSG fault. An OLSG is detected if the cumulated driver on-time equals T_{OLSGON} and the load current I_{LOAD} is below the open load threshold I_{OLTH}.

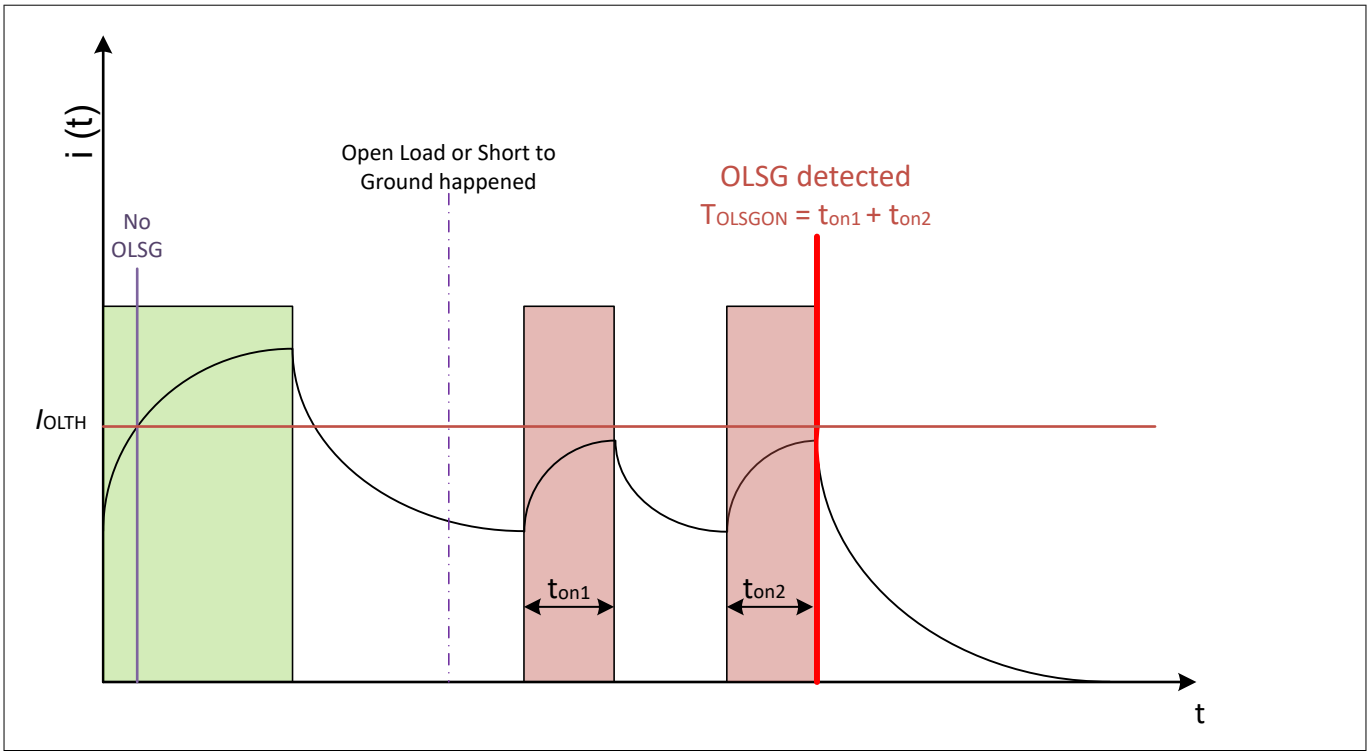


Figure 16 Simplified OLSG detection mechanism

An OLSG fault switches off the respective power stage and is indicated by setting the respective OLSG bit in the DIAG_ERR_CHGR register. The device keeps the channel disabled until the fault is removed, the diagnosis bit is cleared and the <EN_CH> bit is set to “1” again.

R_{OLmin} is the minimum impedance to detect an OL in ON-state via an OLSG fault.

$$R_{OLmin} = \frac{V_{BAT}}{I_{OLTH}} - (R_{LOAD} + R_{shunt} + R_{DSon})$$

Equation 11

R_{SGmax} is the maximum impedance to detect an SG in ON-state via an OLSG fault.

$$R_{SGmax} = \frac{R_{LOAD} \cdot (R_{shunt} + R_{DSon})}{R_{OLmin}}$$

Equation 12

4.9.2.1 TDS_OL-Threshold configuration

The open load threshold I_{OLTH} can be set to a fixed threshold and/or a threshold relative to the setpoint via the CH_CONFIG register. The OLSG diagnosis is disabled by setting both OL-thresholds to 0.

Fixed OL-Threshold

A fixed open load threshold is programmable via bitfield <OL_TH_FIXED>.

$$I_{OLTH} = \frac{< \text{OL\_TH\_FIXED} > \cdot 128 \cdot 2000\text{mA}}{2^{15} - 1}$$
$$I_{OLTH,\,parallel} = \frac{< \text{OL\_TH\_FIXED} > \cdot 128 \cdot 4000\text{mA}}{2^{15} - 1}$$

Equation 13

Note: The OL detection in direct drive mode is only possible with the fixed threshold configuration.

Relative OL-Threshold

The relative threshold refers to the actual setpoint I_{set} including the dither amplitude I_{Dither}. A relative open load threshold is adjustable in bitfield <OL_TH>. The relative open load threshold is disabled by setting <OL_TH> to 0.

$$I_{OLTH} = (I_{set} + I_{Dither}) \cdot \frac{< OL\_TH >}{8}$$

Equation 14

Note: The relative threshold is only available in a current control mode.

Transition phase

During a transition phase, the fixed OL-threshold is always used. A transition phase takes place after a channel activation or setpoint change. A transition phase lasts for one PWM cycle or maximum for a driver on-time of T_{OLSGON} (PWM cycle > T_{OLSGON}). The transition phase time out can be extended or shortened by configuring $t_{OLSG\_TIMEOUT}$ in the TON register. After the transition phase has been finished, the OLSG detection swaps from fixed to relative OL-threshold. If the <OL_TH_FIXED> bitfield is set to 0, no OLSG will be detected during a transition phase.

$$t_{OLSG\_TIMEOUT} = \frac{(< OLSG\_TIMEOUT > \cdot 256 + 255) \cdot 64}{f_{SYS}}$$

Equation 15

4.9.3 TDS_OLSG Warning

An additional OLSG-Warning checks if the voltage at the LOAD pin is greater than $V_{TH\_BAT/2}$ at the end of the freewheeling phase. The blanking time $t_{OLwindow}$ is triggered every time the outputstage is switched off. If the output stage is switched on within $t_{OLwindow}$, no voltage check is possible. This is indicated by setting <OLSG_WARN_CHK_NOK> in the DIAG_WARN_CHGR register to 1. The <OLSG_WARN_CHK_NOK> bit is cleared by reading.

If the check was successful, a detected OLSG-warning is indicated by setting <OLSG_WARN> in the DIAG_WARN_CHGR register to 1. The OLSG-warning is initially enabled and can be disabled by clearing the bit <OLSG_WARN_EN> in the CTRL register. The OLSG-warning check bit <OLSG_WARN_CHK_NOK> is set to 1 after clearing <OLSG_WARN> in the DIAG_WARN_CHGR register.

$t_{OLwindow}$ can be configured in the CTRL register.

$$t_{OLwindow} = \frac{(< OLSG\_WARN\_WINDOW > + 1) \cdot 64}{f_{SYS}}$$

Equation 16

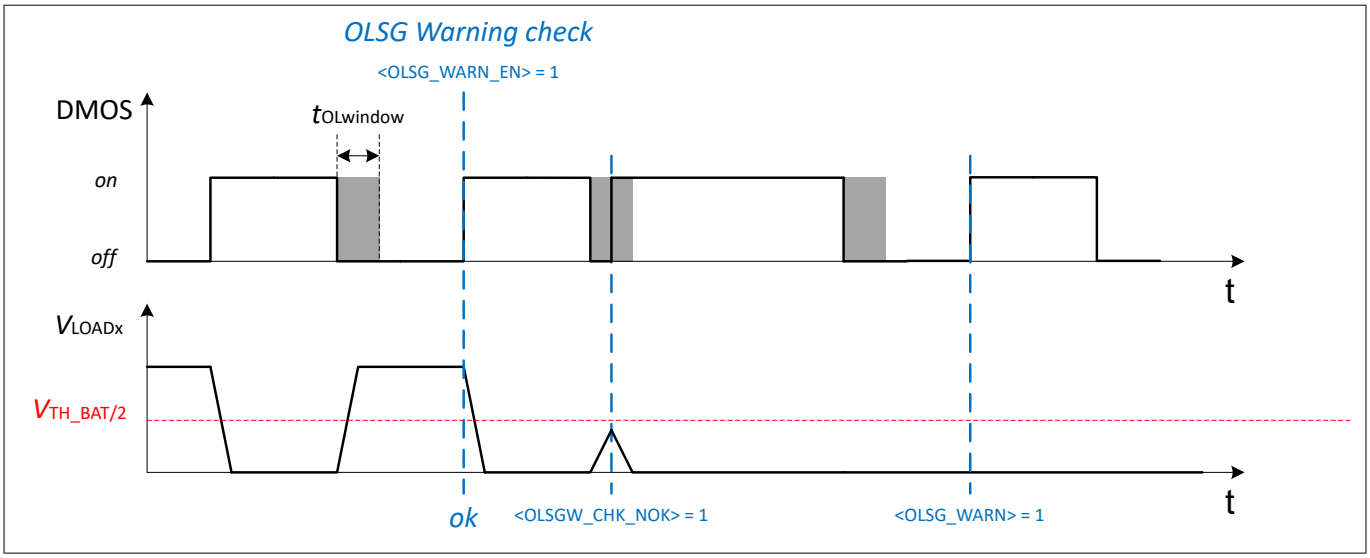


Figure 17 OLSG-Warning and OLSG warning check overview

4.9.4 TDS_Open load (OL)

In ON-state, an open load is indicated via the <OLSG> bit in the DIAG_ERR_CHGR register. The final fault discrimination to identify an open load is done by the OFF-state diagnostic. The device indicates the fault by setting the respective <OL> bit in the DIAG_ERR_CHGR register. The device keeps the channel disabled until the fault is removed, the diagnosis bit is cleared and the <EN_CH> bit is set to “1” again.

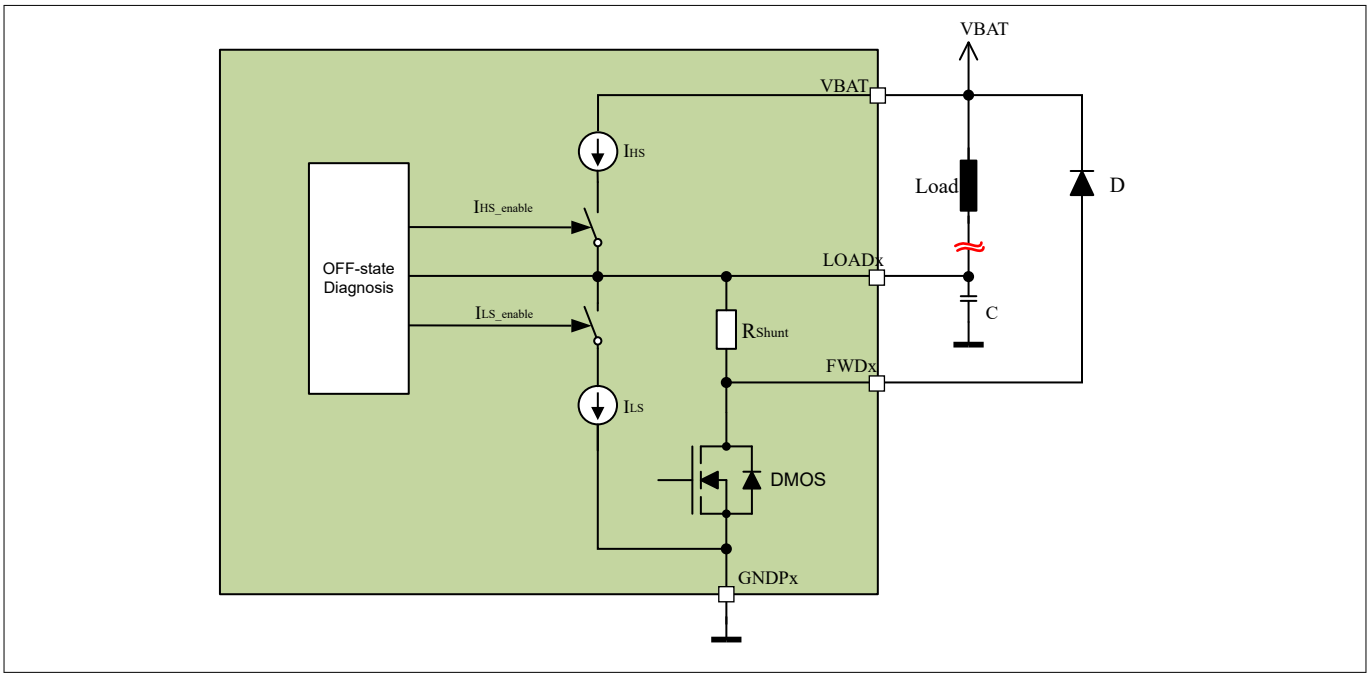


Figure 18 Open load

4.9.5 TDS_Short circuit ground (SG)

In the ON-state, a short circuit to ground is detected via the <OLSG> bit in the DIAG_ERR_CHGR register. The final fault discrimination to identify a short circuit to ground is done by the OFF-state diagnostic. The device indicates the fault by setting the respective <SG> bit in the DIAG_ERR_CHGR register. The device keeps the channel disabled until the fault is removed, the diagnosis bit is cleared and the <EN_CH> bit is set to “1” again.

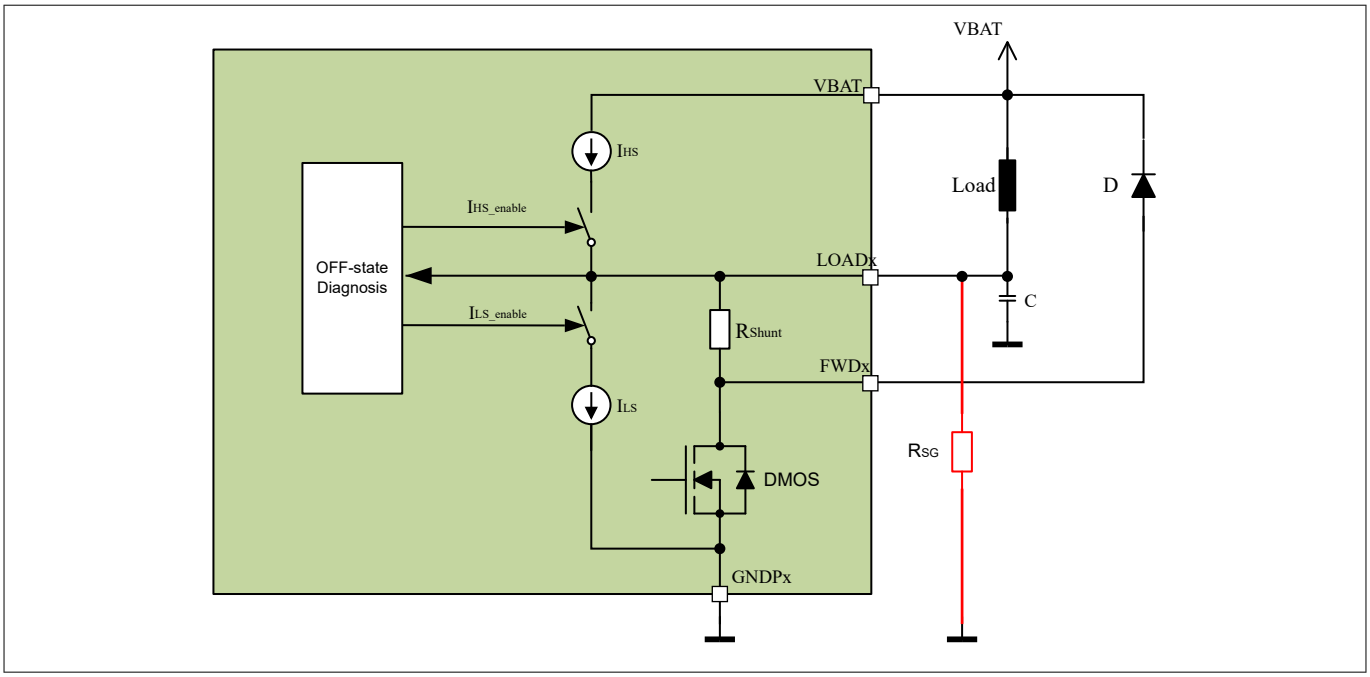


Figure 19 Short to Ground

4.9.6 TDS_Overcurrent (OC)

An overcurrent fault (OC) is an unintended low impedance connection between the LOAD terminal and the battery rail, therefore bypassing the load impedance.

An overcurrent is detected if a current flow through the power stage exceeds I_{OC}. Therefore the power stage must be turned on for a short period of time t_{OCon} to detect an OC in OFF-state. The driver on-time t_{OCon} can be triggered by setting the <OC_DIAG_EN> bit in the CH_CONFIG register and the respective <EN_CH> bit in the CH_CTRL register to 1. The driver on-time t_{OCon} must be configured before executing the OC detection.

$$t_{OCon} = \frac{(< TON\_MANT > + 1) \cdot 2^{< EXP >}}{f_{SYS}}$$

Equation 17

The mantissa <TON_MANT> is located in the TON register and the exponent <EXP> is located in DITHER_CLK_DIV. An enabled OFF-state diagnosis is kept active during t_{OCon}.

<OC_DIAG_EN> is reset after t_{OCon} has expired. If an overcurrent is present, the <EN_CH> bit is cleared and the indication bit <OC> in the DIAG_ERR_CHGR register is set to 1. The device keeps the channel disabled until the fault is removed, the diagnosis bits are cleared by two clear commands and the <EN_CH> bit is set to “1” again.

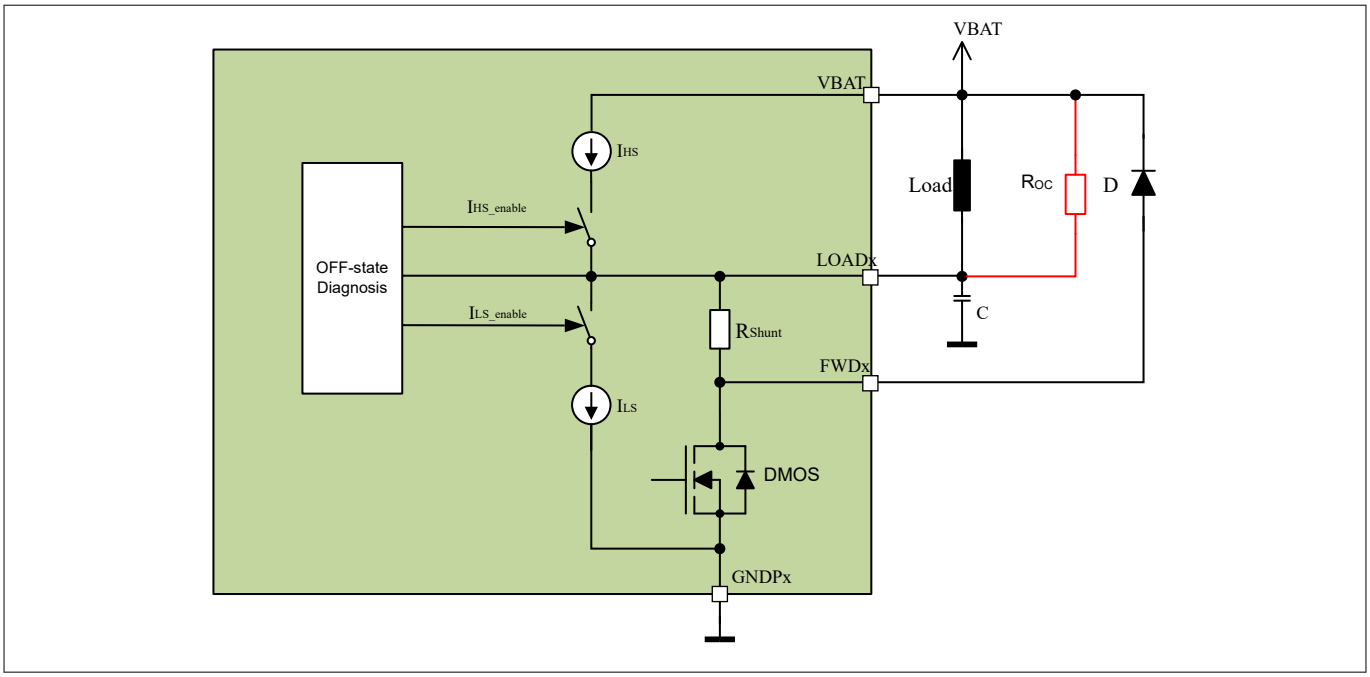


Figure 20 Overcurrent

4.9.7 TDS_Register/OTP ECC

A register/OTP (one time programmable memory) error will be detected by a continuous error checking and correction (ECC) mechanism. If a correction is not possible, a register/OTP ECC error is present and the <REG_ECC_ERR>/<OTP_ECC_ERR> bit in the GLOBAL_DIAG2 register will be set. The <OTP_ECC_ERR> can only be cleared by sending two clear commands. A register ECC error disables all power stages and the product enters the Operation State "Config Mode". The <OTP_VIRGIN> bit in the GLOBAL_DIAG2 indicates a non programmed OTP-memory. This bit must always be 0.

4.9.8 TDS_Built in Self Test (BIST)

The device provides a self-test in order to check the built in error detection and correction feature for safety critical registers. The BIST tests the ability to detect correctable and uncorrectable errors. The BIST can only be triggered in Config Mode by writing a '1' to the <SMU_SLF_TST_EN> bit in the SFF_BIST register. After the safety flip-flop BIST sequence is completed, the bits <SMU_SLF_TST_DONE>, <SMU_SLF_TST_UERR> and <SMU_SLF_TST_CERR> are set to indicate a finished test sequence.

The safety flip-flop BIST result is stored in the <SMU_SLF_TST_FAIL> bit in SFF_BIST register. All result and status bits in the SFF_BIST register are cleared on writing 0. A successfully tested safety flip-flop error (uncorrectable fault) sets the respective error bits <REG_ECC_ERR> in the GLOBAL_DIAG2 register.

4.9.9 Electrical characteristics diagnostic functions

Table 15 Electrical characteristics diagnostic functions

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OLSG threshold single	I_{OLTH}	0	–	492	mA	fixed OLSG threshold in single channel mode

(table continues...)

Table 15 (continued) Electrical characteristics diagnostic functions

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
OLSG threshold parallel	$I_{OLTH,parallel}$	0	-	984	mA	fixed OLSG threshold in parallel mode
OLSG filter detection time	T_{OLSGON}	-	2^{15}	-	cycles	f_{SYS} cycles
OFF-state LOADx threshold voltage	$V_{TH\_BAT/2}$	–	V_{BAT}/ 2	–	V	
OFF-state sequence time	$T_{off,sequence}$	1.2	–	4.8	ms	
Diagnosis Current 0	I_{HS} I_{LS}	30	80	120	µA	<I_DIAG> = 00_B
Diagnosis Current 1	I_{HS} I_{LS}	105	190	275	µA	<I_DIAG> = 01_B
Diagnosis Current 2	I_{HS} I_{LS}	510	720	910	µA	<I_DIAG> = 10_B
Diagnosis Current 3	I_{HS} I_{LS}	910	1250	1520	µA	<I_DIAG> = 11_B

4.10 Current supervision

4.10.1 TDS_Independent current feedback

The device provides independent current feedback paths to the microcontroller for plausibility checks on the load current. The average load current measured via the internal shunt can be read back directly. The independently measured duty cycle and battery voltage can be used to calculate the average load current using a load model.

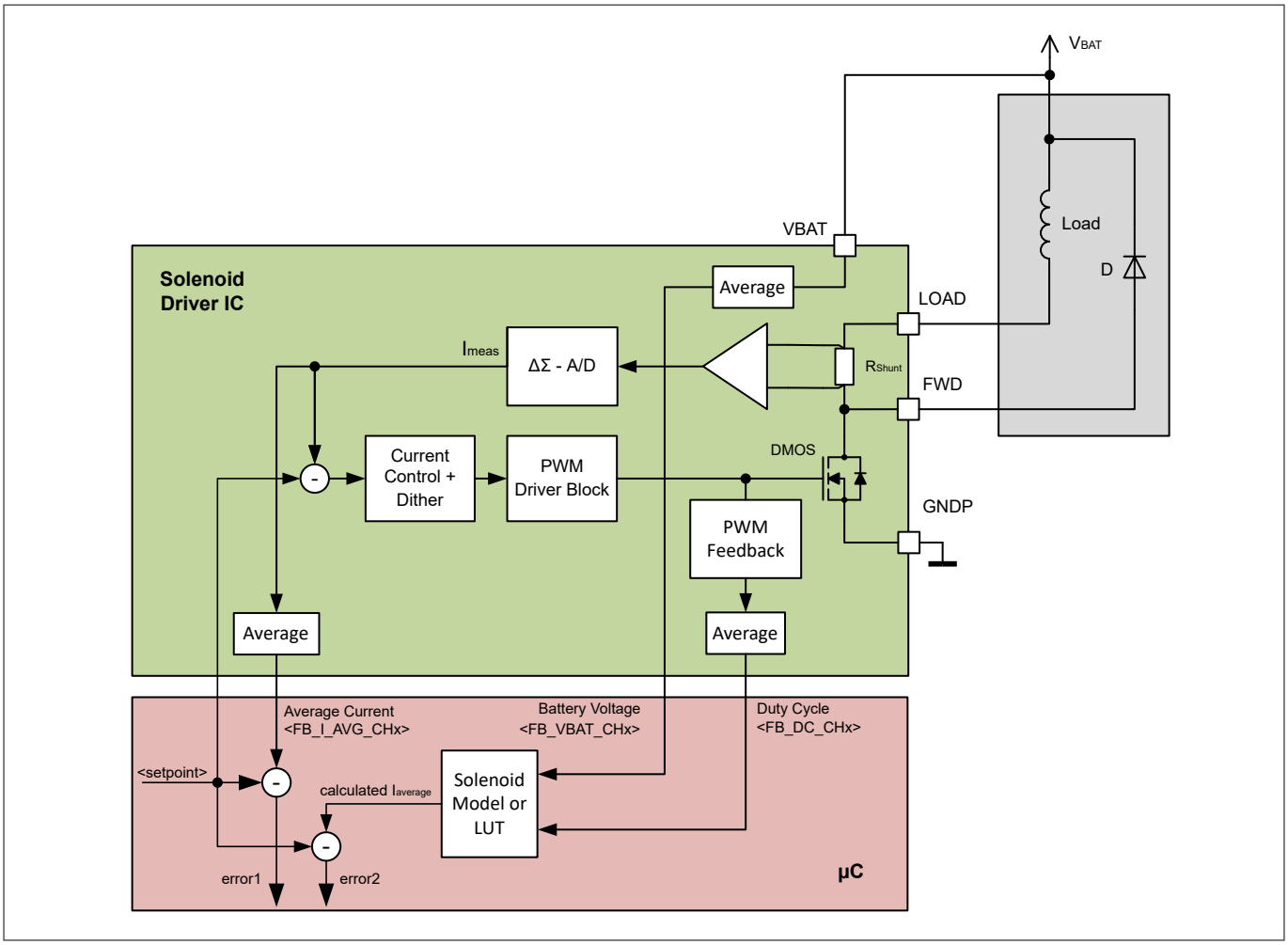


Figure 21 Current supervision

4.10.2 TDS_Average feedback values

The feedback values are provided in the registers FB_DC, FB_VBAT, FB_I_AVG. The feedback values averaged over the configured measurement period T_{meas} (see "Channel modes"). The register contents are updated after each measurement period T_{meas}.

The feedback values can be calculated as follows:

- Measurement period:

$$T_{meas} = \frac{< TP\_MANT > \cdot 2^{< EXP >}}{f_{SYS}}$$

Equation 18

- PWM on time:

$$t_{on} = \frac{< TO\_MANT > \cdot 2^{< EXP >}}{f_{SYS}}$$

Equation 19

- Duty cycle:

$$DC = \frac{< TO\_MANT >}{< TP\_MANT >}$$

Equation 20

- Battery voltage:

$$V_{BAT} = 41.47\text{V} \cdot \frac{< VBAT\_AVG\_MANT >}{< TP\_MANT >}$$

Equation 21

- Average load current (signed):

$$I_{avg} = 4\text{A} \cdot \frac{< I\_AVG\_MANT >}{< TP\_MANT >}$$

Equation 22

The bitfields <TP_MANT> and <TO_MANT> are located in the FB_DC register. The bitfields <VBAT_AVG_MANT> and <EXP> are loacated the FB_VBAT register. The bitfield <I_AVG_MANT> is located in the FB_I_AVG register. The bitfield <I_AVG_MANT> represents a signed current value (two's complement).

4.10.3 TDS_Fast measurement feedback - (6CHx)

Using the dither period T_{Dither} as measurement period, allows to shorten the update interval t_{update} of the feedback values to n_{meas_sample} times of the dither frequency. The Fast Measurement Mode can be configured by programming <FAST_FB_MODE> in the DITHER_CTRL register and takes effect at the start of the next dither period T_{Dither}.

$$t_{update} = \frac{T_{Dither}}{n_{meas\_sample}} = \left(\frac{4 \cdot < STEPS >}{n_{meas\_sample}} + round\left(\frac{2 \cdot < FLAT >}{n_{meas\_sample}}\right)\right) \cdot t_{ref\_clk}$$

$$n_{meas\_sample} = \left[2, 4\right]$$

Equation 23

*Note: For a correct operation the dither period T_{Dither} needs to be at least n_{meas_sample} * t_{ref_clk} and <FLAT> must be greater than 2.*

It´s recommended to use a moving average filter by calculating the average of n_{meas_sample} consecutive measurement samples. Except ICC mode with enabled Dither Synchronisation feature, following formulas should be considered to avoid a calculation error caused by quantization noise.

- Measurement period:

$$T_{meas} = \frac{< TP\_MANT > \cdot 2^{< EXP >}}{f_{SYS}}$$

Equation 24

- PWM on time:

$$t_{on} = \frac{< TO\_MANT > \cdot 2^{< EXP >}}{f_{SYS}}$$

Equation 25

- Duty cycle:

$$DC = \frac{< TO\_MANT > \cdot 2^{< EXP >}}{< TP\_MANT > \cdot 2^{< EXP >}}$$

Equation 26

- Battery voltage:

$$V_{BAT} = 41.47\text{V} \cdot \frac{< VBAT\_AVG\_MANT > \cdot 2^{< EXP >}}{< TP\_MANT > \cdot 2^{< EXP >}}$$

Equation 27

- Average load current (signed):

$$I_{avg} = 4\text{A} \cdot \frac{< I\_AVG\_MANT > \cdot 2^{< EXP >}}{< TP\_MANT > \cdot 2^{< EXP >}}$$

Equation 28

4.10.4 TDS_Sequence counter - (6CHx)

The bitfields <DITHER_PERIOD_CNT> and <DITHER_QUAD_CNT> in the FB_VBAT register are representing sequence counters indicating the actual measurement sample of the feedback values in order to detect a potential loss of data due to undersampling.

The sequence number of <DITHER_PERIOD_CNT> is incremented after a full measurement period. The sequence number <DITHER_QUAD_CNT> is incremented by $4/n_{meas\_sample}$ after t_{update}.

Both counters wrap around after the 4th counter value (0..3) and are only active in Fast Measurement Mode.

4.10.5 TDS_Update/Freeze Mechanism

The Update/Freeze mechanism should be applied for a correct readout of each measurement sample set. The IC indicates new feedback data by setting the respective <CH> bit in the FB_UPD register to 1. Setting <CH> bit in the FB_FRZ register to 1, stops the updating and freezes the latest measurement results of the feedback registers FB_DC, FB_VBAT, FB_I_AVG, FB_PERIOD_MIN_MAX, FB_IMIN_IMAX. Setting the <CH> bit in the FB_FRZ register to 0, also clears the respective <CH> bit in the FB_UPD register and enables the update of the feedback values. Following state diagram shows a recommendation for the readout of the feedback values.

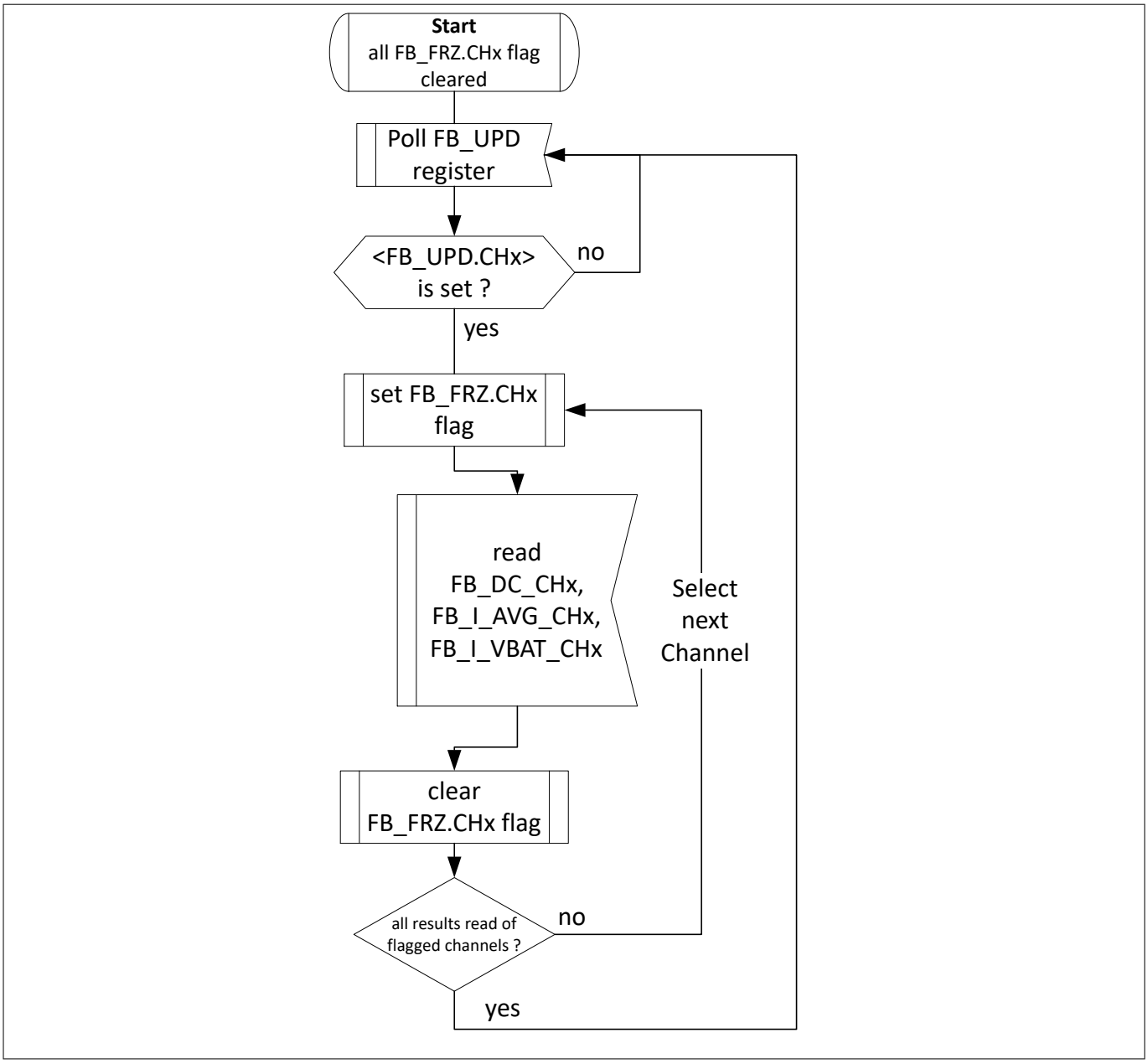


Figure 22 Readout proposal for feedback values

4.10.6 TDS_Iavg16, minimum/maximum current/PWM feedback

The IC provides the average load current I_{avg16} over a free running period of 2^{16} system clocks, as a signed 16 bit value in the FB_I_AVG_s16 register. This value is not intended to be used while in closed loop operation or for current supervision. The value is provided as additional information and can be used for calibration purposes.

$$I_{avg16} = 4\text{A} \cdot \frac{< I\_AVG\_s16 >}{2^{16} - 1}$$

Equation 29

The IC provides measurements of the minimum (min) and maximum (max) current and PWM period. The min/max values represent the highes/lowest current and shortest/longest PWM period captured during a measurement period T_{meas}. If no measurement period T_{meas} is defined, the min/max registers are

permanently updated when a new minimum or maximum current/PWM has been measured. The current values are held in the FB_IMIN_IMAX register and the PWM values can be read out from the FB_PERIOD_MIN_MAX register. The current values in the FB_IMIN_IMAX register are represented as a signed 9 bit value (two´s complement).

$$I_{min} = 4\text{A} \cdot \frac{< IMIN >}{2^9 - 1}$$
$$I_{max} = 4\text{A} \cdot \frac{< IMAX >}{2^9 - 1}$$

Equation 30

$$T_{PWM\_min} = < PMIN > \cdot \frac{256}{f_{SYS}}$$
$$T_{PWM\_max} = < PMAX > \cdot \frac{256}{f_{SYS}}$$

Equation 31

4.11 Protection functions

4.11.1 TDS_Overtemperature protection

The device provides protection against overtemperature by measuring the central IC temperature and every power stage temperature. If an overtemperature $T_{J,ot}$ is measured, the respective power stage is switched off and the respective <OT> bit in the DIAG_ERR_CHGRx register is set. A central overtemperature of the IC disables all power stages and sets the <COTERR> bit in the GLOBAL_DIAG0 register.

If the respective power stage has cooled down to $T_{J,ot}$ -T_H, the power stage can be re-enabled. A pre-warning bit in the diagnostic register is set, if the power stage temperature exceeds the pre-warning threshold T_p.

The overtemperature detection can be tested by setting the <OT_TEST> bit in the GLOBAL_CONFIG register to "1". This test sets the overtemperature threshold to the lowest possible value and the according overtemperature indication bits should be asserted.

The device provides a temperature feedback T_{FB} which can be read out from the bitfield <TEMP_VALUE> in the FB_VOLTAGE2 register. The temperature feedback T_{FB} is given by

$$T_{FB} = \frac{< TEMP\_VALUE > \cdot 0.000593 - 0.819^{*)}}{-0.0016^{*)}} \text{°C}$$

Equation 32

If a higher accuracy of the temperature feedback T_{FB} is required, a calibration of the parameters *) have to be done on system level.

4.11.2 TDS_Overcurrent protection

The maximum current through every power stage of the device is limited. An overcurrent condition is detected if the load current exceeds I_{OC}. The detection of an overcurrent takes maximum $t_{OC,DETECT}$. An overcurrent causes the channel to be switched off and is indicated by setting the respective <OC> bit in the DIAG_ERR_CHGR register to 1. The <OC> bit must be cleared by two SPI write commands.

4.11.3 Electrical characteristics protection functions

4.11.3.1 Overtemperature protection

Table 16 Overtemperature protection

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature pre-warning threshold	T_P	150	-	175	°C	
Overtemperature threshold	$T_{J,OT}$	175	-	200	°C	
Thermal hysteresis	T_H	10	–	15	°C	
Temperature feedback accuracy	T_{FB}	-20	–	20	°C	

4.11.3.2 Overcurrent protection

Table 17 Overcurrent protection

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overcurrent protection threshold	I_{OC}	2.05	–	6	A	
Overcurrent protection filter time	$t_{OC,DETECT}$	–	–	1.5	µs	f_{SYS} = 28 MHz

5 Serial peripheral interface (SPI)

5.1 Description of interface

5.1.1 TDS_General information

The communication interface is based on a standard serial peripheral interface (SPI). The SPI is a full duplex synchronous serial slave interface which uses four signal lines: SO, SI, SCK, and CSN. Data is transferred by the lines SI and SO at the data rate given by SCK. The falling edge of CSN indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCK and shifted out on line SO at the rising edge of SCK. Each access must be terminated by a rising edge of CSN. A counter ensures that data is taken only when 32 bits have been transferred. If the number of bits transferred is not 32, the data frame is ignored.

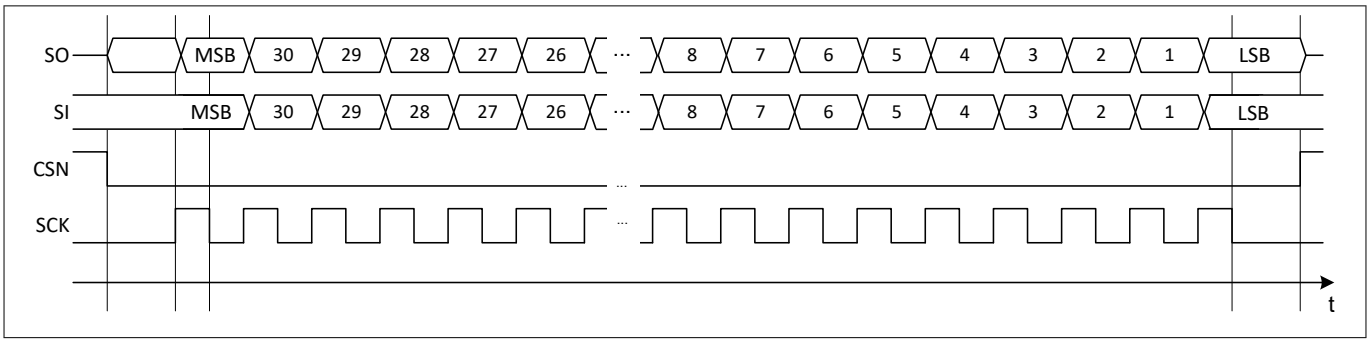


Figure 23 SPI signal overview

5.1.2 TDS_Cyclic redundancy check (CRC)

An 8-bits cyclic redundancy code (*CRC-8 SAE-J1850*) is added to all SPI communication frames to detect corrupt data and to avoid wrong configuration of the IC. The CRC-8 SAE-J1850 polynomial is used for the calculation:

$x^8 + x^4 + x^3 + x^2 + 1$ or 0x1D

Note: CRC is supported by the flexible CRC engine (FCE) of Aurix TC26x, TC27x and TC29x.

The initial value of the CRC-byte is 0xFF. The CRC result is XOR operated with 0xFF. The CRC-byte is located in the most significant byte of the SPI frame. The byte-sequence for the CRC calculation is as follows:

1st byte: SPI frame[7:0]
2nd byte: SPI frame[15:8]
3rd byte: SPI frame[23:16]

Different generator polynomials are supported by the frame encoder/decoder entity definition, but the specific implementation is not part of the reuse module. The product designer has to modify the frame encoder/ decoder source code within the project design environment accordingly.

The CRC byte is located in the most significant frame byte [31:24]. Whenever a SPI frame CRC error is detected, a SPI 16 bit reply frame indicating the SPI CRC error status is send in the subsequent SPI transaction.

The CRC check can be disabled by setting the <CRC_EN> bit in the GLOBAL_CONFIG register to "0".

5.1.3 TDS_Timing Diagram

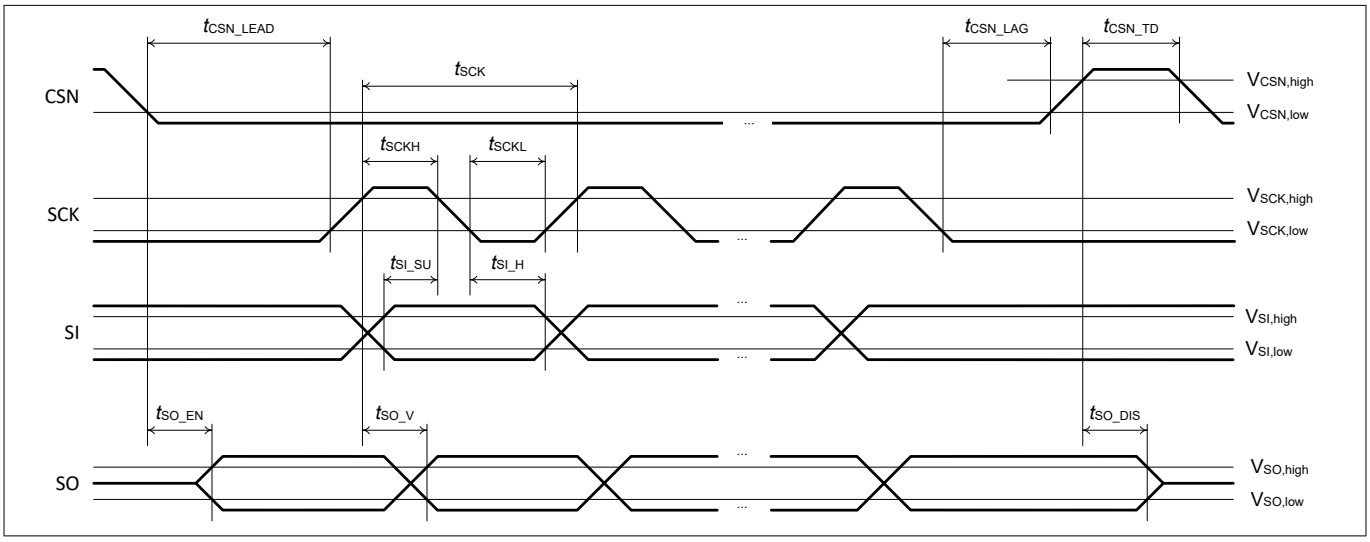


Figure 24 SPI Signal Timing Diagram

5.1.4 Electrical characteristics SPI interface

Table 18 Electrical characteristics SPI interface

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Serial clock high time	t_{SCKH}	50	–	–	ns	
Serial clock low time	t_{SCKL}	50	–	–	ns	
Enable lead time	t_{CSN_LEAD}	250	–	–	ns	falling CSN to rising SCK
Enable lag time	t_{CSN_LAG}	250	–	–	ns	falling SCK to rising CSN
Transfer delay time	t_{CSN_TD}	600	–	–	ns	rising CSN to falling CSN
Data setup time	t_{SI_SU}	20	–	–	ns	required time SI to falling SCK
Data hold time	t_{SI_H}	20	–	–	ns	required time falling SCK to SI
Output disable time	t_{SO_DIS}	–	–	200	ns	rising CSN to SO tri-state C_L = 150 pF
Output enable time	t_{SO_EN}	–	–	200	ns	falling CSN to SO valid C_L = 150 pF
Output data valid time	t_{SO_V}	–	–	100	ns	C_L = 150 pF
Functional range SPI clock	f_{SCK}	–	–	8	MHz	

(table continues...)

Table 18 (continued) Electrical characteristics SPI interface

T_J = -40°C to 150°C; V_{DD} = 4.5 - 5.5 V; V_{IO} = 3.0 - 5.5 V; V_{BAT} = 6 - 18 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
frequency (SCK)						
SPI watchdog decrement frequency	$f_{SPI,WD}$	–	f_{SYS} / 2^{14}	–	MHz	f_{SYS} = 28 MHz
Input pin capacitance (CSN, SCK, SI, CLK)	C_{IN}	–	–	10	pF	V_{bias} = 2 V; V_{test} = 20 mVpp; f =1 MHz
Output pin capacitance (SO)	C_{SO_HIZ}	–	–	15	pF	Tri-state Output V_{bias} = 2 V; V_{test} = 20 mVpp; f = 1 MHz
SPI High Threshold Voltage (SI, SCK, CSN)	$V_{SI,high}$ $V_{SCK,high}$ $V_{CSN,high}$	-	-	2	V	
SPI Low Threshold Voltage (SI, SCK, CSN)	$V_{SI,low}$ $V_{SCK,low}$ $V_{CSN,low}$	0.8	-	-	V	
SPI Input hysteresis (SI, SCK, CSN)	$V_{IN,HYS,SI}$ $V_{IN,HYS,SCK}$ $V_{IN,HYS,CSN}$	-	50	-	mV	
SPI output high voltage (SO)	$V_{SO,high}$	V_{IO} - 0.5	–	V_{IO}	V	pull down current I_{SO} = -0.5 mA/ 3.0 V < V_{IO} < 5.5 V
SPI output low voltage (SO)	$V_{SO,low}$	0	–	0.5	V	pull up current I_{SO} = 0.5 mA
SPI output leakage current (SO)	$I_{SO,OFF}$	-10	–	10	µA	V_{CSN} > $V_{CSN,high}$ 0 V < V_{SO} < V_{IO}
Pull down current (SI, SCK)	$I_{PD,SI}$ $I_{PD,SCK}$	10	–	50	µA	V_{IN} = 2 V
Pull up current (CSN)	$I_{PU,CSN}$	-50	–	-10	µA	VCSN = 0.8 V

5.2 Description of protocol

5.2.1 TDS_Data flow

The message from the microcontroller must be sent MSB first. The data from the SO pin is sent MSB first. For each command received at the SI pin of the SPI interface, a serial data stream is returned at the same time on the SO pin. The content of the SO data frame is dependent on the command which was received on the SI pin during the previous frame. A READ command (R/W = 0) returns the contents of the addressed register one SPI frame later. The data bits in the READ command are ignored.

A WRITE command (R/W = 1) will write the data bits in the SPI word to the addressed register. The actual contents of addressed register will be returned to the SPI master (microcontroller) during the next SPI frame.

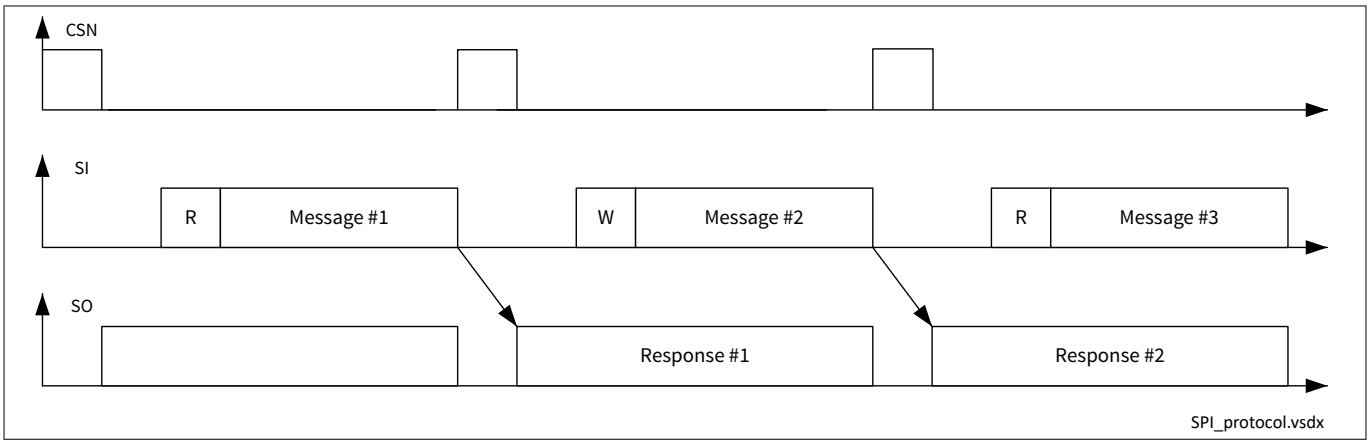


Figure 25 SPI protocol

5.2.2 TDS_SPI watchdog

An SPI watchdog checks the communication on the SPI bus. The SPI watchdog can be enabled by setting <SPI_WD_EN> in the GLOBAL_CONFIG register.

If the SPI watchdog is enabled, the <WD_TIME> value in the WD_RELOAD register is constantly decremented with $f_{SPI,WD}$. In order to avoid a SPI watchdog error, the WD_RELOAD register must be permanently updated.

If the <WD_TIME> value of the WD_RELOAD register transitions from 1 to 0, the <SPI_WD_ERR> bit in the GLOBAL_DIAG0 register is asserted and the IC transits to Config Mode.

As long as a SPI watchdog fault is present the device cannot enter Mission Mode. The SPI error indication bit <SPI_WD_ERR> is set to 0 if the WD_RELOAD register contains a non-zero value.

The SPI watchdog timeout $t_{SPI,WD}$ is given by:

$$t_{SPI,WD} = \frac{< WD\_TIME >}{f_{SPI,WD}}$$

Equation 33

5.2.3 SPI frame definition

5.2.3.1 TDS_MOSI - Write frame

MOSI SPI write frame

Data in frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

CRC								Address							R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data															

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)
Address	23:17	Address field
R/W	16	MOSI Read/Write Indicator 0_B: Read operation 1_B: Write operation
Data	15:0	Data bits are defined in register description

5.2.3.2 TDS_MOSI - Read frame

MOSI SPI read frame
Data in frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC								-							R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address															

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)
-	23:17	Don´t care
R/W	16	MOSI Read/Write Indicator 0_B: Read operation 1_B: Write operation
Address	15:0	Read Address

5.2.3.3 TDS_MISO - 16 bit reply frame

MISO SPI 16 bit reply frame
16 bit data out frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC								Reply Mode		Status					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data															

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)

Field	Bits	Description
Reply Mode	23:22	Indicates type of reply frame: 00_B: 16 bit Reply Frame 01_B: 22 bit Reply Frame 10_B: Critical Fault Frame
Status	21:17	Status indication of the current Frame: 00_B: no error 01_B: SPI frame error 10_B: Parity/CRC error 11_B: Write to read only register $100_B/101_B/110_B$: Internal bus fault *NOTE: The highest priority has the lowest encoding*
R/W	16	Indicator mirrored from previous MOSI frame 0_B: Read indicator 1_B: Write indicator
Data	15:0	Data bits are defined in register description

5.2.3.4 TDS_MISO - 22 bit reply frame

MISO SPI 22 bit reply frame
22 bit data out frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC								0	1	Data					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data (cont'd)															

Field	Bits	Description
CRC	31:24	CRC check (SAE CRC8 J1850)
Reply Mode	23:22	Indicates type of reply frame: 00_B: 16 bit Reply Frame 01_B: 22 bit Reply Frame 10_B: Critical Fault Frame
Data	21:0	22 data bits used for feedback registers defined in register description

5.2.3.5 TDS_MISO - Critical fault reply frame

MISO SPI critical fault reply frame
Critical fault frame of slave device

31	30	29	28	27	26	25	24	23	22	21	20	19	19	17	16
Don't care								1	0	Don't care					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Don't care (cont'd)								1V5	2V5	BG	CLK_TOO_SLOW	CLK_TOO_FAST	DIG_CLK_TOO_SLOW	DIG_CLK_TOO_FAST	WD_REF_CLK

Field	Bits	Description
Don´t care	31:24	-
Reply Mode	23:22	Indicates type of reply frame: 00_B: 16 bit Reply Frame 01_B: 22 bit Reply Frame 10_B: Critical Fault Frame
Don´t care	21:8	-
1V5	7	0_B: 1V5 supply not ok 1_B: 1V5 supply ok
2V5	6	0_B: 2V5 supply not ok 1_B: 2V5 supply ok
BG	5	0_B: ADC Bandgap not ok 1_B: ADC Bandgap ok
CLK_TOO_SLOW	4	0_B: No clock fault detected 1_B: Clock is too slow for IC operation
CLK_TOO_FAST	3	0_B: No clock fault detected 1_B: Clock is too fast for IC operation
DIG_CLK_TOO_SLOW	2	0_B: No clock fault detected 1_B: Digital Clock is too slow *Note: clock watchdog must be enabled.*
DIG_CLK_TOO_FAST	1	0_B: No clock fault detected 1_B: Digital Clock is too fast *Note: clock watchdog must be enabled.*
WD_REF_CLK	0	0_B: Clock watchdog reference clock is ok 1_B: Clock watchdog reference clock is missing

5.3 Register description

5.3.1 Overview of Register Types

Bit type short name	Bit type description	Note
r	Bits are readable (read)	bitfields "RES" do not care
rh	Bits are readable (read) and modifiable by the IC (hardware)	bitfields "RES" do not care
rw	Bits are read- and writeable (read-write)	bitfields "RES" do not care, write "0"
rwh	Bits are read- and writeable (read-write) and modifiable by the IC (hardware)	bitfields "RES" do not care, write "0"

5.3.2 Central registers

5.3.2.1 Register overview - centralRegs (ascending offset address)

Table 19 Register overview - centralRegs (ascending offset address)

Short name	Long name	Offset address	Page number
CH_CTRL	Channel Control Register	0000_H	56
GLOBAL_CONFIG	Global Configuration Register	0002_H	58
GLOBAL_DIAG0	Global Diagnosis Register 0	0003_H	59
GLOBAL_DIAG1	Global Diagnosis Register 1	0004_H	61
GLOBAL_DIAG2	Global Diagnosis Register 2	0005_H	62
VBAT_TH	VBAT Threshold Register	0006_H	63
FB_FRZ	Feedback Freeze Register	0007_H	64
FB_UPD	Feedback Update Register	0008_H	65
WD_RELOAD	SPI Watchdog Register	0009_H	66
DIAG_ERR_CHGR	Diagnosis Error Register Channel Group	$000A_H$+x	67
DIAG_WARN_CHGR	Diagnosis Warning Register Channel Group	0010_H+x	68
FAULT_MASK0	Fault Mask Register 0	0016_H	69
FAULT_MASK1	Fault Mask Register 1	0017_H	70
FAULT_MASK2	Fault Mask Register 2	0018_H	72
CLK_DIV	Clock Control Register	0019_H	73
SFF_BIST	BIST Register	$003F_H$	74
ICVID	Version Register	0200_H	75
PIN_STAT	Pin Status Register	0201_H	76
FB_STAT	Feedback Status Register	0202_H	77
FB_VOLTAGE1	Feedback Voltage Register 1	0203_H	80
FB_VOLTAGE2	Feedback Voltage Register 2	0204_H	81
CHIPID0	Unique Chip Identification Number Register 0	0205_H	82
CHIPID1	Unique Chip Identification Number Register 1	0206_H	83
CHIPID2	Unique Chip Identification Number Register 2	0207_H	84

5.3.2.2 Register address space - centralRegs

Table 20 Registers address space - centralRegs

Module	Base address	End address	Note
apb	00000000_H	$0000FFFE_H$	

5.3.2.3 Channel Control Register

The channel enable bits EN_CHx can only be set in Mission mode. The parallel mode configuration bits CH_PAR_x can only be set in Config mode.

CH_CTRL Offset address: 0000_H

Channel Control Register value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP_MODE	**CH_PAR_1_2**	**CH_PAR_0_3**	**CH_PAR_4_5**	**Res**						**EN_CH5**	**EN_CH4**	**EN_CH3**	**EN_CH2**	**EN_CH1**	**EN_CH0**
rw	rw	rw	rw	r						rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EN_CH0	0	rw	**Enable Channel 0** 0_B Disabled 1_B Enabled
EN_CH1	1	rw	**Enable Channel 1** 0_B Disabled 1_B Enabled
EN_CH2	2	rw	**Enable Channel 2** 0_B Disabled 1_B Enabled
EN_CH3	3	rw	**Enable Channel 3** 0_B Disabled 1_B Enabled
EN_CH4	4	rw	**Enable Channel 4** 0_B Disabled 1_B Enabled
EN_CH5	5	rw	**Enable Channel 5** 0_B Disabled 1_B Enabled
CH_PAR_4_5	12	rw	**Parallel Operation Channel 4/5** 0_B Disabled 1_B Enabled
CH_PAR_0_3	13	rw	**Parallel Operation Channel 0/3** 0_B Disabled 1_B Enabled
CH_PAR_1_2	14	rw	**Parallel Operation Channel 1/2** 0_B Disabled 1_B Enabled
OP_MODE	15	rw	**Chip Operation Mode** 0_B Config Mode

(table continues...)

(continued)

Field	Bits	Type	Description
			1_B Mission Mode

5.3.2.4 Global Configuration Register

Global Configuration Register: write access only possible in Config Mode

GLOBAL_CONFIG Offset address: 0002_H

Global Configuration Register value: 4005_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**VIO_SEL**	**UV_OV_SWAP**	**OT_TEST**	**Res**						**V1V5_OV_TEST**	**V1V5_UV_TEST**	**Res**	**CRC_EN**	**SPI_WD_EN**	**CLK_WD_EN**
r	rw	rw	rw	r						rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
CLK_WD_EN	0	rw	**Clock Watchdog** 0_B Disabled 1_B Enabled
SPI_WD_EN	1	rw	**SPI Watchdog** 0_B Disabled 1_B Enabled
CRC_EN	2	rw	**SPI CRC Check** 0_B Disabled 1_B Enabled
V1V5_UV_TEST	4	rw	**Test Internal Supply Undervoltage Detection** 0_B Disabled 1_B Enabled
V1V5_OV_TEST	5	rw	**Test Internal Supply Overvoltage Detection** 0_B Disabled 1_B Enabled
OT_TEST	12	rw	**Test Overtemperature Detection** 0_B Disabled 1_B Enabled
UV_OV_SWAP	13	rw	**Test Undervoltage/Overvoltage Detection** 0_B Disabled 1_B Enabled
VIO_SEL	14	rw	**VIO voltage selection** 0_B 3.3 V 1_B 5.0 V

5.3.2.5 Global Diagnosis Register 0

Global Diagnosis Register 0

GLOBAL_DIAG0 Offset address: 0003_H

Global Diagnosis Register 0 value: 0600_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**SPI_WD_ERR**	**Res**			**POR_EVENT**	**RES_EVENT**	**COTWARN**	**COTERR**	**CLK_NOK**	**VDD_OV**	**VDD_UV**	**VIO_OV**	**VIO_UV**	**VBAT_OV**	**VBAT_UV**
r	rwh	r			rw	rw	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VBAT_UV	0	rwh	**VBAT Undervoltage Detection** 0_B No Fault Detected 1_B Fault Detected
VBAT_OV	1	rwh	**VBAT Overvoltage Detection** 0_B No Fault Detected 1_B Fault Detected
VIO_UV	2	rwh	**VIO Undervoltage Detection** 0_B No Fault Detected 1_B Fault Detected
VIO_OV	3	rwh	**VIO Overvoltage Detection** 0_B No Fault Detected 1_B Fault Detected
VDD_UV	4	rwh	**VDD Undervoltage Detection** 0_B No Fault Detected 1_B Fault Detected
VDD_OV	5	rwh	**VDD Overvoltage Detection** 0_B No Fault Detected 1_B Fault Detected
CLK_NOK	6	rwh	**Clock Fault Detection** 0_B No Fault Detected 1_B Fault Detected
COTERR	7	rwh	**Central Overtemperature Error** 0_B No Fault Detected 1_B Fault Detected
COTWARN	8	rwh	**Central Overtemperature Warning** 0_B No Fault Detected 1_B Fault Detected
RES_EVENT	9	rw	**Reset occurred due to RESN-pin low** 0_B No Event Occurred 1_B Event Occurred

(table continues...)

(continued)

Field	Bits	Type	Description
POR_EVENT	10	rw	**Event Occurred** 0_B No Event Occurred 1_B A Power On Reset Event occurred since previous read out
SPI_WD_ERR	14	rwh	**SPI Watchdog Fault Detection** 0_B No Fault Detected 1_B Fault Detected

5.3.2.6 Global Diagnosis Register 1

Global Diagnosis Register 1

GLOBAL_DIAG1 Offset address: 0004_H

Global Diagnosis Register 1 value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HVADC_ERR	**Res**								**VPRE_OV**	**REF_OV**	**REF_UV**	**VDD2V5_OV**	**VDD2V5_UV**	**VR_IREF_OV**	**VR_IREF_UV**
rwh	r								rwh	rwh	rwh	rw	rw	rwh	rwh

Field	Bits	Type	Description
VR_IREF_UV	0	rwh	**Internal Bias Current too Low Detection** 0_B No Fault Detected 1_B Fault Detected
VR_IREF_OV	1	rwh	**Internal Bias Current too High Detection** 0_B No Fault Detected 1_B Fault Detected
VDD2V5_UV	2	rw	**Internal 2V5 Supply Undervoltage Detection** 0_B No Fault Detected 1_B Fault Detected
VDD2V5_OV	3	rw	**Internal 2V5 Supply Overvoltage Detection** 0_B No Fault Detected 1_B Fault Detected
REF_UV	4	rwh	**Internal Reference Undervoltage Detection** 0_B No Fault Detected 1_B Fault Detected
REF_OV	5	rwh	**Internal Reference Overvoltage Detection** 0_B No Fault Detected 1_B Fault Detected
VPRE_OV	6	rwh	**Internal Pre-Regulator Overvoltage Detection** 0_B No Fault Detected 1_B Fault Detected
HVADC_ERR	15	rwh	**Internal Monitoring ADC Error Detection** 0_B No Fault Detected 1_B Fault Detected

5.3.2.7 Global Diagnosis Register 2

Global Diagnosis Register 2

GLOBAL_DIAG2 Offset address: 0005_H

Global Diagnosis Register 2 Reset values see: Table 21

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											**OTP_VIRGIN**	**OTP_ECC_ERR**	**Res**	**REG_ECC_ERR**	**Res**
r											rwh	rwh	r	rwh	r

Field	Bits	Type	Description
REG_ECC_ERR	1	rwh	**Register ECC Error** 0_B No Error 1_B Multi Bit Flip Detected
OTP_ECC_ERR	3	rwh	**OTP ECC Error** 0_B No Error 1_B None Repairable Multi Bit Flip Detected
OTP_VIRGIN	4	rwh	**OTP Memory Configured Complete** 0_B OTP completely configured 1_B Virgin OTP Address Detected

Table 21 Reset values of GLOBAL_DIAG2

Reset type	Reset value	Note
	0000 0000 0000 000X_B	

5.3.2.8 VBAT Threshold Register

VBAT Over and Under Voltage Threshold Register

VBAT_TH Offset address: 0006_H

VBAT Threshold Register value: $FF19_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBAT_OV_TH								**VBAT_UV_TH**							
rwh								rwh							

Field	Bits	Type	Description
VBAT_UV_TH	7:0	rwh	**VBAT Undervoltage Threshold** V_{BAT_UV} = <VBAT_UV_TH> * 0.16208 V
VBAT_OV_TH	15:8	rwh	**VBAT Overvoltage Threshold** V_{BAT_OV} = <VBAT_OV_TH> * 0.16208 V

5.3.2.9 Feedback Freeze Register

Feedback Freeze Register

Feedback Values are provided in the registers FB_DC, FB_VBAT, FB_I_AVG

FB_FRZ Offset address: 0007_H

Feedback Freeze Register value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res										**FR_CH5**	**FR_CH4**	**FR_CH3**	**FR_CH2**	**FR_CH1**	**FR_CH0**
r										rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FR_CH0	0	rw	**Freeze of CH0 Feedback Values** 0_B Disabled 1_B Enabled
FR_CH1	1	rw	**Freeze of CH1 Feedback Values** 0_B Disabled 1_B Enabled
FR_CH2	2	rw	**Freeze of CH2 Feedback Values** 0_B Disabled 1_B Enabled
FR_CH3	3	rw	**Freeze of CH3 Feedback Values** 0_B Disabled 1_B Enabled
FR_CH4	4	rw	**Freeze of CH4 Feedback Values** 0_B Disabled 1_B Enabled
FR_CH5	5	rw	**Freeze of CH5 Feedback Values** 0_B Disabled 1_B Enabled

5.3.2.10 Feedback Update Register

Feedback Update Register
Feedback Values are provided in the registers FB_DC, FB_VBAT, FB_I_AVG

FB_UPD Offset address: 0008_H
Feedback Update Register value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res										**UD_CH5**	**UD_CH4**	**UD_CH3**	**UD_CH2**	**UD_CH1**	**UD_CH0**
r										rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
UD_CH0	0	rh	**Indication of CH0 Feedback Values Update** 0_B No new Feedback Values available 1_B New Feedback Values available
UD_CH1	1	rh	**Indication of CH1 Feedback Values Update** 0_B No new Feedback Values available 1_B New Feedback Values available
UD_CH2	2	rh	**Indication of CH2 Feedback Values Update** 0_B No new Feedback Values available 1_B New Feedback Values available
UD_CH3	3	rh	**Indication of CH3 Feedback Values Update** 0_B No new Feedback Values available 1_B New Feedback Values available
UD_CH4	4	rh	**Indication of CH4 Feedback Values Update** 0_B No new Feedback Values available 1_B New Feedback Values available
UD_CH5	5	rh	**Indication of CH5 Feedback Values Update** 0_B No new Feedback Values available 1_B New Feedback Values available

5.3.2.11 SPI Watchdog Register

SPI Watchdog Counter Reload Register

WD_RELOAD Offset address: 0009_H

SPI Watchdog Register value: 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					**WD_TIME**										
r					rw										

Field	Bits	Type	Description
WD_TIME	10:0	rw	**Reload value of SPI watchdog timout t_SPI_WD** <WD_TIME> = rounddown(t_{SPI_WD} * f_{SYS}/ 2^14)

5.3.2.12 Diagnosis Error Register Channel Group

Diagnosis Error Register Channel Group

DIAG_ERR_CHGR (x=0-2) Offset address: $000A_H+x$

Diagnosis Error Register Channel Group value: 0000_H

13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTE	**SG**	**OC**	**OL**	**OLSG**				**OTE**	**SG**	**OC**	**OL**	**OLSG**
	rwh	rwh	rwh	rwh	rwh				rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
OLSG (y=0-1)	8*y	rwh	**Open Load or Short to Ground Detection** 0_B No Fault Detected 1_B Fault Detected
OL (y=0-1)	8*y+1	rwh	**Open Load Detection** 0_B No Fault Detected 1_B Fault Detected
OC (y=0-1)	8*y+2	rwh	**Overcurrent Detection** 0_B No Fault Detected 1_B Fault Detected
SG (y=0-1)	8*y+3	rwh	**Short to Ground Detection** 0_B No Fault Detected 1_B Fault Detected
OTE (y=0-1)	8*y+4	rwh	**Overtemperature Error Detection** 0_B No Fault Detected 1_B Fault Detected

5.3.2.13 Diagnosis Warning Register Channel Group

Diagnosis Warning Register Channel Group

DIAG_WARN_CHGR (x=0-2) Offset address: 0010_H+x

Diagnosis Warning Register Channel Group value: 1010_H

12	11	10	9	8	7	6	5	4	3	2	1	0
OLSG_WARN_CHK_NOK	**OLSG_WARN**	**OTW**	**I_REG_WARN**	**PWM_REG_WARN**				**OLSG_WARN_CHK_NOK**	**OLSG_WARN**	**OTW**	**I_REG_WARN**	**PWM_REG_WARN**
rwh	rwh	rwh	rwh	rwh				rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PWM_REG_WARN (y=0-1)	8*y	rwh	**ICC PWM Regulation Warning Detection** 0_B No Warning Detected 1_B Warning Detected
I_REG_WARN (y=0-1)	8*y+1	rwh	**ICC Current Regulation Warning** 0_B No Warning Detected 1_B Warning Detected
OTW (y=0-1)	8*y+2	rwh	**Overtemperature Warning Detection** 0_B No Warning Detected 1_B Warning Detected
OLSG_WARN (y=0-1)	8*y+3	rwh	**Open Load or Short to Ground Warning Detection** 0_B No Warning Detected 1_B Warning Detected
OLSG_WARN_CHK_NOK (y=0-1)	8*y+4	rwh	**Open Load or Short to Ground Warning Detection performed** 0_B OLSG Warning Detection performed 1_B OLSG Warning Detection not possible

5.3.2.14 Fault Mask Register 0

FAULTN-pin Mask 0 Register

FAULT_MASK0 Offset address: 0016_H

Fault Mask Register 0 value: $C03F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUP_NOK_EXT_MASK	**SUP_NOK_INT_MASK**	**EN_PIN_MASK**	**Res**							**CH5_ERR_MASK**	**CH4_ERR_MASK**	**CH3_ERR_MASK**	**CH2_ERR_MASK**	**CH1_ERR_MASK**	**CH0_ERR_MASK**
rw	rw	rw	r							rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CH0_ERR_MASK	0	rw	**OC0, SG0, OL0, OTE0, OLSG0 FAULTN-pin Indication** 0_B Disabled 1_B Enabled
CH1_ERR_MASK	1	rw	**OC1, SG1, OL1, OTE1, OLSG1 FAULTN-pin Indication** 0_B Disabled 1_B Enabled
CH2_ERR_MASK	2	rw	**OC2, SG2, OL2, OTE2, OLSG2 FAULTN-pin Indication** 0_B Disabled 1_B Enabled
CH3_ERR_MASK	3	rw	**OC3, SG3, OL3, OTE3, OLSG3 FAULTN-pin Indication** 0_B Disabled 1_B Enabled
CH4_ERR_MASK	4	rw	**OC4, SG4, OL4, OTE4, OLSG4 FAULTN-pin Indication** 0_B Disabled 1_B Enabled
CH5_ERR_MASK	5	rw	**OC5, SG5, OL5, OTE5, OLSG5 FAULTN-pin Indication** 0_B Disabled 1_B Enabled
EN_PIN_MASK	13	rw	**EN-pin Status at FAULTN-pin Indication** 0_B Disabled 1_B Enabled
SUP_NOK_INT_MASK	14	rw	**Internal Supply UV/OV at FAULTN-pin Indication (SUP_NOK_INT)** 0_B Disabled 1_B Enabled
SUP_NOK_EXT_MASK	15	rw	**External Supply UV/OV at FAULTN-pin Indication (SUP_NOK_EXT)** 0_B Disabled 1_B Enabled

5.3.2.15 Fault Mask Register 1

FAULTN-pin Mask 1 Register

FAULT_MASK1 Offset address: 0017_H

Fault Mask Register 1 value: $703F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**CLK_LOW_MASK**	**COTERR_MASK**	**COTWARN_MASK**	**Res**						**CH5_WARN_MASK**	**CH4_WARN_MASK**	**CH3_WARN_MASK**	**CH2_WARN_MASK**	**CH1_WARN_MASK**	**CH0_WARN_MASK**
r	rw	rw	rw	r						rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CH0_WARN_MASK	0	rw	**CH0 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)** 0_B Disabled 1_B Enabled
CH1_WARN_MASK	1	rw	**CH1 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)** 0_B Disabled 1_B Enabled
CH2_WARN_MASK	2	rw	**CH2 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)** 0_B Disabled 1_B Enabled
CH3_WARN_MASK	3	rw	**CH3 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)** 0_B Disabled 1_B Enabled
CH4_WARN_MASK	4	rw	**CH4 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)** 0_B Disabled 1_B Enabled
CH5_WARN_MASK	5	rw	**CH5 Warning at FAULTN-pin Indication (OTW, I_REG_WARN, PWM_REG_WARN, OLSG_WARN)** 0_B Disabled 1_B Enabled
COTWARN_MASK	12	rw	**Central Overtemperature Warning at FAULTN-pin Indication (COTWRN)** 0_B Disabled 1_B Enabled
COTERR_MASK	13	rw	**Central Overtemperature Error at FAULTN-pin Indication (COTERR)** 0_B Disabled 1_B Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
CLK_LOW_MASK	14	rw	**Clock too Slow at FAULTN-pin Indication (DIG_CLK_TOO_SLOW, CLK_TOO_SLOW)** 0_B Disabled 1_B Enabled

5.3.2.16 Fault Mask Register 2

FAULTN-pin Mask 2 Register

FAULT_MASK2 Offset address: 0018_H

Fault Mask Register 2 value: $C000_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI_WD_MASK	**DATA_ERR_MASK**	**Res**													
rw	rw	r													

Field	Bits	Type	Description
DATA_ERR_MASK	14	rw	**Data Error at FAULTN-pin Indication (DATA_ERR)** 0_B Disabled 1_B Enabled
SPI_WD_MASK	15	rw	**SPI Watchdog Fault at FAULTN-pin Indication (SPI_WD_ERR)** 0_B Disabled 1_B Enabled

5.3.2.17 Clock Control Register

Clock Control Register: write access only possible in Config Mode

CLK_DIV Offset address: 0019_H

Clock Control Register value: 0438_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXT_CLK	**PLL_REFDIV**						**PLL_FBDIV**								
rwh	rw						rw								

Field	Bits	Type	Description
PLL_FBDIV	8:0	rw	**PLL feedback divider** <PLL_FBDIV> = 56 MHz * <PLL_REFDIV> / f_{CLK}
PLL_REFDIV	14:9	rw	**PLL reference divider** <PLL_REFDIV> = round(f_{CLK} / 1 MHz)
EXT_CLK	15	rwh	**Clock Source Selection** 0_B Internal Clock 1_B External clock (CLK-pin)

5.3.2.18 BIST Register

Built In Self Test (BIST) register: write access only possible in Config Mode

SFF_BIST Offset address: $003F_H$

BIST Register value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											**SMU_SLF_TST_CERR**	**SMU_SLF_TST_UERR**	**SMU_SLF_TST_FAIL**	**SMU_SLF_TST_DONE**	**SMU_SLF_TST_EN**
r											rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SMU_SLF_TST_EN	0	rwh	**BIST Enable** 0_B BIST not triggered 1_B BIST triggered
SMU_SLF_TST_DONE	1	rwh	**BIST Done** 0_B BIST not done 1_B BIST done
SMU_SLF_TST_FAIL	2	rwh	**BIST Sequence** 0_B Passed 1_B Failed
SMU_SLF_TST_UERR	3	rwh	**BIST Uncorrectable Errors** 0_B Not Tested 1_B Tested
SMU_SLF_TST_CERR	4	rwh	**BIST Correctable Errors** 0_B Not Tested 1_B Tested

5.3.2.19 Version Register

IC version and ID

ICVID Offset address: 0200_H

Version Register value: $C1XX_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MANUFACTURER								**VERSION**							
rh								rh							

Field	Bits	Type	Description
VERSION	7:0	rh	**Chip Version** FC_H A11 Design step FE_H A13 Design step
MANUFACTURER	15:8	rh	**Manufacturer ID**

5.3.2.20 Pin Status Register

Pin Status Feedback Register

PIN_STAT Offset address: 0201_H

Pin Status Register Reset values see: Table 22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res									FAULTN_FB	FAULTN	EN	Res		DRV1	DRV0
r									rh	rh	rh	r		rh	rh

Field	Bits	Type	Description
DRV0	0	rh	**Logic Level of DRV0-pin** 0_B Low 1_B High
DRV1	1	rh	**Logic Level of DRV1-pin** 0_B Low 1_B High
EN	4	rh	**Logic Level of EN-pin** 0_B Low 1_B High
FAULTN	5	rh	**Internal Status of FAULTN-pin according to Fault Mask Configuration** 0_B Fault detected 1_B No Fault detected
FAULTN_FB	6	rh	**Logic Level of FAULTN-pin** 0_B Low 1_B High

Table 22 Reset values of PIN_STAT

Reset type	Reset value	Note
	0000 0000 X00X 00XX$_B$	

5.3.2.21 Feedback Status Register

General status register

FB_STAT Offset address: 0202_H

Feedback Status Register Reset values see: Table 23

21	20	19	18	17	16
INIT_DONE	**SPI_WD_ERR**	**Res**			**ERR_CHGR2**
rh	rh	r			rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_CHGR1	**ERR_CHGR0**	**SUP_NOK_INT**	**SUP_NOK_EXT**	**DATA_err**	**POR_event**	**RES_event**	**COTWARN**	**COTERR**	**CLK_NOK**	**OLSG_WARN_CHK_NOK_CHGR2**	**OLSG_WARN_CHK_NOK_CHGR1**	**OLSG_WARN_CHK_NOK_CHGR0**	**DIAG_WARN_CHGR2**	**DIAG_WARN_CHGR1**	**DIAG_WARN_CHGR0**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DIAG_WARN_CHGR0	0	rh	**Current status of DIAG_WARN_CHGR0 register (excluding <OLSG_WARNx_CHK_NOK>)** 0_B No Warning detected 1_B Warning detected
DIAG_WARN_CHGR1	1	rh	**Current status of DIAG_WARN_CHGR1 register (excluding <OLSG_WARNx_CHK_NOK>)** 0_B No Warning detected 1_B Warning detected
DIAG_WARN_CHGR2	2	rh	**Current status of DIAG_WARN_CHGR2 register (excluding <OLSG_WARNx_CHK_NOK>)** 0_B No Warning detected 1_B Warning detected
OLSG_WARN_CHK_NOK_CHGR0	3	rh	**Current status of <OLSG_WARNx_CHK_NOK> bit in the DIAG_WARN_CHGR0 register** 0_B No Warning detected 1_B Warning detected
OLSG_WARN_CHK_NOK_CHGR1	4	rh	**Current status of <OLSG_WARNx_CHK_NOK> bit in the DIAG_WARN_CHGR1 register** 0_B No Warning detected 1_B Warning detected
OLSG_WARN_CHK_NOK_CHGR2	5	rh	**Current status of <OLSG_WARNx_CHK_NOK> bit in the DIAG_WARN_CHGR2 register** 0_B No Warning detected

(table continues...)

(continued)

Field	Bits	Type	Description
			1_B Warning detected
CLK_NOK	6	rh	**Current status of CLK_NOK in GLOBAL_DIAG0 register** 0_B No Fault detected 1_B Fault detected
COTERR	7	rh	**Current status of COTERR in GLOBAL DIAG0 register** 0_B No Fault detected 1_B Fault detected
COTWARN	8	rh	**Current status of COTWARN in GLOBAL DIAG0 register** 0_B No Warning detected 1_B Warning detected
RES_event	9	rh	**Current status of RES_event in GLOBAL DIAG0 register** 0_B No Reset Event 1_B Reset occurred
POR_event	10	rh	**Current status of POR_event in GLOBAL DIAG0 register** 0_B No Power on Reset 1_B Power on Reset occurred
DATA_err	11	rh	**Current status of <OTP_ECC_ERR>, <OTP_VIRGIN>, <HV_ADC_ERR>** 0_B No Fault detected 1_B Fault detected
SUP_NOK_EXT	12	rh	**Current status of <VIO_UV/OV>, <VDD_UV/OV>, <VBAT_UV/OV>** 0_B No Fault detected 1_B Fault detected
SUP_NOK_INT	13	rh	**Current status of <VDD2V5_UV/OV>, <REF_UV/OV>, <VR_IREF_UV/OV>, <VPRE_OV>** 0_B No Fault detected 1_B Fault detected
ERR_CHGR0	14	rh	**Current status of DIAG_ERR_CHGR1 register** 0_B No Fault detected 1_B Fault detected
ERR_CHGR1	15	rh	**Current status of DIAG_ERR_CHGR2 register** 0_B No Fault detected 1_B Fault detected
ERR_CHGR2	16	rh	**Current status of DIAG_ERR_CHGR3 register** 0_B No Fault detected 1_B Fault detected
SPI_WD_ERR	20	rh	**Current status of <SPI_WD_ERR>** 0_B No Fault detected 1_B Fault detected
INIT_DONE	21	rh	**Chip Initialization** 0_B Not Done

(table continues...)

(continued)

Field	Bits	Type	Description
			1_B Done

Table 23 Reset values of FB_STAT

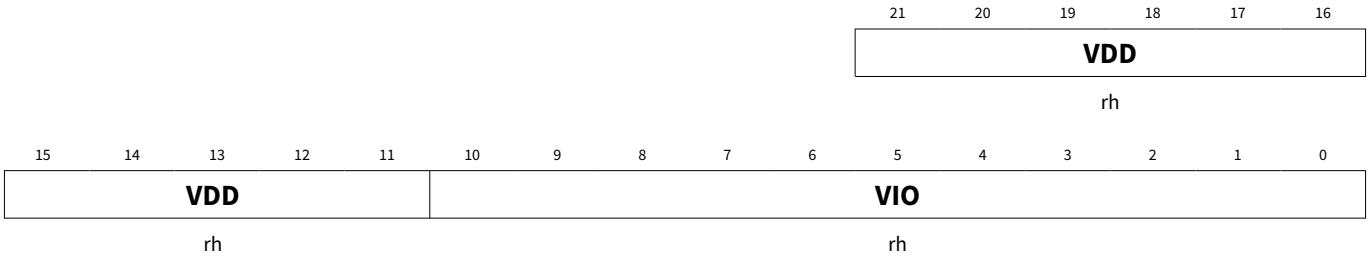
Reset type	Reset value	Note
	10 0000 0000 0110 0011 1000_B	

5.3.2.22 Feedback Voltage Register 1

Supply Voltage Feedback Register 1

FB_VOLTAGE1 Offset address: 0203_H

Feedback Voltage Register 1 value: XX $XXXX_H$



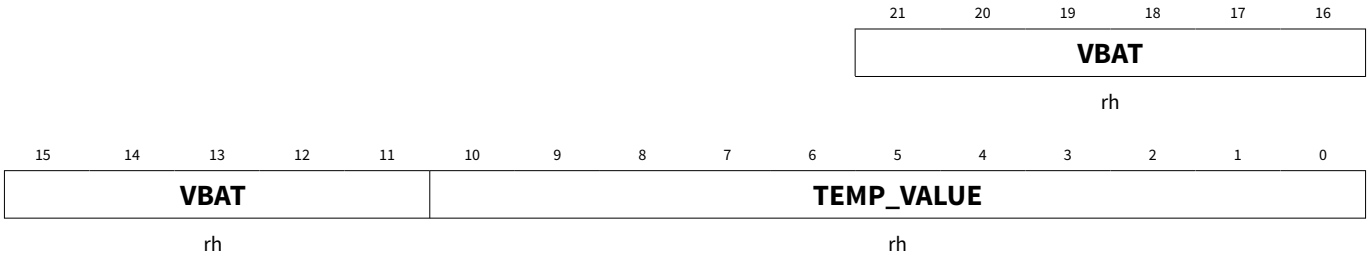
Field	Bits	Type	Description
VIO	10:0	rh	**VIO Voltage** V_{IO} = 0.0034534 V * <VIO>
VDD	21:11	rh	**VDD Voltage** V_{DD} = 0.0034534 V * <VDD>

5.3.2.23 Feedback Voltage Register 2

Supply Voltage Feedback Register 2

FB_VOLTAGE2 Offset address: 0204_H

Feedback Voltage Register 2 value: XX $XXXX_H$



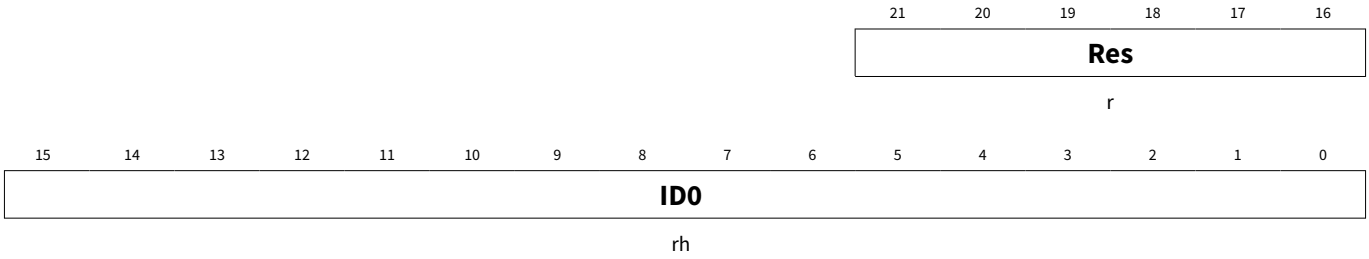
Field	Bits	Type	Description
TEMP_VALUE	10:0	rh	**Temperature Feedback** T_{FB} =(<TEMP_VALUE>*0.000593 - 0.819)/(-0.0016) [Celsius]
VBAT	21:11	rh	**VBAT Voltage** V_{BAT} = 41.47 V * <VBAT>/(2^11-1)

5.3.2.24 Unique Chip Identification Number Register 0

Unique Chip Identification Number Register 0

CHIPID0 Offset address: 0205_H

Unique Chip Identification Number Register 0 value: XX $XXXX_H$



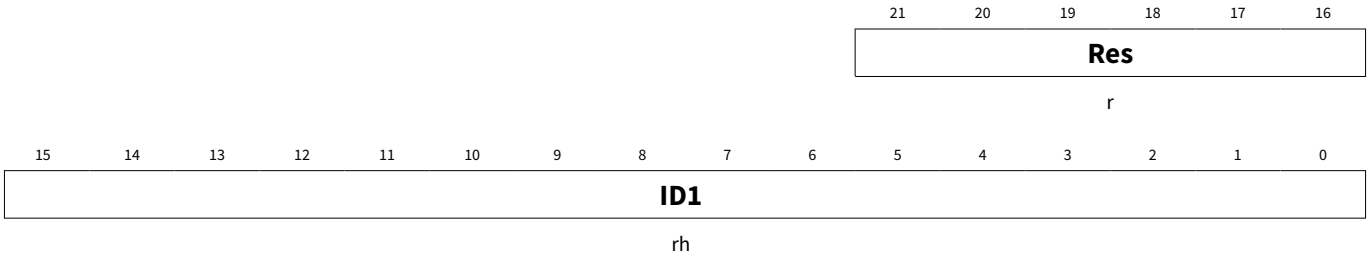
Field	Bits	Type	Description
ID0	15:0	rh	**ID0**

5.3.2.25 Unique Chip Identification Number Register 1

Unique Chip Identification Number Register 1

CHIPID1 Offset address: 0206_H

Unique Chip Identification Number Register 1 value: XX $XXXX_H$



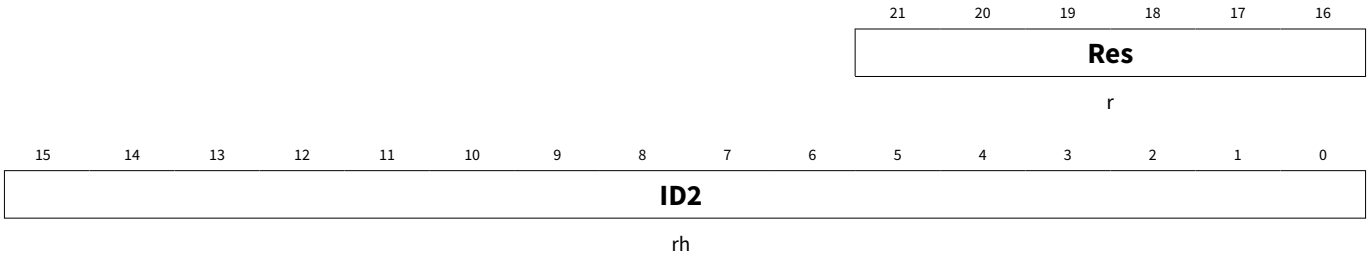
Field	Bits	Type	Description
ID1	15:0	rh	**ID1**

5.3.2.26 Unique Chip Identification Number Register 2

Unique Chip Identification Number Register 2

CHIPID2 Offset address: 0207_H

Unique Chip Identification Number Register 2 value: XX $XXXX_H$



Field	Bits	Type	Description
ID2	15:0	rh	**ID2**

5.3.3 Channel registers

5.3.3.1 Register Overview - Channel (ascending Offset Address)

Table 24 Register Overview - Channel (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
SETPOINT	Setpoint Register	0000_H	86
CTRL	Control Register	0001_H	87
PERIOD	ICC PWM Frequency Controller Register	0002_H	88
INTEGRATOR_LIMIT	ICC Integrator Limitation Register	0003_H	89
DITHER_CLK_DIV	Dither Clock Register	0004_H	90
DITHER_STEP	Dither Step Register	0005_H	91
DITHER_CTRL	Dither Control Register	0006_H	92
CH_CONFIG	Channel Configuration Register	0007_H	93
MODE	Channel Mode Register	$000C_H$	95
TON	On-Time Register	$000D_H$	96
CTRL_INT_THRESH	ICC Integrator Threshold Control Register	$000E_H$	97
FB_DC	Feedback Duty Cycle Register	0200_H	98
FB_VBAT	Feedback Average VBAT	0201_H	99
FB_I_AVG	Feedback Average Current	0202_H	100
FB_IMIN_IMAX	Feedback Min/Max Current	0203_H	101
FB_I_AVG_s16	Feedback signed Current	0204_H	102
FB_INT_THRESH	Feedback ICC Integrator Threshold	0205_H	103
FB_PERIOD_MIN_MAX	Feedback Min/Max PWM Period	0206_H	104

5.3.3.2 Register Address Space - Channel

Table 25 Registers Address Space - Channel

Module	Base Address	End Address	Note
CH0	00000040_H	$0001003E_H$	
CH1	00000050_H	$0001004E_H$	
CH2	00000060_H	$0001005E_H$	
CH3	00000070_H	$0001006E_H$	
CH4	00000020_H	$0001001E_H$	
CH5	00000030_H	$0001002E_H$	

5.3.3.3 Setpoint Register

Current Setpoint Register

SETPOINT Offset address: 0000_H

Setpoint Register Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUTO_LIMIT_DIS	**TARGET**														
rwh	rwh														

Field	Bits	Type	Description
TARGET	14:0	rwh	**Current Setpoint Target** I_{set} = 2A * <TARGET> / (2^15 - 1) $I_{set,par}$ = 4A * <TARGET> / (2^15 - 1) NOTE: Values higher than 0x6000 are saturated
AUTO_LIMIT_DIS	15	rwh	**Autolimit Feature** 0_B Enabled 1_B Disabled

5.3.3.4 Control Register

Channel Control Register

CTRL Offset address: 0001_H

Control Register Value 4600_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**OLSG_WARN_EN**	**OLSG_WARN_WINDOW**					**PWM_PERIOD_CALC_MODE**	**MIN_INT_THRESH**							
r	rw	rw					rw	rw							

Field	Bits	Type	Description
MIN_INT_THRESH	7:0	rw	**Minimum limit for ICC integrator threshold** The value is signed: -128 to 127
PWM_PERIOD_CALC_MODE	8	rw	**ICC PWM controller does not consider falling Dither Slope** 0_B No disabling of threshold calculation 1_B Skip threshold calculation on falling dither
OLSG_WARN_WINDOW	13:9	rw	**OLSG Warning Detection Blanking Time** $t_{OLwindow}$= (<OLSG_WARN_WINDOW>+1) * 64 * 1/ fsys
OLSG_WARN_EN	14	rw	**OLSG Warning Detection** 0_B Disable warning 1_B Enable warning

5.3.3.5 ICC PWM Frequency Controller Register

ICC PWM Frequency Controller Register

PERIOD Offset address: 0002_H

ICC PWM Frequency Controller Register Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_CTRL_PARAM				**LOW_FREQ_RANGE_EN**	**PERIOD_EXP**			**PERIOD_MANT**							
rw				rw	rw			rw							

Field	Bits	Type	Description
PERIOD_MANT	7:0	rw	**Mantissa of PWM Target Frequency** t_{PWM} = <PERIOD_MANT> * 2^<PERIOD_EXP> * $1/f_{sys}$ <PERIOD_MANT> = 0 disables the ICC PWM Frequency Controller
PERIOD_EXP	10:8	rw	**Exponent of PWM Target Frequency** t_{PWM} = <PERIOD_MANT> * 2^<PERIOD_EXP> * $1/f_{sys}$
LOW_FREQ_RANGE_EN	11	rw	**Low PWM Frequency Range** t_{PWM} = <PERID_MANT> * 8 * 2^<PERIOD_EXP> * $1/f_{sys}$ 0_B Disabled 1_B Enabled
PWM_CTRL_PARAM	15:12	rw	**Control parameter ki of PWM Frequency Controller**

5.3.3.6 ICC Integrator Limitation Register

ICC Integrator Limitation Register

INTEGRATOR_LIMIT Offset address: 0003_H

ICC Integrator Limitation Register Value $43FF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**AUTO_LIM_VALUE_ABS**					**LIM_VALUE_ABS**									
r	rw					rw									

Field	Bits	Type	Description
LIM_VALUE_ABS	9:0	rw	**Absolut Integrator Limit of ICC**
AUTO_LIM_VALUE_ABS	14:10	rw	**Integrator Limit of ICC after a setpoint update (Autolimit)**

5.3.3.7 Dither Clock Register

Dither Period Configuration

DITHER_CLK_DIV Offset address: 0004_H

Dither Clock Register Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITHER_SETPOINT_SYNC_EN	**DITHER_PWM_SYNC_EN**	**EXP**				**MANT**									
rw	rw	rw				rw									

Field	Bits	Type	Description
MANT	9:0	rw	**Mantissa of Dither Reference Clock** t_{ref_clk} = (<MANT> * 2 <EXP>) * $1/f_{sys}$
EXP	13:10	rw	**Exponent of Dither Reference Clock** t_{ref_clk} = (<MANT> * 2 <EXP>) * $1/f_{sys}$
DITHER_PWM_SYNC_EN	14	rw	**Synchronization of Dither Period with PWM Period** 0_B Disabled 1_B Enabled
DITHER_SETPOINT_SYNC_EN	15	rw	**Synchronization of the Dither Period to a setpoint change** 0_B Disabled 1_B Enabled

5.3.3.8 Dither Step Register

Dither Amplitude Configuration

DITHER_STEP Offset address: 0005_H

Dither Step Register Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STEPS								**FLAT**							
rw								rw							

Field	Bits	Type	Description
FLAT	7:0	rw	**Number of flat Dither Reference Clocks tref_clk on top and bottom of the Dither waveform** t_{flat}= <FLAT> * t_{ref_clk}
STEPS	15:8	rw	**Number of Dither steps within a quarter Dither Period** T_{Dither} = [4* (<STEPS>) + 2 * <FLAT>] * t_{ref_clk} I_{Dither} =<STEPS>*<STEP_SIZE> * 2 A / (2^{15}-1) NOTE: If <STEP_SIZE> = 0, the dither overlay I_{Dither} is disabled. NOTE: If <STEPS> = 0, the dither overlay I_{Dither} is disabled and the dither period T_{Dither} is determined by <FLAT> NOTE: If <STEPS> = 0 and <FLAT> = 0, the dither period T_{Dither}=t_{ref_clk}

5.3.3.9 Dither Control Register

Dither Control Register

DITHER_CTRL Offset address: 0006_H

Dither Control Register Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAST_MEAS		**DEEP_DITHER**	**Res**	**STEP_SIZE**											
rw		rw	r	rw											

Field	Bits	Type	Description
STEP_SIZE	11:0	rw	**Size of Dither Steps resulting in a Dither Amplitude IDither** I_{Dither} =<STEPS>*<STEP_SIZE> * 2 A / (2^{15}-1)
DEEP_DITHER	13	rw	**Deep Dither Feature** 0_B Disabled 1_B Enabled
FAST_MEAS	15:14	rw	**Fast Measurement Feedback Period** 00_B Dither Period 01_B Half of Dither Period (n_meas_sampe = 2) 10_B Quad of Dither Period (n_meas_sampe = 4)

5.3.3.10 Channel Configuration Register

Channel Configuration Register

CH_CONFIG Offset address: 0007_H

Channel Configuration Register Value 0003_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFF_DIAG_CH		**OC_DIAG_EN**	**OL_TH_FIXED**						**OL_TH**			**I_DIAG**		**SLEWR**	
rwh		rwh	rw						rw			rw		rw	

Field	Bits	Type	Description
SLEWR	1:0	rw	**Channel Slew Rate** 00_B 1.0 V/us 01_B 2.5 V/us 10_B 5.0 V/us 11_B 10.0 V/us
I_DIAG	3:2	rw	**OFF-state Diagostic current** 00_B 80 uA 01_B 190 uA 10_B 720 uA 11_B 1250 uA
OL_TH	6:4	rw	**Open Load Threshold relative to Setpoint** 000_B Disabled 001_B 1/8 of Current Setpoint 010_B 2/8 of Current Setpoint 011_B 3/8 of Current Setpoint 100_B 4/8 of Current Setpoint 101_B 5/8 of Current Setpoint 110_B 6/8 of Current Setpoint 111_B 7/8 of Current Setpoint
OL_TH_FIXED	12:7	rw	**Fixed Open Load Threshold** I_{OLTH} = <OL_TH_FIXED> * 128 * 2000mA / (2^15 - 1) $I_{OLTH,parallel}$ = <OL_TH_FIXED> * 128 * 4000mA / (2^15 - 1)
OC_DIAG_EN	13	rwh	**OC Diagnosis in OFF-state** 0_B Disabled 1_B Enable Output Stage for t_OCon t_{OCon} = [(<TON_MANT>+1)*2^<EXP>)] * $1/f_{SYS}$ NOTE: <TON_MANT> is located in the TON register. NOTE: <EXP> is located in the DITHER_CLK_DIV register.
OFF_DIAG_CH	15:14	rwh	**OFF-state Diagnosis Current Sources Control** 00_B OFF-state Diagnosis Enabled 01_B Low Side Current Source Enabled 10_B High Side Current Source Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
			11_B OFF-state Diagnosis Disabled

5.3.3.11 Channel Mode Register

Channel Mode Register: write access only possible in Config Mode

MODE Offset address: $000C_H$

Channel Mode Register Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res												**CH_MODE**			
r												rw			

Field	Bits	Type	Description
CH_MODE	3:0	rw	**Channel Operation Mode** 0_H Off 1_H ICC Current Control 2_H Direct Drive Mode via SPI on-time setting (TON register) 3_H Direct Drive via DRV0 pin 4_H Direct Drive via DRV1 pin C_H Free running Measurement (2^16 samples)

5.3.3.12 On-Time Register

Driver On-Time Configuration Register

TON Offset address: $000D_H$

On-Time Register Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OLSG_TIMEOUT						**TON_MANT**									
rw						rw									

Field	Bits	Type	Description
TON_MANT	9:0	rw	**On-Time of Output stage in SPI Direct Drive Mode** t_{OCon} = [(<TON_MANT>+1)*2^<EXP>)] * $1/f_{sys}$ NOTE: For OC detection in OFF-state the maximum t_{on} period is 300ms and <TON_MANT> must be different to 0. t_{on} = (<TON_MANT> * 2^<EXP>) * $1/f_{sys}$ NOTE: The Period is derived from the Dither Period (DITHER_CLK_DIV) NOTE: <EXP> is located in the DITHER_CLK_DIV register
OLSG_TIMEOUT	15:10	rw	**Time out period for OLSG detection** $t_{OLSG\_TIMEOUT}$ = (<OLSG_TIMEOUT> *256 +255) *64 * $1/f_{sys}$

5.3.3.13 ICC Integrator Threshold Control Register

ICC Integrator Threshold Control Register

CTRL_INT_THRESH Offset address: $000E_H$

ICC Integrator Threshold Control Register Value 0003_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							**INT_THRESH**								
r							rw								

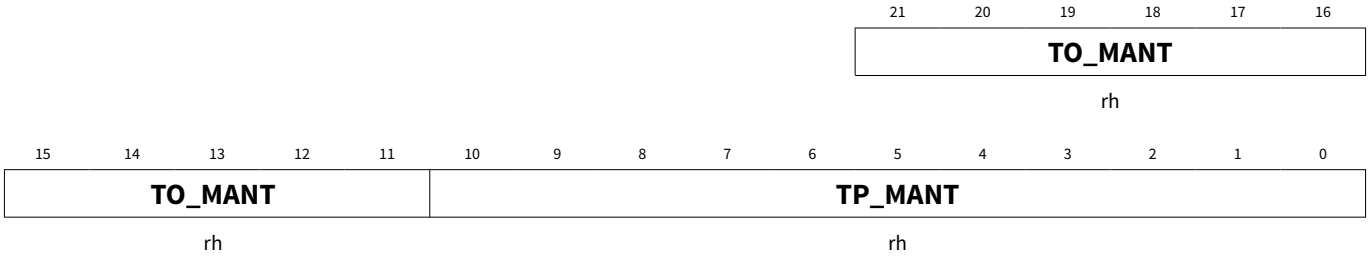
Field	Bits	Type	Description
INT_THRESH	8:0	rw	**ICC Integrator Threshold which determines the on-time of the PWM period** NOTE: <INT_THRESH> is used as inital threshold value for the ICC PWM Frequency Controller.

5.3.3.14 Feedback Duty Cycle Register

Duty Cycle Feedback Value
Read Only Register

FB_DC Offset address: 0200_H

Feedback Duty Cycle Register Value $00\ 0000_H$



Field	Bits	Type	Description
TP_MANT	10:0	rh	**Period Mantissa** T_{meas} = <TP_MANT> * 2^<EXP> * $1/f_{sys}$ NOTE: <EXP> is located in the FB_VBAT or FB_I_AVG register.
TO_MANT	21:11	rh	**On-time Mantissa** t_{ON} = <TO_MANT>*2^<EXP> * $1/f_{sys}$ *DC*= <TO_MANT>/<TP_MANT> NOTE: <EXP> is located in the FB_VBAT or FB_I_AVG register.

5.3.3.15 Feedback Average VBAT

Average Battery Voltage (VBAT) Feedback Register
Read Only Register

FB_VBAT Offset address: 0201_H

Feedback Average VBAT Value $00\ 0000_H$

21	20	19	18	17	16
Res		**DITHER_PERIOD_CNT**		**DITHER_QUAD_CNT**	
r		rh		rh	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXP				**Res**	**VBAT_AVG_MANT**										
rh				r	rh										

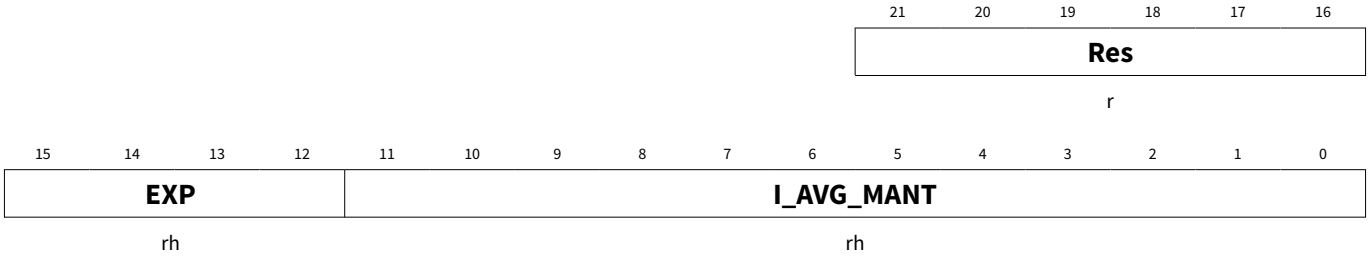
Field	Bits	Type	Description
VBAT_AVG_MANT	10:0	rh	**Average Battery Voltage Mantissa** V_{BAT} = 41.47V * <VBAT_AVG_MANT>/<TP_MANT> NOTE: <TP_MANT> is located in the FB_DC register
EXP	15:12	rh	**Measurement Exponent**
DITHER_QUAD_CNT	17:16	rh	**Quad Dither Interval Counter** 00_B First Quad of Dither Period 01_B Second Quad/First Half of Dither Period 10_B Third Quad of Dither Period 11_B Fourth Quad/Second Half of Dither Period
DITHER_PERIOD_CNT	19:18	rh	**Dither Interval Counter** 00_B First Dither Period 01_B Second Dither Period 10_B Third Dither Period 11_B Fourth Dither Period

5.3.3.16 Feedback Average Current

Average Current Feedback Value
Read Only Register

FB_I_AVG Offset address: 0202_H

Feedback Average Current Value $00\ 0000_H$



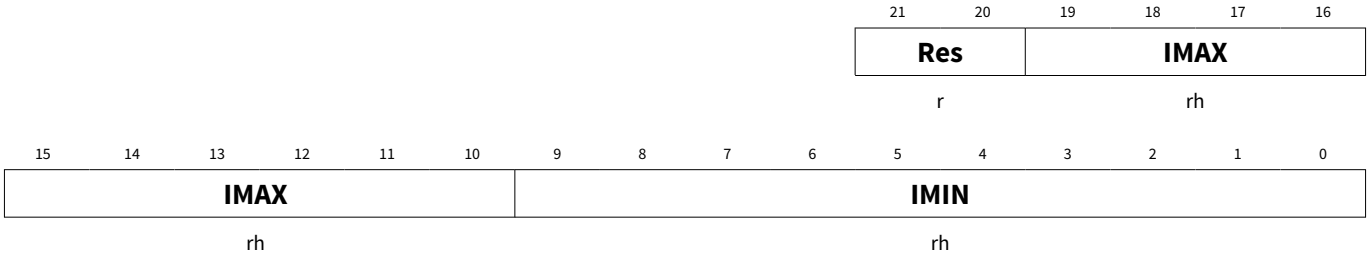
Field	Bits	Type	Description
I_AVG_MANT	11:0	rh	**Signed Mantissa of Average Current Feedback (two's complement)** I_{avg} = 4A * <I_AVG_MANT> / <TP_MANT> NOTE: <TP_MANT> is located in the FB_DC register
EXP	15:12	rh	**Measurement Exponent**

5.3.3.17 Feedback Min/Max Current

Minimum/Maximum Current Feedback Register
Read Only Register

FB_IMIN_IMAX Offset address: 0203_H

Feedback Min/Max Current Value $00\ 0000_H$



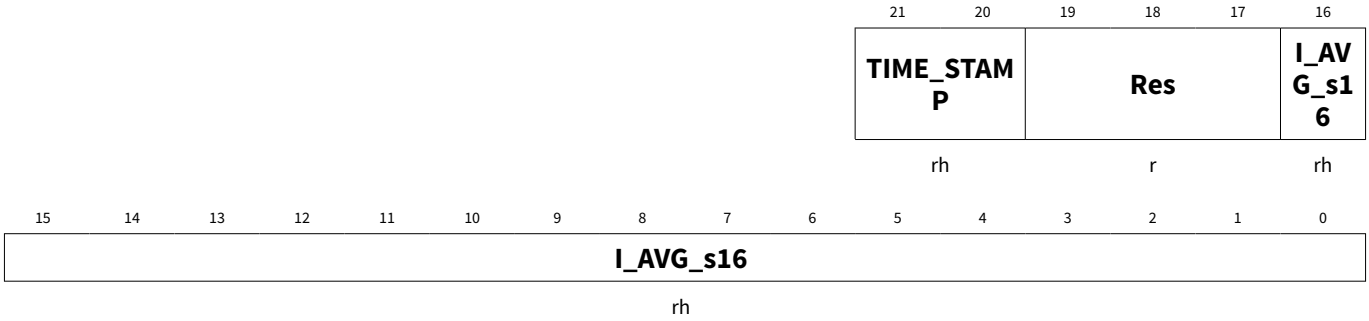
Field	Bits	Type	Description
IMIN	9:0	rh	**Signed Minimum Current of last measurement period (two's complement)** I_{min} = <IMIN>*4A / (2^9-1)
IMAX	19:10	rh	**Signed Maximum Current of last measurement period (two's complement)** I_{max} = <IMAX>*4A / (2^9-1)

5.3.3.18 Feedback signed Current

Signed Average Current Measurement over free running period (2^16 f_{sys} cycles)
Read Only Register

FB_I_AVG_s16 Offset address: 0204_H

Feedback signed Current Value $00\ 0000_H$



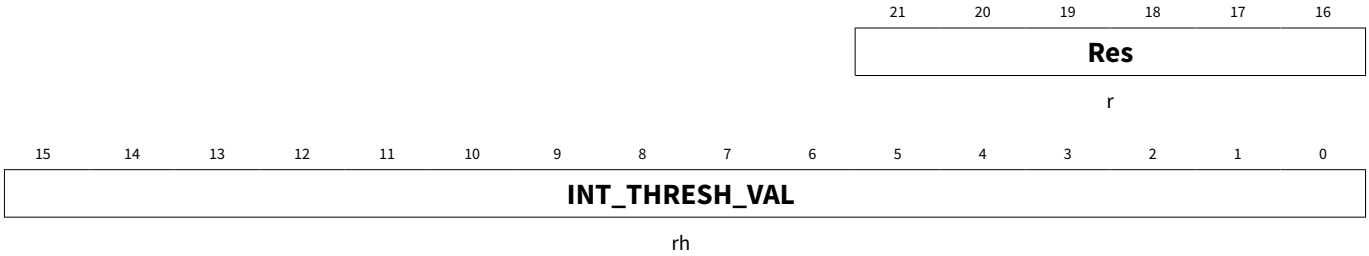
Field	Bits	Type	Description
I_AVG_s16	16:0	rh	**Average Current Measurement over free running period (2^16 fsys cycles) - two's complement** I_{avg16} = 4A* <I_AVG_s16>/(2^16-1)
TIME_STAMP	21:20	rh	**Time Stamp for signed Average Current Measurement over free running period**

5.3.3.19 Feedback ICC Integrator Threshold

ICC PWM Frequency Controller Integrator Thershold Feedback
Read Only Register

FB_INT_THRESH Offset address: 0205_H

Feedback ICC Integrator Threshold Value $00\ 0180_H$



Field	Bits	Type	Description
INT_THRESH_VAL	15:0	rh	**ICC PWM Frequency Controller Calculated Integrator Threshold Value**

5.3.3.20 Feedback Min/Max PWM Period

Minimum and Maximum PWM Frequency Feedback of last Measurement period
Read Only Register

FB_PERIOD_MIN_MAX Offset address: 0206_H

Feedback Min/Max PWM Period Value $00\ 0000_H$

21	20	19	18	17	16
Res		**PMAX**			
r		rh			

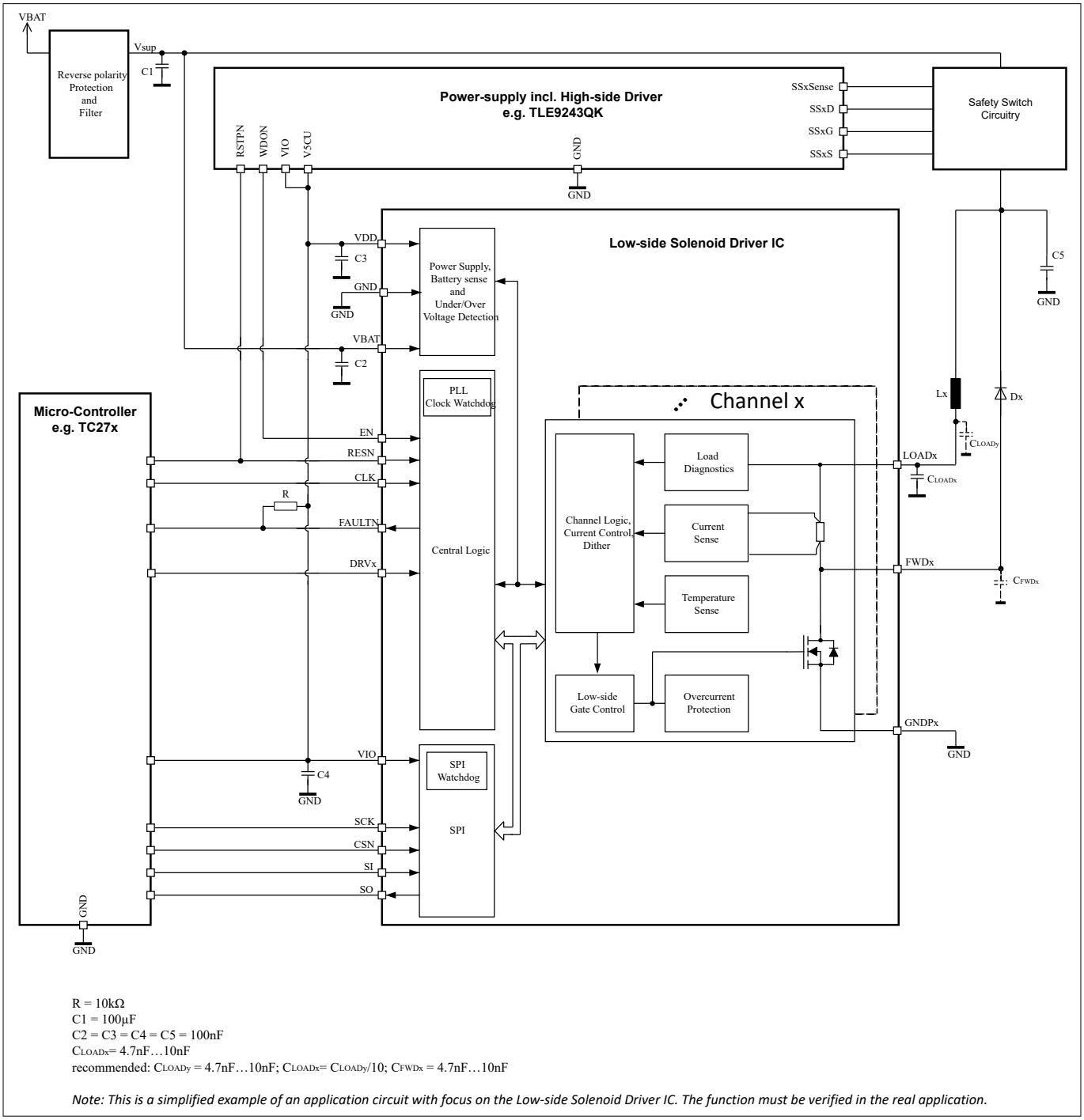
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMAX						**PMIN**									
rh						rh									

Field	Bits	Type	Description
PMIN	9:0	rh	**Minimum PWM period of last Measurement period** f_{PWM_min} = <PMIN> * 256 * 1/f_{sys}
PMAX	19:10	rh	**Maximum PWM period of last Measurement period** f_{PWM_max} = <PMAX> * 256 * 1/f_{sys}

6 Application information

6.1 TDS_Application information

The following application diagram shows how the IC is used in its environment.



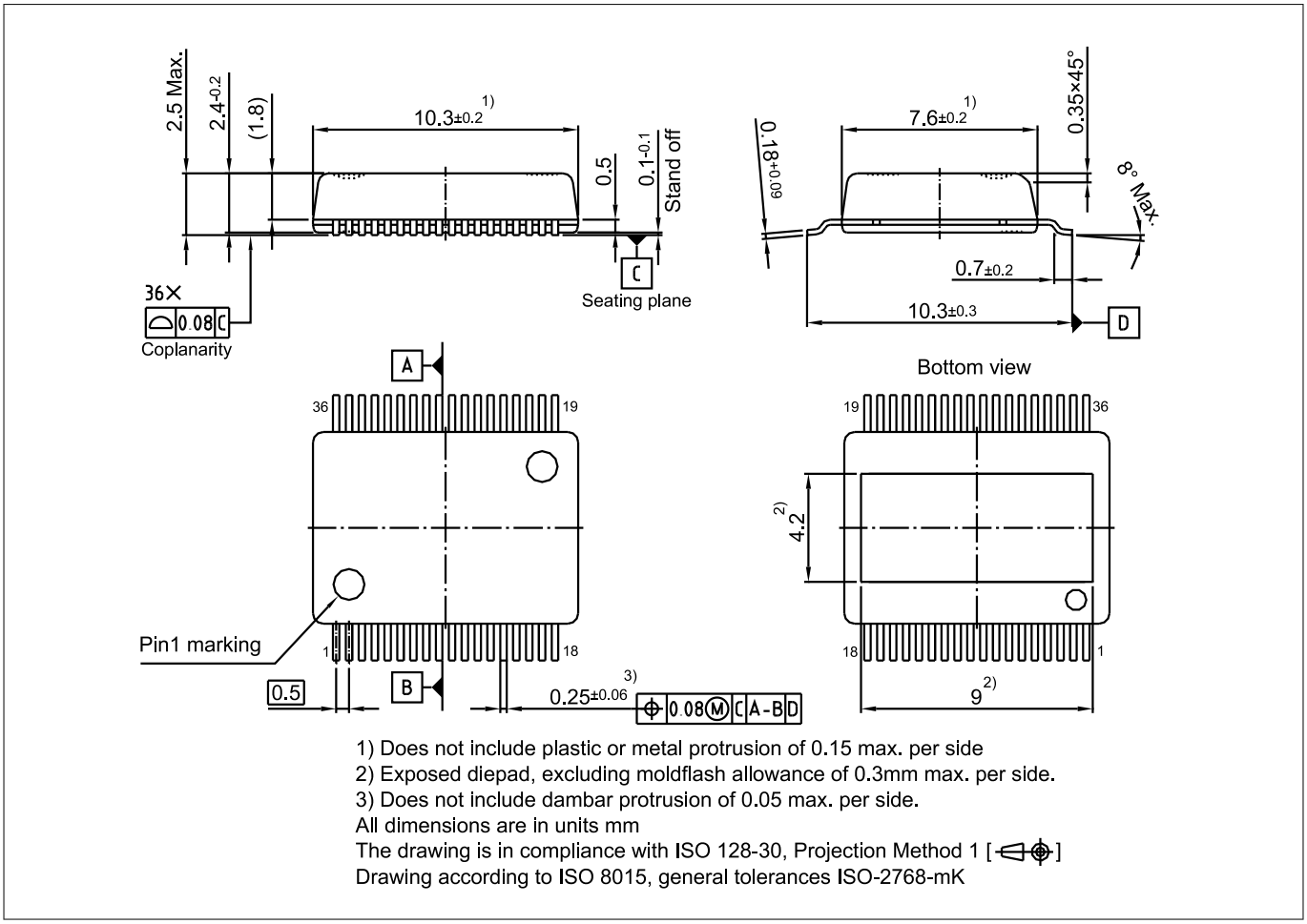
R = 10kΩ
C1 = 100µF
C2 = C3 = C4 = C5 = 100nF
C_{LOADx}= 4.7nF…10nF
recommended: C_{LOADy} = 4.7nF…10nF; C_{LOADx}= C_{LOADy}/10; C_{FWDx} = 4.7nF…10nF

Note: This is a simplified example of an application circuit with focus on the Low-side Solenoid Driver IC. The function must be verified in the real application.

Figure 26 Simplified Application Circuit

7 Package dimensions

7.1 TDS_Package dimensions



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Exposed diepad, excluding moldflash allowance of 0.3mm max. per side.
3) Does not include dambar protrusion of 0.05 max. per side.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ISO-2768-mK

Figure 27 Package outlines

Green Product

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with the government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision history

Revision	Date	Changes
Datasheet v1.2	2022-02-01	• new Package Drawing Layout (no changes in dimensions) • changes in register "GLOBAL_DIAG2"
Datasheet v1.0	2020-11-20	initial release

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