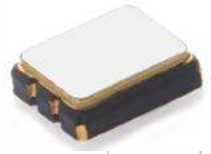
Model 634P/L

Advanced PLL LVPECL or LVDS Clock



Part Dimensions:
3.2 × 2.5 × 1.1mm • 24mg

Features

- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 500fs Typical
- Advanced PLL Design w/ Low Fundamental Crystal
- Frequency Range 10MHz – 800MHz *
- +2.5V or +3.3V Operation
- Output Enable Standard, Pin 2 Option Available
- Tape and Reel Packaging, EIA-418

Applications

- Broadcast Video Systems
- Storage Area Networking
- Broadband Access
- PCI Express
- Networking Equipment
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Standard Frequencies

- 50.00MHz	- 125.00MHz	- 200.00MHz
- 100.00MHz	- 150.00MHz	
- 106.25MHz	- 156.25MHz	

* See Page 8 for additional developed frequencies.
Check with factory for availability of frequencies not listed.

Description

CTS Model 634P/L is a low cost, high performance PLL clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M634P/L has excellent stability and low phase jitter performance.

Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
634	P	XXX or XXXX	3	I	3	T

Code	Output
P	LVPECL - Pin 1 Enable
L	LVDS - Pin 1 Enable
E	LVPECL - Pin 2 Enable
V	LVDS - Pin 2 Enable

Code	Stability
6	±20ppm [2]
5	±25ppm [3]
4	±30ppm
3	±50ppm

Code	Voltage
2	+2.5Vdc
3	+3.3Vdc

Code	Frequency
	Product Frequency Code [1]

Code	Temp. Range
C	-20°C to +70°C
I	-40°C to +85°C

Code	Packing
T	1k pcs./reel

Notes:
1] Refer to document 016-1454-0, Frequency Code Tables.
3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
2] 6I Stability/Temperature combination not available.
3] Check factory availability when paired with 'I' temperature code.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.0	V
Supply Voltage	V_{CC}	±5%	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current LVPECL LVDS	I_{CC}	Maximum Load Maximum Current Value @ +3.3V	 - -	 54 23	 88 65	mA
Operating Temperature	T_A	-	-20 -40	+25	+70 +85	℃
Storage Temperature	T_{STG}	-	-55	-	+125	℃

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_O	-		10 - 800		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	-		20, 25 or 50		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25℃, nominal V_{CC}	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	R_L	Terminated to V_{CC} - 2.0V	-	50	-	Ohms
Output Voltage Levels	V_{OH} V_{OL}	PECL Load	V_{CC} - 1.03 V_{CC} - 1.85	- -	V_{CC} - 0.60 V_{CC} - 1.60	V
Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 50 Ohms	-	0.25	0.60	ns

Output Type	-	-		LVDS		-
Output Load	R_L	Between Outputs	-	100	-	Ohms
Output Voltage Levels	V_{OH} V_{OL}	LVDS Load	- 0.90	1.43 1.10	1.60 -	V
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V_{OD}	R_L = 100 Ohms	175	330	454	mV
Offset Voltage	V_{OS}	LVDS Load	1.20	1.25	1.30	V
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 100 Ohms	-	-	0.5	ns

Electrical Specifications

Output Parameters

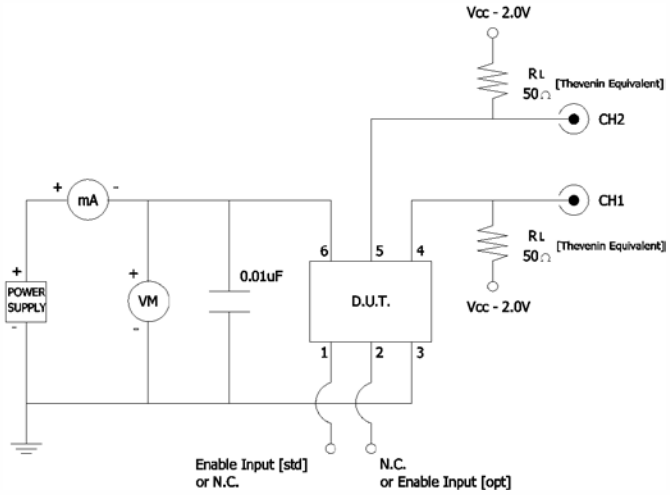
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T_S	Application of V_{CC}	-	3	5	ms
Enable Function [Tri-State]						
Enable Input Voltage	V_{IH}	Pin 1 or 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Current	I_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	16	22	mA
Enable Time	T_{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	200	ns
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	500	<1000	fs
Period Jitter, RMS	pjrms	-	-	2.5	-	ps
Period Jitter, pk-pk	pjpk-pk	-	-	25	-	ps

Enable Truth Table

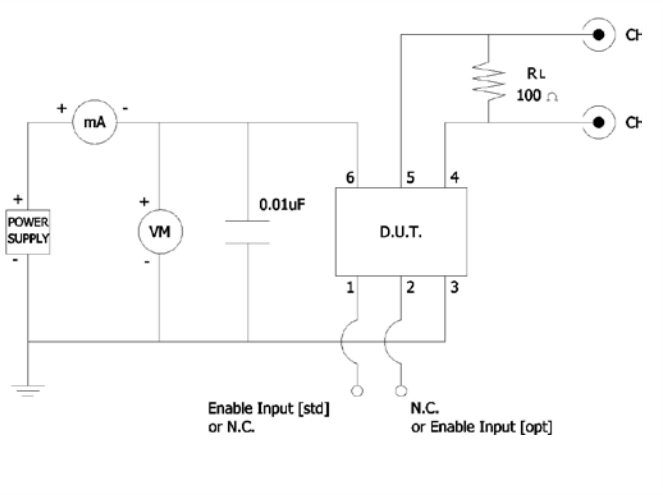
Pin 1 or Pin 2	Pin 4 & Pin 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

Test Circuit

LVPECL

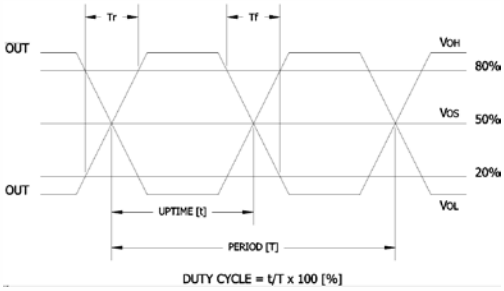


LVDS



Output Waveform

LVPECL or LVDS

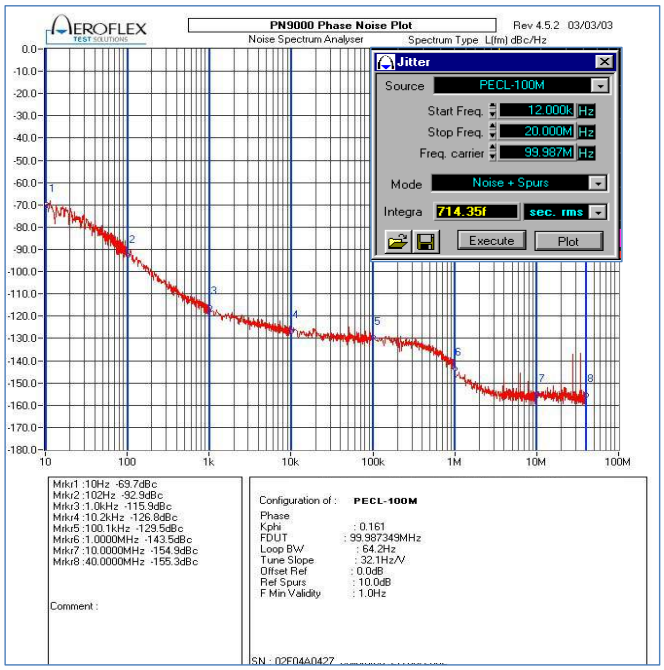


Electrical Specifications

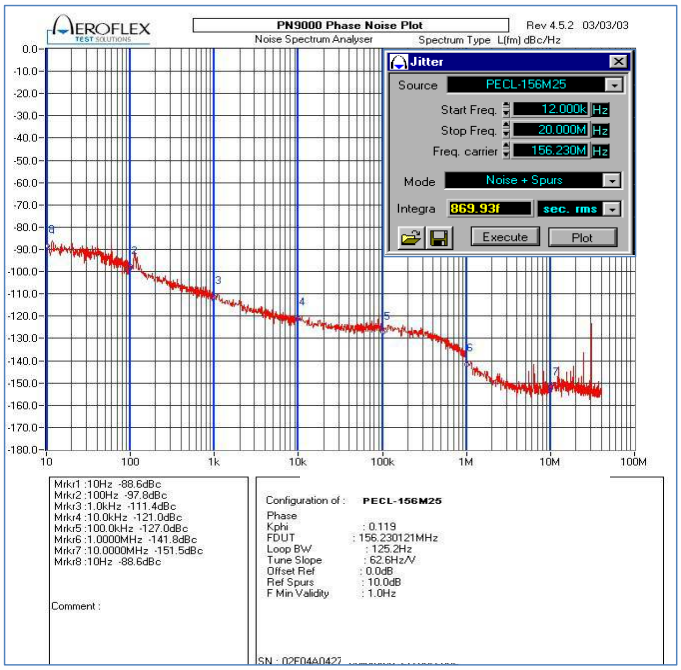
Performance Data

Phase Noise [typical]

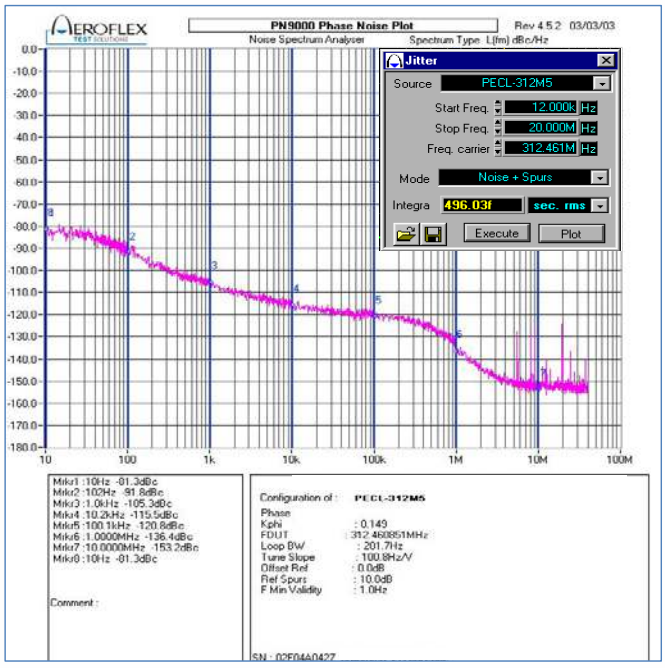
100.00MHz, LVPECL, V_{CC} = 3.3V, T_A = +25°C



156.25MHz, LVPECL, V_{CC} = 3.3V, T_A = +25°C



312.50MHz, LVPECL, V_{CC} = 3.3V, T_A = +25°C



Performance Data

Phase Noise Tabulated

Typical, HCMOS, V_{CC} = 3.3V, T_A = +25°C

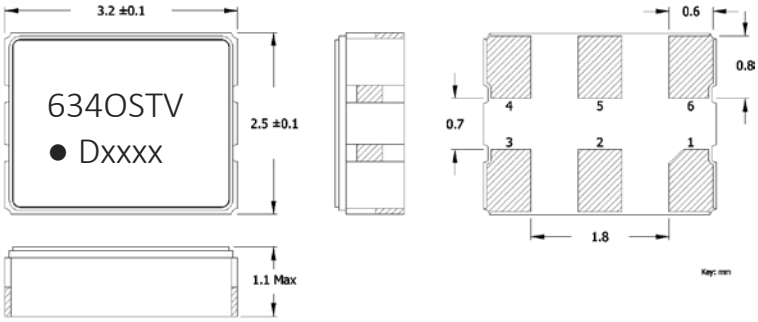
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 100.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-69.70	
		@ 100Hz	-92.90	
		@ 1kHz	-115.90	
	-	@ 10kHz	-126.80	dBc/Hz
		@ 100kHz	-129.50	
		@ 1MHz	-143.50	
		@ 10MHz	-154.90	
		@ 40MHz	-155.30	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	714.35	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 156.25MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-88.60	
		@ 100Hz	-97.80	
		@ 1kHz	-111.40	
	-	@ 10kHz	-121.00	dBc/Hz
		@ 100kHz	-127.00	
		@ 1MHz	-141.80	
		@ 10MHz	-151.50	
		@ 40MHz	-153.30	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	869.93	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 312.50MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-81.30	
		@ 100Hz	-91.80	
		@ 1kHz	-105.30	
	-	@ 10kHz	-115.50	dBc/Hz
		@ 100kHz	-120.80	
		@ 1MHz	-136.40	
		@ 10MHz	-153.20	
		@ 40MHz	-153.20	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	496.03	fs

Mechanical Specifications

Package Drawing

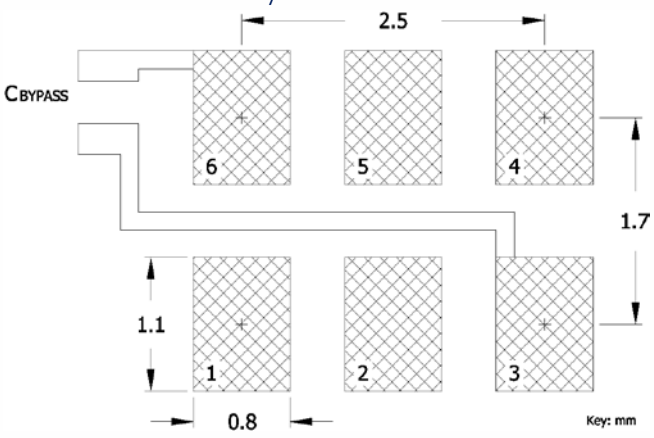


Marking Information

1. O – Output Type; P = LVPECL, L = LVDS.
2. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
3. V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
4. D – Date Code. See Table I for codes.
5. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater

[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

Pin Assignments

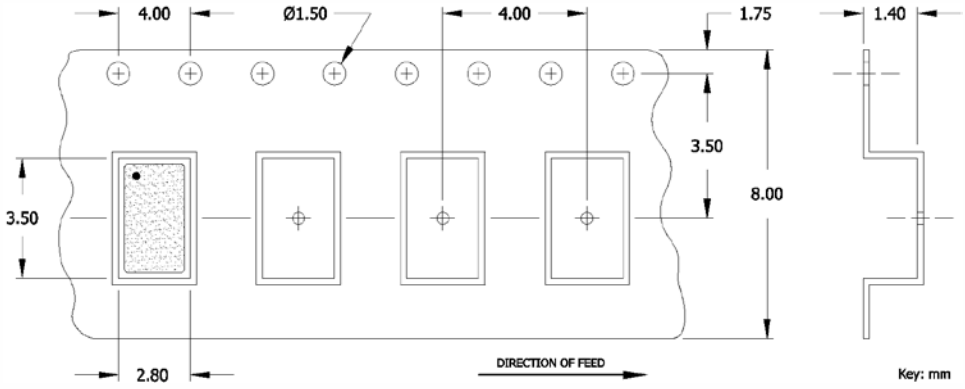
Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	$\overline{\text{Output}}$	Complimentary RF Output
6	V_{CC}	Supply Voltage

Table I - Date Code

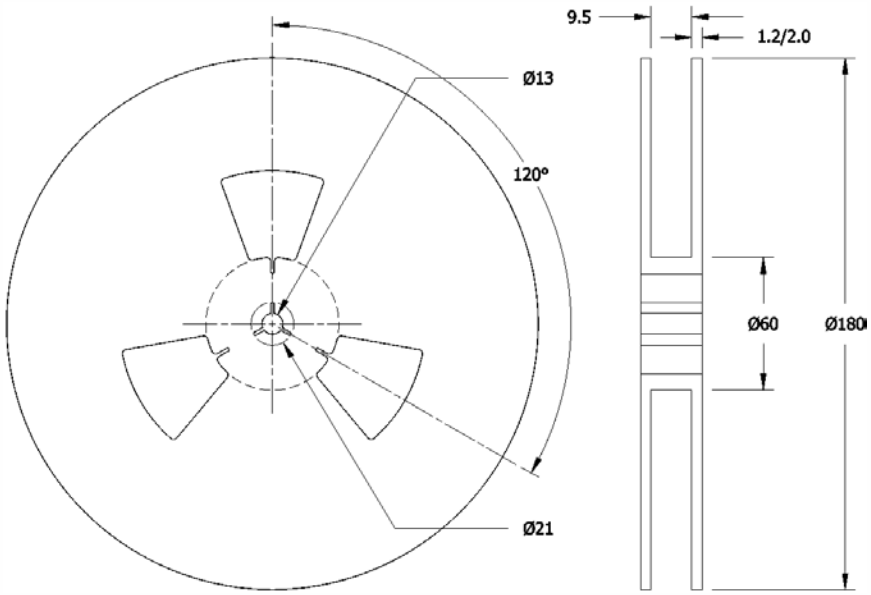
YEAR / MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces minimum and 3k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

Addendum

Additional Developed Frequencies – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
25.000000	250	148.500000	1485				
62.500000	625	153.600000	1536				
77.760000	777	155.520000	1555				
122.880000	1228	250.000000	2500				
132.000000	1320	300.000000	3000				

Frequency Codes for Cover Page Table – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
50.000000	500	156.250000	1562				
100.000000	1000	200.000000	2000				
106.250000	1062						
125.000000	1250						
150.000000	1500						