Features

- **Ultra High Performance**
  - **System Speeds to 100 MHz**
  - **Array Multipliers > 50 MHz**
  - **10ns Flexible SRAM**
  - **Internal 3-State Capability in each Cell**
- **FreeRAM™**
  - **Flexible, Single/Dual Port, Sync/Async 10 ns SRAM**
  - **2,048 - 18,432 Bits of Distributed SRAM Independent of Logic Cells**
- **84 - 384 PCI Compliant I/Os**
  - **3V/5V Capability**
  - **Programmable Output Drive**
  - **Fast, Flexible Array Access Facilitates Pin-Locking**
  - **Pin Compatible with XC4000, XC5200 FPGAs**
- **8 Global Clocks**
  - **Fast, Low Skew Clock Distribution**
  - **Programmable Rising/Falling Edge Transitions**
  - **Distributed Clock Shut-Down Capability for Low Power Management**
  - **Global Reset/Asynchronous Reset Options**
  - **4 Additional Dedicated PCI Clocks**
- **Cache Logic® Dynamic Full/Partial Reconfigurability In-System**
  - **Unlimited Reprogrammability via Serial or Parallel Modes**
  - **Enables Adaptive Designs**
  - **Enables Fast Vector Multiplier Updates**
  - **QuickChange™ Tools for Fast, Easy Design Changes**
- **Pin-Compatible Package Options**
  - **Plastic Leaded Chip Carriers (PLCC)**
  - **Thin, Plastic Quad Flat Packs (VQFP, TQFP, PQFP)**
  - **Ball Grid Arrays (BGA)**
  - **Pin Grid Arrays (PGAs)**
- **Industry-Standard Design Tools**
  - **Seamless Integration (Libraries, Interface, Full Back-Annotation) with Concept, Everest, Exemplar, Mentor, OrCAD, Synario, Synopsys, Verilog, Veribest, Viewlogic, Synplicity**
  - **Timing Driven Placement & Routing**
  - **Automatic/Interactive Multi-Chip Partitioning**
  - **Fast, Efficient Synthesis**
  - **Over 50 Automatic Component Generators Create 1000's of Reusable, Fully Deterministic Logic and RAM Functions**
- **Intellectual Property Cores**
  - **Fir Filters, UARTs, PCI, FFT and other System Level Functions**
- **Easy Migration to Atmel Gate Arrays for High Volume Production**

Device	AT40K05	AT40K10	AT40K20	AT40K40
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
RowsXColumns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	256	576	1,024	2,304
RAM Bits	2,048	4,608	8,192	18,432
I/O (max)	128	192	256	384

AT40K FPGAs with FreeRAM™

AT40K05
AT40K10
AT40K20
AT40K40

Rev. 0896B–01/99

Description

The AT40K is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, dual port/single port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 475-pin BGA, and support 3.3V and 5V designs.

The AT40K is designed to quickly implement high performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC, Sun and HP platform. Atmel's design tools provide seamless integration with industry standard tools from Cadence (Concept/Verilog), Everest, Exemplar, Mentor, OrCAD, Synario, Veribest, and Viewlogic.

The AT40K can be used as a Coprocessor for high speed (DSP/Processor-based) designs by implementing a variety of compute-intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40K FPGA offers a patented distributed 10ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual port or single port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array & Vector Multipliers

The AT40K's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40K is the only FPGA family capable of implementing Cache Logic (Dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40K is the only FPGA family capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patent-pending AT40K Series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the initial family, and 256 to 2,304 registers. Pin locations are consistent throughout the AT40K Series for easy design migration in the same package footprint. AT40K Series FPGAs utilize a reliable 0.6 micron single-poly, triple-metal CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based Integrated Development System is used to create AT40K Series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous from one edge to the other, except for bus repeaters spaced every four cells (Figure 2). At the intersection of each repeater row and column is a 32 x 4 RAM block accessible by adjacent buses. The Ram can be configured as either a single-ported or dual-ported RAM, with either synchronous or asynchronous operation.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20)

▫ = I/O Pad

○ = AT40K Cell

--- = Repeater Row

¦ = Repeater Column

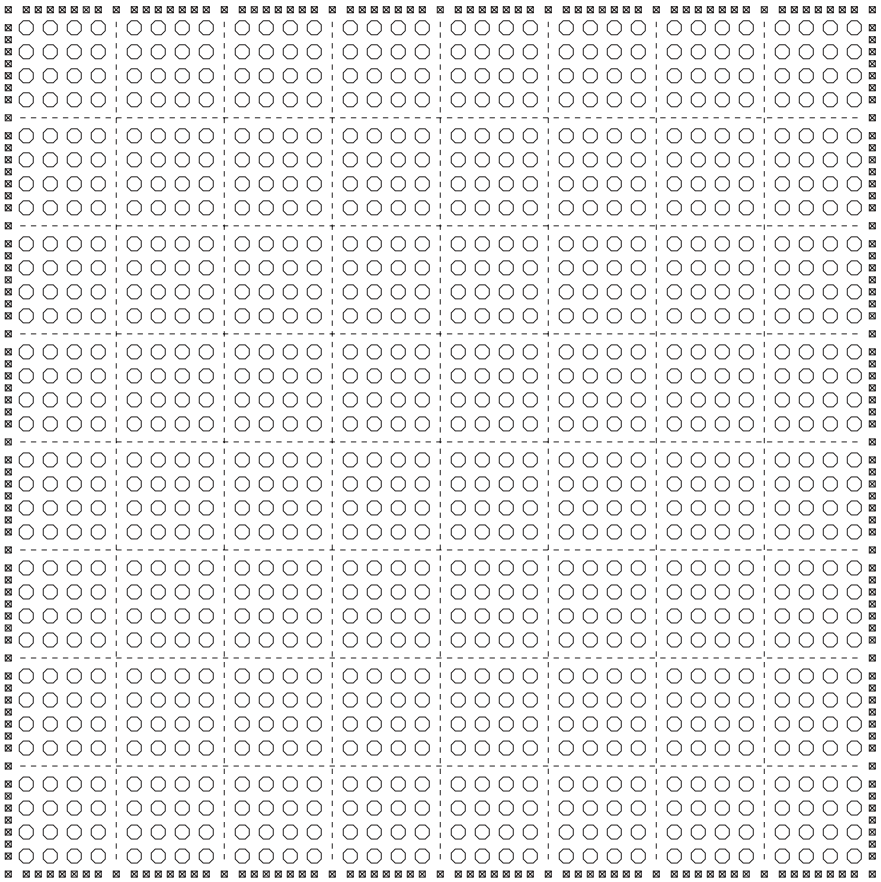
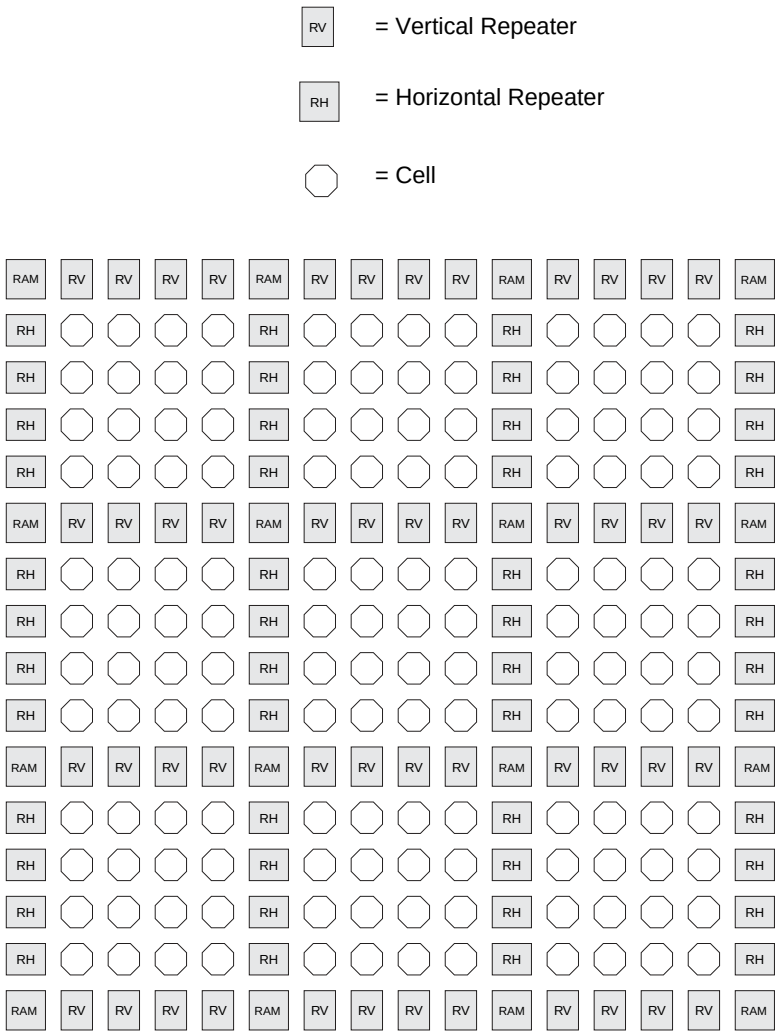


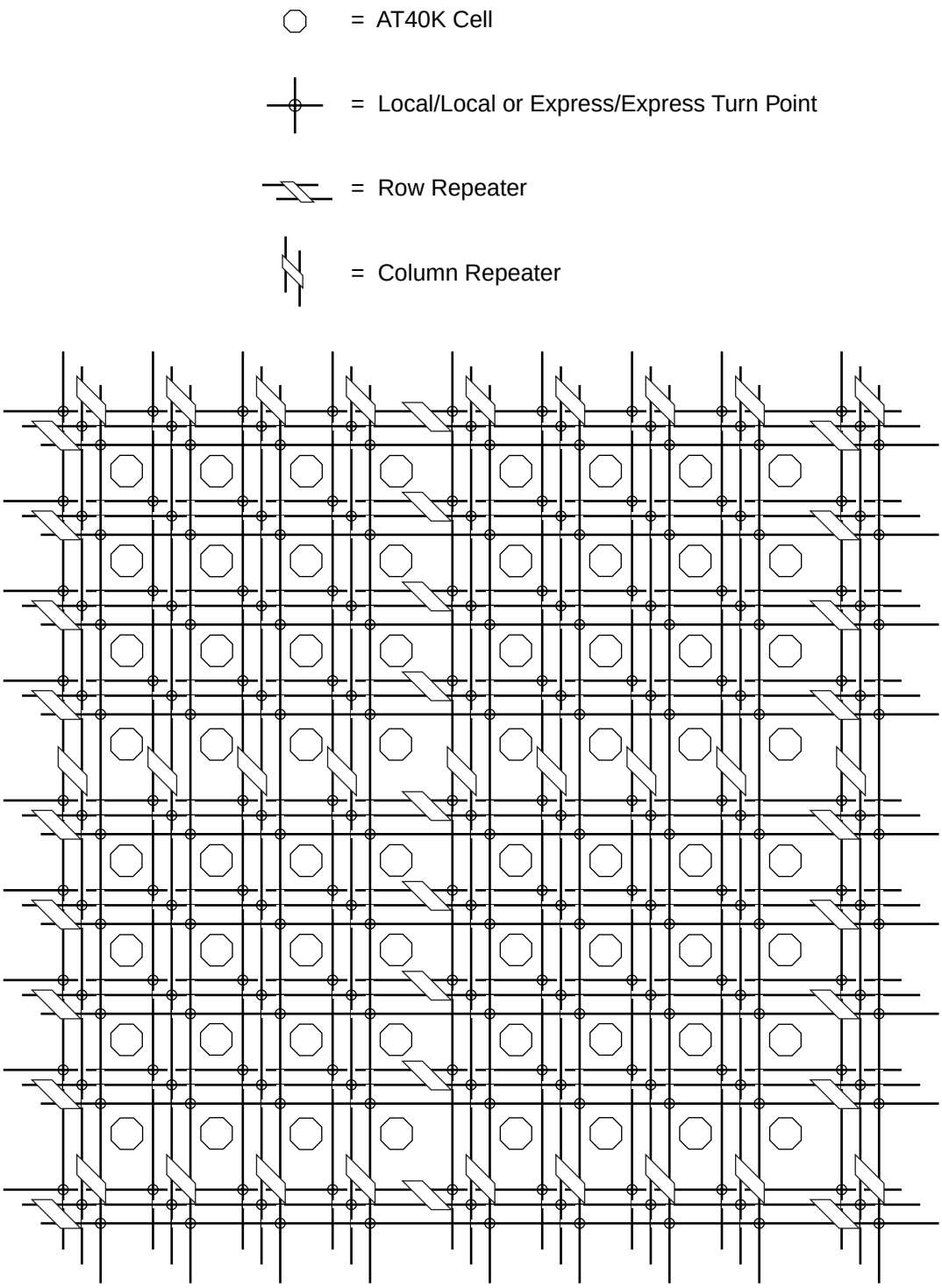
Figure 2. Floorplan (representative portion)



The Busing Network

Figure 3 depicts one of five identical busing planes. Each plane has 3 bus resources: a local-bus resource (the middle bus) and 2 express-bus resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip three state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface (see following page). Express/Express turns are implemented through separate pass gates distributed throughout the array.

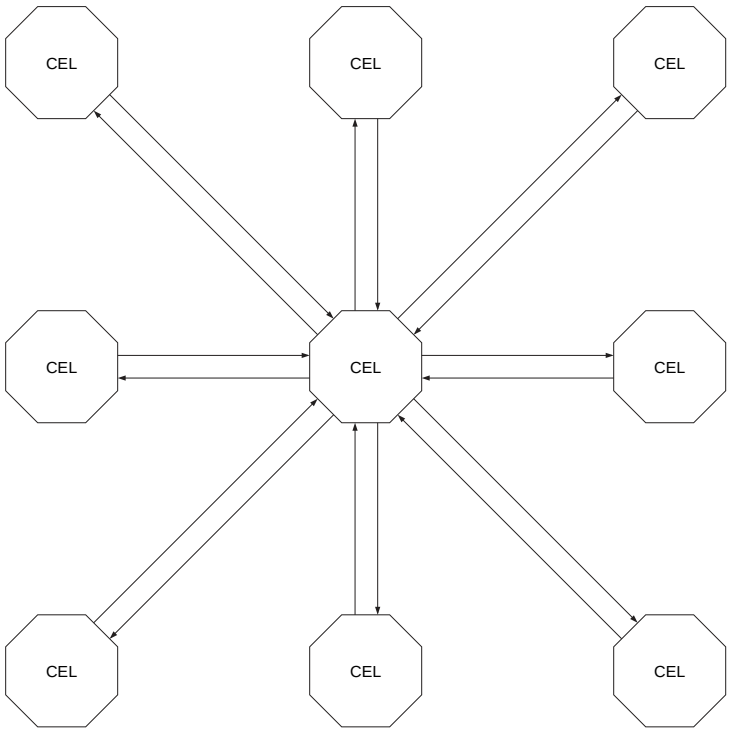
Figure 3. Busing Plane (one of five)



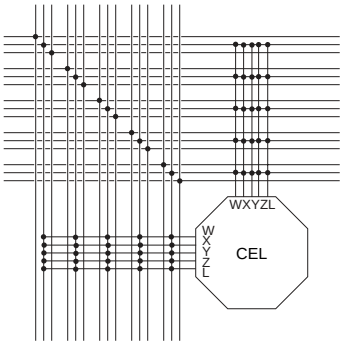
Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane).

Figure 4. Cell Connections



(a) Cell to Cell Connections

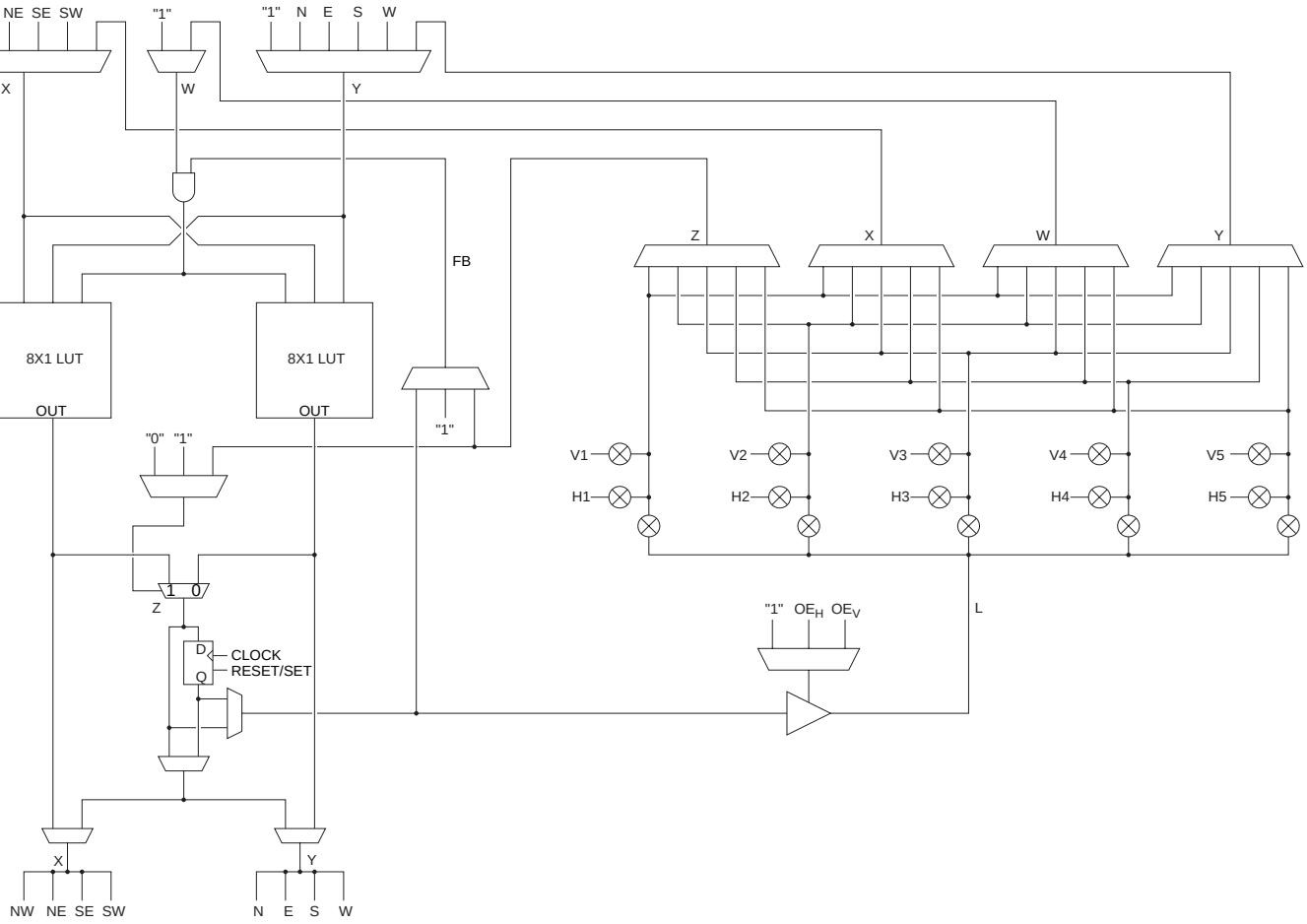


(b) Cell to Bus Connections

The Cell

Figure 5 depicts the AT40K cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. Vn is connected to the vertical local bus in plane n. Hn is connected to the horizontal local bus in plane n. A local/local turn in plane n is achieved by turning on the two pass gates connected to Vn and Hn. Up to five simultaneous local/local turns are possible.

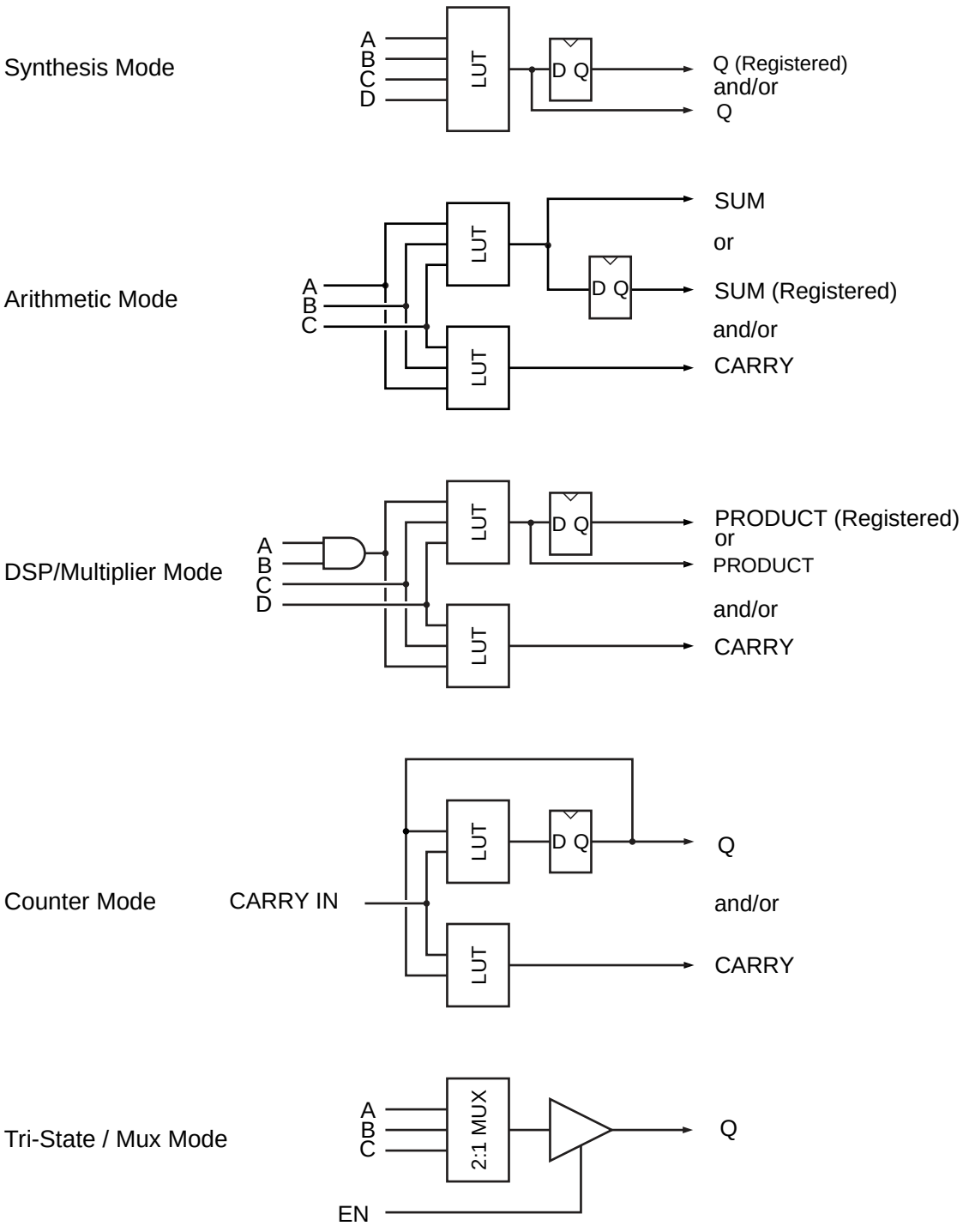
Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

The core cell can be configured in several “modes”. The core cell flexibility makes the AT40K architecture well suited to most digital design application areas (see Figure 6).

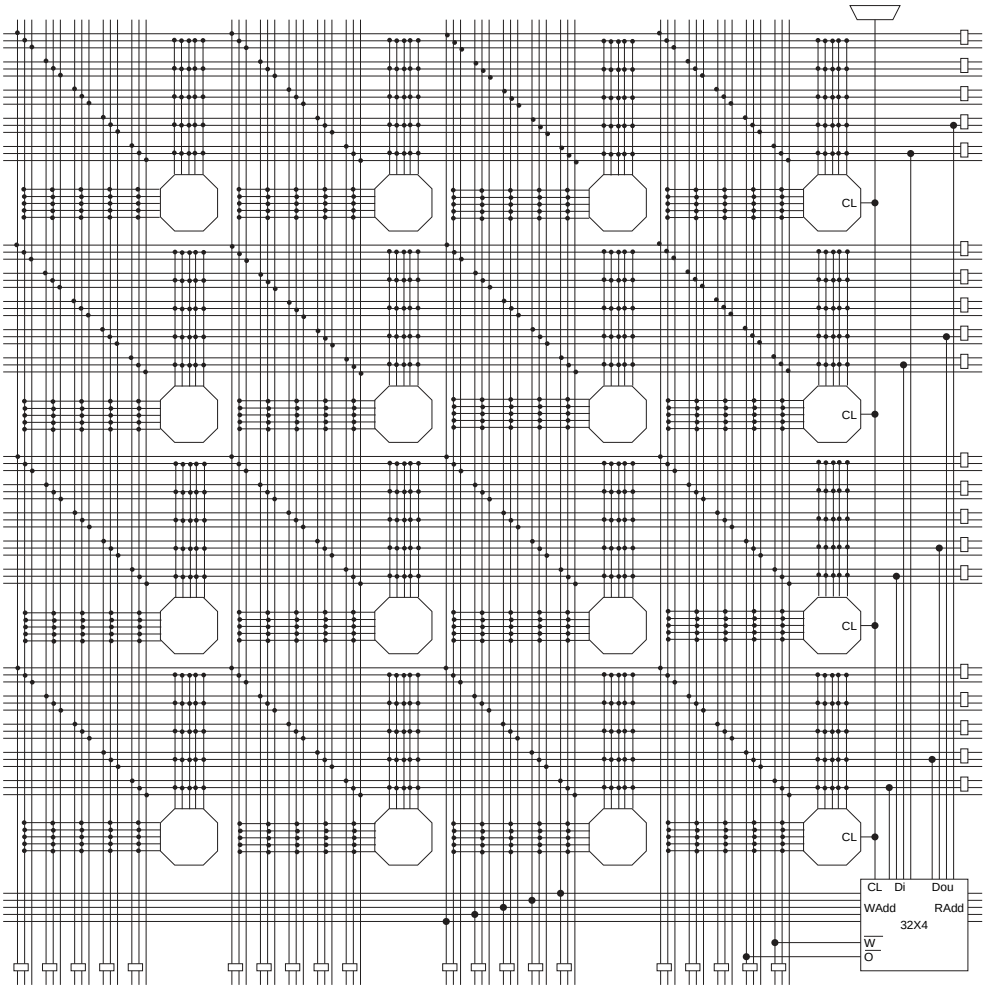
Figure 6. Some Single Cell Modes



RAM

32 x 4 Dual-Ported RAM blocks are dispersed throughout the array as shown in Figure 7. A four-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A four-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A five-bit Input-Address Bus connects to five vertical express buses in same column. A five-bit Output-Address Bus connects to five vertical express buses in same column. WAddr (Write Address) and RAddr (Read Address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, RAddr is on the left and WAddr is on the right. For the right-most RAM blocks, WAddr is on the left and RAddr is tied off. For single-ported RAM, WAddr is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. /WE & /OE connect to the vertical express buses in the same column. WAddr, RAddr, /WE and /OE connect to express buses that are full length at array edge.

Figure 7. RAM Connections (One Ram Block)



Reading and writing the 32 x 4 Dual-Port RAM are independent of each other. Reading the 32 x 4 Dual-Port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. Each bit in the 32 x 4 Dual-Port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a Bit = 7 Nibble is (Write) addressed and LOAD is Logic 1 and $\overline{WE}$ is logic 0, DATA flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{WE}$ is logic 1, DATA is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK or they both select “1”. CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM Clear Byte during configuration clears the RAM (see Bit Map Spec).

Figure 8. RAM Logic

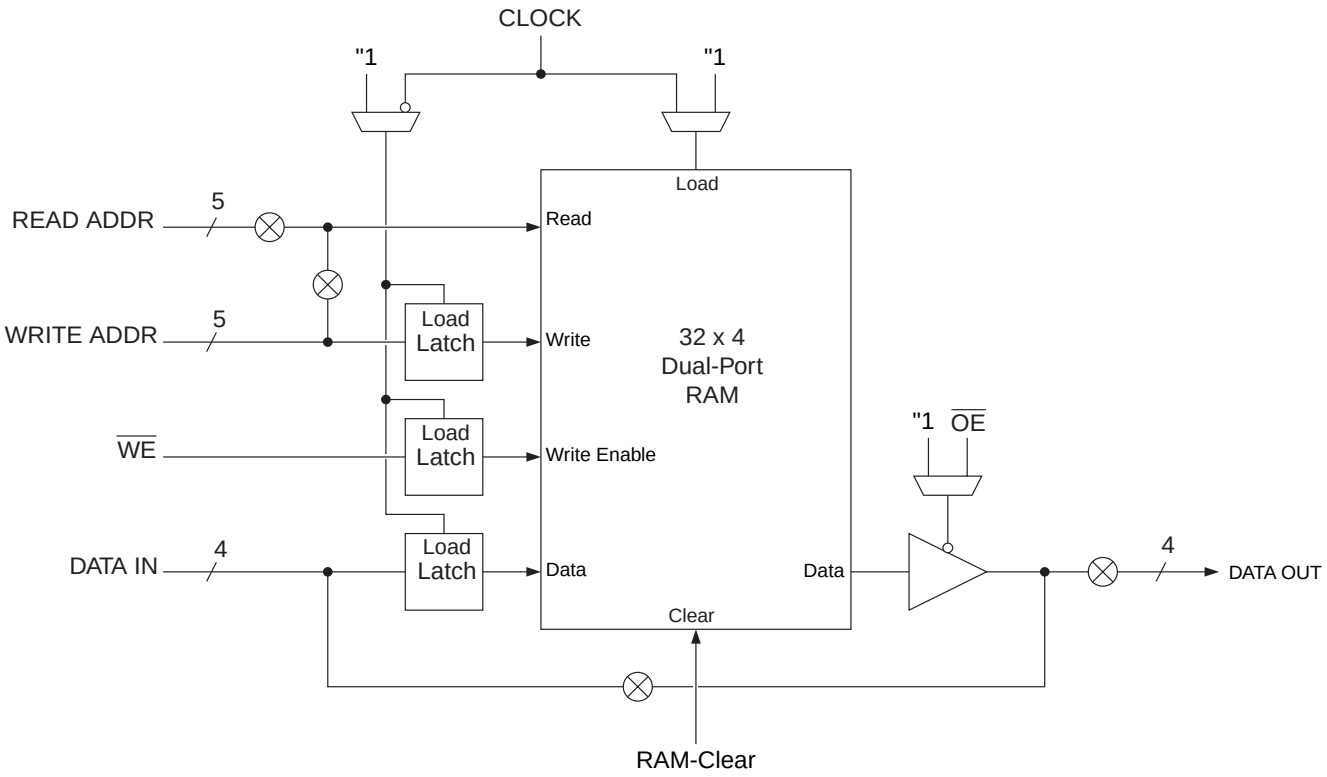
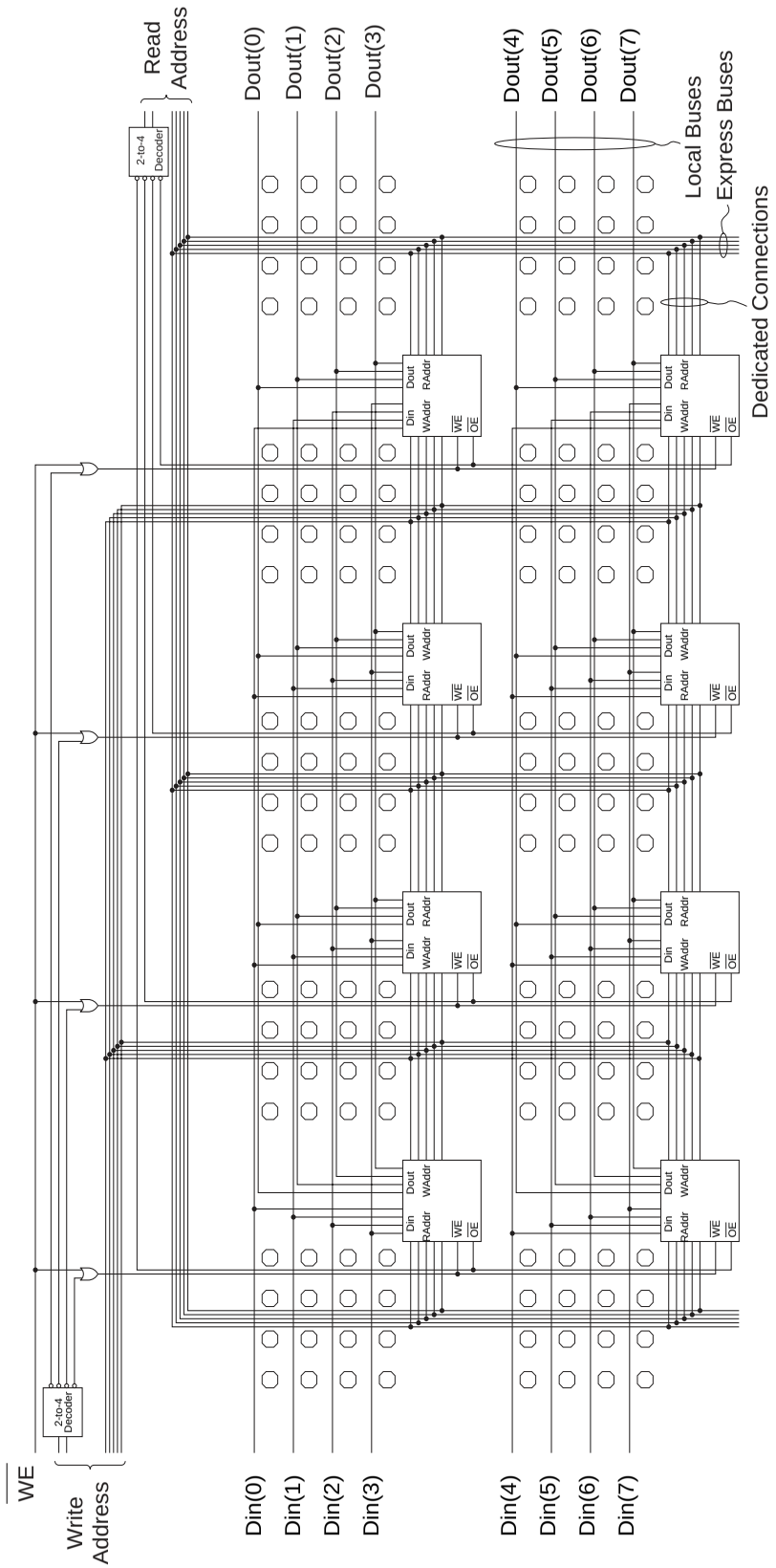


Figure 9. RAM Example: 128 x 8 Dual-Ported RAM (asynchronous)



Clocking and Set/Reset

Each of 8 dedicated Global Clock buses is connected to a dual-use Global Clock pad (GCK1 - GCK8). An internal signal can be placed on a Global Clock bus by routing that signal to a Global Clock pad. Each column of the array has a Column Clock selected from one of the 8 Global Clock buses. The extreme-left Column Clock mux has two additional inputs from dual-use pins FCK1 & FCK2 to provide fast clocking to left-side I/O. The extreme-right Column Clock mux has two additional inputs from dual-use pins FCK3 & FCK4 to provide fast clocking to right-side I/O. Each sector column of 4 cells can be clocked from a (Plane 4) express bus or from the Column Clock. Clocking to the 4 cells can be disabled. The Plane 4 express bus used for clocking is half length at the array edge. The clock provided to each sector column of 4 cells can be either inverted or not inverted. The register in each cell is triggered on a rising clock edge. On power up, constant “0” is provided to each registers clock pins.

A dedicated Global Set/Reset bus can be driven by any USER I/O pad, except those used for clocking, Global or Fast. An internal signal can be placed on the Global Set/Reset bus by routing that signal to the pad programmed as the Global Set/Reset input. Global Set/Reset is distributed to each column of the array. Each sector column of 4 cells can be Set/Reset by a (Plane 5) express bus or by the Global Set/Reset. The Plane 5 express bus used for Set/Reset is half length at array edge. The Set/Reset provided to each sector column of 4 cells can be either inverted or not inverted. The function of the Set/Reset input of a register (either Set or Reset) is determined by a configuration bit in each cell. The Set/Reset input of a register is Active Low (logic 0). Setting or resetting of a register is asynchronous. On power up, a logic 1 (a high) is provided by each register, i.e., all registers are set at power up.

Figure 10. Clocking (for one column of cells)

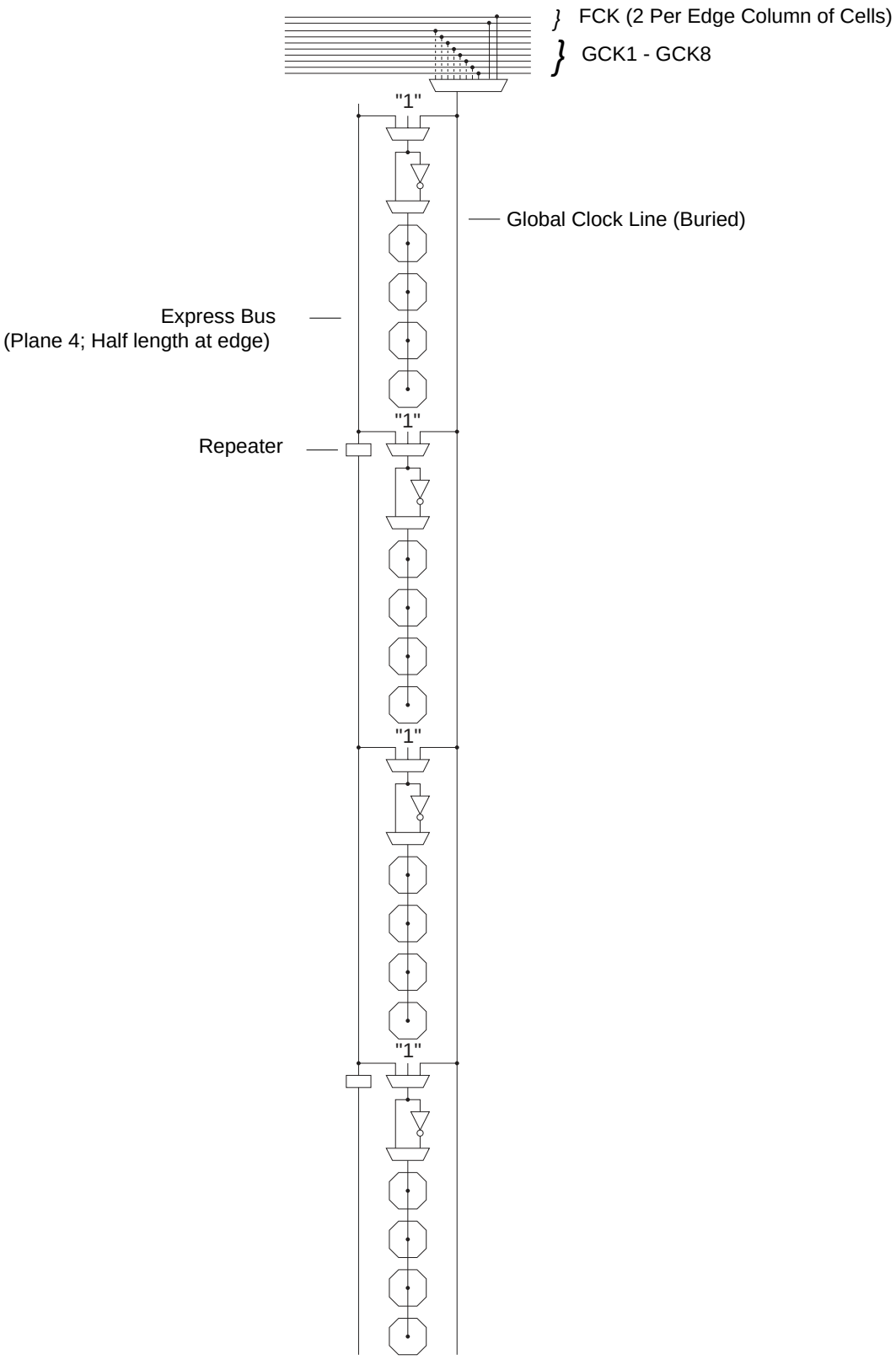
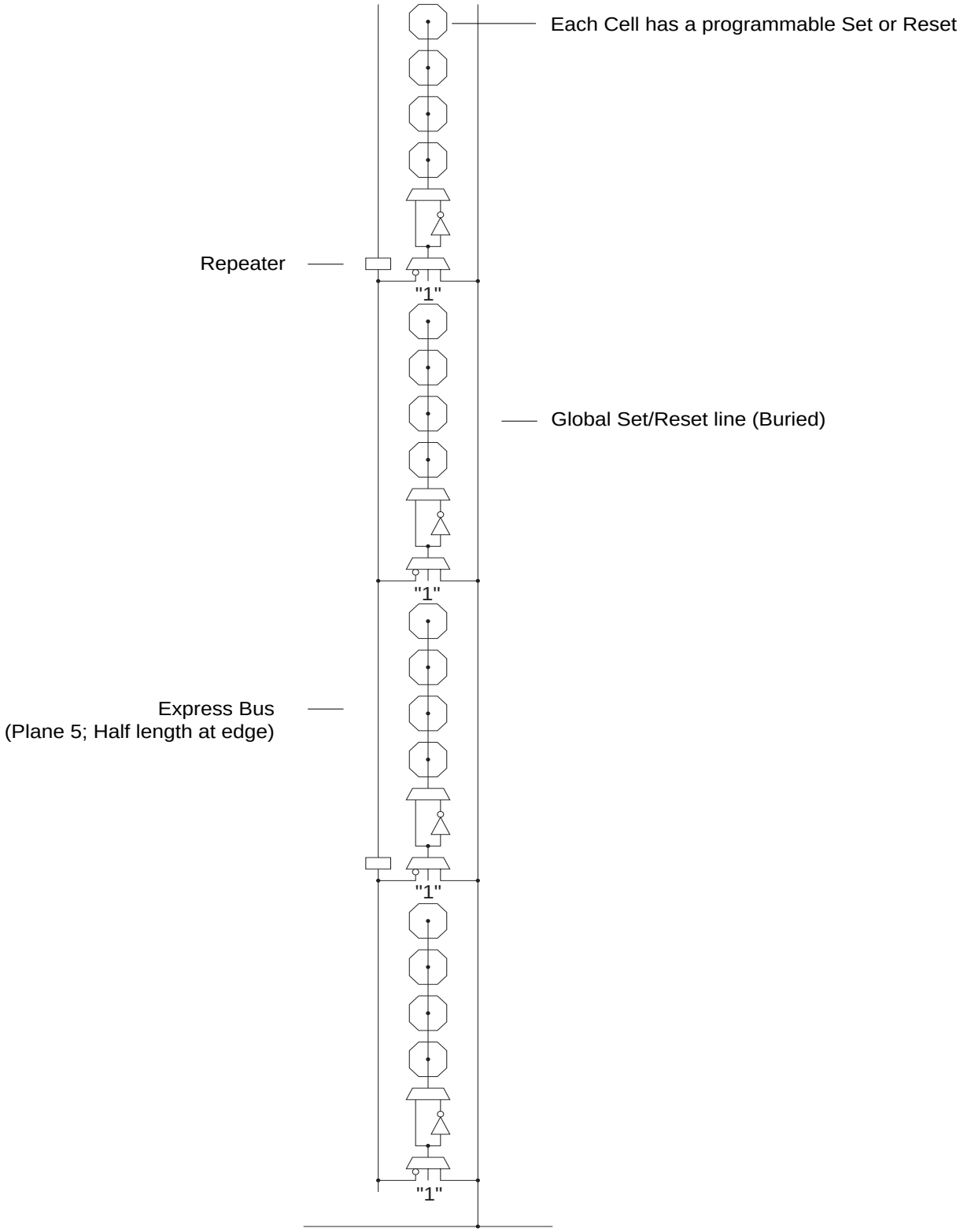
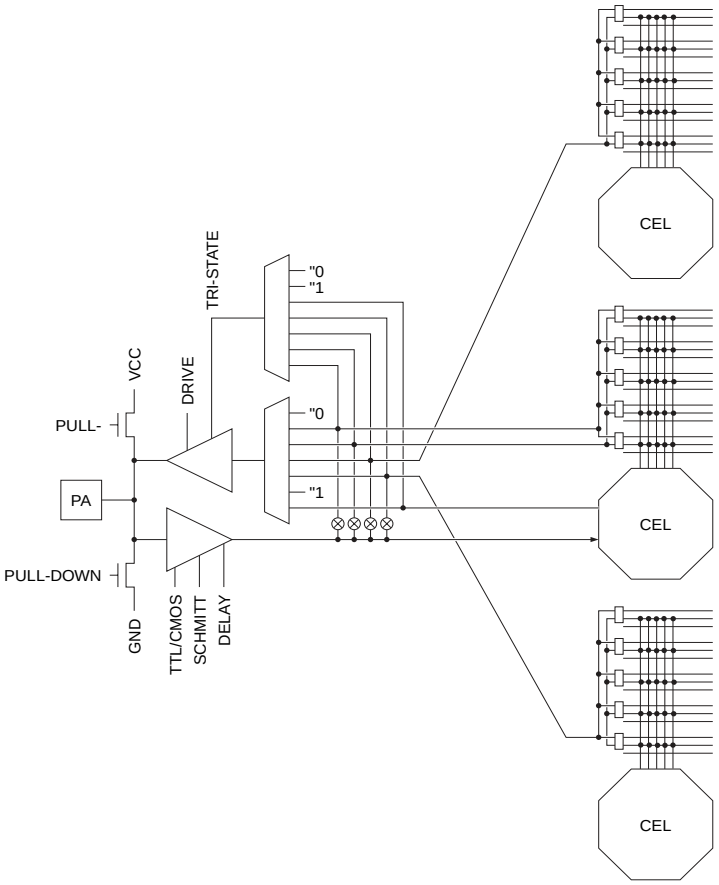


Figure 11. Set/Reset (for one column of cells)

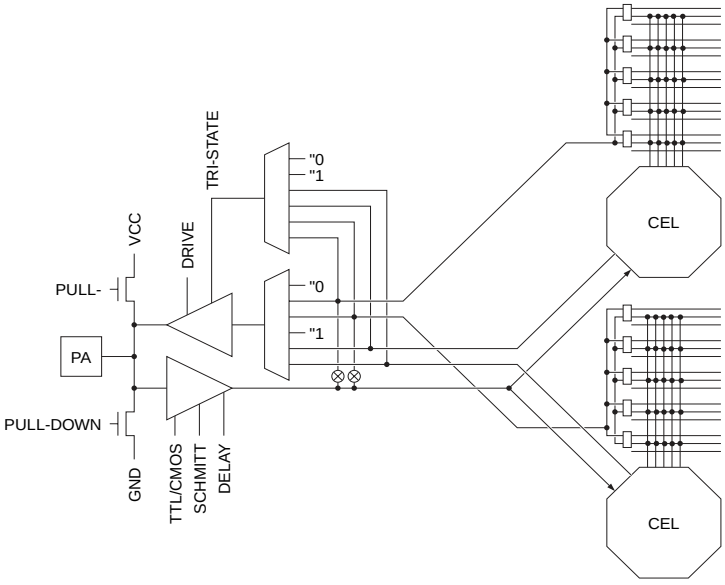


Any User I/O can drive Global Set/Reset line

Figure 12. West I/O (Mirrored for East I /O)

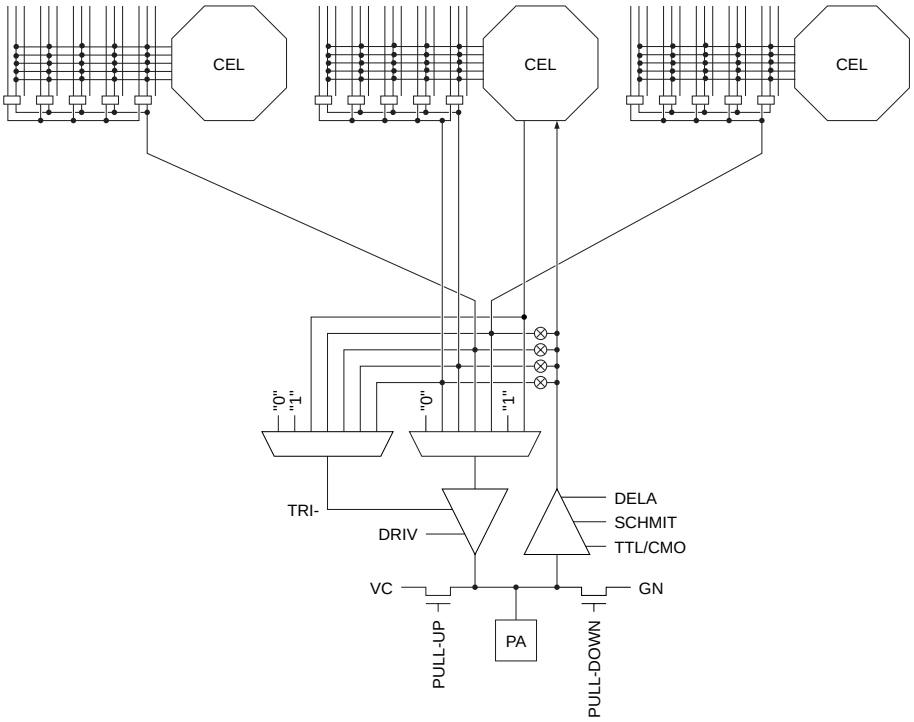


(a) Primary

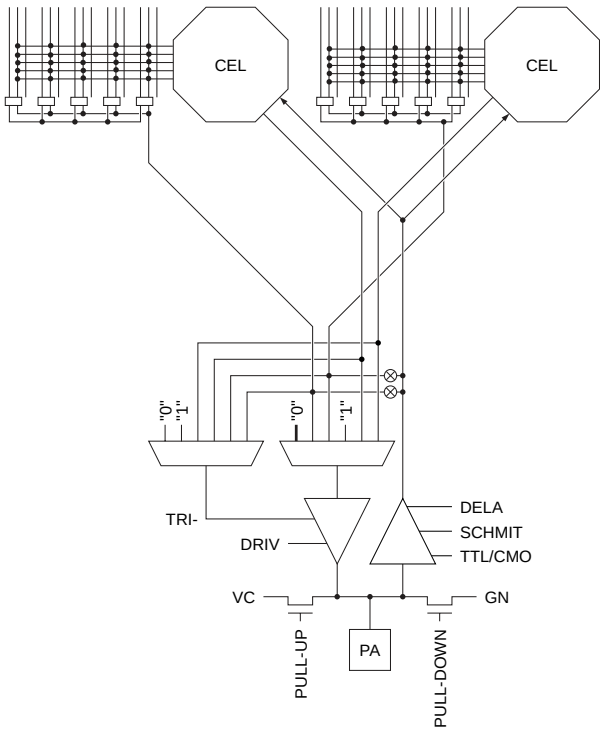


(a) Secondary

Figure 13. South I/O (Mirrored for North I/O)

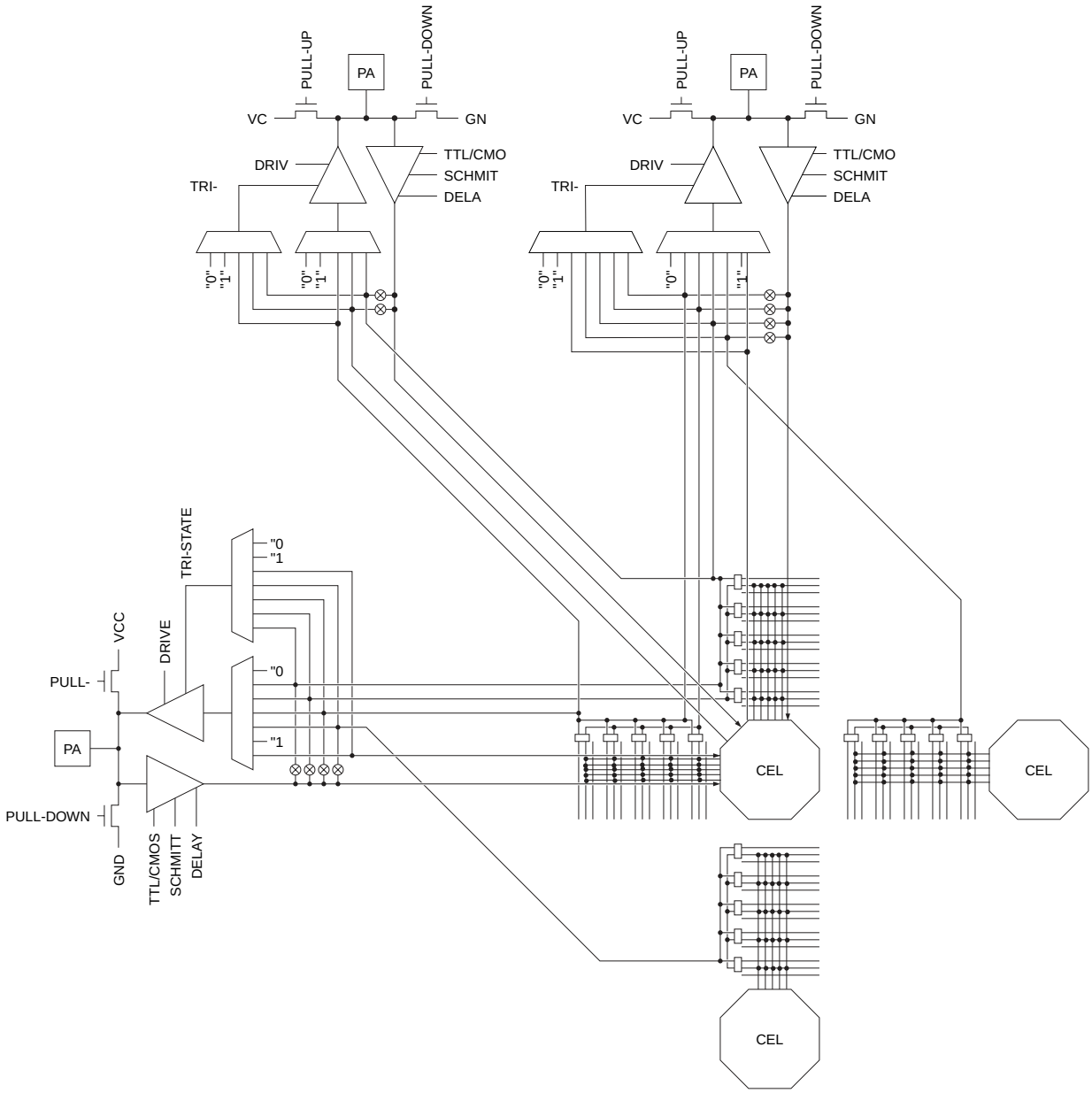


(a) Primary



(a) Secondary

Figure 14. North/West Corner, (similar for NE/SE/SW corners)



Some of the bus resource on ATK40K is used as a dual-function resource. Table 1 shows which buses are used in a dual-function mode and which bus plane is used. The ATK40K software tools are designed to accommodate dual-function buses in an efficient manner.

Table 1. Dual-Function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1-5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	
RAM Data Out	Local	2	Horizontal	
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

Absolute Maximum Ratings - 5V Commercial/Industrial*

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage	With respect to GND	-0.5	7.0	V
V_I	DC Input Voltage(1)	With respect ot GND	-0.5	7.0	V
V_O	DC Output Voltaage	With respect ot GND	-0.5	7.0	V
T_{STG}	Storage Temperature		-65°C	+150°C	
T_J	Junction Temperature			+150°C	
T_L	Lead Temperature (Soldering, 10 sec.)			+250°C	
ESD		R_{ZAP} = 1.5K, C_{ZAP} = 100 pF		2000	V

Note: 1. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range - 5V Operation

		AT40K05-2 AT40K10-2 AT40K20-2 AT40K40-2 Commercial	**AT40K05-2 AT40K10-2 AT40K20-2 AT40K40-2 Industrial**	**AT40K05-2 AT40K10-2 AT40K20-2 AT40K40-2 Military**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}	2.0V - V_{CC}	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics - 5V Operation - Commercial/Industrial/Military

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-Level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-Level Output Voltage	I_{OH} = 6mA V_{CC} = V_{CC} min	4.0			V
		I_{OH} = 14mA V_{CC} = V_{CC} min	4.0			V
		I_{OH} = 20mA Comm. = 4.75V Ind./Military = 4.5V	4.0			V
V_{OL}	Low-Level Output Voltage	I_{OL} = -6mA Comm. = 4.75V Ind./Military = 4.5V			0.4	V
		I_{OL} = -14mA Comm. = 4.75V Ind./Military = 4.5V			0.4	V
		I_{OL} = -20mA Comm. = 4.75V Ind./Military = 4.5V			0.4	V
I_{IH}	High-Level Input Current	V_{IN} = V_{CC} max			10	µA
		With pulldown, V_{IN} = V_{CC}	125	250	500	µA
I_{IL}	Low-Level Input Current	V_{IN} = V_{SS}	-10			µA
		With pullup, V_{IN} = V_{SS}	-500	-250	-125	µA
I_{OZH}	High-Level Tristate Output leakage current	Without pulldown, V_{IN} = V_{CC}			10	µA
		With pulldown, V_{IN} = V_{CC}	125	250	500	µA
I_{OZL}	Low-Level Tristate Output leakage current	Without pullup, V_{IN} = V_{SS} max	-10			µA
		With pullup, V_{IN} = V_{SS} max	-500	-250	-125	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1	mA
C_{IN}	Input Capacitance	All pins			10	pF

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Core					
2 input gate	t_{PD}(max)	x/y -> x/y	1.8	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/z -> x/y	2.1	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/w -> x/y	2.2	ns	1 unit load
4 input gate	t_{PD}(max)	x/y/w/z -> x/y	2.2	ns	1 unit load
fast carry	t_{PD}(max)	y -> y	1.4	ns	1 unit load
fast carry	t_{PD}(max)	x -> y	1.7	ns	1 unit load
fast carry	t_{PD}(max)	y -> x	1.8	ns	1 unit load
fast carry	t_{PD}(max)	x -> x	1.5	ns	1 unit load
fast carry	t_{PD}(max)	w -> y	2.2	ns	1 unit load
fast carry	t_{PD}(max)	w -> x	2.3	ns	1 unit load
fast carry	t_{PD}(max)	z -> y	2.3	ns	1 unit load
fast carry	t_{PD}(max)	z -> x	1.7	ns	1 unit load
DFF	t_{PD}(max)	q -> x/y	1.8	ns	1 unit load
DFF	t_{setup}(min)	x/y -> clk		ns	
DFF	t_{hold}(min)	x/y -> clk		ns	
DFF	t_{PD}(max)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD}(max)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD}(max)	q -> w	1.8	ns	
incremental --> L	t_{PD}(max)	x/y -> L	1.5	ns	1 unit load
Local output enable	t_{PZX}(max)	oe -> L	1.4	ns	1 unit load
Local output enable	t_{PXZ}(max)	oe -> L	1.8	ns	

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_C.
All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
Repeaters					
Repeater	t_{PD}(max)	L->E	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->E	1.3	ns	1 unit load
Repeater	t_{PD}(max)	L->L	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->L	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->IO	0.8	ns	1 unit load
Repeater	t_{PD}(max)	L->IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}.
All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
IO					
Input	t_{PD}(max)	pad -> x/y	1.2	ns	no extra delay
Input	t_{PD}(max)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD}(max)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD}(max)	pad -> x/y	10.8	ns	3 extra delays
Output, slow	t_{PD}(max)	x/y/E/L -> pad	5.9	ns	50pf load
Output, medium	t_{PD}(max)	x/y/E/L -> pad	4.8	ns	50pf load
Output, fast	t_{PD}(max)	x/y/E/L -> pad	3.9	ns	50pf load
Output, slow	t_{PZX}(max)	oe -> pad	6.2	ns	50pf load
Output, low	t_{PXZ}(max)	oe -> pad	1.3	ns	50pf load
Output, medium	t_{PZX}(max)	oe -> pad	4.8	ns	50pf load
Output, medium	t_{PXZ}(max)	oe -> pad	1.9	ns	50pf load
Output, fast	t_{PZX}(max)	oe -> pad	3.7	ns	50pf load
Output, fast	t_{PXZ}(max)	oe -> pad	1.6	ns	50pf load

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-2	Units	Notes
Global Clocks and Set/Reset						
GCLK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	1.1	ns	rising edge clock
		pad -> clock	AT40K10	1.2	ns	
		pad -> clock	AT40K20	1.2	ns	
		pad -> clock	AT40K40	1.4	ns	
FCLK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	0.7	ns	rising edge clock
		pad -> clock	AT40K10	0.8	ns	
		pad -> clock	AT40K20	0.8	ns	
		pad -> clock	AT40K40	0.8	ns	
Clock column driver	t_{PD}(max)	clock -> colclk	AT40K05	0.8	ns	rising edge clock
		clock -> colclk	AT40K10	0.9	ns	
		clock -> colclk	AT40K20	1.0	ns	
		clock -> colclk	AT40K40	1.1	ns	
Clock sector driver	t_{PD}(max)	colclk -> secclk	AT40K05	0.5	ns	rising edge clock
		colclk -> secclk	AT40K10	0.5	ns	
		colclk -> secclk	AT40K20	0.5	ns	
		colclk -> secclk	AT40K40	0.5	ns	
GSRN Input buffer	t_{PD}(max)	pad -> GSRN	AT40K05	3.0	ns	
		colclk -> secclk	AT40K10	3.7	ns	
		colclk -> secclk	AT40K20	4.3	ns	
		colclk -> secclk	AT40K40	5.6	ns	
Global clock to output	t_{PD}(max)	clock pad -> out	AT40K05	8.3	ns	rising edge clock
		clock pad -> out	AT40K10	8.4	ns	fully loaded clock tree
		clock pad -> out	AT40K20	8.6	ns	rising edge DFF
		clock pad -> out	AT40K40	8.8	ns	20mA output buffer
						50 pf pin load
Output, fast	t_{PD}(max)	clock pad -> out	AT40K05	7.9	ns	rising edge clock
		clock pad -> out	AT40K10	8.0	ns	fully loaded clock tree
		clock pad -> out	AT40K20	8.1	ns	rising edge DFF
		clock pad -> out	AT40K40	8.3	ns	20mA output buffer
						50 pf pin load

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Async RAM					
Write	t_{WECYC}(min)	cycle time	8.0	ns	
Write	t_{WEL}(min)	we	3.0	ns	pulse width low
Write	t_{WEH}(min)	we	3.0	ns	pulse width high
Write	t_{setup}(min)	wr addr setup-> we	2.0	ns	
Write	t_{hold}(min)	wr addr hold -> we	0.0	ns	
Write	t_{setup}(min)	din setup -> we	2.0	ns	
Write	t_{hold}(min)	din hold -> we	0.0	ns	
Write	t_{hold}(min)	oe hold -> we	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	4.6	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	3.1	ns	
Read	t_{PZX}(max)	oe -> dout	1.6	ns	
Read	t_{PXZ}(max)	oe -> dout	2.0	ns	
Sync RAM					
Write	t_{CYC}(min)	cycle time	8.0	ns	
Write	t_{CLKL}(min)	clk	3.0	ns	pulse width low
Write	t_{CLKH}(min)	clk	3.0	ns	pulse width high
Write	t_{setup}(min)	we setup-> clk	2.0	ns	
Write	t_{hold}(min)	we hold -> clk	0.0	ns	
Write	t_{setup}(min)	wr addr setup-> clk	2.0	ns	
Write	t_{hold}(min)	wr addr hold -> clk	0.0	ns	
Write	t_{setup}(min)	wr data setup-> clk	2.0	ns	
Write	t_{hold}(min)	wr data hold -> clk	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	4.6	ns	rd addr = wr addr
Write/Read	t_{PD}(max)	clk -> dout	3.5	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	3.1	ns	
Read	t_{PZX}(max)	oe -> dout	1.6	ns	
Read	t_{PXZ}(max)	oe -> dout	2.0	ns	

Absolute Maximum Ratings - 3.3V Commercial/Industrial*

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage	With respect to GND	-0.5	7.0	V
V_I	DC Input Voltage(1)	With respect ot GND	-0.5	7.0	V
V_O	DC Output Voltaage	With respect ot GND	-0.5	7.0	V
T_{STG}	Storage Temperature		-65°C	+150°C	
T_J	Junction Temperature			+150°C	
T_L	Lead Temperature (Soldering, 10 sec.)			+250°C	
ESD		R_{ZAP} = 1.5K, C_{ZAP} = 100 pF		2000	V

Note: 1. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range - 3.3V Operation

		AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Commercial	**AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Industrial**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics - 3.3V Operation - Commercial/Industrial

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-Level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-Level Output Voltage	I_{OH} = 4 mA V_{CC} = V_{CC} min	2.1			V
		I_{OH} = 12 mA V_{CC} = 3.0V	2.1			V
		I_{OH} = 16 mA V_{CC} = 3.0V	2.1			V
V_{OL}	Low-Level Output Voltage	I_{OL} = -4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-Level Input Current	V_{IN} = V_{CC} max			10	µA
		With pulldown, V_{IN} = V_{CC}	75	150	300	µA
I_{IL}	Low-Level Input Current	V_{IN} = V_{SS}	-10			µA
		With pullup, V_{IN} = V_{SS}	-300	-150	-75	µA
I_{OZH}	High-Level Tristate Output leakage current	Without pulldown, V_{IN} = V_{CC} max			10	µA
		With pulldown, V_{IN} = V_{CC} max	75	150	300	µA
I_{OZL}	Low-Level Tristate Output leakage current	Without pullup, V_{IN} = V_{SS}	-10			µA
		With pullup, V_{IN} = V_{SS}	-300	-150	-75	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1	mA
C_{IN}	Input Capacitance	All pins			10	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-3	Units	Notes
Core					
2 input gate	t_{PD}(max)	x/y -> x/y	2.9	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/z -> x/y	2.8	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/w -> x/y	3.4	ns	1 unit load
4 input gate	t_{PD}(max)	x/y/w/z -> x/y	3.4	ns	1 unit load
fast carry	t_{PD}(max)	y -> y	2.3	ns	1 unit load
fast carry	t_{PD}(max)	x -> y	2.9	ns	1 unit load
fast carry	t_{PD}(max)	y -> x	3.0	ns	1 unit load
fast carry	t_{PD}(max)	x -> x	2.3	ns	1 unit load
fast carry	t_{PD}(max)	w -> y	3.4	ns	1 unit load
fast carry	t_{PD}(max)	w -> x	3.4	ns	1 unit load
fast carry	t_{PD}(max)	z -> y	3.4	ns	1 unit load
fast carry	t_{PD}(max)	z -> x	2.4	ns	1 unit load
DFF	t_{PD}(max)	q -> x/y	2.8	ns	1 unit load
DFF	t_{setup}(min)	x/y -> clk		ns	
DFF	t_{hold}(min)	x/y -> clk		ns	
DFF	t_{PD}(max)	R -> x/y	3.2	ns	1 unit load
DFF	t_{PD}(max)	S -> x/y	3.0	ns	1 unit load
DFF	t_{PD}(max)	q -> w	2.7	ns	
incremental --> L	t_{PD}(max)	x/y -> L	2.4	ns	1 unit load
Local output enable	t_{PZX}(max)	oe -> L	2.8	ns	1 unit load
Local output enable	t_{PXZ}(max)	oe -> L	2.4	ns	

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
Repeaters					
Repeater	t_{PD}(max)	L -> E	2.2	ns	1 unit load
Repeater	t_{PD}(max)	E -> E	2.2	ns	1 unit load
Repeater	t_{PD}(max)	L -> L	2.2	ns	1 unit load
Repeater	t_{PD}(max)	E -> L	2.2	ns	1 unit load
Repeater	t_{PD}(max)	E -> IO	1.4	ns	1 unit load
Repeater	t_{PD}(max)	L -> IO	1.4	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
IO					
Input	t_{PD}(max)	pad -> x/y	1.9	ns	no extra delay
Input	t_{PD}(max)	pad -> x/y	5.8	ns	1 extra delay
Input	t_{PD}(max)	pad -> x/y	11.5	ns	2 extra delays
Input	t_{PD}(max)	pad -> x/y	17.4	ns	3 extra delays
Output, slow	t_{PD}(max)	x/y/E/L -> pad	9.1	ns	50pf load
Output, medium	t_{PD}(max)	x/y/E/L -> pad	7.6	ns	50pf load
Output, fast	t_{PD}(max)	x/y/E/L -> pad	6.2	ns	50pf load
Output, slow	t_{PZX}(max)	oe -> pad	9.5	ns	50pf load
Output, slow	t_{PXZ}(max)	oe -> pad	2.1	ns	50pf load
Output, medium	t_{PZX}(max)	oe -> pad	7.4	ns	50pf load
Output, medium	t_{PXZ}(max)	oe -> pad	2.7	ns	50pf load
Output, fast	t_{PZX}(max)	oe -> pad	5.9	ns	50pf load
Output, fast	t_{PXZ}(max)	oe -> pad	2.4	ns	50pf load

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a VIH of 1.5V at the input pad to the internal VIH of 50% of VCC. Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-3	Units	Notes
Global Clocks and Set/Reset						
GCK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	1.3	ns	rising edge clock
		pad -> clock	AT40K10	1.5	ns	
		pad -> clock	AT40K20	1.6	ns	
		pad -> clock	AT40K40	1.9	ns	
FCK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	0.7	ns	rising edge clock
		pad -> clock	AT40K10	0.8	ns	
		pad -> clock	AT40K20	0.8	ns	
		pad -> clock	AT40K40	0.9	ns	
Clock column driver	t_{PD}(max)	clock -> colclk	AT40K05	1.5	ns	rising edge clock
		clock -> colclk	AT40K10	1.8	ns	
		clock -> colclk	AT40K20	2.0	ns	
		clock -> colclk	AT40K40	2.5	ns	
Clock sector driver	t_{PD}(max)	colclk -> secclk	AT40K05	1.0	ns	rising edge clock
		colclk -> secclk	AT40K10	1.0	ns	
		colclk -> secclk	AT40K20	1.0	ns	
		colclk -> secclk	AT40K40	1.0	ns	
GSRN Input buffer	t_{PD}(max)	pad -> GSRN	AT40K05	4.5	ns	
		colclk -> secclk	AT40K10	5.4	ns	
		colclk -> secclk	AT40K20	6.3	ns	
		colclk -> secclk	AT40K40	8.2	ns	
Global clock to output	t_{PD}(max)	clock pad -> out	AT40K05	13.0	ns	rising edge clock
		clock pad -> out	AT40K10	13.4	ns	fully loaded clock tree
		clock pad -> out	AT40K20	13.8	ns	rising edge DFF
		clock pad -> out	AT40K40	14.5	ns	20mA output buffer
						50 pf pin load
Fast clock to output	t_{PD}(max)	clock pad -> out	AT40K05	12.4	ns	rising edge clock
		clock pad -> out	AT40K10	12.7	ns	fully loaded clock tree
		clock pad -> out	AT40K20	13.0	ns	rising edge DFF
		clock pad -> out	AT40K40	13.5	ns	20mA output buffer
						50 pf pin load

AC Timing Characteristics - 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-4	-3	Units	Notes
Async RAM						
Write	t_{WECYC}(min)	cycle time	14.0	12.0	ns	
Write	t_{WEL}(min)	we	6.0	5.0	ns	pulse width low
Write	t_{WEH}(min)	we	6.0	5.0	ns	pulse width high
Write	t_{setup}(min)	wr addr setup-> we	5.3	5.3	ns	
Write	t_{hold}(min)	wr addr hold -> we	0.0	0.0	ns	
Write	t_{setup}(min)	din setup -> we	6.0	5.0	ns	
Write	t_{hold}(min)	din hold -> we	0.0	0.0	ns	
Write	t_{hold}(min)	oe hold -> we	0.0	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	12.1	8.7	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	9.7	6.3	ns	
Read	t_{PZX}(max)	oe -> dout	4.2	2.9	ns	
Read	t_{PXZ}(max)	oe -> dout	3.5	3.5	ns	
Sync RAM						
Write	t_{CYC}(min)	cycle time	12.0	12.0	ns	
Write	t_{CLKL}(min)	clk	6.0	5.0	ns	pulse width low
Write	t_{CLKH}(min)	clk	6.0	5.0	ns	pulse width high
Write	t_{setup}(min)	we setup-> clk	3.2	3.2	ns	
Write	t_{hold}(min)	we hold -> clk	0.0	0.0	ns	
Write	t_{setup}(min)	wr addr setup-> clk	6.0	5.0	ns	
Write	t_{hold}(min)	wr addr hold -> clk	0.0	0.0	ns	
Write	t_{setup}(min)	wr data setup-> clk	3.0	3.9	ns	
Write	t_{hold}(min)	wr data hold -> clk	0.0	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	12.1	8.7	ns	rd addr = wr addr
Write/Read	t_{PD}(max)	clk -> dout	9.9	5.8	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	9.7	6.3	ns	
Read	t_{PZX}(max)	oe -> dout	4.01	2.9	ns	
Read	t_{PXZ}(max)	oe -> dout	3.5	3.5	ns	

Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer Software.

Part/Package Availability

	AT40K05	AT40K10	AT40K20	AT40K40
PC 84	X	X	X	
RQ100	X	X		
VQ 100	X	X	X	
TQ 144	X	X	X	X
PQ 160	X	X	X	
PQ 208	X	X	X	X
PQ 240		X	X	X
PQ 304			X	X
BG 225			X	X
BG 352			X	X
BG 432				X
PG 475				X

USER I/O Counts - (Including Dual-Function Pins)

	AT40K05	AT40K10	AT40K20	AT40K40
PC 84	62	62	62	
RQ 100	78	78		
VQ 100	78	78	78	
TQ 144	114	114	114	114
PQ 160	128	130	130	
PQ 208	128	161	161	161
PQ 240		192	193	193
PQ 304			256	256
BG 225			192	192
BG 352			256	289
BG 432				352
PG 475				384

Devices in same packages are pin-for-pin replaceable.

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
GND	GND	GND	GND	12	4	1	1	1	2	GND(1)	1	304	GND(1)	GND(1)
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	5	2	2	2	4	D4	2	303	D23	D29
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	6	3	3	3	5	B1	3	302	C25	C30
I/O3	I/O3	I/O3	I/O3				4	4	6	C2	4	301	D24	E28
I/O4	I/O4	I/O4	I/O4				5	5	7	E5	5	300	E23	E29
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	7	4	6	6	8	D3	6	299	C26	D30
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	8	5	7	7	9	C1	7	298	E24	D31
			GND											GND(1)
			I/O7											F28
			I/O8											F29
			I/O9										D25	E30
			I/O10										F23	E31
		I/O7	I/O11									297	F24	G28
		I/O8	I/O12									296	E25	G29
		VCC	VCC										VCC(1)	VCC(1)
		GND	GND										GND(1)	GND(1)
			I/O13											F30
			I/O14											F31
I/O7	I/O7	I/O9	I/O15					8	10	D2	8	295	D26	H28
I/O8	I/O8	I/O10	I/O16					9	11	G6	9	294	G24	H29
	I/O9	I/O11	I/O17						12	E4	10	293	F25	G30
	I/O10	I/O12	I/O18						13	D1	11	292	F26	H30
			GND											GND(1)
			I/O19											
			I/O20											
	I/O11	I/O13	I/O21							E3	12	291	H23	J28
	I/O12	I/O14	I/O22							E2	13	290	H24	J29
		I/O15	I/O23									289	G25	H31
		I/O16	I/O24									288	G26	J30
GND	GND	GND	GND				8	10	14	GND*	14	287	GND(1)	GND(1)
I/O9, FCK1	I/O13, FCK1	I/O17, FCK1	I/O25, FCK1				9	11	15	F5	15	286	J23	K28
I/O10	I/O14	I/O18	I/O26				10	12	16	E1	16	285	J24	K29
I/O11 (A20)	I/O15 (A20)	I/O19 (A20)	I/O27 (A20)	17	9	6	11	13	17	F4	17	284	H25	K30
I/O12 (A21)	I/O16 (A21)	I/O20 (A21)	I/O28 (A21)	18	10	7	12	14	18	F3	18	283	K23	K31
	VCC	VCC	VCC							VCC*	19	282	VCC(1)	VCC(1)
	I/O17	I/O21	I/O29							F2	20	280	K24	L29

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
	I/O18	I/O22	I/O30							F1	21	279	J25	L30
			GND											GND*
			I/O31											M30
			I/O32											M28
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O33										J26	M29
			I/O34										L23	M31
		I/O23	I/O35									278	L24	N31
		I/O24	I/O36									277	K25	N28
		GND	GND								22		GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
			I/O37											N29
			I/O38											N30
		I/O25	I/O39									276	L25	P30
		I/O26	I/O40									275	L26	P28
	I/O19	I/O27	I/O41						19	G4	23	274	M23	P29
	I/O20	I/O28	I/O42						20	G3	24	273	M24	R31
			GND											GND(1)
I/O13	I/O21	I/O29	I/O43				13	15	21	G2	25	272	M25	R30
I/O14	I/O22	I/O30	I/O44		11	8	14	16	22	G1	26	271	M26	R28
			I/O45											
			I/O46											
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	12	9	15	17	23	G5	27	270	N24	R29
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	13	10	16	18	24	H3	28	269	N25	T31
GND	GND	GND	GND	21	14	11	17	19	25	GND(1)	29	268	GND(1)	GND(1)
VCC	VCC	VCC	VCC	22	15	12	18	20	26	VCC(1)	30	267	VCC(1)	VCC(1)
I/O17	I/O25	I/O33	I/O49	23	16	13	19	21	27	H4	31	266	N26	T30
I/O18	I/O26	I/O34	I/O50	24	17	14	20	22	28	H5	32	265	P25	T29
			I/O51											
			I/O52											
I/O19	I/O27	I/O35	I/O53		18	15	21	23	29	J2	33	264	P23	U31
I/O20	I/O28	I/O36	I/O54				22	24	30	J1	34	263	P24	U30
			GND											GND(1)
	I/O29	I/O37	I/O55						31	J3	35	262	R26	U28
	I/O30	I/O38	I/O56						32	J4	36	261	R25	U29
		I/O39	I/O57									260	R24	V30
		I/O40	I/O58									259	R23	V29
			I/O59											V28
			I/O60											W31
			VCC										VCC(1)	VCC(1)
		GND	GND								37		GND(1)	GND(1)
		I/O41	I/O61									258	T26	W30
		I/O42	I/O62									257	T25	W29

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O63											W28
			I/O64											Y31
			I/O65										T24	Y30
			I/O66										U25	Y29
			GND											GND(1)
	I/O31	I/O43	I/O67							J5	38	256	T23	Y28
	I/O32	I/O44	I/O68							K1	39	255	V26	AA30
	VCC	VCC	VCC							VCC(1)	40	253	VCC(1)	VCC(1)
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
I/O21	I/O33	I/O45	I/O69	25	19	16	23	25	33	K2	41	252	U24	AA29
I/O22	I/O34	I/O46	I/O70	26	20	17	24	26	34	K3	42	251	V25	AB31
I/O23	I/O35	I/O47	I/O71				25	27	35	J6	43	250	V24	AB30
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2				26	28	36	L1	44	249	U23	AB29
GND	GND	GND	GND				27	29	37	GND*	45	248	GND(1)	GND(1)
		I/O49	I/O73									247	Y26	AB28
		I/O50	I/O74									246	W25	AC30
	I/O37	I/O51	I/O75							L2	46	245	W24	AC29
	I/O38	I/O52	I/O76							K4	47	244	V23	AC28
			I/O77											
			I/O78											
			GND											GND(1)
														VCC(1)
			I/O79											AD31
			I/O80											AD30
	I/O39	I/O53	I/O81						38	L3	48	243	AA26	AD29
	I/O40	I/O54	I/O82						39	M1	49	242	Y25	AD28
I/O25	I/O41	I/O55	I/O83					30	40	K5	50	241	Y24	AE30
I/O26	I/O42	I/O56	I/O84					31	41	M2	51	240	AA25	AE29
		GND	GND										GND(1)	GND(1)
		VCC	VCC										VCC(1)	VCC(1)
		I/O57	I/O85									239	AB25	AF31
		I/O58	I/O86									238	AA24	AE28
			I/O87											AF30
			I/O88											AF29
I/O27	I/O43	I/O59	I/O89	27	21	18	28	32	42	L4	52	237	Y23	AG31
I/O28	I/O44	I/O60	I/O90		22	19	29	33	43	N1	53	236	AC26	AF28
			GND											GND(1)
			I/O91										AD26	AG30
			I/O92										AC25	AG29
I/O29	I/O45	I/O61	I/O93				30	34	44	M3	54	235	AA23	AH31
I/O30	I/O46	I/O62	I/O94				31	35	45	N2	55	234	AB24	AG28
I/O31 (/OTS)	I/O47 (/OTS)	I/O63 (/OTS)	I/O95 (/OTS)	28	23	20	32	36	46	K6	56	233	AD25	AH30

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	24	21	33	37	47	P1	57	232	AC24	AJ30
M1	M1	M1	M1	30	25	22	34	38	48	N3	58	231	AB23	AH29
GND	GND	GND	GND	31	26	23	35	39	49	GND(1)	59	230	GND(1)	GND(1)
M0	M0	M0	M0	32	27	24	36	40	50	P2	60	229	AD24	AH28

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
VCC	VCC	VCC	VCC	33	28	25	37	41	55	VCC*	61	228	VCC(1)	VCC(1)
M2	M2	M2	M2	34	29	26	38	42	56	M4	62	227	AC23	AJ28
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	30	27	39	43	57	R2	63	226	AE24	AK29
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	31	28	40	44	58	P3	64	225	AD23	AH27
I/O35	I/O51	I/O67	I/O99				41	45	59	L5	65	224	AC22	AK28
I/O36	I/O52	I/O68	I/O100				42	46	60	N4	66	223	AF24	AJ27
I/O37	I/O53	I/O69	I/O101		32	29	43	47	61	R3	67	222	AD22	AL28
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	33	30	44	48	62	P4	68	221	AE23	AH26
			GND											GND(1)
			I/O103											AK27
			I/O104											AJ26
			I/O105										AC21	AL27
			I/O106										AD21	AH25
		I/O71	I/O107									220	AE22	AK26
		I/O72	I/O108									219	AF23	AL26
		VCC	VCC										VCC(1)	VCC(1)
		GND	GND										GND(1)	GND(1)
I/O39	I/O55	I/O73	I/O109					49	63	K7	69	218	AD20	AH24
I/O40	I/O56	I/O74	I/O110					50	64	M5	70	217	AE21	AJ25
	I/O57	I/O75	I/O111						65	R4	71	216	AF21	AK25
	I/O58	I/O76	I/O112						66	N5	72	215	AC19	AJ24
			I/O113											AH23
			I/O114											AK24
														VCC(1)
			GND											GND(1)
			I/O115											
			I/O116											
	I/O59	I/O77	I/O117							P5	73	214	AD19	AL24
	I/O60	I/O78	I/O118							L6	74	213	AE20	AH22
		I/O79	I/O119									212	AF20	AJ23
		I/O80	I/O120									211	AC18	AK23
GND	GND	GND	GND				45	51	67	GND(1)	75	210	GND(1)	GND(1)

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
I/O41	I/O61	I/O81	I/O121				46	52	68	R5	76	209	AD18	AJ22
I/O42	I/O62	I/O82	I/O122				47	53	69	M6	77	208	AE19	AK22
I/O43	I/O63	I/O83	I/O123	38	34	31	48	54	70	N6	78	207	AC17	AL22
I/O44	I/O64	I/O84	I/O124	39	35	32	49	55	71	P6	79	206	AD17	AJ21
	VCC	VCC	VCC							VCC(1)	80	204	VCC(1)	VCC(1)
	I/O65	I/O85	I/O125						72	R6	81	203	AE18	AH20
	I/O66	I/O86	I/O126						73	M7	82	202	AF18	AK21
			GND											GND(1)
			I/O127											AJ20
			I/O128											AH19
			I/O129										AC16	AK20
			I/O130										AD16	AJ19
		I/O87	I/O131									201	AE17	AL20
		I/O88	I/O132									200	AE16	AH18
		GND	GND								83		GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
		I/O89	I/O133									199	AF16	AK19
		I/O90	I/O134									198	AC15	AJ18
	I/O67	I/O91	I/O135							N7	84	197	AD15	AL19
	I/O68	I/O92	I/O136							P7	85	196	AE15	AK18
I/O45	I/O69	I/O93	I/O137		36	33	50	56	74	R7	86	195	AF15	AH17
I/O46	I/O70	I/O94	I/O138		37	34	51	57	75	L7	87	194	AD14	AJ17
			GND											GND(1)
			I/O139											
			I/O140											
			I/O141											AK17
			I/O142											AL17
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	38	35	52	58	76	N8	88	193	AE14	AJ16
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	39	36	53	59	77	P8	89	192	AF14	AK16
VCC	VCC	VCC	VCC	42	40	37	54	60	78	VCC(1)	90	191	VCC(1)	VCC(1)
GND	GND	GND	GND	43	41	38	55	61	79	GND(1)	91	190	GND(1)	GND(1)
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	42	39	56	62	80	L8	92	189	AE13	AL16
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	43	40	57	63	81	P9	93	188	AC13	AH15
			I/O147											AL15
			I/O148											AJ15
			I/O149											
			I/O150											
			GND											GND(1)
I/O51	I/O75	I/O99	I/O151		44	41	58	64	82	R9	94	187	AD13	AK15
I/O52	I/O76	I/O100	I/O152		45	42	59	65	83	N9	95	186	AF12	AJ14
	I/O77	I/O101	I/O153						84	M9	96	185	AE12	AH14
	I/O78	I/O102	I/O154						85	L9	97	184	AD12	AK14
		I/O103	I/O155									183	AC12	AL13

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
		I/O104	I/O156									182	AF11	AK13
			VCC										VCC(1)	VCC(1)
		GND	GND								98		GND(1)	GND(1)
		I/O105	I/O157									181	AE11	AJ13
		I/O106	I/O158									180	AD11	AH13
			I/O159										AE10	AL12
			I/O160										AC11	AK12
			I/O161											AJ12
			I/O162											AK11
			GND											GND(1)
	I/O79	I/O107	I/O163							R10	99	179	AF9	AH12
	I/O80	I/O108	I/O164							P10	100	178	AD10	AJ11
	VCC	VCC	VCC							VCC(1)	101	177	VCC(1)	VCC(1)
I/O53 (D12)	I/O81 (D12)	I/O109 (D12)	I/O165 (D12)	46	46	43	60	66	86	N10	102	175	AE9	AL10
I/O54 (D11)	I/O82 (D11)	I/O110 (D11)	I/O166 (D11)	47	47	44	61	67	87	K9	103	174	AD9	AK10
I/O55	I/O83	I/O111	I/O167				62	68	88	R11	104	173	AC10	AJ10
I/O56	I/O84	I/O112	I/O168				63	69	89	P11	105	172	AF7	AK9
GND	GND	GND	GND				64	70	90	GND(1)	106	171	GND(1)	GND(1)
		I/O113	I/O169									170	AE8	AL8
		I/O114	I/O170									169	AD8	AH10
	I/O85	I/O115	I/O171							M10	107	168	AC9	AJ9
	I/O86	I/O116	I/O172							N11	108	167	AF6	AK8
			I/O173											
			I/O174											
			GND											GND(1)
														VCC(1)
			I/O175											AJ8
			I/O176											AH9
	I/O87	I/O117	I/O177						91	R12	109	166	AE7	AK7
	I/O88	I/O118	I/O178						92	L10	110	165	AD7	AL6
I/O57	I/O89	I/O119	I/O179					71	93	P12	111	164	AE6	AJ7
I/O58	I/O90	I/O120	I/O180					72	94	M11	112	163	AE5	AH8
		GND	GND										GND(1)	GND(1)
		VCC	VCC										VCC(1)	VCC(1)
		I/O121	I/O181									162	AD6	AK6
		I/O122	I/O182									161	AC7	AL5
I/O59 (D10)	I/O91 (D10)	I/O123 (D10)	I/O183 (D10)	48	48	45	65	73	95	R13	113	160	AF4	AH7
I/O60 (D9)	I/O92 (D9)	I/O124 (D9)	I/O184 (D9)	49	49	46	66	74	96	N12	114	159	AF3	AJ6
			I/O185										AE4	AK5

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O186										AC6	AL4
			GND											GND(1)
			I/O187											AH6
			I/O188											AJ5
I/O61	I/O93	I/O125	I/O189				67	75	97	P13	115	158	AD5	AK4
I/O62	I/O94	I/O126	I/O190				68	76	98	K10	116	157	AE3	AH5
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	50	47	69	77	99	R14	117	156	AD4	AK3
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192 ,GCK4	51	51	48	70	78	100	N13	118	155	AC5	AJ4
GND	GND	GND	GND	52	52	49	71	79	101	GND(1)	119	154	GND(1)	GND(1)
/CON	/CON	/CON	/CON	53	53	50	72	80	103	P14	120	153	AD3	AH4

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
VCC	VCC	VCC	VCC	54	54	51	73	81	106	VCC(1)	121	152	VCC(1)	VCC(1)
/RESET	/RESET	/RESET	/RESET	55	55	52	74	82	108	M12	122	151	AC4	AH3
I/O65 (D7)	I/O97 (D7)	I/O129 (D7)	I/O193 (D7)	56	56	53	75	83	109	P15	123	150	AD2	AJ2
I/O66, GCK5	I/O98, GCK5	I/O130, GCK5	I/O194, GCK5	57	57	54	76	84	110	N14	124	149	AC3	AG4
I/O67	I/O99	I/O131	I/O195				77	85	111	L11	125	148	AB4	AG3
I/O68	I/O100	I/O132	I/O196				78	86	112	M13	126	147	AD1	AH2
			I/O197										AB3	AH1
			I/O198										AC2	AF4
			GND											GND(1)
	I/O101	I/O133	I/O199							N15	127	146	AA4	AF3
	I/O102	I/O134	I/O200							M14	128	145	AA3	AG2
			I/O201											AG1
			I/O202											AE4
		I/O135	I/O203									144	AB2	AE3
		I/O136	I/O204									143	AC1	AF2
		VCC	VCC										VCC(1)	VCC(1)
		GND	GND										GND(1)	GND(1)
I/O69 (D6)	I/O103 (D6)	I/O137 (D6)	I/O205 (D6)	58	58	55	79	87	113	J10	129	142	Y3	AF1
I/O70	I/O104	I/O138	I/O206		59	56	80	88	114	L12	130	141	AA2	AD4
I/O71	I/O105	I/O139	I/O207					89	115	M15	131	140	AA1	AD3
I/O72	I/O106	I/O140	I/O208					90	116	L13	132	139	W4	AE2
			I/O209											AD2
			I/O210											AC4
														VCC(1)
			GND											GND(1)

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O211											
			I/O212											
	I/O107	I/O141	I/O213						117	L14	133	138	W3	AC3
	I/O108	I/O142	I/O214						118	K11	134	137	Y2	AD1
		I/O143	I/O215									136	Y1	AC2
		I/O144	I/O216									135	V4	AB4
GND	GND	GND	GND				81	91	119	GND(1)	135	134	GND(1)	GND(1)
	I/O109	I/O145	I/O217							L15	136	133	V3	AB3
	I/O110	I/O146	I/O218							K12	137	132	W2	AB2
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3				82	92	120	K13	138	131	U4	AB1
I/O74	I/O112	I/O148	I/O220				83	93	121	K14	139	130	U3	AA3
	VCC	VCC	VCC							VCC(1)	140	129	VCC(1)	VCC(1)
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	60	57	84	94	122	K15	141	127	V2	AA2
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	61	58	85	95	123	J12	142	126	V1	Y2
			GND											GND(1)
			I/O223										T4	Y4
			I/O224										T3	Y3
			I/O225											Y1
			I/O226											W1
		I/O151	I/O227									125	U2	W4
		I/O152	I/O228									124	T2	W3
		GND	GND								143		GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
			I/O229											W2
			I/O230											V2
		I/O153	I/O231									123	T1	V4
		I/O154	I/O232									122	R4	V3
	I/O115	I/O155	I/O233						124	J13	144	121	R3	U1
	I/O116	I/O156	I/O234						125	J14	145	120	R2	U2
			GND											GND(1)
I/O77	I/O117	I/O157	I/O235		62	59	86	96	126	J15	146	119	R1	U4
I/O78	I/O118	I/O158	I/O236		63	60	87	97	127	J11	147	118	P3	U3
			I/O237											
			I/O238											
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	64	61	88	98	128	H13	148	117	P2	T1
I/O80	I/O120	I/O160	I/O240	62	65	62	89	99	129	H14	149	116	P1	T2
VCC	VCC	VCC	VCC	63	66	63	90	100	130	VCC(1)	150	115	VCC(1)	VCC(1)
GND	GND	GND	GND	64	67	64	91	101	131	GND(1)	151	114	GND(1)	GND(1)
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	68	65	92	102	132	H12	152	113	N2	T3
I/O82 (/CHECK)	I/O122 (/CHECK)	I/O162 (/CHECK)	I/O242 (/CHECK)	66	69	66	93	103	133	H11	153	112	N4	R1
			I/O243											

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			I/O244											
I/O83	I/O123	I/O163	I/O245		70	67	94	104	134	G14	154	111	N3	R2
I/O84	I/O124	I/O164	I/O246				95	105	135	G15	155	110	M1	R4
			GND											GND(1)
	I/O125	I/O165	I/O247						136	G13	156	109	M2	R3
	I/O126	I/O166	I/O248						137	G12	157	108	M3	P2
		I/O167	I/O249									107	M4	P3
		I/O168	I/O250									106	L1	P4
			I/O251											N1
			I/O252											N2
			VCC										VCC(1)	VCC(1)
		GND	GND								158		GND(1)	GND(1)
		I/O169	I/O253									105	L2	N3
		I/O170	I/O254									104	L3	N4
			I/O255										K2	M1
			I/O256										L4	M2
			I/O257											M3
			I/O258											M4
			GND											GND(1)
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	71	68	96	106	138	G11	159	103	J1	L2
I/O86	I/O128	I/O172	I/O260	68	72	69	97	107	139	F15	160	102	K3	L3
	VCC	VCC	VCC							VCC(1)	161	101	VCC(1)	VCC(1)
I/O87	I/O129	I/O173	I/O261				98	108	140	F14	162	99	J2	K1
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4				99	109	141	F13	163	98	J3	K2
	I/O131	I/O175	I/O263							G10	164	97	K4	K3
	I/O132	I/O176	I/O264							E15	165	96	G1	K4
GND	GND	GND	GND				100	110	142	GND(1)	166	95	GND(1)	GND(1)
		I/O177	I/O265									94	H2	J2
		I/O178	I/O266									93	H3	J3
	I/O133	I/O179	I/O267							E14	167	92	J4	J4
	I/O134	I/O180	I/O268							F12	168	91	F1	H1
			I/O269											
			I/O270											
			GND											GND(1)
	I/O135	I/O181	I/O271						143	E13	169	90	G2	H2
	I/O136	I/O182	I/O272						144	D15	170	89	G3	H3
I/O89	I/O137	I/O183	I/O273					111	145	F11	171	88	F2	H4

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
I/O90	I/O138	I/O184	I/O274					112	146	D14	172	87	E2	G2
			I/O275											G3
			I/O276											F1
		GND	GND										GND(1)	GND(1)
		VCC	VCC										VCC(1)	VCC(1)
I/O91 (D1)	I/O139 (D1)	I/O185 (D1)	I/O277 (D1)	69	73	70	101	113	147	E12	173	86	F3	G4
I/O92	I/O140	I/O186	I/O278	70	74	71	102	114	148	C15	174	85	G4	F2
			I/O279										D1	F3
			I/O280										C1	E1
			I/O281											F4
			I/O282											E2
			GND											GND(1)
		I/O187	I/O283									84	D2	E3
		I/O188	I/O284									83	F4	D1
I/O93	I/O141	I/O189	I/O285				103	115	149	D13	175	82	E3	E4
I/O94	I/O142	I/O190	I/O286				104	116	150	C14	176	81	C2	D2
I/O95 (D0)	I/O143 (D0)	I/O191 (D0)	I/O287 (D0)	71	75	72	105	117	151	F10	177	80	D3	C2
I/O96, GCK6 (/CSOUT)	I/O144, GCK6 (/CSOUT)	I/O192, GCK6 (/CSOUT)	I/O288, GCK6 (/CSOUT)	72	76	73	106	118	152	B15	178	79	E4	D3
CCLK	CCLK	CCLK	CCLK	73	77	74	107	119	153	C13	179	78	C3	D4
VCC	VCC	VCC	VCC	74	78	75	108	120	154	VCC(1)	180	77	VCC(1)	VCC(1)

AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
GND	GND	GND	GND	76	80	77	110	122	160	GND(1)	182	75	GND(1)	GND(1)
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	81	78	111	123	161	A14	183	74	B3	B3
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	82	79	112	124	162	B13	184	73	C4	D5
I/O99	I/O147	I/O195	I/O291				113	125	163	E11	185	72	D5	B4
I/O100	I/O148	I/O196	I/O292				114	126	164	C12	186	71	A3	C5
			I/O293											A4
			I/O294											D6
			GND											GND(1)
			I/O295										C5	B5
			I/O296										B4	C6
I/O101 (/CS1,A2)	I/O149 (/CS1,A2)	I/O197 (/CS1,A2)	I/O297 (/CS1,A2)	79	83	80	115	127	165	A13	187	70	D6	A5
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	84	81	116	128	166	B12	188	69	C6	D7
		I/O199	I/O299									68	B5	B6
		I/O200	I/O300									67	A4	A6
		VCC	VCC										VCC(1)	VCC(1)

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
		GND	GND										GND(1)	GND(1)
	I/O151	I/O201	I/O301	75	79	76	109	121	159	F9	189	66	C7	D8
	I/O152	I/O202	I/O302							D11	190	65	B6	C7
I/O103	I/O153	I/O203	I/O303				117	129	167	A12	191	64	A6	B7
I/O104	I/O154	I/O204	I/O304	75(2)	79(2)	76(2)	109(2)	130	168	C11	192	63	D8	D9
			I/O305										C8	B8
			I/O306											A8
														VCC(1)
			GND											GND(1)
			I/O307											
			I/O308											
	I/O155	I/O205	I/O309						169	B11	193	62	B7	D10
	I/O156	I/O206	I/O310						170	E10	194	61	A7	C9
		I/O207	I/O311								195	60	D9	B9
		I/O208	I/O312									59	C9	C10
GND	GND	GND	GND				118	131	171	GND(1)	196	58	GND(1)	GND(1)v
I/O105	I/O157	I/O209	I/O313				119	132	172	A11	197	57	B8	B10
I/O106	I/O158	I/O210	I/O314				120	133	173	D10	198	56	D10	A10
	I/O159	I/O211	I/O315							C10	199	55	C10	C11
	I/O160	I/O212	I/O316							B10	200	54	B9	D12
	VCC	VCC	VCC							VCC*	201	52	VCC(1)	VCC(1)
		I/O213	I/O317									51	A9	B11
		I/O214	I/O318									50	D11	C12
			GND											GND(1)
			I/O319											D13
			I/O320											B12
			I/O321										C11	C13
			I/O322										B10	A12
		I/O215	I/O323									49	B11	D14
		I/O216	I/O324									48	A11	B13
		GND	GND										GND(1)	GND(1)
			VCC										VCC(1)	VCC(1)
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	85	82	121	134	174	A10	202	47	D12	C14
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	86	83	122	135	175	D9	203	46	C12	A13
	I/O163	I/O219	I/O327						176	C9	205	45	B12	B14
	I/O164	I/O220	I/O328					136	177	B9	206	44	A12	D15
I/O109	I/O165	I/O221	I/O329		87	84	123	137	178	A9	207	43	C13	C15
I/O110	I/O166	I/O222	I/O330		88	85	124	138	179	E9	208	42	B13	B15

Notes: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This applies to the AT40K05 only.

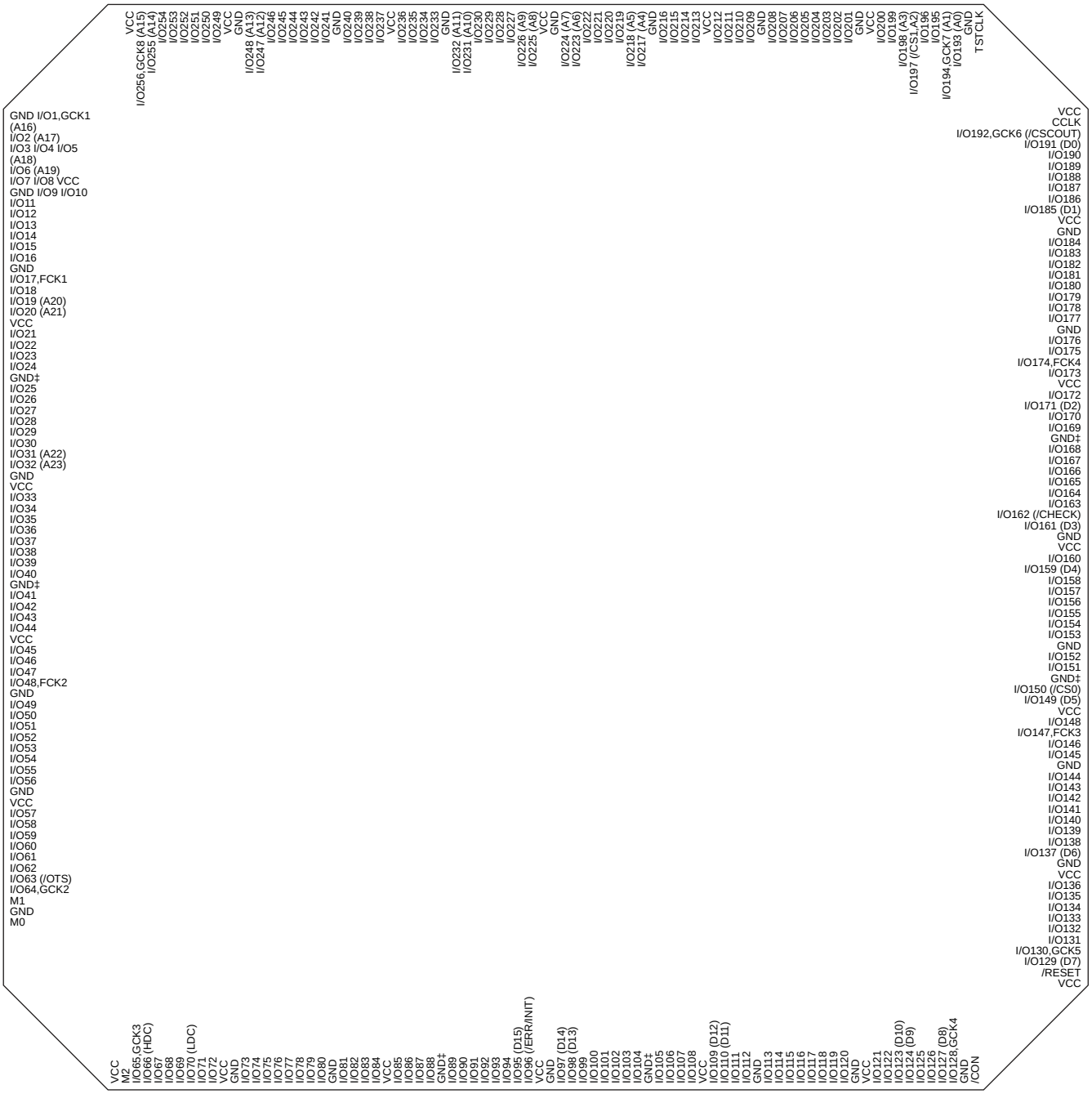
AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
			GND											GND(1)
			I/O331											
			I/O332											
			I/O333											A15
			I/O334											C16
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	89	86	125	139	180	C8	209	41	A13	B16
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	90	87	126	140	181	B8	210	40	B14	A16
GND	GND	GND	GND	1	91	88	127	141	182	GND(1)	211	39	GND(1)	GND(1)
VCC	VCC	VCC	VCC	2	92	89	128	142	183	VCC(1)	212	38	VCC(1)	VCC(1)
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	93	90	129	143	184	E8	213	37	D14	D17
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	94	91	130	144	185	B7	214	36	C14	A17
			I/O339											C17
			I/O340											B17
			I/O341											
			I/O342											
			GND											GND(1)
I/O115	I/O171	I/O227	I/O343		95	92	131	145	186	A7	215	35	A15	C18
I/O116	I/O172	I/O228	I/O344		96	93	132	146	187	C7	216	34	B15	D18
	I/O173	I/O229	I/O345						188	D7	217	33	C15	B18
	I/O174	I/O230	I/O346						189	E7	218	32	D15	A19
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	97	94	133	147	190	A6	220	31	A16	B19
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	98	95	134	148	191	B6	221	30	B16	C19
			VCC										VCC(1)	VCC(1)
		GND	GND										GND(1)	GND(1)
		I/O233	I/O349									29	C16	D19
		I/O234	I/O350									28	B17	A20
			I/O351										D16	B20
			I/O352										A18	C20
			I/O353											B21
			I/O354											D20
			GND											GND(1)
		I/O235	I/O355									27	C17	C21
		I/O236	I/O356									26	B18	A22
	VCC	VCC	VCC							VCC(1)	222	25	VCC(1)	VCC(1)
	I/O177	I/O237	I/O357							C6	223	23	C18	B22
	I/O178	I/O238	I/O358							F7	224	22	D17	C22
I/O119	I/O179	I/O239	I/O359				135	149	192	A5	225	21	A20	B23
I/O120	I/O180	I/O240	I/O360				136	150	193	B5	226	20	B19	A24

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)										
128 I/O	192 I/O	256 I/O	384 I/O	PC84	RQ100	VQ100	TQ144	PQ160	PQ208	BG225	PQ240	PQ304	BG352	BG432
GND	GND	GND	GND				137	151	194	GND*	227	19	GND[1]	GND[1]
		I/O241	I/O361									18	C19	D22
		I/O242	I/O362									17	D18	C23
	I/O181	I/O243	I/O363						195	D6	228	16	A21	B24
	I/O182	I/O244	I/O364						196	C5	229	15	B20	C24
			I/O365											
			I/O366											
			GND											GND[1]
			I/O367											D23
			I/O368											B25
I/O121	I/O183	I/O245	I/O369					152	197	A4	230	14	C20	A26
I/O122	I/O184	I/O246	I/O370					153	198	E6	231	13	B21	C25
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	99	96	138	154	199	B4	232	12	B22	D24
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	100	97	139	155	200	D5	233	10	C21	B26
		GND	GND										GND*	GND*
		VCC	VCC										VCC*	VCC*
		I/O249	I/O373									9	D20	A27
		I/O250	I/O374									8	A23	D25
			I/O375										A24	C26
			I/O376										B23	B27
			I/O377											A28
			I/O378											D26
			GND											GND*
	I/O187	I/O251	I/O379							A3	234	7	D21	C27
	I/O188	I/O252	I/O380							C4	235	6	C22	B28
I/O125	I/O189	I/O253	I/O381				140	156	201	B3	236	5	B24	D27
I/O126	I/O190	I/O254	I/O382				141	157	202	F6	237	4	C23	B29
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	1	98	142	158	203	A2	238	3	D22	C28
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	2	99	143	159	204	C3	239	2	C24	D28
VCC	VCC	VCC	VCC	11	3	100	144	160	205	VCC*	240	1	VCC[1]	VCC[1]

Note: 1. Pads labelled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

Figure 15. AT40K20 Pad Ring



AT40K05 Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
5,000-10,000	2	AT40K05-2AJC AT40K05-2AQC AT40K05-2BQC AT40K05-2CQC AT40K05-2DQC	84J 100Q 144Q 160Q 208Q	5V Commercial (0°C to 70°C)
5,000-10,000	2	AT40K05-2AJI AT40K05-2AQI AT40K05-2BQI AT40K05-2CQI AT40K05-2DQI	84J 100Q 144Q 160Q 208Q	5V Industrial (-40°C to 85°C)

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
5,000-10,000	3	AT40K05LV-3AJC AT40K05LV-3AQC AT40K05LV-3BQC AT40K05LV-3CQC AT40K05LV-3DQC	84J 100Q 144Q 160Q 208Q	3.3V Commercial (0°C to 20°C)

Package Type	
84J	84-lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q	100-lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (VQFP)
100RQ	100-lead, Rectangular Plastic Plastic Gull Wing Quad Flat Package (RQPD)
144Q	144-lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
160Q	160-lead, Plastic Gull Wing Quad Flat Package (PQFP)
208Q	208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
225G	225-lead, Ball Grid Array Package (BGA)
240Q	240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
304Q	304-lead, Plastic Gull Wing Quad Flat Package (PQFP)
352G	352-ball, Ball Grid Array Package (BGA)
432G	432-ball, Ball Grid Array Package (BGA)

AT40K10 Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
10,000-20,000	2	AT40K10-2AJC	84J	5V Commercial
		AT40K10-2AQC	100Q	(0°C to 70°C)
		AT40K10-2RQC	100RQ	
		AT40K10-2BQC	144Q	
		AT40K10-2CQC	160Q	
		AT40K10-2DQC	208Q	
		AT40K10-2EQC	240Q	
		AT40K10-2AGC	225G	
10,000-20,000	2	AT40K10-2AJI	84J	5V Industrial
		AT40K10-2AQI	100Q	(-40°C to 85°C)
		AT40K10-2BQI	144Q	
		AT40K10-2CQI	160Q	
		AT40K10-2DQI	208Q	
		AT40K10-2EQI	240Q	
		AT40K10-2AGI	225G	

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
10,000-20,000	3	AT40K10LV-3AJC	84J	3.3V Commercial
		AT40K10LV-3AQC	100Q	(0°C to 20°C)
		AT40K10LV-3RQC	100RQ	
		AT40K10LV-3BQC	144Q	
		AT40K10LV-3CQC	160Q	
		AT40K10LV-3DQC	208Q	
		AT40K10LV-3EQC	240Q	
		AT40K10LV-3AGC	225G	

Package Type	
84J	84-lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q	100-lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (VQFP)
100RQ	100-lead, Rectangular Plastic Plastic Gull Wing Quad Flat Package (RQPD)
144Q	144-lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
160Q	160-lead, Plastic Gull Wing Quad Flat Package (PQFP)
208Q	208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
225G	225-lead, Ball Grid Array Package (BGA)
240Q	240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
304Q	304-lead, Plastic Gull Wing Quad Flat Package (PQFP)
352G	352-ball, Ball Grid Array Package (BGA)
432G	432-ball, Ball Grid Array Package (BGA)

AT40K20 Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
20,000-30,000	2	AT40K20-2AJC	84J	5V Commercial
		AT40K20-2AQC	100Q	(0°C to 70°C)
		AT40K20-2BQC	144Q	
		AT40K20-2CQC	160Q	
		AT40K20-2DQC	208Q	
		AT40K20-2EQC	240Q	
		AT40K20-2FQC	304Q	
		AT40K20-2BGC	352G	
		AT40K20-2AGC	225G	
20,000-30,000	2	AT40K20-2AJI	84J	5V Industrial
		AT40K20-2BQI	144Q	(-40°C to 85°C)
		AT40K20-2CQI	160Q	
		AT40K20-2DQI	208Q	
		AT40K20-2EQI	240Q	
		AT40K20-2FQI	304Q	
		AT40K20-2BGI	352G	
		AT40K20-2AGI	225G	

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
20,000-30,000	3	AT40K20LV-2AJC	84J	3.3V Commercial
		AT40K20LV-2AQC	100Q	(0°C to 20°C)
		AT40K20LV-2BQC	144Q	
		AT40K20LV-2CQC	160Q	
		AT40K20LV-2DQC	208Q	
		AT40K20LV-2EQC	240Q	
		AT40K20LV-2FQC	304Q	
		AT40K20LV-2BGC	352G	
		AT40K20LV-2AGC	225G	

Package Type	
84J	84-lead, Plastic J-Leaded Chip Carrier (PLCC)
100Q	100-lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (VQFP)
144Q	144-lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
160Q	160-lead, Plastic Gull Wing Quad Flat Package (PQFP)
208Q	208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
225G	225-lead, Ball Grid Array Package (BGA)
240Q	240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
304Q	304-lead, Plastic Gull Wing Quad Flat Package (PQFP)
352G	352-ball, Ball Grid Array Package (BGA)
432G	432-ball, Ball Grid Array Package (BGA)

AT40K40 Ordering Information

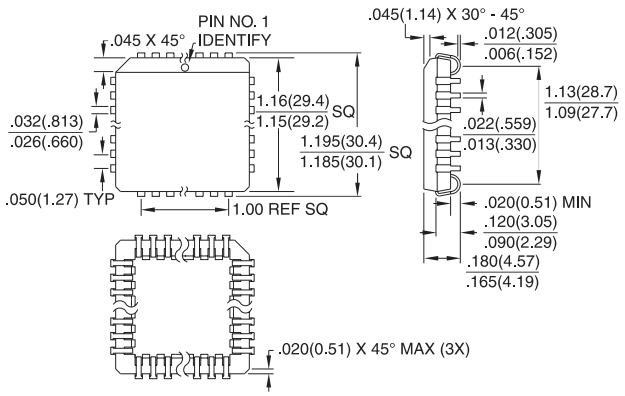
Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
40,000-50,000	2	AT40K40-2BQC	144Q	5V Commercial
		AT40K40-2DQC	208Q	(0°C to 70°C)
		AT40K40-2EQC	240Q	
		AT40K40-2FQC	304Q	
		AT40K40-2BGC	352G	
		AT40K40-2CGC	432G	
40,000-50,000	2	AT40K40-2BQI	144Q	5V Industrial
		AT40K40-2DQI	208Q	(-40°C to 85°C)
		AT40K40-2EQI	240Q	
		AT40K40-2FQI	304Q	
		AT40K40-2BGI	352G	
		AT40K40-2CGI	432G	

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
40,000-50,000	3	AT40K40LV-3BQC	144Q	3.3V Commercial
		AT40K40LV-3DQC	208Q	(0°C to 20°C)
		AT40K40LV-3EQC	240Q	
		AT40K40LV-3FQC	304Q	
		AT40K40LV-3BGC	352G	
		AT40K40LV-3CGC	432G	

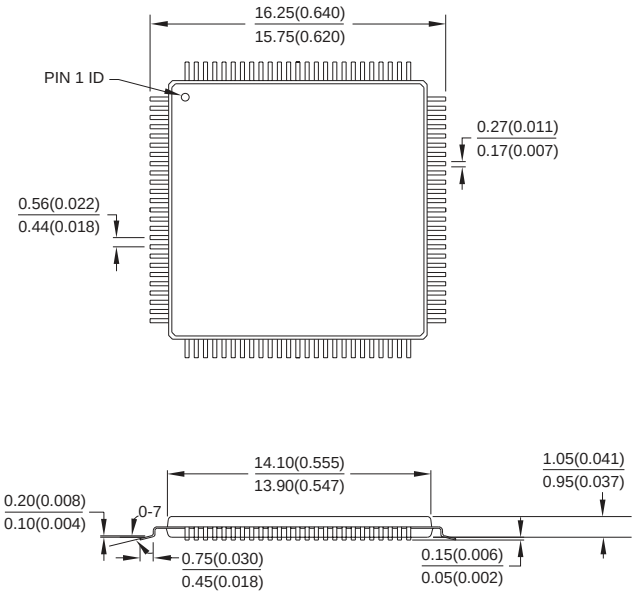
Package Type	
144Q	144-lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
160Q	160-lead, Plastic Gull Wing Quad Flat Package (PQFP)
208Q	208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
225G	225-lead, Ball Grid Array Package (BGA)
240Q	240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
304Q	304-lead, Plastic Gull Wing Quad Flat Package (PQFP)
352G	352-ball, Ball Grid Array Package (BGA)
432G	432-ball, Ball Grid Array Package (BGA)

Packaging Information

84J, 84-lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AF

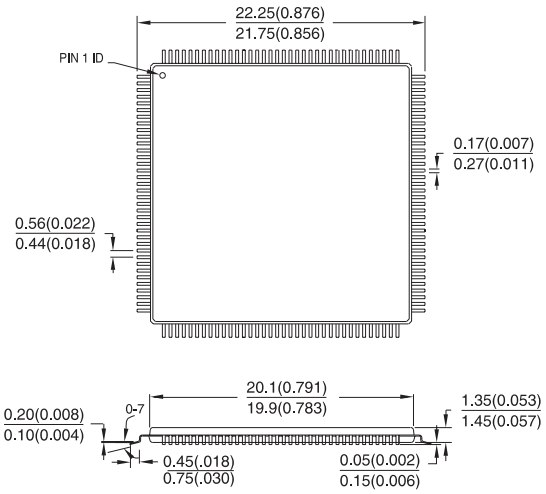


100Q, 100-lead, Plastic Gull Wing Quad Flat Package (VQFP)
Dimensions in Millimeters and (Inches)*



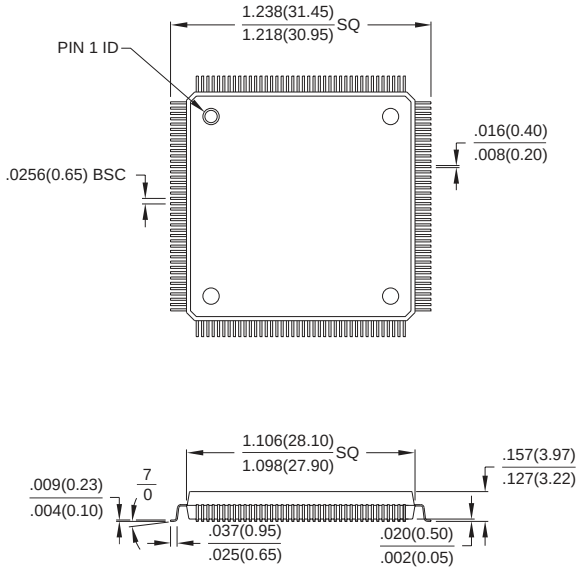
*Controlling dimension: millimeters

144Q, 144-lead, Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*



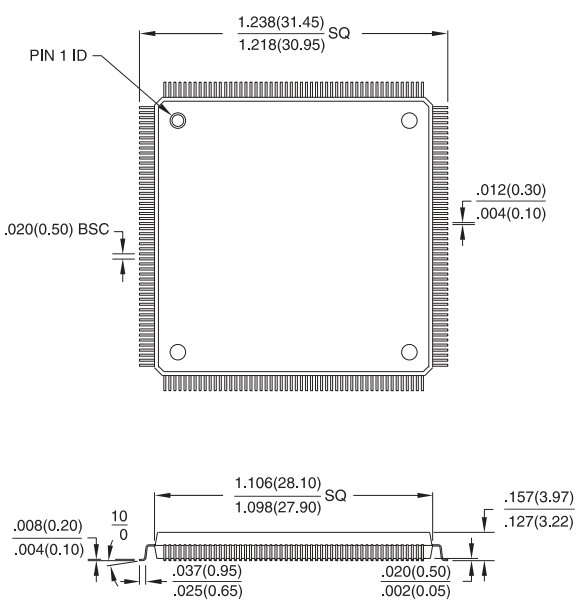
*Controlling dimension: millimeters

160Q, 160-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



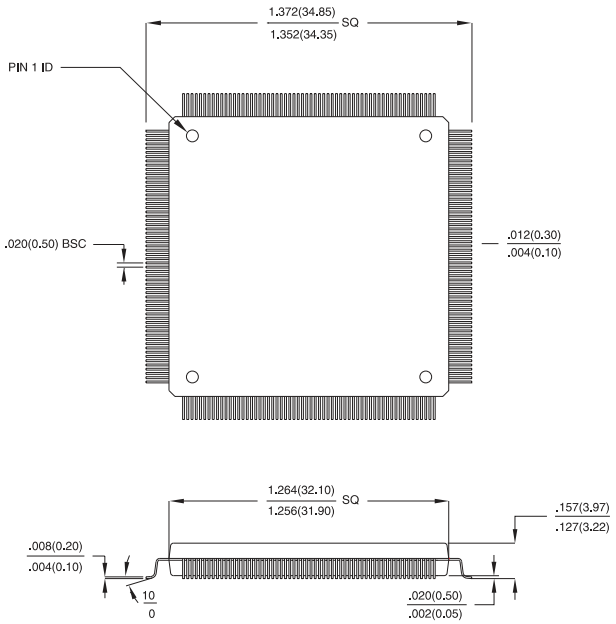
Packaging Information

208Q, 208-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



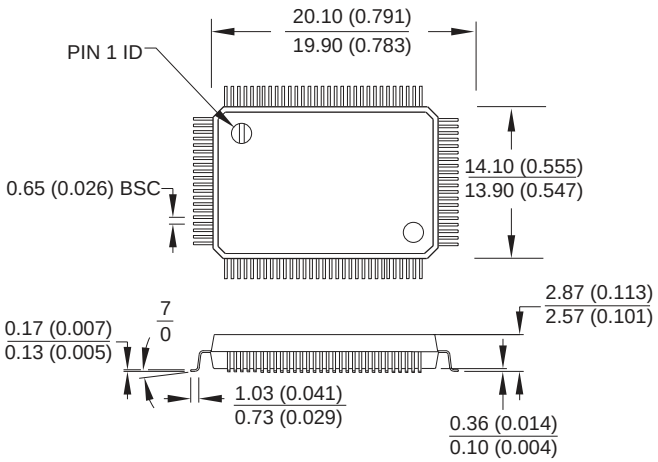
*Controlling dimension: millimeters

240Q, 240-lead, Plastic Gull Wing Quad Flat Package (PQFP)
Dimensions in (Millimeters) and Inches



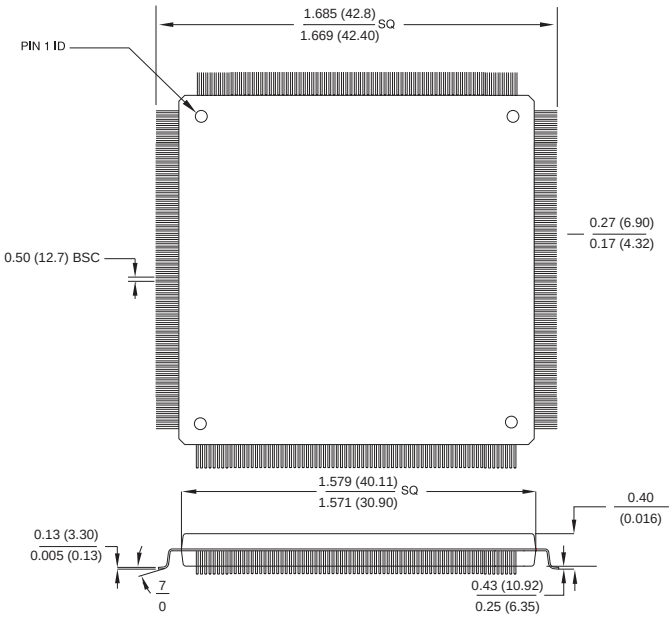
*Controlling dimension: millimeters

100RQ, 100-lead, Rectangular Plastic Gull Wing Quad Flat Pack (RQFP)
Dimensions in Millimeters and (Inches)*



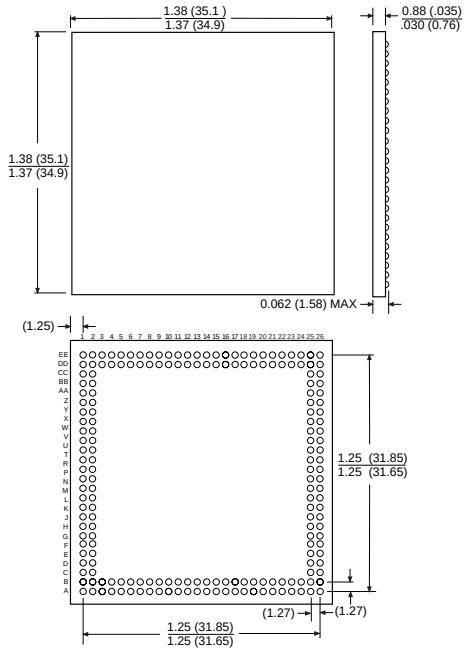
*Controlling dimension: millimeters

304Q, 304-lead, Plastic Gull Wing Quad Flat Pack (PQFP)
Dimensions in (Millimeters) and Inches

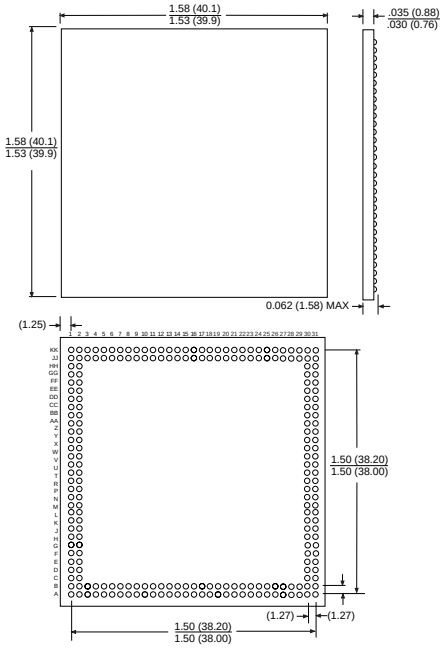


Packaging Information

352B, 352-ball Ball Grid Array (BGA)
Dimensions in (Millimeters) and Inches



432B, 432-ball Ball Grid Array (BGA)
Dimensions in (Millimeters) and Inches



Thermal Coefficient Table

Package Style	Lead Count	Theta J-A 0 LFPM	Theta J-A 225 LFPM	Theta J-A 500 LPFM	Theta J-C
PQFP	144	33	27	23	8.5
PQFP	160	30	24	20	7
PQFP	208	32	28	24	10
PQFP	240	27	No Data	No Data	
PQFP	304	19	No Data	No Data	
TQFP	100	47	39	33	22
RQFP	100	3			
PLCC	84	37	30	25	12
BGA	225	26	No Data	No Data	
BGA	352				
BGA	432				

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