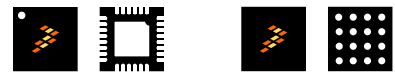


# MKW41Z/31Z/21Z Data Sheet

A Bluetooth® Low Energy, IEEE® Standard 802.15.4, Generic FSK System on a Chip (SoC) Supports the following: MKW41Z512VHT4, MKW31Z512VHT4, MKW21Z512VHT4, MKW41Z256VHT4, MKW31Z256VHT4, MKW21Z256VHT4, MKW41Z512CAT4, MKW31Z512CAT4

MKW41Z512  
MKW31Z512  
MKW21Z512  
MKW41Z256  
MKW31Z256  
MKW21Z256



48 LQFN  
7 x 7 x 0.98 mm Pitch  
0.5 mm

75 WLCSP  
3.893 x 3.797 x 0.564  
mm Pitch 0.4 mm

## Multi-Standard Radio

- 2.4 GHz Bluetooth Low Energy ver. 4.2 compliant supporting up to 2 simultaneous hardware connections
- IEEE Std. 802.15.4 compliant with dual-PAN support
- Generic FSK modulation
  - Data Rate: 250, 500 and 1000 kbps
  - Modulations: GFSK BT = 0.3, 0.5, 0.7; FSK/MSK
  - Modulation Index: 0.32, 0.5, or 0.7
- Typical Receiver Sensitivity (BLE) = -95 dBm
- Typical Receiver Sensitivity (802.15.4) = -100 dBm
- Typical Receiver Sensitivity (250 kbps GFSK-BT=0.5, h=0.5) = -100 dBm
- Prog Transmitter Output Power: -30 dBm to 3.5 dBm
- Low external component counts for low cost application
- On-chip balun with single ended bidirectional RF port

## MCU and Memories

- Up to 48 MHz ARM® Cortex-M0+ core
- On-chip 512/256 KB Flash memory
- On-chip 128/64 KB SRAM

## Low Power Consumption

- Transceiver current (DC-DC buck mode, 3.6 V supply)
  - Typical Rx Current: 6.8 mA
  - Typical Tx current: 6.1 mA (0 dBm output)
- Low Power Mode (VLLS0) Current: 182 nA

## System peripherals

- Nine MCU low-power modes to provide power optimization based on application requirements
- DC-DC Converter supporting Buck, Boost, and Bypass operating modes
- Direct memory access(DMA) Controller
- Computer operating properly(COP) watchdog
- Serial wire debug(SWD) Interface and Micro Trace buffer
- Bit Manipulation Engine (BME)

## Analog Modules

- 16-bit Analog-to-Digital Converter (ADC)
- 12-bit Digital-to-Analog Converter (DAC)
- 6-bit High Speed Analog Comparator (CMP)
- 1.2 V voltage reference (VREF)

## Timers

- 16-bit low-power timer (LPTMR)
- 3 Timers Modules(TPM): One 4 channel TPM and two 2 channel TPMs
- Programmable Interrupt Timer (PIT)
- Real-Time Clock (RTC)

## Communication interfaces

- 2 serial peripheral interface (SPI) modules
- 2 inter-integrated circuit (I2C) modules



**Clocks**

- 26 and 32 MHz supported for BLE and FSK modes
- 32 MHz supported for IEEE Standard 802.15.4
- 32.768 kHz Crystal Oscillator

**Operating Characteristics**

- Voltage range: 0.9 V to 4.2 V
- Temperature range:
  - –40 to 105 °C (Laminate-QFN)
  - –40 to 85 °C (WLCSP)

**Human-machine interface**

- Touch sensing input
- General-purpose input/output

- Low Power UART module
- Carrier Modulator Timer (CMT)

**Security**

- AES-128 Hardware Accelerator (AES-A)
- True Random Number Generator (TRNG)
- Advanced flash security
- 80-bit unique identification number per chip
- 40-bit unique media access control (MAC) sub-address
- Bluetooth-LE v4.2 Secure Connections
- IEEE Standard 802.15.4-2011 compliant security

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# 1 Introduction

The KW41Z/31Z/21Z (called KW41Z throughout this document) is an ultra low-power, highly integrated single-chip device that enables Bluetooth low energy (BLE), Generic FSK (at 250, 500 and 1000 kbps) or IEEE Standard 802.15.4 RF connectivity for portable, extremely low-power embedded systems. Applications include portable health care devices, wearable sports and fitness devices, AV remote controls, computer keyboards and mice, gaming controllers, access control, security systems, smart energy and home area networks.

The KW41Z SoC integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of FSK/GFSK and O-QPSK modulations, an ARM Cortex-M0+ CPU, up to 512 KB Flash and up to 128 KB SRAM, BLE Link Layer hardware, 802.15.4 packet processor hardware and peripherals optimized to meet the requirements of the target applications.

The KW41Z SoC's radio frequency transceiver is compliant with Bluetooth version 4.2 for Low Energy (aka Bluetooth Smart or BLE), Generic FSK and the IEEE Standard 802.15.4 using O-QPSK in the 2.4 GHz ISM band. NXP provides fully certified Bluetooth Low Energy and IEEE Standard 802.15.4 protocol stacks, including Zigbee 3.0, Thread, and application profiles to support KW41Z.

The KW41Z SoC can be used in applications as a "BlackBox" modem by simply adding BLE or IEEE Standard 802.15.4 connectivity to an existing embedded controller system, or used as a stand-alone smart wireless sensor with embedded application where no host controller is required.

KW41Z has 512/256 KB of on-chip Flash and 128/64 KB of on-chip SRAM memory available to be used by customer applications and chosen communication protocol stack using a choice of either NXP or 3rd party software development tools.

The RF section of the KW41Z SoC is optimized to require very few external components, achieving the smallest RF footprint possible on a printed circuit board.

Extremely long battery life is achieved through efficiency of code execution in the Cortex-M0+ CPU core and the multiple low power operating modes of the KW41Z SoC. Additionally, an integrated DC-DC converter enables a wide operating range from 0.9 V to 4.2 V. The DC-DC in Buck mode enables KW41Z to operate from a single coin cell battery with a significant reduction of peak Rx and Tx current consumption. The DC-DC in boost mode enables a single alkaline battery to be used throughout its entire useful voltage range of 0.9 V to 1.795 V.

## 2 Ordering Information

Table 1. Orderable parts details

| Device           | Part Marking  | Memory Configuration        | Package                | Description  |
|------------------|---------------|-----------------------------|------------------------|--|
| MKW21Z512VHT4(R) | M21W9VT4      | 512 KB Flash<br>128 KB SRAM | 48-pin Laminate<br>QFN | IEEE 802.15.4  |
| MKW21Z256VHT4(R) | M21W8VT4      | 256 KB Flash<br>64 KB SRAM  |                        |  |
| MKW31Z512CAT4R   | MKW31Z512CAT4 | 512 KB Flash<br>128 KB SRAM | 75-pin WLCSP           | Bluetooth Low Energy and<br>Generic FSK                      |
| MKW31Z512VHT4(R) | M31W9VT4      | 512 KB Flash<br>128 KB SRAM | 48-pin Laminate<br>QFN | Bluetooth Low Energy and<br>Generic FSK                      |
| MKW31Z256VHT4(R) | M31W8VT4      | 256 KB Flash<br>64 KB SRAM  |                        |  |
| MKW41Z512CAT4R   | MKW41Z512CAT4 | 512 KB Flash<br>128 KB SRAM | 75-pin WLCSP           | Bluetooth Low Energy and<br>IEEE 802.15.4 and Generic<br>FSK |
| MKW41Z512VHT4(R) | M41W9VT4      | 512 KB Flash<br>128 KB SRAM | 48-pin Laminate<br>QFN | Bluetooth Low Energy and<br>IEEE 802.15.4 and Generic<br>FSK |
| MKW41Z256VHT4(R) | M41W8VT4      | 256 KB Flash<br>64 KB SRAM  |                        |  |

## 3 Feature Descriptions

This section provides a simplified block diagram and highlights the KW41Z features.

### 3.1 Block Diagram

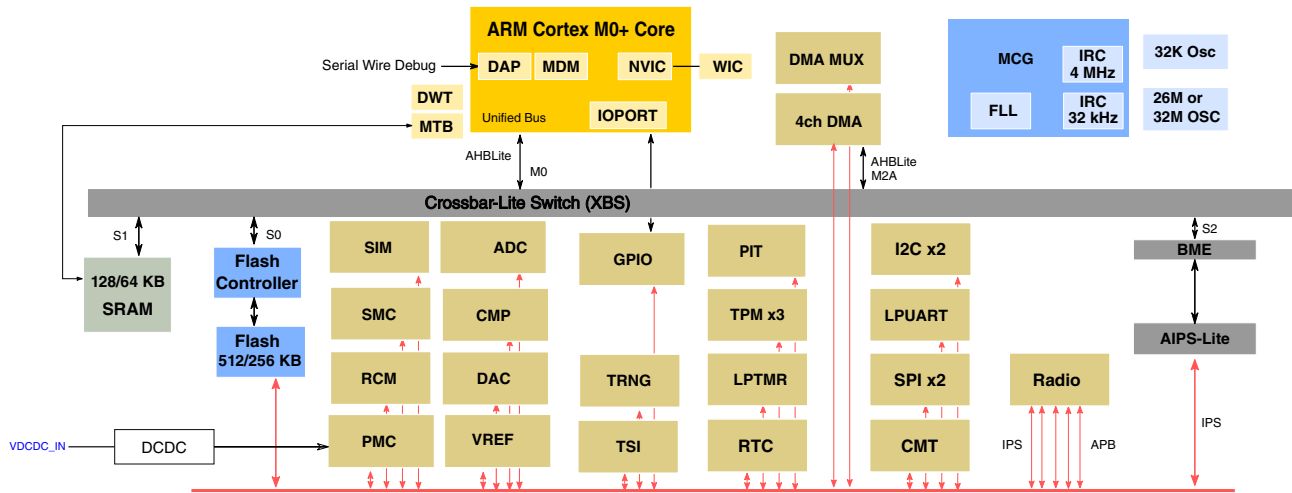


Figure 1. KW41Z Detailed Block Diagram

### 3.2 Radio features

#### Operating frequencies:

- 2.4 GHz ISM band (2400-2483.5 MHz)
- MBAN 2360-2400 MHz

#### Supported standards:

- Bluetooth v4.2 Low Energy compliant 1 Mbps GFSK modulation supporting up to 2 simultaneous connections in hardware (master-slave, master-master, slave-slave)
- IEEE Standard 802.15.4-2011 compliant O-QPSK modulation and security features
- Zigbee 3.0
- Thread Networking Stack
- Bluetooth Low Energy(BLE) Application Profiles

#### Receiver performance:

- Receive sensitivity of -95 dBm for BLE
- Receive sensitivity of -100 dBm typical for IEEE Standard 802.15.4
- Receive sensitivity of up to -100 dBm for a 250 kbps GFSK mode with a modulation index of 0.5. Receive sensitivity in generic FSK modes depends on mode selection and data rate.

#### Other features:

- Programmable transmit output power from -30 dBm to 3.5 dBm
- Integrated on-chip balun
- Single ended bidirectional RF port shared by transmit and receive
- Low external component count
- Supports transceiver range extension using external PA and/or LNA
- 26 and 32 MHz supported for BLE and FSK modes
- 32 MHz supported for IEEE Standard 802.15.4
- Bluetooth Low Energy ver. 4.2 Link Layer hardware with 2 independent hardware connection engines
- Hardware acceleration for IEEE Standard 802.15.4 packet processing/link layer
- Hardware acceleration for Generic FSK packet processing
- Supports dual PAN for IEEE Standard 802.15.4 with hardware-assisted address matching acceleration
- Generic FSK modulation at 250, 500 and 1000 kbps
- Supports antenna diversity option for IEEE Std. 802.15.4

### 3.3 Microcontroller features

#### ARM Cortex-M0+ CPU

- Up to 48 MHz CPU
- As compared to Cortex-M0, the Cortex-M0+ uses an optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Supports up to 32 interrupt request sources
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Micro Trace Buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory

#### Nested Vectored Interrupt Controller (NVIC)

- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt

#### Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes

## Feature Descriptions

- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected

## Debug Controller

- Two-wire Serial Wire Debug (SWD) interface
- Hardware breakpoint unit for 2 code addresses
- Hardware watchpoint unit for 2 data items
- Micro Trace Buffer for program tracing

## On-Chip Memory

- 512/256 KB
  - Firmware distribution protection. Program flash can be marked execute-only on a per-sector (8 KB) basis to prevent firmware contents from being read by third parties
  - Flash implemented as two equal blocks each of 256 KB block. Code can execute or read from one block while the other block is being erased or programmed.
- 128/64 KB SRAM
- Security circuitry to prevent unauthorized access to RAM and flash contents through the debugger

## 3.4 System features

### Power Management Control Unit (PMC)

- Programmable power saving modes
- Available wake-up from power saving modes via internal and external sources
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal Buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

### DC-DC Converters



- Internal switched mode power supply supporting Buck, Boost, and Bypass operating modes
- Buck operation supports external voltage sources of 2.1 V to 4.2 V. This reduces peak current consumption during Rx and Tx by ~25%, ideal for single coin-cell battery operation (typical CR2032 cell).
- Boost operation supports external voltage sources of 0.9 V to 1.795 V, which is efficiently increased to the static internal core voltage level, ideal for single battery operation (typical AA or AAA alkaline cell).
- When DC-DC is not used, the device supports an external voltage range of 1.5 V to 3.6 V (1.5 - 3.6 V on VDD\_RF1, VDD\_RF2, VDD\_XTAL and VDD\_1P5OUT\_PMCIN pins. 1.71 - 3.6 V on VDD\_0, VDD\_1 and VDDA pins)
- An external inductor is required to support the Buck or Boost modes
- The DC-DC Converter 1.8 V output current drive for external devices (MCU in RUN mode, Radio is enabled, other peripherals are disabled)
  - Up to 44 mA in buck mode with VDD\_1P8 = 1.8 V
  - Up to 31.4 mA in buck mode with VDD\_1P8 = 3.0 V

### Direct Memory Access (DMA) Controller

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses and transfer size
- Support for enhanced addressing modes
- 4-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Internal data buffer, used as temporary storage to support 16- and 32-byte transfers
- Connections to the crossbar switch for bus mastering the data movement
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- 32-byte TCD stored in local memory for each channel
- An inner data transfer loop defined by a minor byte transfer count
- An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests, one per channel
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests

## Feature Descriptions

- One interrupt per channel, optionally asserted at completion of major iteration count
- Optional error terminations per channel and logically summed together to form one error interrupt to the interrupt controller
- Optional support for scatter/gather DMA processing
- Support for complex data structures

## DMA Channel Multiplexer (DMA MUX)

- 4 independently selectable DMA channel routers
- 2 periodic trigger sources available
- Each channel router can be assigned to 1 of the peripheral DMA sources

## COP Watchdog Module

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources
  - LPO oscillator
  - Bus clock

## System Clocks

- Both 26 MHz and 32 MHz crystal reference oscillator supported for BLE and FSK radio modes
- 32 MHz crystal reference oscillator supported for IEEE 802.15.4 radio mode
- MCU can derive its clock either from the crystal reference oscillator or the frequency locked loop (FLL)<sup>1</sup>
- 32.768 kHz crystal reference oscillator used to maintain precise Bluetooth radio time in low power modes
- Multipurpose Clock Generator (MCG)
- Internal reference clocks — Can be used as a clock source for other on-chip peripherals
  - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 2% accuracy across full temperature range
  - On-chip 4MHz oscillator with 5% accuracy across full temperature range
- Frequency-locked loop (FLL) controlled by internal or external reference
  - 20 MHz to 48 MHz FLL output

## Unique Identifiers

- 10 bytes(or 80-bits) of the Unique ID represents a unique identifier for each chip
- 40 bits of unique media access control (MAC) address, which can be used to build a unique 48-bit Bluetooth-LE or 64-bit IEEE 802.15.4 device address

1. Clock options can have restrictions based on the chosen SoC configuration.

## 3.5 Peripheral features

### 16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with 16-bit resolution
- Output formatted in differential-ended 16-, 13-, 11-, and 9-bit mode
- Output formatted in single-ended 16-, 12-, 10-, and 8-bit mode
- Single or continuous conversion
- Configurable sample time and conversion speed / power
- Conversion rates in 16-bit mode with no averaging up to ~500Ksamples/sec
- Input clock selection
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater than, or equal to programmable value
- Temperature sensor
- Battery voltage measurement
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

### 12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotonicity over input word
- High- and low-speed conversions
  - 1  $\mu$ s conversion rate for high speed, 2  $\mu$ s for low speed
- Power-down mode
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth
- Automatic mode allows programmable period, update rate, and range
- DMA support with configurable watermark level

### High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output

## Feature Descriptions

- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes except VLLS0 mode

### Voltage Reference(VREF1)

- Programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset
- Programmable buffer mode selection:
  - Off
  - Bandgap enabled/standby (output buffer disabled)
  - High power buffer mode (output buffer enabled)
- 1.2 V output at room temperature
- VREF\_OUT output signal

### Low Power Timer (LPTMR)

- One channel
- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare
- Functional in all power modes

### Timer/PWM (TPM)

- TPM0: 4 channels, TPM1 and TPM2: 2 channels each
- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Generation of hardware triggers
- TPM1 and TPM2: Quadrature decoder with input filters
- Global time base mode shares single time base across multiple TPM instances

### Programmable Interrupt Timer (PIT)

- Up to 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by bus clock frequency

### **Real-Time Clock (RTC)**

- 32-bit seconds counter with 32-bit alarm
  - Can be invalidated on detection of tamper detect
- 16-bit prescaler with compensation
- Register write protection
  - Hard Lock requires MCU POR to enable write access
  - Soft lock requires POR or software reset to enable write/read access
- Capable of waking up the system from low power modes

### **Inter-Integrated Circuit (I<sup>2</sup>C)**

- Two channels
- Compatible with I2C bus standard and SMBus Specification Version 2 features
- Up to 400 kHz operation
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

### **LPUART**

- One channel
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Programmable 1 or 2 stop bits
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wakeup methods:

## Feature Descriptions

- Idle line wakeup
- Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low power modes
- Hardware Flow Control RTS\CTS
- Functional in Stop/VLPS modes

## Serial Peripheral Interface (DSPI)

- Two independent SPI channels
- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

## Carrier Modulator Timer (CMT)

- Four modes of operation
  - Time; with independent control of high and low times
  - Baseband
  - Frequency shift key (FSK)
  - Direct software control of CMT\_IRO signal
- Extended space operation in time, baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end of cycle
- Ability to disable CMT\_IRO signal and use as timer interrupt

## General Purpose Input/Output (GPIO)

- Hysteresis and configurable pull up device on all input pins
- Independent pin value register to read logic level on digital pin
- All GPIO pins can generate IRQ and wakeup events
- Configurable drive strength on some output pins

## Touch Sensor Input (TSI)

- Support up to 16 external electrodes
- Automatic detection of electrode capacitance across all operational power modes
- Internal reference oscillator for high-accuracy measurement
- Configurable software or hardware scan trigger
- Capability to wake MCU from low power modes
- Compensate for temperature and supply voltage variations
- High sensitivity change with 16-bit resolution register
- Configurable up to 4096 scan times
- Support DMA data transfer

## Keyboard Interface

- GPIO can be configured to function as a interrupt driven keyboard scanning matrix
  - In the 48-pin package there are a total of 26 digital pins
  - These pins can be configured as needed by the application as GPIO, LPUART, SPI, I2C, ADC, timer I/O as well as other functions

## 3.6 Security Features

### Advanced Encryption Standard Accelerator(AES-128 Accelerator)

The advanced encryption standard accelerator (AESA) module is a standalone hardware coprocessor capable of accelerating the 128-bit advanced encryption standard (AES) cryptographic algorithms.

The AESA engine supports the following cryptographic features.

LTC includes the following features:

- Cryptographic authentication
  - Message authentication codes (MAC)
    - Cipher-based MAC (AES-CMAC)
    - Extended cipher block chaining message authentication code (AES-XCBC-MAC)
  - Auto padding
  - Integrity Check Value(ICV) checking
- Authenticated encryption algorithms
  - Counter with CBC-MAC (AES-CCM)
  - Galois counter mode (AES-GCM)

## Feature Descriptions

- Symmetric key block ciphers
  - AES (128-bit keys)
  - Cipher modes:
    - AES-128 modes
      - Electronic codebook (ECB)
      - Cipher block chaining (CBC)
      - Counter (CTR)
    - DES modes
      - Electronic codebook (ECB)
      - Cipher block chaining (CBC)
      - Cipher feedback (CFB)
      - Output Feedback (OFB)
- Secure scan

## True Random Number Generator (TRNG)

True Random Number Generator (TRNG) is a hardware accelerator module that constitutes a high-quality entropy source.

- TRNG generates a 512-bit (4x 128-bit) entropy as needed by an entropy-consuming module, such as a deterministic random number generator.
- TRNG output can be read and used by a deterministic pseudo-random number generator (PRNG) implemented in software.
- TRNG-PRNG combination achieves NIST compliant true randomness and cryptographic-strength random numbers using the TRNG output as the entropy source.
- A fully FIPS 180 compliant solution can be realized using the TRNG together with a FIPS compliant deterministic random number generator and the SoC-level security.

## Flash Memory Protection

The on-chip flash memory controller enables the following useful features:

- Program flash protection scheme prevents accidental program or erase of stored data.
- Program flash access control scheme prevents unauthorized access to selected code segments.
- The flash can be protected from mass erase even when the MCU is not secured.
- Automated, built-in, program and erase algorithms with verify.
- Read access to one program flash block is possible while programming or erasing data in the other program flash block.



## 4 Transceiver Description

- Direct Conversion Receiver
- Constant Envelope Transmitter
- 2.36 GHz to 2.483 GHz PLL Range
- Low Transmit and Receive Current Consumption
- Low BOM

### 4.1 Key Specifications

The KW41Z SoC meets or exceeds all Bluetooth Low Energy v4.2 and IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specification for the KW41 are:

#### Frequency Band:

- ISM Band: 2400 to 2483.5MHz
- MBAN Band: 2360 to 2400MHz

#### Bluetooth Low Energy v4.2 modulation scheme:

- Symbol rate: 1000 kbps
- Modulation: GFSK
- Receiver sensitivity: -95 dBm, typical
- Programmable transmitter output power: -30 dBm to 3.5 dBm

#### IEEE Standard 802.15.4 2.4 GHz modulation scheme:

- Chip rate: 2000 kbps
- Data rate: 250 kbps
- Symbol rate: 62.5 kbps
- Modulation: OQPSK
- Receiver sensitivity: -100 dBm, typical (@1% PER for 20 byte payload packet)
- Single ended bidirectional RF input/output port with integrated transmit/receive switch
- Programmable transmitter output power: -30 dBm to 3.5 dBm

#### Generic FSK modulation scheme:

- Symbol rate: 250, 500 and 1000 kbps

## Transceiver Description

- Modulation(s): GFSK (modulation index = 0.32, 0.5, and 0.7, BT =0.5, 0.3 and 0.7), MSK
- Receiver Sensitivity: Mode and data rate dependant. -100 dBm typical for GFSK (r=250 kbps, BT = 0.5, h = 0.5)

## 4.2 Channel Map Frequency Plans

### 4.2.1 Channel Plan for Bluetooth Low Energy

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for Bluetooth Low Energy.

#### 2.4 GHz ISM Channel numbering:

- $F_c = 2402 + k * 2$  MHz,  $k=0, \dots, 39$ .

#### MBAN Channel numbering:

- $F_c = 2363 + 5 * k$  in MHz, for  $k=0, \dots, 6$
- $F_c = 2367 + 5 * (k-7)$  in MHz, for  $k=7, 8, \dots, 13$

where k is the channel number.

**Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations**

| 2.4 GHz ISM <sup>1</sup> |            | MBAN <sup>2</sup> |            | 2.4GHz ISM + MBAN |            |
|--------------------------|------------|-------------------|------------|-------------------|------------|
| Channel                  | Freq (MHz) | Channel           | Freq (MHz) | Channel           | Freq (MHz) |
| 0                        | 2402       | 0                 | 2360       | 28                | 2390       |
| 1                        | 2404       | 1                 | 2361       | 29                | 2391       |
| 2                        | 2406       | 2                 | 2362       | 30                | 2392       |
| 3                        | 2408       | 3                 | 2363       | 31                | 2393       |
| 4                        | 2410       | 4                 | 2364       | 32                | 2394       |
| 5                        | 2412       | 5                 | 2365       | 33                | 2395       |
| 6                        | 2414       | 6                 | 2366       | 34                | 2396       |
| 7                        | 2416       | 7                 | 2367       | 35                | 2397       |
| 8                        | 2418       | 8                 | 2368       | 36                | 2398       |
| 9                        | 2420       | 9                 | 2369       | 0                 | 2402       |
| 10                       | 2422       | 10                | 2370       | 1                 | 2404       |

*Table continues on the next page...*

**Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)**

| 2.4 GHz ISM <sup>1</sup> |            | MBAN <sup>2</sup> |            | 2.4GHz ISM + MBAN |            |
|--------------------------|------------|-------------------|------------|-------------------|------------|
| Channel                  | Freq (MHz) | Channel           | Freq (MHz) | Channel           | Freq (MHz) |
| 11                       | 2424       | 11                | 2371       | 2                 | 2406       |
| 12                       | 2426       | 12                | 2372       | 3                 | 2408       |
| 13                       | 2428       | 13                | 2373       | 4                 | 2410       |
| 14                       | 2430       | 14                | 2374       | 5                 | 2412       |
| 15                       | 2432       | 15                | 2375       | 6                 | 2414       |
| 16                       | 2434       | 16                | 2376       | 7                 | 2416       |
| 17                       | 2436       | 17                | 2377       | 8                 | 2418       |
| 18                       | 2438       | 18                | 2378       | 9                 | 2420       |
| 19                       | 2440       | 19                | 2379       | 10                | 2422       |
| 20                       | 2442       | 20                | 2380       | 11                | 2424       |
| 21                       | 2444       | 21                | 2381       | 12                | 2426       |
| 22                       | 2446       | 22                | 2382       | 13                | 2428       |
| 23                       | 2448       | 23                | 2383       | 14                | 2430       |
| 24                       | 2450       | 24                | 2384       | 15                | 2432       |
| 25                       | 2452       | 25                | 2385       | 16                | 2434       |
| 26                       | 2454       | 26                | 2386       | 17                | 2436       |
| 27                       | 2456       | 27                | 2387       | 18                | 2438       |
| 28                       | 2458       | 28                | 2388       | 19                | 2440       |
| 29                       | 2460       | 29                | 2389       | 20                | 2442       |
| 30                       | 2462       | 30                | 2390       | 21                | 2444       |
| 31                       | 2464       | 31                | 2391       | 22                | 2446       |
| 32                       | 2466       | 32                | 2392       | 23                | 2448       |
| 33                       | 2468       | 33                | 2393       | 24                | 2450       |
| 34                       | 2470       | 34                | 2394       | 25                | 2452       |
| 35                       | 2472       | 35                | 2395       | 26                | 2454       |
| 36                       | 2474       | 36                | 2396       | 27                | 2456       |
| 37                       | 2476       | 37                | 2397       | 37                | 2476       |
| 38                       | 2478       | 38                | 2398       | 38                | 2478       |
| 39                       | 2480       | 39                | 2399       | 39                | 2480       |

1. ISM frequency of operation spans from 2400.0 MHz to 2483.5 MHz
2. Per FCC guideline rules, IEEE (R) 802.15.1 and Bluetooth Low Energy single mode operation is allowed in these channels.

## 4.2.2 Channel Plan for IEEE 802.15.4 in 2.4GHz ISM and MBAN frequency bands

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for IEEE 802.15.4.

### 2.4GHz ISM Channel numbering:

- $F_c = 2405 + 5 \cdot (k - 11)$  MHz,  $k = 11, 12, \dots, 26$ .

### MBAN Channel numbering:

- $F_c = 2363.0 + 5 \cdot k$  in MHz, for  $k = 0, \dots, 6$
- $F_c = 2367.0 + 5 \cdot (k - 7)$  in MHz, for  $k = 7, \dots, 14$

where  $k$  is the channel number.

**Table 3. 2.4 GHz ISM and MBAN frequency plan and channel designations**

| 2.4 GHz ISM |                 | MBAN <sup>1</sup> |                 |
|-------------|-----------------|-------------------|-----------------|
| Channel #   | Frequency (MHz) | Channel #         | Frequency (MHz) |
| 11          | 2405            | 0                 | 2363            |
| 12          | 2410            | 1                 | 2368            |
| 13          | 2415            | 2                 | 2373            |
| 14          | 2420            | 3                 | 2378            |
| 15          | 2425            | 4                 | 2383            |
| 16          | 2430            | 5                 | 2388            |
| 17          | 2435            | 6                 | 2393            |
| 18          | 2440            | 7                 | 2367            |
| 19          | 2445            | 8                 | 2372            |
| 20          | 2450            | 9                 | 2377            |
| 21          | 2455            | 10                | 2382            |
| 22          | 2460            | 11                | 2387            |
| 23          | 2465            | 12                | 2392            |
| 24          | 2470            | 13                | 2397            |
| 25          | 2475            | 14                | 2395            |
| 26          | 2480            |                   |                 |

1. Usable channel spacing to assist in co-existence.

### 4.2.3 Other Channel Plans

The RF synthesizer can be configured to use any channel frequency between 2.36 and 2.487 GHz.

## 4.3 Transceiver Functions

### Receive

The receiver architecture is Zero IF (ZIF) where the received signal after passing through RF front end is down-converted to a baseband signal. The signal is filtered and amplified before it is fed to analog-to-digital converter. The digital signal is then decimated to a baseband clock frequency before it is digitally processed, demodulated and passed on to packet processing/link-layer processing.

### Transmit

The transmitter transmits O-QPSK or GFSK/FSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RF\_P, RF\_N) are converted to a single ended(SE) output signal by an on-chip balun.

## 5 Transceiver Electrical Characteristics

### 5.1 Radio operating conditions

**Table 4. Radio operating conditions**

| Characteristic            | Symbol   | Min   | Typ | Max                        | Unit |
|---------------------------|----------|-------|-----|----------------------------|------|
| Input Frequency           | $f_{in}$ | 2.360 | —   | 2.480                      | GHz  |
| Ambient Temperature Range | $T_A$    | -40   | 25  | 105                        | °C   |
| Logic Input Voltage Low   | $V_{IL}$ | 0     | —   | 30%<br>$V_{DD_{INT}}$<br>1 | V    |

*Table continues on the next page...*

**Table 4. Radio operating conditions (continued)**

| Characteristic  | Symbol    | Min                   | Typ | Max            | Unit |
|---|-----------|-----------------------|-----|----------------|------|
| Logic Input Voltage High  | $V_{IH}$  | 70%<br>$V_{DD_{INT}}$ | —   | $V_{DD_{INT}}$ | V    |
| SPI Clock Rate  | $f_{SPI}$ | —                     | —   | 12.0           | MHz  |
| RF Input Power  | $P_{max}$ | —                     | —   | 10             | dBm  |
| Crystal Reference Oscillator Frequency ( $\pm 40$ ppm over operating conditions to meet the 802.15.4 Standard.) | $f_{ref}$ | 26 MHz or 32 MHz      |     |                |      |

1.  $V_{DD_{INT}}$  is the internal LDO regulated voltage supplying various circuit blocks,  $V_{DD_{INT}}=1.2$  V

## 5.2 Receiver Feature Summary

**Table 5. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted)**

| Characteristic <sup>1</sup>  | Symbol              | Min.  | Typ. | Max.   | Unit |
|--|---------------------|-------|------|--------|------|
| Supply current power down on VDD_RFx supplies  | $I_{pdn}$           | —     | 200  | 1000   | nA   |
| Supply current Rx On with DC-DC converter enable (Buck; $V_{DD_{DCDC\_in}} = 3.6$ V) <sup>2</sup>                | $I_{Rxon}$          | —     | 6.76 | —      | mA   |
| Supply current Rx On with DC-DC converter disabled (Bypass) <sup>2</sup>   | $I_{Rxon}$          | —     | 16.2 | —      | mA   |
| Input RF Frequency   | $f_{in}$            | 2.360 | —    | 2.4835 | GHz  |
| GFSK Rx Sensitivity(250 kbps GFSK-BT=0.5, h=0.5)   | $SENS_{GFSK}$       | —     | -100 | —      | dBm  |
| BLE Rx Sensitivity <sup>3</sup>  | $SENS_{BLE}$        | —     | -95  | —      | dBm  |
| IEEE 802.15.4 Rx Sensitivity <sup>4</sup>  | $SENS_{15.4}$       | —     | -100 | —      | dBm  |
| Noise Figure for max gain mode @ typical sensitivity   | $NF_{HG}$           | —     | 7.5  | —      | dB   |
| Receiver Signal Strength Indicator Range <sup>5</sup>  | $RSSI_{Range}$      | -100  | —    | 5      | dBm  |
| Receiver Signal Strength Indicator Resolution  | $RSSI_{Res}$        | —     | 1    | —      | dBm  |
| Typical RSSI variation over frequency  |                     | -2    | —    | 2      | dB   |
| Typical RSSI variation over temperature  |                     | -2    | —    | 2      | dB   |
| Narrowband RSSI accuracy <sup>6</sup>  | $RSSI_{Acc}$        | -3    | —    | 3      | dB   |
| BLE Co-channel Interference (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz).                | $BLE_{co-channel}$  |       | -7   |        | dB   |
| IEEE 802.15.4 Co-channel Interference (Wanted signal 3 dB over reference sensitivity level)                      | $15.4_{co-channel}$ | —     | -2   | —      | dB   |
| <b>Adjacent/Alternate Channel Performance<sup>7</sup></b>  |                     |       |      |        |      |
| BLE Adjacent +/- 1 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.) | $SEL_{BLE, 1 MHz}$  | —     | 2    | —      | dB   |

Table continues on the next page...

**Table 5. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted) (continued)**

| Characteristic <sup>1</sup>   | Symbol                    | Min. | Typ. | Max. | Unit |
|---|---------------------------|------|------|------|------|
| BLE Adjacent +/- 2 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)  | SEL <sub>BLE, 2 MHz</sub> | —    | 40   | —    | dB   |
| BLE Alternate ≥ +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)   | SEL <sub>BLE, 3 MHz</sub> | —    | 50   | —    | dB   |
| IEEE 802.15.4 Adjacent +/- 5 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%)  | SEL <sub>15.4,5 MHz</sub> | —    | 45   | —    | dB   |
| IEEE 802.15.4 Alternate ≥ +/- 10 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%).   | SEL <sub>15.4,5 MHz</sub> | —    | 60   | —    | dB   |
| <b>Intermodulation Performance</b>  |                           |      |      |      |      |
| BLE Intermodulation with continuous wave interferer at ± 3MHz and modulated interferer is at ± 6MHz (Wanted signal at -67 dBm , BER<0.1%.)  |                           | —    | -42  | —    | dBm  |
| BLE Intermodulation with continuous wave interferer at ±5MHz and modulated interferer is at ±10MHz (Wanted signal at -67 dBm , BER<0.1%.)   |                           | —    | -35  | —    | dBm  |
| <b>Blocking Performance<sup>7</sup></b>   |                           |      |      |      |      |
| BLE Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.) <sup>8</sup>  | —                         | —    | -5   | —    | dBm  |
| BLE Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)  | —                         | —    | -12  | —    | dBm  |
| BLE Out of band blocking from 2001 MHz to 2339MHz and 2484 MHz to 2999 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)  | —                         | —    | -20  | —    | dBm  |
| BLE Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.) <sup>8</sup>  | —                         | —    | 0    | —    | dBm  |
| IEEE 802.15.4 Out of band blocking for frequency offsets > 10 MHz and ≤ 80 MHz(Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.) <sup>9</sup>                              |                           | —    | -36  | —    | dBm  |
| IEEE 802.15.4 Out of band blocking from carrier frequencies in 1GHz to 4GHz range excluding frequency offsets < ±80 MHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.) |                           | —    | -25  | —    | dBm  |
| IEEE 802.15.4 Out of band blocking frequency from carrier frequencies < 1 GHz and > 4 GHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.) <sup>8</sup>                  |                           | —    | -15  | —    | dBm  |

Table continues on the next page...

**Table 5. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted) (continued)**

| Characteristic <sup>1</sup>  | Symbol | Min. | Typ. | Max. | Unit |
|--|--------|------|------|------|------|
| Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency $f_c$ and spurious power measured in 1 MHz at RF frequency $f$ ), where $ f-f_c  < 1.6$ MHz               | —      | —    | -54  | —    | dBc  |
| Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency $f_c$ and spurious power measured in 1 MHz at RF frequency $f$ ), where $ f-f_c  > 2.5$ MHz <sup>10</sup> | —      | —    | -70  | —    | dBc  |

1. All the RX parameters are measured at the KW41 RF pins
2. Transceiver power consumption
3. Measured at 0.1% BER using 37 byte long packets in max gain mode and nominal conditions
4. In max gain mode and nominal conditions
5. RSSI performance in narrowband mode
6. With one point calibration over frequency and temperature
7. BLE Adjacent and Block parameters are measured with modulated interference signals
8. Exceptions allowed for carrier frequency harmonics.
9. Exception to the 10 MHz > freq offset <= 80 MHz out-of-band blocking limit allowed for frequency offsets of twice the reference frequency( $f_{ref}$ ).
10. Exceptions allowed for twice the reference clock frequency( $f_{ref}$ ) multiples.

**Table 6. Receiver Specifications with Generic FSK Modulations**

| Modulation Type       | Data Rate (kbps) | Channel BW (kHz) | Typical Sensitivity (dBm) | Adjacent/Alternate Channel Selectivity (dB) <sup>1</sup> |   |   |   |   | Co-channel |
|-----------------------|------------------|------------------|---------------------------|--|---|---|---|---|------------|
|                       |                  |                  |                           | Desired signal level (dBm)                               | Interferer at $\pm 1^*$ channel BW offset | Interferer at $\pm 2^*$ channel BW offset | Interferer at $\pm 3^*$ channel BW offset | Interferer at $\pm 4^*$ channel BW offset |            |
| GFSK BT = 0.5, h=0.5  | 1000             | 2000             | -95                       | -67  | 45  | 50  | 52  | 52  | -7         |
|                       | 500              | 1000             | -97                       | -85  | 33  | 44  | 49  | 51  | -7         |
|                       | 250              | 500              | -100                      | -85  | 20  | 33  | 42  | 46  | -7         |
| GFSK, BT = 0.5, h=0.3 | 1000             | 1000             | -89                       | -67  | 30  | 36  | 41  | 42  | -7         |
|                       | 500              | 800              | -91                       | -85  | 25  | 36  | 37  | 43  | -13        |
|                       | 250              | 500              | -93                       | -85  | 25  | 25  | 37  | 37  | -13        |
| GFSK, BT = 0.5, h=0.7 | 1000             | 2000             | -96                       | -85  | 35  | 45  | 50  | 55  | -7         |
|                       | 500              | 1000             | -98                       | -85  | 32  | 44  | 47  | 50  | -7         |
|                       | 250              | 600              | -99                       | -85  | 30  | 34  | 46  | 45  | -7         |
| GMSK BT=0.3           | 1000             | 1600             | -91                       | -85  | 35  | 40  | 45  | 50  | -8         |
|                       | 500              | 800              | -93                       | -85  | 30  | 40  | 40  | 45  | -7         |
|                       | 250              | 500              | -95                       | -85  | 20  | 32  | 32  | 40  | -7         |
| GMSK, BT = 0.7        | 1000             | 2000             | -96                       | -85  | 35  | 45  | 50  | 55  | -7         |
|                       | 500              | 1000             | -97                       | -85  | 30  | 45  | 48  | 50  | -7         |

Table continues on the next page...



**Table 6. Receiver Specifications with Generic FSK Modulations (continued)**

|                 |                  |                  |                           | Adjacent/Alternate Channel Selectivity (dB) <sup>1</sup> |                                       |  |  |  |            |
|-----------------|------------------|------------------|---------------------------|--|---------------------------------------|--|--|--|------------|
| Modulation Type | Data Rate (kbps) | Channel BW (kHz) | Typical Sensitivity (dBm) | Desired signal level (dBm)                               | Interferer at -/+1* channel BW offset | Interferer at -/+ 2* channel BW offset | Interferer at -/+ 3* channel BW offset | Interferer at -/+ 4* channel BW offset | Co-channel |
|                 | 250              | 600              | -99                       | -85  | 30                                    | 33                                     | 45                                     | 45                                     | -7         |
| Generic MSK     | 1000             | 3000             | -96                       | -85  | 39                                    | 50                                     | 58                                     | 63                                     | -7         |
|                 | 500              | 1600             | -98                       | -85  | 38                                    | 47                                     | 50                                     | 55                                     | -7         |
|                 | 250              | 800              | -99                       | -85  | 30                                    | 46                                     | 45                                     | 50                                     | -7         |

1. Selectivity measured with an unmodulated blocker

### 5.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM and 2.36 GHz MBAN frequency bands
- Fast PLL Lock time: < 25  $\mu$ s
- Reference Frequency:
  - 26 and 32 MHz supported for BLE and FSK modes
  - 32 MHz supported for IEEE Standard 802.15.4

**Table 7. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted)**

| Characteristic <sup>1</sup>  | Symbol         | Min.  | Typ.      | Max.   | Unit |
|--|----------------|-------|-----------|--------|------|
| Supply current power down on VDD_RFX supplies  | $I_{pdn}$      | —     | 200       | —      | nA   |
| Supply current Tx On with $P_{RF} = 0$ dBm and DC-DC converter enabled (Buck; $VDD_{DCDC\_in} = 3.6$ V) <sup>2</sup> | $I_{Txone}$    | —     | 6.08      | —      | mA   |
| Supply current Tx On with $P_{RF} = 0$ dBm and DC-DC converter disabled (Bypass) <sup>2</sup>                        | $I_{Txond}$    | —     | 14.7      | —      | mA   |
| Output Frequency   | $f_c$          | 2.360 | —         | 2.4835 | GHz  |
| Maximum RF Output power <sup>3</sup>   | $P_{RF,max}$   | —     | 3.5       | —      | dBm  |
| Minimum RF Output power <sup>3</sup>   | $P_{RF,min}$   | —     | -30       | —      | dBm  |
| RF Output power control range  | $P_{RF,CR}$    | —     | 34        | —      | dB   |
| IEEE 802.15.4 Peak Frequency Deviation   | $F_{dev15.4}$  | —     | $\pm 500$ | —      | kHz  |
| IEEE 802.15.4 Error Vector Magnitude <sup>4</sup>  | $EVM_{15.4}$   | —     | 4.5       | 8      | %    |
| IEEE 802.15.4 Offset Error Vector Magnitude <sup>5</sup>   | $OEVM_{15.4}$  | —     | 0.5       | 2      | %    |
| IEEE 802.15.4 TX spectrum level at 3.5MHz offset <sup>4, 6</sup>   | $TXPSD_{15.4}$ | —     | —         | -40    | dBc  |
| BLE TX Output Spectrum 20dB BW   | $TXBW_{BLE}$   | 1.0   | —         | —      | MHz  |

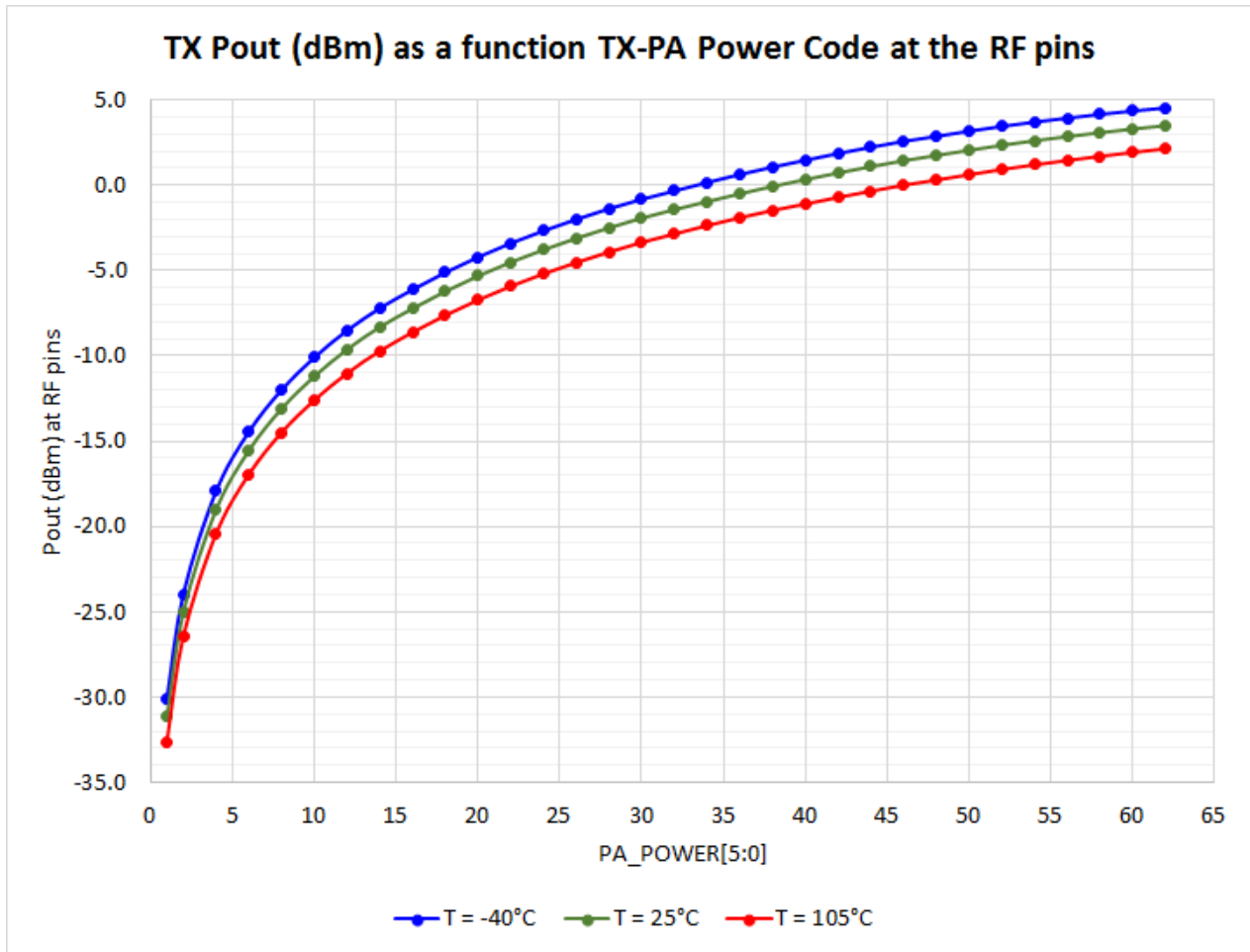
Table continues on the next page...

**Table 7. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted) (continued)**

| Characteristic <sup>1</sup>  | Symbol                 | Min. | Typ. | Max. | Unit    |
|--|------------------------|------|------|------|---------|
| BLE average frequency deviation using a 00001111 modulation sequence                 | $\Delta f_{1,avg,BLE}$ |      | 250  |      | kHz     |
| BLE average frequency deviation using a 01010101 modulation sequence                 | $\Delta f_{2,avg,BLE}$ |      | 220  |      | kHz     |
| BLE RMS FSK Error  | $FSK_{err,BLE}$        |      | 3%   |      |         |
| BLE Maximum Deviation of the Center Frequency <sup>7</sup>                           | $F_{cdev,BLE}$         | —    | ±10  | —    | kHz     |
| BLE Adjacent Channel Transmit Power at 2MHz offset <sup>6</sup>                      | $P_{RF2MHz,BLE}$       | —    | —    | -50  | dBm     |
| BLE Adjacent Channel Transmit Power at >= 3MHz offset <sup>6</sup>                   | $P_{RF3MHz,BLE}$       | —    | —    | -55  | dBm     |
| BLE Frequency Hopping Support  |                        |      | YES  |      |         |
| 2 <sup>nd</sup> Harmonic of Transmit Carrier Frequency (Pout = PRF,max) <sup>8</sup> | TXH2                   | —    | -46  | —    | dBm/MHz |
| 3 <sup>rd</sup> Harmonic of Transmit Carrier Frequency (Pout = PRF,max) <sup>8</sup> | TXH3                   | —    | -58  | —    | dBm/MHz |

1. All the TX parameters are measured at test hardware SMA connector
2. Transceiver power consumption
3. Measured at the KW41Z RF pins
4. Measured as per IEEE Standard 802.15.4
5. Offset EVM is computed at one point per symbol, by combining the I value from the beginning of each symbol and the Q value from the middle of each symbol into a single complex value for EVM computations
6. Measured at Pout = 5dBm and recommended TX match
7. Maximum drift of carrier frequency of the PLL during a BLE packet with a nominal 32MHz reference crystal
8. Harmonic Levels based on recommended 2 component match. Transmit harmonic levels depend on the tolerances and quality of the matching components.

Transmit PA driver output as a function of the PA\_POWER[5:0] field when measured at the IC pins is as follows:



**Table 8. Transmit Output Power as a function of PA\_POWER[5:0]**

| PA_POWER[5:0] | TX Pout (dBm) |           |            |
|---------------|---------------|-----------|------------|
|               | T = -40 °C    | T = 25 °C | T = 105 °C |
| 1             | -30.1         | -31.1     | -32.6      |
| 2             | -24.0         | -25.0     | -26.4      |
| 4             | -17.9         | -19.0     | -20.4      |
| 6             | -14.5         | -15.6     | -17.0      |
| 8             | -12.0         | -13.1     | -14.5      |
| 10            | -10.1         | -11.2     | -12.6      |
| 12            | -8.5          | -9.6      | -11.0      |
| 14            | -7.2          | -8.3      | -9.7       |
| 16            | -6.1          | -7.2      | -8.6       |
| 18            | -5.1          | -6.2      | -7.6       |

Table continues on the next page...

**Table 8. Transmit Output Power as a function of PA\_POWER[5:0] (continued)**

| PA_POWER[5:0] | TX Pout (dBm) |           |            |
|---------------|---------------|-----------|------------|
|               | T = -40 °C    | T = 25 °C | T = 105 °C |
| 20            | -4.2          | -5.3      | -6.7       |
| 22            | -3.4          | -4.5      | -5.9       |
| 24            | -2.7          | -3.8      | -5.2       |
| 26            | -2.0          | -3.1      | -4.5       |
| 28            | -1.4          | -2.5      | -3.9       |
| 30            | -0.8          | -1.9      | -3.3       |
| 32            | -0.3          | -1.4      | -2.8       |
| 34            | 0.2           | -1.0      | -2.4       |
| 36            | 0.6           | -0.5      | -1.9       |
| 38            | 1.1           | -0.1      | -1.5       |
| 40            | 1.5           | 0.3       | -1.1       |
| 42            | 1.9           | 0.7       | -0.7       |
| 44            | 2.2           | 1.1       | -0.3       |
| 46            | 2.6           | 1.4       | 0.0        |
| 48            | 2.9           | 1.8       | 0.3        |
| 50            | 3.2           | 2.1       | 0.6        |
| 52            | 3.5           | 2.4       | 0.9        |
| 54            | 3.7           | 2.6       | 1.2        |
| 56            | 3.9           | 2.9       | 1.5        |
| 58            | 4.2           | 3.1       | 1.7        |
| 60            | 4.4           | 3.3       | 1.9        |
| 62            | 4.5           | 3.5       | 2.1        |

## 6 System and Power Management

### 6.1 Power Management

The KW41Z includes internal power management features that can be used to control the power usage. The power management of the KW41Z includes power management controller (PMC) and a DC-DC converter which can operate in a buck, boost or bypass configuration. The PMC is designed such that the RF radio will remain in state-

retention while the core is in various stop modes. It can make sure the device can stay in low current consumption mode while the RF radio can wakeup quick enough for communication.

### 6.1.1 DC-DC Converter

The features of the DC-DC converter include the following:

- Single inductor, multiple outputs.
- Boost mode (pin selectable; CFG=GND).
- Buck mode (pin selectable; CFG=VDCDC\_IN).
- Continuous or pulsed operation (hardware/software configurable).
- Power switch input to allow external control of power up, and to select bypass mode.
- Output signal to indicate power stable. Purpose is for the rest of the chip to be used as a POR.
- Scaled battery output voltage suitable for SAR ADC utilization.
- Internal oscillator for support when the reference oscillator is not present.
- 1.8 V output is capable of supplying the external device a maximum of 38.9 mA (VDD\_1P8OUT = 1.8 V, VDCDC\_IN = 3.0 V) and 20.9 mA (VDD\_1P8OUT = 3.0 V, VDCDC\_IN = 3.0 V), with MCU in RUN mode, peripherals are disabled.

## 6.2 Modes of Operation

The ARM Cortex-M0+ core in the KW41Z has three primary modes of operation: Run, Wait, and Stop modes. For each run mode, there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes are similar to ARM deep sleep modes. The very low power run (VLPR) operation mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The WFI instruction invokes both wait and stop modes. The primary modes are augmented in a number of ways to provide lower power based on application needs.

### 6.2.1 Power modes

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes either wait or stop depending on the SLEEPDEEP bit in Cortex-M0+ System Control Register. The primary modes are augmented in a number of ways to provide lower power based on application needs.

**Table 9. Power modes (At 25 deg C)**

| Power mode   | Description   | CPU recovery method | Radio  |
|--|---|---------------------|--|
| Normal Run (all peripherals clock off)                     | Allows maximum performance of chip.   | —                   | Radio can be active  |
| Normal Wait - via WFI                                      | Allows peripherals to function, while allowing CPU to go to sleep reducing power.   | Interrupt           |  |
| Normal Stop - via WFI                                      | Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection.   | Interrupt           |  |
| PStop2 (Partial Stop 2)                                    | Core and system clocks are gated. Bus clock remains active. Masters and slaves clocked by bus clock remain in Run or VLPRun mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.   | Interrupt           |  |
| PStop1 (Partial Stop 1)                                    | Core, system clocks and bus clock are gated. All bus masters and slaves enter Stop mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.  | Interrupt           |  |
| VLPR (Very Low Power Run) (all peripherals off)            | Reduced frequency (1MHz) Flash access mode, regulator in low power mode, LVD off. Internal oscillator can provide low power 4 MHz source for core. (Values @2MHz core/ 1MHz bus and flash, module off, execution from flash).<br><br>Biasing is disabled when DC-DC is configured for continuous mode in VLPR/W | —                   | Radio operation is possible only when DC-DC is configured for continuous mode. <sup>1</sup> However, there may be insufficient MIPS with a 4MHz MCU to support much in the way of radio operation. |
| VLPW (Very Low Power Wait) - via WFI (all peripherals off) | Similar to VLPR, with CPU in sleep to further reduce power. (Values @4MHz core/ 1MHz bus, module off)<br><br>Biasing is disabled when DC-DC is configured for continuous mode in VLPR/W   | Interrupt           |  |

*Table continues on the next page...*

**Table 9. Power modes (At 25 deg C) (continued)**

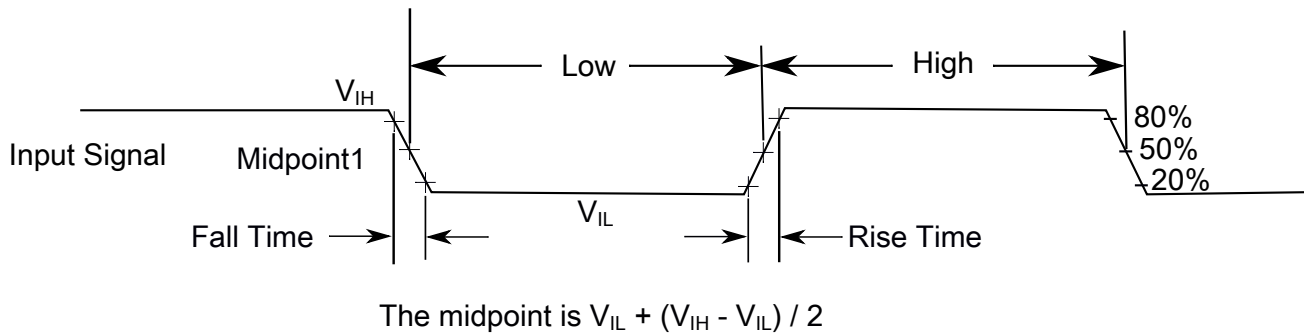
| Power mode   | Description  | CPU recovery method | Radio   |
|--|--|---------------------|---|
| VLPS (Very Low Power Stop) via WFI                         | Places MCU in static state with LVD operation off. Lowest power mode with ADC and all pin interrupts functional. LPTMR, RTC, CMP, TSI can be operational.<br><br>Biasing is disabled when DC-DC is configured for continuous mode in VLPS  | Interrupt           |   |
| LLS3 (Low Leakage Stop)                                    | State retention power mode. LLWU, LPTMR, RTC, CMP, TSI can be operational. All of the radio Sea of Gates (SOG) logic is in state retention   | Wakeup<br>Interrupt | Radio SOG is in state retention in LLSx. The BLE/802.15.4/Generic FSK DSM <sup>2</sup> logic can be active using the 32 kHz clock |
| LLS2 (Low Leakage Stop)                                    | State retention power mode. LLWU, LPTMR, RTC, CMP, TSI can be operational. 16 KB or 32 KB of programmable RAM can be powered on. All of the radio SOG logic is in state retention  | Wakeup<br>Interrupt |   |
| VLLS3 (Very Low Leakage Stop3)                             | Full SRAM retention. LLWU, LPTMR, RTC, CMP, TSI can be operational. All of the radio SOG logic is in state retention   | Wakeup<br>Reset     | Radio SOG is in state retention in VLLS3/2. The BLE/802.15.4/Generic FSK DSM logic can be active using the 32 kHz clock           |
| VLLS2 (Very Low Leakage Stop2)                             | Partial SRAM retention. 16 KB or 32 KB of programmable RAM can be powered on.. LLWU, LPTMR, RTC, CMP, TSI can be operational. All of the radio SOG logic is in state retention -   | Wakeup<br>Reset     |   |
| VLLS1 (Very Low Leakage Stop1) with RTC + 32 kHz OSC       | All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP can be operational. Radio logic is power gated.   | Wakeup<br>Reset     | Radio operation not supported. The Radio SOG is power-gated in VLLS1/0. Radio state is lost at VLLS1 and lower power states       |
| VLLS1 (Very Low Leakage Stop1) with LPTMR + LPO            | All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP, TSI can be operational.  | Wakeup<br>Reset     |   |
| VLLS0 (Very Low Leakage Stop0) with Brown-out Detection    | VLLS0 is not supported with DC-DC<br><br>The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection enabled, Pin interrupt only. Radio logic is power gated.  | Wakeup<br>Reset     | Radio operation not supported. The Radio digital is power-gated in VLLS1/0  |
| VLLS0 (Very Low Leakage Stop0) without Brown-out Detection | VLLS0 is not supported with DC-DC buck/boost configuration but is supported with bypass configuration<br><br>The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection disabled, Pin interrupt only. Radio logic is power gated. | Wakeup<br>Reset     |   |

1. Biasing is disabled, but the Flash is in a low power mode for VLPx, so this configuration can realize some power savings over use of Run/Wait/Stop
2. DSM refers to Radio's deepsleep mode. DSM does not refer to the ARM sleep deep mode.

## 7 MCU Electrical Characteristics

### 7.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



**Figure 2. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30$  pF loads
- Slew rate disabled
- Normal drive strength

### 7.2 Nonswitching electrical specifications

#### 7.2.1 Voltage and current operating requirements

**Table 10. Voltage and current operating requirements**

| Symbol             | Description                                  | Min. | Max. | Unit | Notes |
|--------------------|--|------|------|------|-------|
| $V_{DD}$           | Supply voltage                               | 1.71 | 3.6  | V    |       |
| $V_{DDA}$          | Analog supply voltage                        | 1.71 | 3.6  | V    |       |
| $V_{DD} - V_{DDA}$ | $V_{DD}$ -to- $V_{DDA}$ differential voltage | -0.1 | 0.1  | V    |       |
| $V_{SS} - V_{SSA}$ | $V_{SS}$ -to- $V_{SSA}$ differential voltage | -0.1 | 0.1  | V    |       |
| $V_{IH}$           | Input high voltage                           |      |      |      |       |

*Table continues on the next page...*



**Table 10. Voltage and current operating requirements (continued)**

| Symbol       | Description  | Min.                 | Max.                 | Unit | Notes |
|--------------|--|----------------------|----------------------|------|-------|
|              | <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>                           | $0.7 \times V_{DD}$  | —                    | V    |       |
|              |  | $0.75 \times V_{DD}$ | —                    | V    |       |
| $V_{IL}$     | Input low voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>         | —                    | $0.35 \times V_{DD}$ | V    |       |
|              |  | —                    | $0.3 \times V_{DD}$  | V    |       |
| $V_{HYS}$    | Input hysteresis   | $0.06 \times V_{DD}$ | —                    | V    |       |
| $I_{ICIO}$   | IO pin negative DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3\text{V}</math></li> </ul>  | -3                   | —                    | mA   | 1     |
| $I_{ICcont}$ | Contiguous pin DC injection current — regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> </ul> | -25                  | —                    | mA   |       |
| $V_{ODPU}$   | Open drain pullup voltage level  | $V_{DD}$             | $V_{DD}$             | V    | 2     |
| $V_{RAM}$    | $V_{DD}$ voltage required to retain RAM  | 1.2                  | —                    | V    |       |

- All I/O pins are internally clamped to  $V_{SS}$  through a ESD protection diode. There is no diode connection to  $V_{DD}$ . If  $V_{IN}$  greater than  $V_{IO\_MIN}$  ( $= V_{SS}-0.3\text{ V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (V_{IO\_MIN} - V_{IN})/|I_{ICIO}|$ .
- Open drain outputs must be pulled to  $V_{DD}$ .

## 7.2.2 LVD and POR operating requirements

**Table 11.  $V_{DD}$  supply LVD and POR operating requirements**

| Symbol      | Description   | Min. | Typ.     | Max. | Unit | Notes |
|-------------|---|------|----------|------|------|-------|
| $V_{POR}$   | Falling $V_{DD}$ POR detect voltage   | 0.8  | 1.1      | 1.5  | V    |       |
| $V_{LVDH}$  | Falling low-voltage detect threshold — high range (LVDV = 01)                 | 2.48 | 2.56     | 2.64 | V    |       |
|             | Low-voltage warning thresholds — high range                                   |      |          |      |      | 1     |
| $V_{LVW1H}$ | <ul style="list-style-type: none"> <li>Level 1 falling (LVWV = 00)</li> </ul> | 2.62 | 2.70     | 2.78 | V    |       |
| $V_{LVW2H}$ | <ul style="list-style-type: none"> <li>Level 2 falling (LVWV = 01)</li> </ul> | 2.72 | 2.80     | 2.88 | V    |       |
| $V_{LVW3H}$ | <ul style="list-style-type: none"> <li>Level 3 falling (LVWV = 10)</li> </ul> | 2.82 | 2.90     | 2.98 | V    |       |
| $V_{LVW4H}$ | <ul style="list-style-type: none"> <li>Level 4 falling (LVWV = 11)</li> </ul> | 2.92 | 3.00     | 3.08 | V    |       |
| $V_{HYSH}$  | Low-voltage inhibit reset/recover hysteresis — high range                     | —    | $\pm 60$ | —    | mV   |       |
| $V_{LVDL}$  | Falling low-voltage detect threshold — low range (LVDV=00)                    | 1.54 | 1.60     | 1.66 | V    |       |
|             | Low-voltage warning thresholds — low range                                    |      |          |      |      | 1     |

Table continues on the next page...

**Table 11.  $V_{DD}$  supply LVD and POR operating requirements (continued)**

| Symbol      | Description   | Min. | Typ. | Max. | Unit | Notes |
|-------------|---|------|------|------|------|-------|
| $V_{LVW1L}$ | <ul style="list-style-type: none"> <li>Level 1 falling (LVWV = 00)</li> </ul> | 1.74 | 1.80 | 1.86 | V    |       |
| $V_{LVW2L}$ | <ul style="list-style-type: none"> <li>Level 2 falling (LVWV = 01)</li> </ul> | 1.84 | 1.90 | 1.96 | V    |       |
| $V_{LVW3L}$ | <ul style="list-style-type: none"> <li>Level 3 falling (LVWV = 10)</li> </ul> | 1.94 | 2.00 | 2.06 | V    |       |
| $V_{LVW4L}$ | <ul style="list-style-type: none"> <li>Level 4 falling (LVWV = 11)</li> </ul> | 2.04 | 2.10 | 2.16 | V    |       |
| $V_{HYSL}$  | Low-voltage inhibit reset/recover hysteresis — low range                      | —    | ±40  | —    | mV   |       |
| $V_{BG}$    | Bandgap voltage reference   | 0.97 | 1.00 | 1.03 | V    |       |
| $t_{LPO}$   | Internal low power oscillator period — factory trimmed                        | 900  | 1000 | 1100 | μs   |       |

1. Rising thresholds are falling threshold + hysteresis voltage

## 7.2.3 Voltage and current operating behaviors

**Table 12. Voltage and current operating behaviors**

| Symbol    | Description   | Min.                             | Max.       | Unit   | Notes |
|-----------|---|----------------------------------|------------|--------|-------|
| $V_{OH}$  | Output high voltage — Normal drive pad (except RESET_b) <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -5\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -2.5\text{ mA}</math></li> </ul> | $V_{DD} - 0.5$<br>$V_{DD} - 0.5$ | —<br>—     | V<br>V | 1, 2  |
| $V_{OH}$  | Output high voltage — High drive pad (except RESET_b) <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -20\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -10\text{ mA}</math></li> </ul>   | $V_{DD} - 0.5$<br>$V_{DD} - 0.5$ | —<br>—     | V<br>V | 1, 2  |
| $I_{OHT}$ | Output high current total for all ports   | —                                | 100        | mA     |       |
| $V_{OL}$  | Output low voltage — Normal drive pad <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 5\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 2.5\text{ mA}</math></li> </ul>                     | —<br>—                           | 0.5<br>0.5 | V<br>V | 1     |
| $V_{OL}$  | Output low voltage — High drive pad <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 20\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 10\text{ mA}</math></li> </ul>                       | —<br>—                           | 0.5<br>0.5 | V<br>V | 1     |
| $I_{OLT}$ | Output low current total for all ports  | —                                | 100        | mA     |       |
| $I_{IN}$  | Input leakage current (per pin) for full temperature range  | —                                | 500        | nA     | 3     |
| $I_{IN}$  | Input leakage current (per pin) at 25 °C  | —                                | 0.025      | μA     | 3     |
| $I_{IN}$  | Input leakage current (total all pins) for full temperature range   | —                                | 5          | μA     | 3     |

Table continues on the next page...

**Table 12. Voltage and current operating behaviors (continued)**

| Symbol          | Description               | Min. | Max. | Unit | Notes |
|-----------------|---------------------------|------|------|------|-------|
| R <sub>PU</sub> | Internal pullup resistors | 20   | 50   | kΩ   | 4     |

1. PTB0-1 and PTC0-3, PTC6, PTC7, PTC17, PTC18 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull up device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V<sub>DD</sub> = 3.6 V
4. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>SS</sub>

## 7.2.4 Power mode transition operating behaviors

All specifications except t<sub>POR</sub> and VLLS<sub>x</sub>→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLS<sub>x</sub>→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

**Table 13. Power mode transition operating behaviors**

| Symbol           | Description  | Max. | Unit | Notes |
|------------------|--|------|------|-------|
| t <sub>POR</sub> | After a POR event, amount of time from the point V <sub>DD</sub> reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | 300  | μs   | 1     |
|                  | • VLLS0 → RUN  | 147  | μs   |       |
|                  | • VLLS1 → RUN  | 144  | μs   |       |
|                  | • VLLS2 → RUN  | 76   | μs   |       |
|                  | • VLLS3 → RUN  | 76   | μs   |       |
|                  | • LLS2 → RUN   | 5.8  | μs   |       |
|                  | • LLS3 → RUN   | 5.8  | μs   |       |

Table continues on the next page...

**Table 13. Power mode transition operating behaviors (continued)**

| Symbol | Description  | Max. | Unit | Notes |
|--------|--------------|------|------|-------|
|        | • VLPS → RUN | 6.2  | μs   |       |
|        | • STOP → RUN | 6.2  | μs   |       |

1. Normal boot (FTFA\_FOFT[LPBOOT]=11). When the DC-DC converter is in bypass mode, TPOR will not meet the 300μs spec when 1) VDD\_1P5 < 1.6V at 25°C and °C. 2) 1.5V ≤ VDD\_1P5 ≤ 1.8V. For the bypass mode special case where VDD\_1P5 = VDD\_1P8, TPOR did not meet the 300μs maximum spec when the supply slew rate ≤ 100V/s.

## 7.2.5 Power consumption operating behaviors

**Table 14. Power consumption operating behaviors - Bypass Mode**

| Symbol                    | Description   | Typ. | Max.     | Unit | Notes |
|---------------------------|---|------|----------|------|-------|
| I <sub>DDA</sub>          | Analog supply current   | —    | See note | mA   | 1     |
| I <sub>DD_RUNCO_CM</sub>  | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus disabled, LPTMR running using LPO clock at 1kHz, CoreMark benchmark code executing from flash at 3.0 V                                       | 7.79 | 8.64     | mA   | 2     |
| I <sub>DD_RUNCO</sub>     | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V  | 4.6  | 5.45     | mA   | 3     |
| I <sub>DD_RUN</sub>       | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V  | 5.6  | 6.45     | mA   | 3     |
| I <sub>DD_RUN</sub>       | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V   |      |          |      | 3, 4  |
|                           | at 25 °C  | 6.9  | 7.2      | mA   |       |
|                           | at 85 °C  | 7.2  | 8        | mA   |       |
|                           | at 105 °C   | 7.7  | 8.5      | mA   |       |
| I <sub>DD_WAIT</sub>      | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V   | 4.2  | 5.05     | mA   | 3     |
| I <sub>DD_WAIT</sub>      | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V   | 3.5  | 4.35     | mA   | 3     |
| I <sub>DD_PSTOP2</sub>    | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V  | 2.7  | 3.55     | mA   | 3     |
| I <sub>DD_VLPRCO_CM</sub> | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running using LPO clock at 1 kHz reference clock, CoreMark benchmark code executing from flash at 3.0 V | 760  | 960      | μA   | 5     |

Table continues on the next page...

**Table 14. Power consumption operating behaviors - Bypass Mode (continued)**

| Symbol                 | Description  | Typ.  | Max.  | Unit | Notes |
|------------------------|--|-------|-------|------|-------|
| I <sub>DD_VLPRCO</sub> | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V  | 157   | 357   | μA   | 6     |
| I <sub>DD_VLPR</sub>   | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V    | 195   | 395   | μA   | 6     |
| I <sub>DD_VLPR</sub>   | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V     | 250   | 450   | μA   | 4, 6  |
| I <sub>DD_VLPW</sub>   | Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 142   | 342   | μA   | 6     |
| I <sub>DD_STOP</sub>   | Stop mode current at 3.0 V   |       |       |      |       |
|                        | at 25 °C   | 0.204 | 0.294 | mA   |       |
|                        | at 70 °C   | 0.275 | 0.692 | mA   |       |
|                        | at 85 °C   | 0.434 | 0.716 | mA   |       |
|                        | at 105 °C  | 0.561 | 1.3   | mA   |       |
| I <sub>DD_VLPS</sub>   | Very-low-power stop mode current at Bypass mode(3.0 V),  |       |       |      |       |
|                        | at 25 °C   | 4.3   | 18    | μA   |       |
|                        | at 70 °C   | 17    | 42    | μA   |       |
|                        | at 85 °C   | 86.2  | 166   | μA   |       |
|                        | at 105 °C  | 157   | 328   | μA   |       |
| I <sub>DD_LLS3</sub>   | Low-leakage stop mode 3 current at Bypass mode(3.0 V),   |       |       |      |       |
|                        | at 25 °C   | 2.7   | 5     | μA   |       |
|                        | at 70 °C   | 9     | 16.5  | μA   |       |
|                        | at 85 °C   | 36.6  | 78.1  | μA   |       |
|                        | at 105 °C  | 69    | 128   | μA   |       |
| I <sub>DD_LLS2</sub>   | Low-leakage stop mode 2 current at Bypass mode(3.0 V),   |       |       |      |       |
|                        | at 25 °C   | 2     | 3.13  | μA   |       |
|                        | at 70 °C   | 3.2   | 10.5  | μA   |       |
|                        | at 85 °C   | 20.8  | 45.6  | μA   |       |
|                        | at 105 °C  | 39    | 65.5  | μA   |       |
| I <sub>DD_VLLS3</sub>  | Very-low-leakage stop mode 3 current at Bypass mode(3.0 V),  |       |       |      |       |
|                        | at 25 °C   | 2.3   | 4     | μA   |       |
|                        | at 70 °C   | 15    | 28.5  | μA   |       |
|                        | at 85 °C   | 31.8  | 69.3  | μA   |       |

Table continues on the next page...

**Table 14. Power consumption operating behaviors - Bypass Mode (continued)**

| Symbol                | Description  | Typ.                        | Max.                         | Unit                 | Notes |
|-----------------------|--|-----------------------------|------------------------------|----------------------|-------|
|                       | at 105 °C  | 58                          | 108                          | µA                   |       |
| I <sub>DD_VLLS2</sub> | Very-low-leakage stop mode 2 current at Bypass mode(3.0 V),<br>at 25 °C<br>at 70 °C<br>at 85 °C<br>at 105 °C             | 1.5<br>6.3<br>14.5<br>27    | 2.21<br>11.8<br>33.5<br>42.6 | µA<br>µA<br>µA<br>µA |       |
| I <sub>DD_VLLS1</sub> | Very-low-leakage stop mode 1 current at Bypass mode(3.0 V),<br>at 25°C<br>at 70°C<br>at 85°C<br>at 105°C                 | 0.56<br>3<br>8.8<br>16.8    | 1.3<br>9.4<br>23.2<br>27.1   | µA<br>µA<br>µA<br>µA |       |
| I <sub>DD_VLLS0</sub> | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V<br>at 25 °C<br>at 70 °C<br>at 85 °C<br>at 105 °C | 0.36<br>2.7<br>7.4<br>16.5  | 0.949<br>8.2<br>14.3<br>27   | µA<br>µA<br>µA<br>µA |       |
| I <sub>DD_VLLS0</sub> | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V<br>at 25 °C<br>at 70 °C<br>at 85 °C<br>at 105 °C | 0.182<br>2.5<br>7.2<br>16.3 | 0.765<br>6.7<br>13.3<br>26   | µA<br>µA<br>µA<br>µA | 7     |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode. CoreMark benchmark compiled using IAR 7.70 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 7.70 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout

**Table 15. Power consumption operating behaviors - Buck Mode**

| Symbol           | Description           | Typ. | Max.     | Unit | Notes |
|------------------|-----------------------|------|----------|------|-------|
| I <sub>DDA</sub> | Analog supply current | —    | See note | mA   | 1     |

Table continues on the next page...

**Table 15. Power consumption operating behaviors - Buck Mode (continued)**

| Symbol                 | Description  | Typ.   | Max.   | Unit | Notes |
|------------------------|--|--------|--------|------|-------|
| I <sub>DD_RUNCO</sub>  | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V                 | 3.1    | —      | mA   | 2     |
| I <sub>DD_RUN</sub>    | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V                   | 3.85   | —      | mA   | 2     |
| I <sub>DD_RUN</sub>    | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V                    |        |        |      | 2, 3  |
|                        | at 25 °C   | 4.8    | —      | mA   |       |
|                        | at 85 °C   | 5.3    | —      | mA   |       |
|                        | at 105 °C  | 5.7    | —      | mA   |       |
| I <sub>DD_WAIT</sub>   | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V                | 3.1    | —      | mA   | 2     |
| I <sub>DD_WAIT</sub>   | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V                | 2.9    | —      | mA   | 2     |
| I <sub>DD_PSTOP2</sub> | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V   | 1.9    | —      | mA   | 2     |
| I <sub>DD_VLPRCO</sub> | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V  | 137    | —      | μA   | 4     |
| I <sub>DD_VLPR</sub>   | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V    | 154    | —      | μA   | -1    |
| I <sub>DD_VLPR</sub>   | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V     | 216    | —      | μA   | 3, 4  |
| I <sub>DD_VLPW</sub>   | Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 131    | —      | μA   | 4     |
| I <sub>DD_STOP</sub>   | Stop mode current at 3.0 V   |        |        |      |       |
|                        | at 25 °C   | 1.61   | 2.32   | mA   |       |
|                        | at 70 °C   | 1.73   | 4.35   | mA   |       |
|                        | at 105 °C  | 2.02   | 4.68   | mA   |       |
| I <sub>DD_VLPS</sub>   | Very-low-power stop mode current at Buck mode(3.0 V),  |        |        |      |       |
|                        | at 25 °C   | 3.58   | 14.98  | μA   |       |
|                        | at 70 °C   | 15.08  | 37.27  | μA   |       |
|                        | at 105 °C  | 116.94 | 244.30 | μA   |       |
| I <sub>DD_LLS3</sub>   | Low-leakage stop mode 3 current at Buck mode(3.0 V),   |        |        |      |       |

Table continues on the next page...

**Table 15. Power consumption operating behaviors - Buck Mode (continued)**

| Symbol                | Description   | Typ.  | Max.  | Unit | Notes |
|-----------------------|---|-------|-------|------|-------|
|                       | at 25 °C  | 2.20  | 4.08  | μA   |       |
|                       | at 70 °C  | 7.44  | 13.63 | μA   |       |
|                       | at 105 °C   | 48.78 | 90.49 | μA   |       |
| I <sub>DD_LLS2</sub>  | Low-leakage stop mode 2 current at Buck mode(3.0 V),      |       |       |      |       |
|                       | at 25 °C  | 1.86  | 2.91  | μA   |       |
|                       | at 70 °C  | 3.19  | 10.48 | μA   |       |
|                       | at 105 °C   | 31.44 | 52.80 | μA   |       |
| I <sub>DD_VLLS3</sub> | Very-low-leakage stop mode 3 current at Buck mode(3.0 V), |       |       |      |       |
|                       | at 25 °C  | 1.79  | 3.12  | μA   |       |
|                       | at 70 °C  | 12    | 22.8  | μA   |       |
|                       | at 105 °C   | 37.49 | 69.81 | μA   |       |
| I <sub>DD_VLLS2</sub> | Very-low-leakage stop mode 2 current at Buck mode(3.0 V), |       |       |      |       |
|                       | at 25 °C  | 1.09  | 1.60  | μA   |       |
|                       | at 70 °C  | 5.56  | 10.40 | μA   |       |
|                       | at 105 °C   | 18.71 | 29.52 | μA   |       |
| I <sub>DD_VLLS1</sub> | Very-low-leakage stop mode 1 current at Buck mode(3.0 V), |       |       |      |       |
|                       | at 25 °C  | 0.46  | 1.07  | μA   |       |
|                       | at 70 °C  | 2.17  | 6.8   | μA   |       |
|                       | at 105 °C   | 14.08 | 22.71 | μA   |       |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode.
3. Incremental current consumption from peripheral activity is not included.
4. MCG configured for BLPI mode.

**Table 16. Power consumption operating behaviors - Boost Mode**

| Symbol                | Description  | Typ. | Max.     | Unit | Notes |
|-----------------------|--|------|----------|------|-------|
| I <sub>DDA</sub>      | Analog supply current  | —    | See note | mA   | 1     |
| I <sub>DD_RUNCO</sub> | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 1.3 V | 8.1  | —        | mA   | 2     |
| I <sub>DD_RUN</sub>   | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 1.3 V   | 9.76 | —        | mA   | 2     |
| I <sub>DD_RUN</sub>   | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 1.3 V    |      |          |      | 2, 3  |

Table continues on the next page...



**Table 16. Power consumption operating behaviors - Boost Mode (continued)**

| Symbol                 | Description  | Typ.    | Max.    | Unit | Notes |
|------------------------|--|---------|---------|------|-------|
|                        | at 25 °C   | 13.2    | —       | mA   |       |
|                        | at 85 °C   | 14.1    | —       | mA   |       |
|                        | at 105 °C  | 15.2    | —       | mA   |       |
| I <sub>DD_WAIT</sub>   | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 1.3 V                | 6.9     | —       | mA   | 2     |
| I <sub>DD_WAIT</sub>   | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 1.3 V                | 5.8     | —       | mA   | 2     |
| I <sub>DD_PSTOP2</sub> | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 1.3 V   | 8.3     | —       | mA   | 2     |
| I <sub>DD_VLPRCO</sub> | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 1.3 V  | 378     | —       | μA   | 4     |
| I <sub>DD_VLPR</sub>   | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 1.3 V    | 476     | —       | μA   | 4     |
| I <sub>DD_VLPR</sub>   | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 1.3 V     | 606     | —       | μA   | 3, 4  |
| I <sub>DD_VLPW</sub>   | Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 1.3 V | 357     | —       | μA   | 4     |
| I <sub>DD_STOP</sub>   | Stop mode current at 1.3 V   |         |         |      |       |
|                        | at 25 °C   | 3.22    | 4.64    | mA   |       |
|                        | at 70 °C   | 3.56    | 8.96    | mA   |       |
|                        | at 105 °C  | 3.74    | 9.73    | mA   |       |
| I <sub>DD_VLPS</sub>   | Very-low-power stop mode current at Boost mode(1.3 V),   |         |         |      |       |
|                        | at 25 °C   | 29.89   | 125.13  | μA   |       |
|                        | at 70 °C   | 191.62  | 473.41  | μA   |       |
|                        | at 105 °C  | 1429.24 | 2985.93 | μA   |       |
| I <sub>DD_LLS3</sub>   | Low-leakage stop mode 3 current at Boost mode(1.3 V),  |         |         |      |       |
|                        | at 25 °C   | 12.16   | 22.53   | μA   |       |
|                        | at 70 °C   | 84.61   | 155.12  | μA   |       |
|                        | at 105 °C  | 534.09  | 990.79  | μA   |       |
| I <sub>DD_LLS2</sub>   | Low-leakage stop mode 2 current at Boost mode(1.3 V),  |         |         |      |       |
|                        | at 25 °C   | 12.05   | 18.86   | μA   |       |
|                        | at 70 °C   | 17.36   | 56.96   | μA   |       |

Table continues on the next page...

**Table 16. Power consumption operating behaviors - Boost Mode (continued)**

| Symbol                | Description  | Typ.   | Max.   | Unit | Notes |
|-----------------------|--|--------|--------|------|-------|
|                       | at 105 °C  | 221.29 | 371.66 | µA   |       |
| I <sub>DD_VLLS3</sub> | Very-low-leakage stop mode 3 current at Boost mode(1.3 V), |        |        |      |       |
|                       | at 25 °C   | 7.99   | 13.89  | µA   |       |
|                       | at 70 °C   | 88.4   | 167.96 | µA   |       |
|                       | at 105 °C  | 287.14 | 534.67 | µA   |       |
| I <sub>DD_VLLS2</sub> | Very-low-leakage stop mode 2 current at Boost mode(1.3 V), |        |        |      |       |
|                       | at 25 °C   | 7.09   | 10.45  | µA   |       |
|                       | at 70 °C   | 23.38  | 43.79  | µA   |       |
|                       | at 105 °C  | 95.67  | 150.94 | µA   |       |
| I <sub>DD_VLLS1</sub> | Very-low-leakage stop mode 1 current at Boost mode(1.3 V), |        |        |      |       |
|                       | at 25 °C   | 3.63   | 8.44   | µA   |       |
|                       | at 70 °C   | 16.23  | 50.86  | µA   |       |
|                       | at 105 °C  | 67.77  | 109.32 | µA   |       |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode.
3. Incremental current consumption from peripheral activity is not included.
4. MCG configured for BLPI mode.

**Table 17. Low power mode peripheral adders — typical value**

| Symbol                     | Description  | Temperature (°C) |     |     |     |      | Unit |
|----------------------------|--|------------------|-----|-----|-----|------|------|
|                            |  | -40              | 25  | 50  | 70  | 85   |      |
| I <sub>IREFSTEN4MHz</sub>  | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.             | 46               | 46  | 47  | 47  | 47   | µA   |
| I <sub>IREFSTEN32KHz</sub> | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.               | 88               | 91  | 90  | 89  | 88   | µA   |
| I <sub>IREFSTEN32KHz</sub> | External 32 kHz crystal clock adder by means of the RTC bits. Measured by entering all modes with the crystal enabled. |                  |     |     |     |      |      |
|                            | VLLS1  | 1.4              | 1.3 | 1.6 | 2.4 | 4.1  | µA   |
|                            | VLLS2  | 1.6              | 1.5 | 1.9 | 4.2 | 7.7  |      |
|                            | VLLS3  | 2.7              | 1.9 | 2.9 | 7.7 | 15   |      |
|                            | LLS2   | 1.8              | 1.4 | 1.7 | 4.1 | 8    |      |
|                            | LLS3   | 2.6              | 1.7 | 2.8 | 7.6 | 15.2 |      |

Table continues on the next page...

**Table 17. Low power mode peripheral adders — typical value (continued)**

| Symbol              | Description  | Temperature (°C) |     |     |     |     | Unit |
|---------------------|--|------------------|-----|-----|-----|-----|------|
|                     |  | -40              | 25  | 50  | 70  | 85  |      |
| I <sub>CMP</sub>    | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.  | 22               | 19  | 20  | 21  | 21  | μA   |
| I <sub>RTC</sub>    | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.   | 1.4              | 1.3 | 1.6 | 2.4 | 4.3 | μA   |
| I <sub>LPUART</sub> | LPUART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.  |                  |     |     |     |     |      |
|                     | MCGIRCLK (4 MHz internal reference clock)  | 53               | 54  | 54  | 54  | 54  | μA   |
| I <sub>LPTMR</sub>  | LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.  |                  |     |     |     |     |      |
|                     |  | 30               | 30  | 30  | 85  | 100 | nA   |
| I <sub>TPM</sub>    | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. |                  |     |     |     |     |      |
|                     | MCGIRCLK (4 MHz internal reference clock)  | 58               | 59  | 59  | 59  | 59  | μA   |
| I <sub>BG</sub>     | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.   | 76               | 82  | 85  | 87  | 87  | μA   |
| I <sub>ADC</sub>    | ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>DDA</sub> by placing the device in STOP or VLPS mode. ADC is configured for low-power mode using the internal clock and continuous conversions.   | 331              | 327 | 327 | 327 | 328 | μA   |

### 7.2.6 Diagram: Typical IDD\_RUN operating behavior

The following data was measured from previous devices with same MCU core (ARM® Cortex-M0+) under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

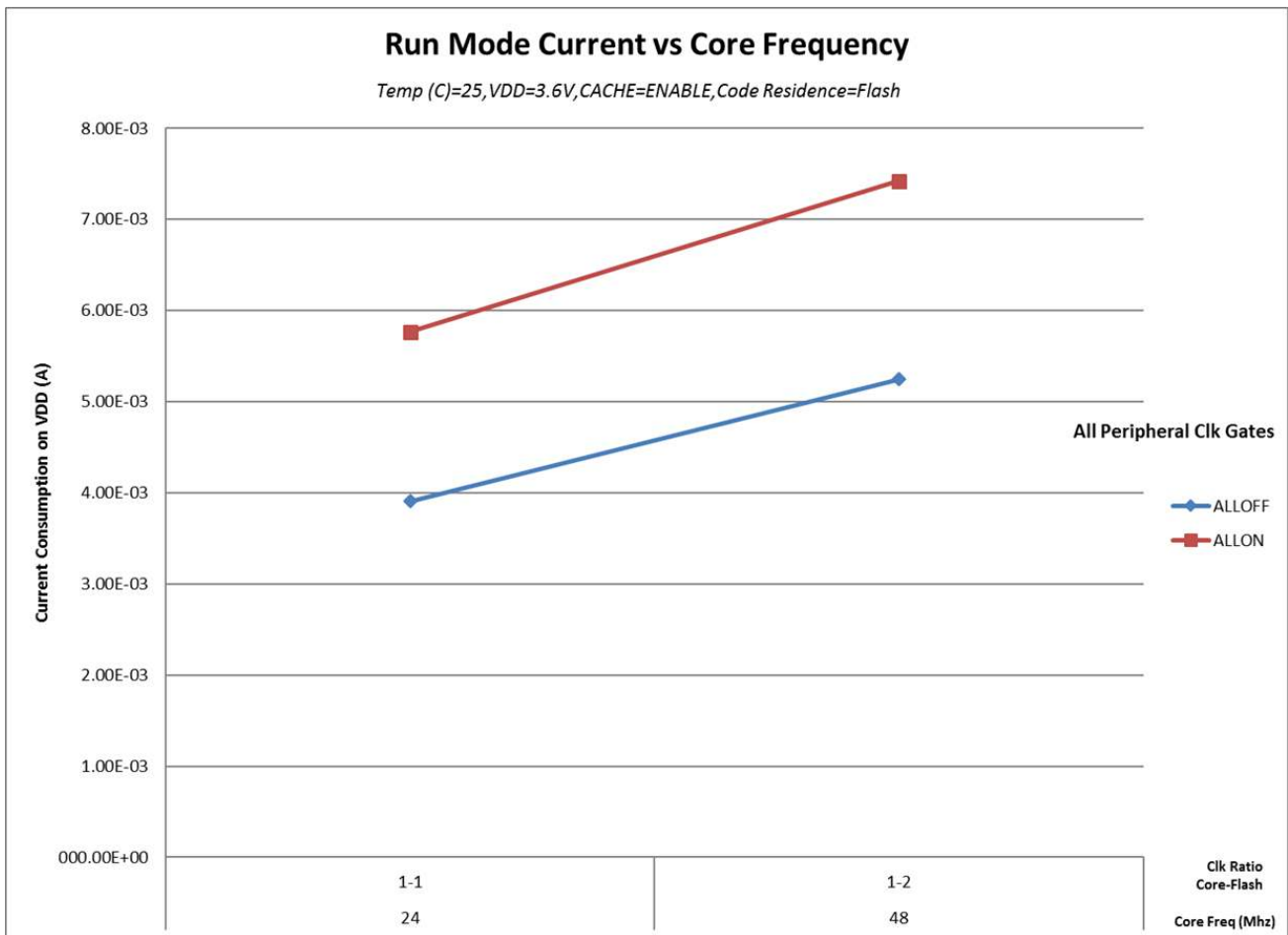


Figure 3. Run mode supply current vs. core frequency

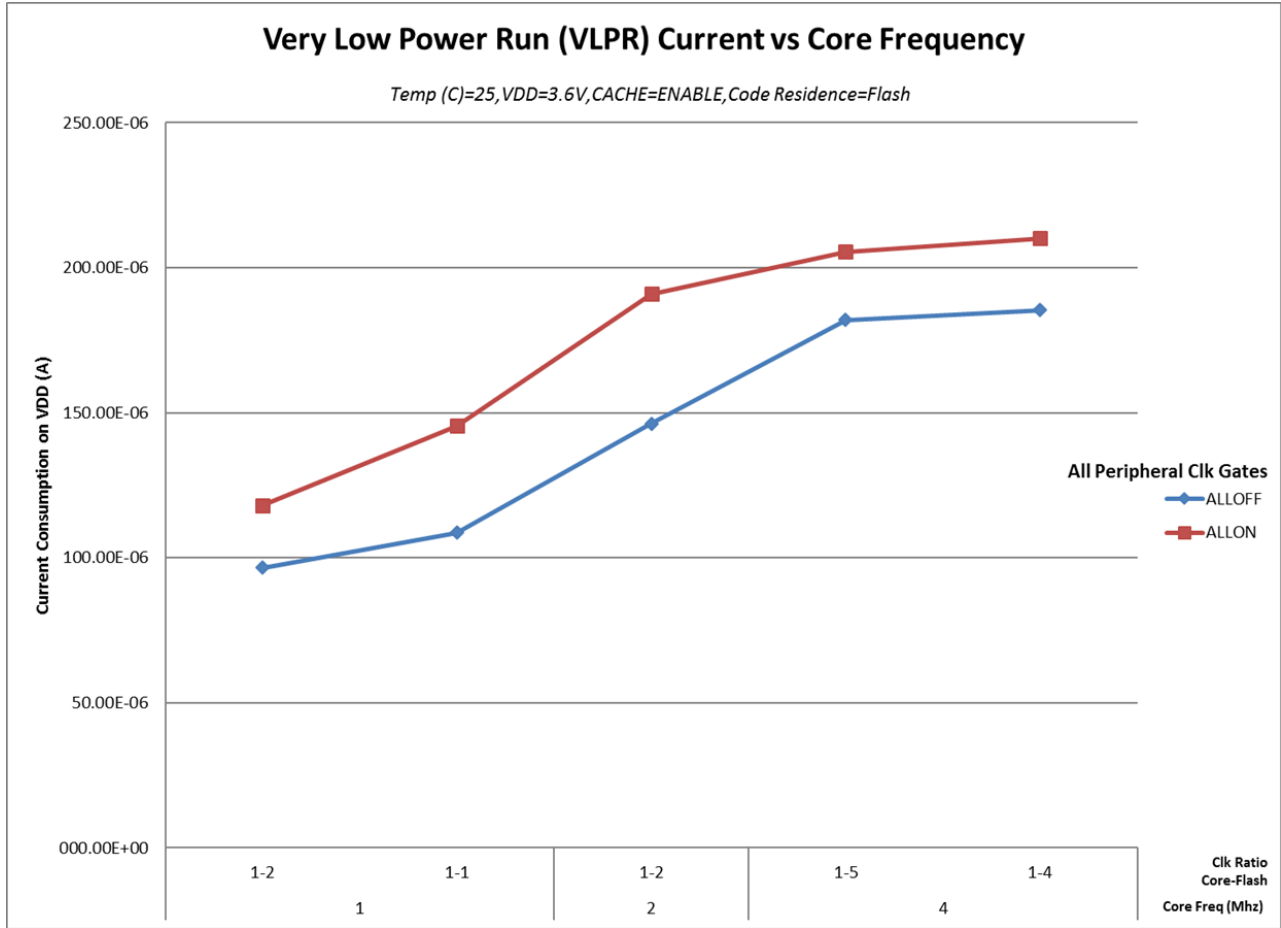


Figure 4. VLPR mode current vs. core frequency

### 7.2.7 SoC Power Consumption

Full KW41Z/31Z/21Z system-on-chip (SoC) power consumption is a function of the many configurations possible for the MCU platform and its peripherals including the 2.4GHz radio and the DC-DC converter. A few measured SoC configurations are as follows:

Table 18. SoC Power Consumption

| MCU State | Flash State | Radio State  | DCDC State                          | Typical Average IC current | Unit |
|-----------|-------------|--------------|-------------------------------------|----------------------------|------|
| STOP      | Doze        | Rx           | Buck(VDD <sub>DCDC_in</sub> =3.6 V) | 8.4                        | mA   |
| STOP      | Doze        | Tx(at 0 dBm) | Buck(VDD <sub>DCDC_in</sub> =3.6 V) | 7.6                        | mA   |
| RUN       | Enabled     | Rx           | Buck(VDD <sub>DCDC_in</sub> =3.6 V) | 10.2                       | mA   |

Table continues on the next page...

**Table 18. SoC Power Consumption (continued)**

| MCU State | Flash State | Radio State  | DCDC State                          | Typical Average IC current | Unit |
|-----------|-------------|--------------|-------------------------------------|----------------------------|------|
| RUN       | Enabled     | Tx(at 0 dBm) | Buck(VDD <sub>DCDC_in</sub> =3.6 V) | 9.6                        | mA   |
| STOP      | Doze        | Rx           | Disabled/Bypass                     | 16.6                       | mA   |
| STOP      | Doze        | Tx(at 0 dBm) | Disabled/Bypass                     | 15.2                       | mA   |
| RUN       | Enabled     | Rx           | Disabled/Bypass                     | 19.7                       | mA   |
| RUN       | Enabled     | Tx(at 0 dBm) | Disabled/Bypass                     | 19.2                       | mA   |

### 7.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.nxp.com](http://www.nxp.com)
2. Perform a keyword search for “EMC design.”

### 7.2.9 Capacitance attributes

**Table 19. Capacitance attributes**

| Symbol          | Description       | Min. | Max. | Unit |
|-----------------|-------------------|------|------|------|
| C <sub>IN</sub> | Input capacitance | —    | 7    | pF   |

## 7.3 Switching electrical specifications

### 7.3.1 Device clock specifications

**Table 20. Device clock specifications**

| Symbol             | Description           | Min. | Max. | Unit |
|--------------------|-----------------------|------|------|------|
| Normal run mode    |                       |      |      |      |
| f <sub>SYS</sub>   | System and core clock | —    | 48   | MHz  |
| f <sub>BUS</sub>   | Bus clock             | —    | 24   | MHz  |
| f <sub>FLASH</sub> | Flash clock           | —    | 24   | MHz  |

*Table continues on the next page...*

**Table 20. Device clock specifications (continued)**

| Symbol                           | Description                    | Min. | Max. | Unit |
|----------------------------------|--------------------------------|------|------|------|
| f <sub>LPTMR</sub>               | LPTMR clock                    | —    | 24   | MHz  |
| VLPR and VLPS modes <sup>1</sup> |                                |      |      |      |
| f <sub>SYS</sub>                 | System and core clock          | —    | 4    | MHz  |
| f <sub>BUS</sub>                 | Bus clock                      | —    | 1    | MHz  |
| f <sub>FLASH</sub>               | Flash clock                    | —    | 1    | MHz  |
| f <sub>LPTMR</sub>               | LPTMR clock <sup>2</sup>       | —    | 24   | MHz  |
| f <sub>ERCLK</sub>               | External reference clock       | —    | 16   | MHz  |
| f <sub>LPTMR_ERCLK</sub>         | LPTMR external reference clock | —    | 16   | MHz  |
| f <sub>TPM</sub>                 | TPM asynchronous clock         | —    | 8    | MHz  |
| f <sub>LPUART0</sub>             | LPUART0 asynchronous clock     | —    | 12   | MHz  |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

### 7.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, CMT and I<sup>2</sup>C signals.

**Table 21. General switching specifications**

| Description  | Min. | Max. | Unit             | Notes |
|--|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path   | 1.5  | —    | Bus clock cycles | 1, 2  |
| NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path  | 200  | —    | ns               | 3     |
| GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path  | 20   | —    | ns               | 3     |
| External RESET_b input pulse width (digital glitch filter disabled)  | 100  | —    | ns               |       |
| Port rise and fall time(high drive strength) <ul style="list-style-type: none"> <li>• Slew enabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq VDD \leq 2.7 \text{ V}</math></li> <li>• <math>2.7 \leq VDD \leq 3.6 \text{ V}</math></li> </ul> </li> <li>• Slew disabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq VDD \leq 2.7 \text{ V}</math></li> <li>• <math>2.7 \leq VDD \leq 3.6 \text{ V}</math></li> </ul> </li> </ul> | —    | 25   | ns               | 4, 5  |
|  | —    | 16   | ns               |       |
|  | —    | 8    | ns               |       |
|  | —    | 6    | ns               |       |
| Port rise and fall time(low drive strength) <ul style="list-style-type: none"> <li>• Slew enabled</li> </ul>   |      |      |                  | 6, 7  |

**Table 21. General switching specifications**

| Description  | Min. | Max. | Unit | Notes |
|--|------|------|------|-------|
| <ul style="list-style-type: none"> <li>• <math>1.71 \leq VDD \leq 2.7 V</math></li> <li>• <math>2.7 \leq VDD \leq 3.6 V</math></li> </ul>                          | —    | 24   | ns   |       |
| <ul style="list-style-type: none"> <li>• Slew disabled</li> <li>• <math>1.71 \leq VDD \leq 2.7 V</math></li> <li>• <math>2.7 \leq VDD \leq 3.6 V</math></li> </ul> | —    | 16   | ns   |       |
|  | —    | 10   | ns   |       |
|  | —    | 6    | ns   |       |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater of synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized.
4. PTB0, PTB1, PTC0, PTC1, PTC2, PTC3, PTC6, PTC7, PTC17, PTC18.
5. 75 pF load.
6. Ports A, B, and C.
7. 25 pF load.

## 7.4 Thermal specifications

### 7.4.1 Thermal operating requirements

**Table 22. Thermal operating requirements**

| Symbol | Description   | Min. | Max. | Unit | Notes |
|--------|---|------|------|------|-------|
| $T_J$  | Die junction temperature <ul style="list-style-type: none"> <li>• For Laminate QFN package</li> </ul> | -40  | 125  | °C   |       |
| $T_J$  | Die junction temperature <ul style="list-style-type: none"> <li>• For WLCSP package</li> </ul>        | -40  | 95   | °C   |       |
| $T_A$  | Ambient temperature <ul style="list-style-type: none"> <li>• For Laminate QFN package</li> </ul>      | -40  | 105  | °C   | 1     |
| $T_A$  | Ambient temperature <ul style="list-style-type: none"> <li>• For WLCSP package</li> </ul>             | -40  | 85   | °C   | 1     |

1. Maximum  $T_A$  can be exceeded only if the user ensures that  $T_J$  does not exceed the maximum. The simplest method to determine  $T_J$  is:  $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$ .



## 7.4.2 Thermal attributes

**Table 23. Thermal attributes**

| Board type        | Symbol               | Description  | 48-pin Laminate QFN | 75-pin WLCSP | Unit | Notes |
|-------------------|----------------------|--|---------------------|--------------|------|-------|
| Single-layer (1S) | $R_{\theta JA}$      | Thermal resistance, junction to ambient (natural convection)                                       | 59.3                | 106.7        | °C/W | 2, 1  |
| Four-layer (2s2p) | $R_{\theta JA}$      | Thermal resistance, junction to ambient (natural convection)                                       | 42.9                | 57.2         | °C/W | 2, 1  |
| Single-layer (1S) | $R_{\theta JMA}$     | Thermal resistance, junction to ambient (200 ft./min. air speed)                                   | 51.6                | 88.0         | °C/W | 2, 1  |
| Four-layer (2s2p) | $R_{\theta JMA}$     | Thermal resistance, junction to ambient (200 ft./min. air speed)                                   | 38.9                | 51.7         | °C/W | 2, 1  |
| —                 | $R_{\theta JB}$      | Thermal resistance, junction to board  | 37.7                | 24.7         | °C/W | 3     |
| —                 | $R_{\theta JC}$      | Thermal resistance, junction to case   | 0.48                | 4.3          | °C/W | 4     |
| —                 | $\Psi_{JT}$          | Thermal characterization parameter, junction to package top outside center (natural convection)    | 0.2                 | 0.2          | °C/W | 5     |
| —                 | $R_{\theta JB\_CSB}$ | Thermal characterization parameter, junction to package bottom outside center (natural convection) | —                   | 13.7         | °C/W | 6     |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
4. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
5. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
6. Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

## 7.5 Peripheral operating requirements and behaviors

### 7.5.1 Core modules

### 7.5.1.1 SWD electricals

Table 24. SWD full voltage range electricals

| Symbol | Description  | Min. | Max. | Unit |
|--------|--|------|------|------|
|        | Operating voltage  | 1.71 | 3.6  | V    |
| J1     | SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul> | 0    | 25   | MHz  |
| J2     | SWD_CLK cycle period   | 1/J1 | —    | ns   |
| J3     | SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>      | 20   | —    | ns   |
| J4     | SWD_CLK rise and fall times  | —    | 3    | ns   |
| J9     | SWD_DIO input data setup time to SWD_CLK rise  | 10   | —    | ns   |
| J10    | SWD_DIO input data hold time after SWD_CLK rise  | 0    | —    | ns   |
| J11    | SWD_CLK high to SWD_DIO data valid   | —    | 32   | ns   |
| J12    | SWD_CLK high to SWD_DIO high-Z   | 5    | —    | ns   |

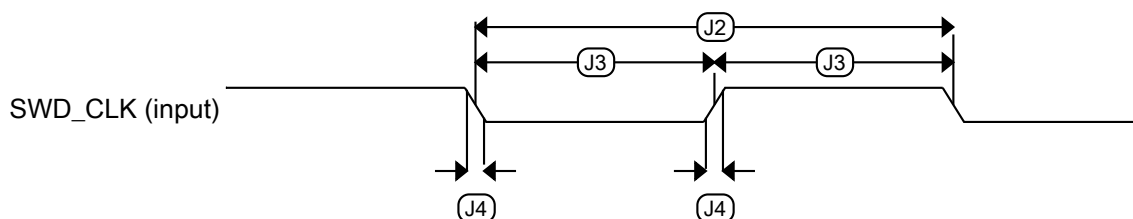


Figure 5. Serial wire clock input timing

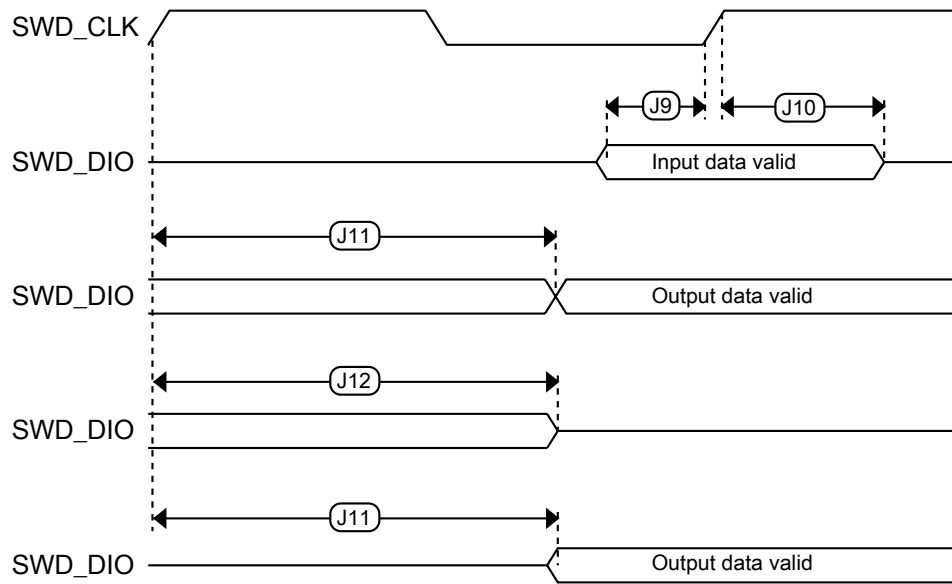


Figure 6. Serial wire data timing

## 7.5.2 System modules

There are no specifications necessary for the device's system modules.

## 7.5.3 Clock modules

### 7.5.3.1 MCG specifications

Table 25. MCG specifications

| Symbol                   | Description  | Min.  | Typ.      | Max.    | Unit        | Notes |
|--------------------------|--|-------|-----------|---------|-------------|-------|
| $f_{ints\_ft}$           | Internal reference frequency (slow clock) — factory trimmed at nominal $V_{DD}$ and 25 °C                              | —     | 32.768    | —       | kHz         |       |
| $f_{ints\_t}$            | Internal reference frequency (slow clock) — user trimmed   | 31.25 | —         | 39.0625 | kHz         |       |
| $\Delta f_{dco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM] | —     | ± 0.3     | ± 0.6   | % $f_{dco}$ | 1     |
| $\Delta f_{dco\_t}$      | Total deviation of trimmed average DCO output frequency over voltage and temperature                                   | —     | +0.5/-0.7 | ± 3     | % $f_{dco}$ | 1, 2  |

Table continues on the next page...

**Table 25. MCG specifications (continued)**

| Symbol                | Description   | Min.   | Typ.  | Max.    | Unit             | Notes |      |
|-----------------------|---|--|-------|---------|------------------|-------|------|
| $\Delta f_{dco\_t}$   | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C                               | —  | ± 0.4 | ± 1.5   | % $f_{dco}$      | 1, 2  |      |
| $f_{intf\_ft}$        | Internal reference frequency (fast clock) — factory trimmed at nominal $V_{DD}$ and 25 °C   | —  | 4     | —       | MHz              |       |      |
| $\Delta f_{intf\_ft}$ | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal $V_{DD}$ and 25 °C | —  | +1/-2 | ± 3     | % $f_{intf\_ft}$ | 2     |      |
| $f_{intf\_t}$         | Internal reference frequency (fast clock) — user trimmed at nominal $V_{DD}$ and 25 °C  | 3  | —     | 5       | MHz              |       |      |
| $f_{loc\_low}$        | Loss of external clock minimum frequency — RANGE = 00   | $(3/5) \times f_{ints\_t}$                         | —     | —       | kHz              |       |      |
| $f_{loc\_high}$       | Loss of external clock minimum frequency — RANGE = 01, 10, or 11  | $(16/5) \times f_{ints\_t}$                        | —     | —       | kHz              |       |      |
| FLL                   |   |  |       |         |                  |       |      |
| $f_{fil\_ref}$        | FLL reference frequency range   | 31.25  | —     | 39.0625 | kHz              |       |      |
| $f_{dco}$             | DCO output frequency range  | Low range (DRS = 00)<br>$640 \times f_{fil\_ref}$  | 20    | 20.97   | 25               | MHz   | 3, 4 |
|                       |   | Mid range (DRS = 01)<br>$1280 \times f_{fil\_ref}$ | 40    | 41.94   | 48               | MHz   |      |
| $f_{dco\_t\_DMX32}$   | DCO output frequency  | Low range (DRS = 00)<br>$732 \times f_{fil\_ref}$  | —     | 23.99   | —                | MHz   | 5, 6 |
|                       |   | Mid range (DRS = 01)<br>$1464 \times f_{fil\_ref}$ | —     | 47.97   | —                | MHz   |      |
| $J_{cyc\_fil}$        | FLL period jitter<br>• $f_{VCO} = 48$ MHz   | —  | 180   | —       | ps               | 7     |      |
| $t_{fil\_acquire}$    | FLL target frequency acquisition time   | —  | —     | 1       | ms               | 8     |      |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal  $V_{DD}$  and 25 °C,  $f_{ints\_ft}$ .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

### 7.5.3.2 Reference Oscillator Specification

The KW41Z has been designed to meet targeted specifications with a +/-20 ppm frequency error over the life of the part, which includes the temperature, mechanical and aging excursions.

The table below shows the recommended crystal specifications. Note that these are recommendations only and deviation may be allowed. However, deviations may result in degraded RF performance or possibly a failure to meet RF protocol certification standards. Designers should do due diligence to ensure that the crystal(s) they use will meet the requirements of their application.

**Table 26. Recommended Crystal Specification**

| Symbol           | Description   | Comment  | 32M   |      |       | 26M   |      |       | Unit         |
|------------------|---|--|-------|------|-------|-------|------|-------|--------------|
|                  |   |  | Min   | Typ  | Max   | Min   | Typ  | Max   |              |
|                  | Operating Temperature                                       |  | -40   |      | 105   | -40   |      | 105   | °C           |
| Faging           | Frequency accuracy over aging                               | 1st year   | -5    |      | 5     | -5    |      | 5     | ppm - 1st yr |
| iFac             | Initial Frequency accuracy                                  | with respect to XO                                       | -10   |      | 10    | -10   |      | 10    | ppm          |
| Fstab            | Frequency stability   | across temperature, mechanical, load and voltage changes | -10   |      | 10    | -10   |      | 10    | ppm          |
| CL               | Values of CL supported (Integrated on die and programmable) |  | 7     | 10   | 13    | 7     | 10   | 13    | pF           |
| Co               | Shunt parasitic capacitance                                 |  | 0.469 | 0.67 | 0.871 | 0.42  | 0.6  | 0.78  | pF           |
| Cm1              | Motional capacitance Cm1                                    |  | 1.435 | 2.05 | 2.665 | 1.435 | 2.05 | 2.665 | fF           |
| Lm1              | Motional inductance Lm1                                     |  | 8.47  | 12.1 | 15.73 | 12.81 | 18.3 | 23.79 | mH           |
| TS               | Trim Sensitivity (TS) for the supported [Co,CL] values      |  | 6.30  | 9.00 | 11.70 | 6.39  | 9.12 | 11.86 | ppm/pF       |
| T <sub>osc</sub> | Oscillator Startup Time                                     |  | —     | 680  | —     | —     | 680  | —     | μs           |
| Rm1              | ESR: Maximum value of Rm1                                   |  |       | 25   | 60    |       | 35   | 60    | Ohms         |
|                  | Maximum crystal drive level limit                           |  |       |      | 200   |       |      | 200   | μW           |

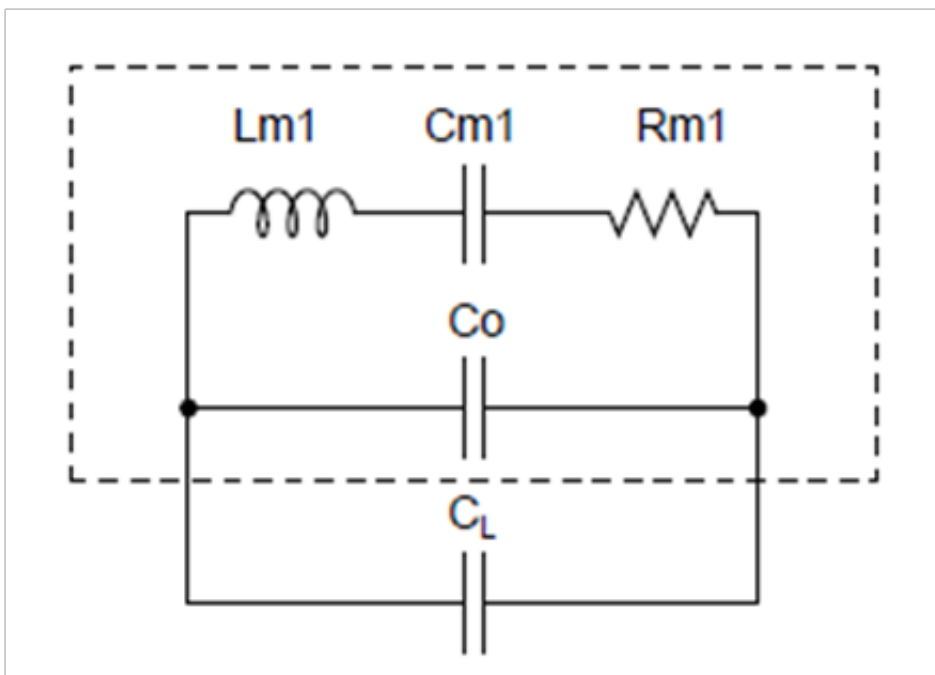


Figure 7. Crystal Electrical Block Diagram

### 7.5.3.3 32 kHz Oscillator Frequency Specifications

Table 27. 32 kHz oscillator frequency specifications

| Symbol            | Description                               | Min. | Typ.   | Max.     | Unit | Notes |
|-------------------|---|------|--------|----------|------|-------|
| $f_{osc\_lo}$     | Oscillator crystal                        | —    | 32.768 | —        | kHz  |       |
| $t_{start}$       | Crystal start-up time                     | —    | 1000   | —        | ms   | 1     |
| $f_{ec\_extal32}$ | Externally provided input clock frequency | —    | 32.678 | —        | kHz  | 2     |
| $V_{ec\_extal32}$ | Externally provided input clock amplitude | 700  | —      | $V_{DD}$ | mV   | 2, 3  |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and  $V_{IH}$  and  $V_{IL}$  specifications do not apply. The voltage of the applied clock must be within the range of  $V_{SS}$  to  $V_{DD}$ .

### 7.5.4 Memories and memory interfaces

### 7.5.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 7.5.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 28. NVM program/erase timing specifications**

| Symbol             | Description                              | Min. | Typ. | Max. | Unit    | Notes |
|--------------------|--|------|------|------|---------|-------|
| $t_{hvp4}$         | Longword Program high-voltage time       | —    | 7.5  | 18   | $\mu$ s | —     |
| $t_{hversscr}$     | Sector Erase high-voltage time           | —    | 13   | 113  | ms      | 1     |
| $t_{hversblk256k}$ | Erase Block high-voltage time for 256 KB | —    | 104  | 904  | ms      | 1     |

1. Maximum time based on expectations at cycling end-of-life.

#### 7.5.4.1.2 Flash timing specifications — commands

**Table 29. Flash command timing specifications**

| Symbol           | Description  | Min. | Typ. | Max. | Unit    | Notes |
|------------------|--|------|------|------|---------|-------|
| $t_{rd1blk256k}$ | Read 1s Block execution time<br>• 256 KB program flash     | —    | —    | 1.7  | ms      | 1     |
| $t_{rd1sec2k}$   | Read 1s Section execution time (flash sector)              | —    | —    | 60   | $\mu$ s | 1     |
| $t_{pgmchk}$     | Program Check execution time                               | —    | —    | 45   | $\mu$ s | 1     |
| $t_{rdsrc}$      | Read Resource execution time                               | —    | —    | 30   | $\mu$ s | 1     |
| $t_{pgm4}$       | Program Longword execution time                            | —    | 65   | 145  | $\mu$ s | —     |
| $t_{ersblk256k}$ | Erase Flash Block execution time<br>• 256 KB program flash | —    | 250  | 1500 | ms      | 2     |
| $t_{ersscr}$     | Erase Flash Sector execution time                          | —    | 14   | 114  | ms      | 2     |
| $t_{rd1all}$     | Read 1s All Blocks execution time                          | —    | —    | 1.8  | ms      | 1     |
| $t_{rdonce}$     | Read Once execution time                                   | —    | —    | 30   | $\mu$ s | 1     |
| $t_{pgmonce}$    | Program Once execution time                                | —    | 100  | —    | $\mu$ s | —     |
| $t_{ersall}$     | Erase All Blocks execution time                            | —    | 500  | 3000 | ms      | 2     |
| $t_{vfykey}$     | Verify Backdoor Access Key execution time                  | —    | —    | 30   | $\mu$ s | 1     |
| $t_{ersallu}$    | Erase All Blocks Unsecure execution time                   | —    | 500  | 3000 | ms      | 2     |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 7.5.4.1.3 Flash high voltage current behaviors

Table 30. Flash high voltage current behaviors

| Symbol              | Description   | Min. | Typ. | Max. | Unit |
|---------------------|---|------|------|------|------|
| I <sub>DD_PGM</sub> | Average current adder during high voltage flash programming operation | —    | 2.5  | 6.0  | mA   |
| I <sub>DD_ERS</sub> | Average current adder during high voltage flash erase operation       | —    | 1.5  | 4.0  | mA   |

### 7.5.4.1.4 Reliability specifications

Table 31. NVM reliability specifications

| Symbol                  | Description                            | Min. | Typ. <sup>1</sup> | Max. | Unit   | Notes |
|-------------------------|--|------|-------------------|------|--------|-------|
| Program Flash           |  |      |                   |      |        |       |
| t <sub>nvmretp10k</sub> | Data retention after up to 10 K cycles | 5    | 50                | —    | years  | —     |
| t <sub>nvmretp1k</sub>  | Data retention after up to 1 K cycles  | 20   | 100               | —    | years  | —     |
| n <sub>nvmcycp</sub>    | Cycling endurance                      | 10 K | 50 K              | —    | cycles | 2     |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T<sub>j</sub> ≤ 125 °C.

## 7.5.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 7.5.6 Analog

### 7.5.6.1 ADC electrical specifications

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications. The following specification is defined with the DC-DC converter operating in Bypass mode.

#### 7.5.6.1.1 16-bit ADC operating conditions

Table 32. 16-bit ADC operating conditions

| Symbol           | Description    | Conditions | Min. | Typ. <sup>1</sup> | Max. | Unit | Notes |
|------------------|----------------|------------|------|-------------------|------|------|-------|
| V <sub>DDA</sub> | Supply voltage | Absolute   | 1.71 | —                 | 3.6  | V    |       |

Table continues on the next page...



**Table 32. 16-bit ADC operating conditions (continued)**

| Symbol           | Description                         | Conditions   | Min.                   | Typ. <sup>1</sup> | Max.                                  | Unit       | Notes |
|------------------|-------------------------------------|--|------------------------|-------------------|---------------------------------------|------------|-------|
| $\Delta V_{DDA}$ | Supply voltage                      | Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ )   | -100                   | 0                 | +100                                  | mV         | 2     |
| $\Delta V_{SSA}$ | Ground voltage                      | Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ )   | -100                   | 0                 | +100                                  | mV         | 2     |
| $V_{REFH}$       | ADC reference voltage high          |  | 1.13                   | $V_{DDA}$         | $V_{DDA}$                             | V          | 3     |
| $V_{REFL}$       | ADC reference voltage low           |  | $V_{SSA}$              | $V_{SSA}$         | $V_{SSA}$                             | V          | 3     |
| $V_{ADIN}$       | Input voltage                       | <ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>            | $V_{SSA}$<br>$V_{SSA}$ | —<br>—            | $31/32 \times V_{REFH}$<br>$V_{REFH}$ | V          |       |
| $C_{ADIN}$       | Input capacitance                   | <ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>           | —<br>—                 | 8<br>4            | 10<br>5                               | pF         |       |
| $R_{ADIN}$       | Input series resistance             |  | —                      | 2                 | 5                                     | k $\Omega$ |       |
| $R_{AS}$         | Analog source resistance (external) | 13-bit / 12-bit modes<br>$f_{ADCK} < 4$ MHz  | —                      | —                 | 5                                     | k $\Omega$ | 4     |
| $f_{ADCK}$       | ADC conversion clock frequency      | $\leq$ 13-bit mode   | 1.0                    | —                 | 18.0                                  | MHz        | 5     |
| $f_{ADCK}$       | ADC conversion clock frequency      | 16-bit mode  | 2.0                    | —                 | 12.0                                  | MHz        | 5     |
| $C_{rate}$       | ADC conversion rate                 | $\leq$ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000                 | —                 | 818.330                               | kS/s       | 6     |
| $C_{rate}$       | ADC conversion rate                 | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time         | 37.037                 | —                 | 461.467                               | kS/s       | 6     |

1. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated  $V_{REFH}$  and  $V_{REFL}$  pins,  $V_{REFH}$  is internally tied to  $V_{DDA}$ , and  $V_{REFL}$  is internally tied to  $V_{SSA}$ .
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had  $< 8 \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $< 1$  ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

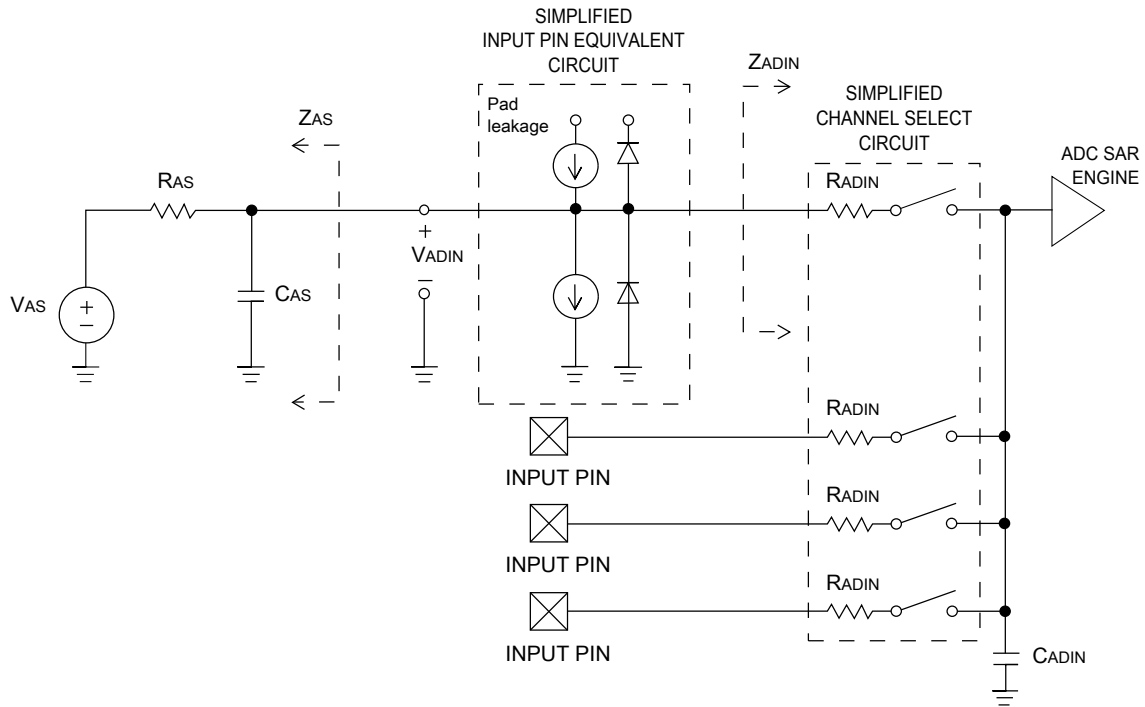


Figure 8. ADC input impedance equivalency diagram

7.5.6.1.2 16-bit ADC electrical characteristics

Table 33. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

| Symbol         | Description                   | Conditions <sup>1</sup>   | Min.  | Typ. <sup>2</sup> | Max.         | Unit             | Notes                     |
|----------------|-------------------------------|---|-------|-------------------|--------------|------------------|---------------------------|
| $I_{DDA\_ADC}$ | Supply current                |   | 0.215 | —                 | 1.7          | mA               | 3                         |
| $f_{ADACK}$    | ADC asynchronous clock source | <ul style="list-style-type: none"> <li>ADLPC=1, ADHSC=0</li> <li>ADLPC=1, ADHSC=1</li> <li>ADLPC=0, ADHSC=0</li> <li>ADLPC=0, ADHSC=1</li> </ul>                    | 1.2   | 2.4               | 3.9          | MHz              | $t_{ADACK} = 1/f_{ADACK}$ |
|                | Sample Time                   | See Reference Manual chapter for sample times   |       |                   |              |                  |                           |
| TUE            | Total unadjusted error        | <ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>  | —     | ±4                | ±6.8         | LSB <sup>4</sup> | 5                         |
| DNL            | Differential non-linearity    | <ul style="list-style-type: none"> <li>12-bit mode; Buck Mode<sup>6</sup></li> <li>12-bit mode; Boost Mode<sup>6</sup></li> <li>12-bit mode; Bypass Mode</li> </ul> | —     | ±0.7              | -1.1 to +1.9 | LSB <sup>4</sup> | 5                         |

Table continues on the next page...

**Table 33. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

| Symbol                                | Description                     | Conditions <sup>1</sup>                           | Min.               | Typ. <sup>2</sup> | Max.         | Unit             | Notes                             |
|---------------------------------------|---------------------------------|---|--------------------|-------------------|--------------|------------------|-----------------------------------|
| INL                                   | Integral non-linearity          | • 12-bit mode; Buck Mode <sup>6</sup>             | —                  | ±1.0              | -2.7 to +1.9 | LSB <sup>4</sup> | 5                                 |
|                                       |                                 | • 12-bit mode; Boost Mode <sup>6</sup>            | —                  | ±0.7              | -2.7 to +1.9 |                  |                                   |
|                                       |                                 | • 12-bit mode; Bypass Mode                        | —                  | ±0.6              | -2.7 to +1.9 |                  |                                   |
| E <sub>FS</sub>                       | Full-scale error                | • 12-bit modes                                    | —                  | -4                | -5.4         | LSB <sup>4</sup> | $V_{ADIN} = V_{DDA}$ <sup>5</sup> |
|                                       |                                 | • <12-bit modes                                   | —                  | -1.4              | -1.8         |                  |                                   |
| E <sub>Q</sub>                        | Quantization error              | • 16-bit modes                                    | —                  | -1 to 0           | —            | LSB <sup>4</sup> |                                   |
|                                       |                                 | • ≤13-bit modes                                   | —                  | —                 | ±0.5         |                  |                                   |
| ENOB                                  | Effective number of bits        | 16-bit differential mode; Buck Mode <sup>6</sup>  |                    |                   |              | bits             | 7                                 |
|                                       |                                 | • Avg = 32  | 12                 | 12.75             | —            |                  |                                   |
|                                       |                                 | • Avg = 4   | 11.25              | 11.75             | —            |                  |                                   |
|                                       |                                 | 16-bit single-ended mode; Buck Mode <sup>6</sup>  |                    |                   |              |                  |                                   |
|                                       |                                 | • Avg = 32  | 11                 | 11.5              | —            |                  |                                   |
|                                       |                                 | • Avg = 4   | 9.5                | 10.5              | —            |                  |                                   |
|                                       |                                 | 16-bit differential mode; Boost Mode <sup>6</sup> |                    |                   |              |                  |                                   |
|                                       |                                 | • Avg = 32  | 11.5               | 12                | —            |                  |                                   |
|                                       |                                 | • Avg = 4   | 9.75               | 11                | —            |                  |                                   |
|                                       |                                 | 16-bit single-ended mode; Boost Mode <sup>6</sup> |                    |                   |              |                  |                                   |
| • Avg = 32                            | 11                              | 11.5  | —                  |                   |              |                  |                                   |
| • Avg = 4                             | 9.75                            | 10.5  | —                  |                   |              |                  |                                   |
| 16-bit differential mode; Bypass Mode |                                 |   |                    |                   |              |                  |                                   |
| • Avg = 32                            | 12.5                            | 13  | —                  |                   |              |                  |                                   |
| • Avg = 4                             | 11.25                           | 12  | —                  |                   |              |                  |                                   |
| 16-bit single-ended mode; Bypass Mode |                                 |   |                    |                   |              |                  |                                   |
| • Avg = 32                            | 11                              | 11.75   | —                  |                   |              |                  |                                   |
| • Avg = 4                             | 10                              | 10.5  | —                  |                   |              |                  |                                   |
| SINAD                                 | Signal-to-noise plus distortion | See ENOB  | 6.02 × ENOB + 1.76 |                   |              | dB               |                                   |
| THD                                   | Total harmonic distortion       | 16-bit differential mode; Buck Mode <sup>6</sup>  |                    |                   |              |                  | 8                                 |
|                                       |                                 | • Avg = 32  | —                  | -90               | —            | dB               |                                   |

Table continues on the next page...

**Table 33. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

| Symbol          | Description                                  | Conditions <sup>1</sup>  | Min.                   | Typ. <sup>2</sup> | Max. | Unit | Notes                            |
|-----------------|--|--|------------------------|-------------------|------|------|----------------------------------|
|                 |  | 16-bit single-ended mode;<br>Buck Mode <sup>6</sup><br>• Avg = 32  | —                      | -88               | —    |      |                                  |
|                 |  | 16-bit differential mode; Boost<br>Mode <sup>6</sup><br>• Avg = 32 | —                      | -89               | —    |      |                                  |
|                 |  | 16-bit single-ended mode;<br>Boost Mode <sup>6</sup><br>• Avg = 32 | —                      | -89               | —    |      |                                  |
|                 |  | 16-bit differential mode;<br>Bypass Mode<br>• Avg = 32             | —                      | -89               | —    |      |                                  |
|                 |  | 16-bit single-ended mode;<br>Bypass Mode<br>• Avg = 32             | —                      | -87               | —    |      |                                  |
| SINAD           | Signal-to-noise plus<br>distortion           | See ENOB   | 6.02 × ENOB + 1.76     |                   |      | dB   |                                  |
| SFDR            | Spurious free<br>dynamic range<br>distortion | 16-bit differential mode; Buck<br>Mode <sup>6</sup><br>• Avg = 32  | 85                     | 89                | —    | dB   | 8                                |
|                 |  | 16-bit single-ended mode;<br>Buck Mode <sup>6</sup><br>• Avg = 32  | 85                     | 87                | —    |      |                                  |
|                 |  | 16-bit differential mode; Boost<br>Mode <sup>6</sup><br>• Avg = 32 | 78                     | 86                | —    |      |                                  |
|                 |  | 16-bit single-ended mode;<br>Boost Mode <sup>6</sup><br>• Avg = 32 | 85                     | 87                | —    |      |                                  |
|                 |  | 16-bit differential mode;<br>Bypass Mode<br>• Avg = 32             | 87                     | 94                | —    |      |                                  |
|                 |  | 16-bit single-ended mode;<br>Bypass Mode<br>• Avg = 32             | 85                     | 88                | —    |      |                                  |
| E <sub>IL</sub> | Input leakage error                          |  | $I_{in} \times R_{AS}$ |                   |      | mV   | $I_{in}$ =<br>leakage<br>current |

Table continues on the next page...

**Table 33. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

| Symbol       | Description         | Conditions <sup>1</sup>                         | Min. | Typ. <sup>2</sup> | Max. | Unit  | Notes                                       |
|--------------|---------------------|---|------|-------------------|------|-------|---|
|              |                     |   |      |                   |      |       | (see Voltage and current operating ratings) |
|              | Temp sensor slope   | Across the full temperature range of the device | 1.67 | 1.74              | 1.81 | mV/°C | 9   |
| $V_{TEMP25}$ | Temp sensor voltage | 25 °C   | 706  | 716               | 726  | mV    | 9   |

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$ .
2. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4.  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$ .
5. ADC conversion clock < 16 MHz, maximum hardware averaging (AVGE = %1, AVGS = %11).
6. VREFH = Output of Voltage Reference(VREF).
7. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
8. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
9. ADC conversion clock < 3 MHz.

### 7.5.6.2 Voltage reference electrical specifications

**Table 34. VREF full-range operating requirements**

| Symbol    | Description             | Min.       | Max. | Unit | Notes |
|-----------|-------------------------|------------|------|------|-------|
| $V_{DDA}$ | Supply voltage          | 1.71       | 3.6  | V    |       |
| $T_A$     | Temperature             | -40 to 105 |      | °C   |       |
| $C_L$     | Output load capacitance | 100        |      | nF   | 1, 2  |

1.  $C_L$  must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified  $C_L$  value over the operating temperature range of the device.

**Table 35. VREF full-range operating behaviors**

| Symbol     | Description  | Min.   | Typ.   | Max.   | Unit | Notes |
|------------|--|--------|--------|--------|------|-------|
| $V_{out}$  | Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25°C | 1.190  | 1.1950 | 1.2    | V    | 1     |
| $V_{out}$  | Voltage reference output with user trim at nominal $V_{DDA}$ and temperature=25°C    | 1.1945 | 1.1950 | 1.1955 | V    | 1     |
| $V_{step}$ | Voltage reference trim step  | —      | 0.5    | —      | mV   | 1     |

Table continues on the next page...

**Table 35. VREF full-range operating behaviors (continued)**

| Symbol                          | Description  | Min. | Typ. | Max. | Unit | Notes |
|---------------------------------|--|------|------|------|------|-------|
| V <sub>tdrift</sub>             | Temperature drift (V <sub>max</sub> -V <sub>min</sub> across the full temperature range) | —    | —    | 20   | mV   | 1     |
| I <sub>bg</sub>                 | Bandgap only current   | —    | —    | 80   | μA   |       |
| I <sub>lp</sub>                 | Low-power buffer current   | —    | —    | 360  | uA   | 1     |
| I <sub>hp</sub>                 | High-power buffer current  | —    | —    | 1    | mA   | 1     |
| ΔV <sub>LOAD</sub>              | Load regulation<br>• current = ± 1.0 mA  | —    | 200  | —    | μV   | 1, 2  |
| T <sub>stup</sub>               | Buffer startup time  | —    | —    | 100  | μs   |       |
| T <sub>chop_osc_st<br/>up</sub> | Internal bandgap start-up delay with chop oscillator enabled                             | —    | —    | 35   | ms   |       |
| V <sub>vdrift</sub>             | Voltage drift (V <sub>max</sub> -V <sub>min</sub> across the full voltage range)         | —    | 2    | —    | mV   | 1     |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 36. VREF limited-range operating requirements**

| Symbol         | Description | Min. | Max. | Unit | Notes |
|----------------|-------------|------|------|------|-------|
| T <sub>A</sub> | Temperature | 0    | 70   | °C   |       |

**Table 37. VREF limited-range operating behaviors**

| Symbol              | Description   | Min. | Max. | Unit | Notes |
|---------------------|---|------|------|------|-------|
| V <sub>tdrift</sub> | Temperature drift (V <sub>max</sub> -V <sub>min</sub> across the limited temperature range) | —    | 15   | mV   |       |

### 7.5.6.3 CMP and 6-bit DAC electrical specifications

**Table 38. Comparator and 6-bit DAC electrical specifications**

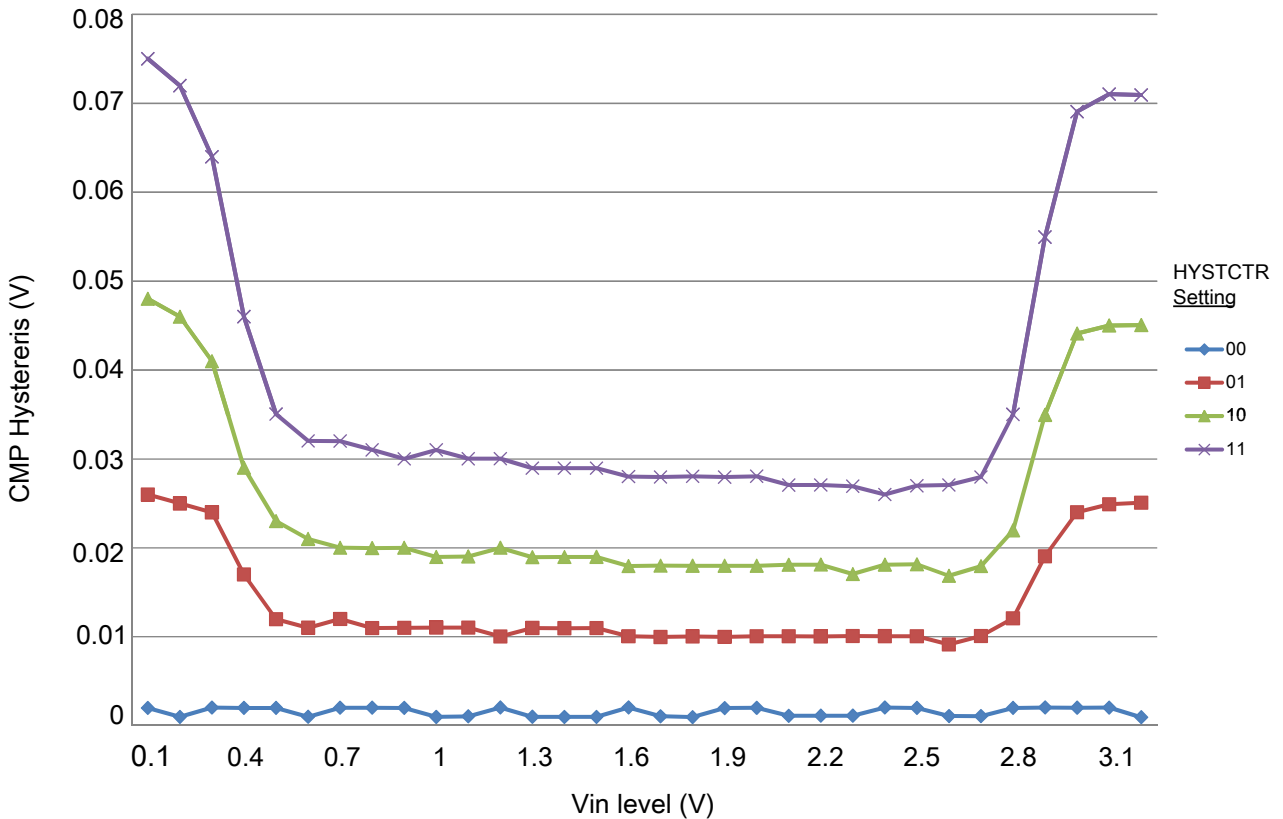
| Symbol            | Description  | Min.                  | Typ. | Max.            | Unit |
|-------------------|--|-----------------------|------|-----------------|------|
| V <sub>DD</sub>   | Supply voltage   | 1.71                  | —    | 3.6             | V    |
| I <sub>DDHS</sub> | Supply current, High-speed mode (EN=1, PMODE=1)                  | —                     | —    | 200             | μA   |
| I <sub>DDL</sub>  | Supply current, low-speed mode (EN=1, PMODE=0)                   | —                     | —    | 20              | μA   |
| V <sub>AIN</sub>  | Analog input voltage   | V <sub>SS</sub> - 0.3 | —    | V <sub>DD</sub> | V    |
| V <sub>AIO</sub>  | Analog input offset voltage                                      | —                     | —    | 20              | mV   |
| V <sub>H</sub>    | Analog comparator hysteresis <sup>1</sup><br>• CR0[HYSTCTR] = 00 | —                     | 5    | —               | mV   |

Table continues on the next page...

**Table 38. Comparator and 6-bit DAC electrical specifications (continued)**

| Symbol             | Description   | Min.                  | Typ. | Max. | Unit             |
|--------------------|---|-----------------------|------|------|------------------|
|                    | <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul> | —                     | 10   | —    | mV               |
|                    |   | —                     | 20   | —    | mV               |
|                    |   | —                     | 30   | —    | mV               |
| V <sub>CMPOh</sub> | Output high   | V <sub>DD</sub> - 0.5 | —    | —    | V                |
| V <sub>CMPOl</sub> | Output low  | —                     | —    | 0.5  | V                |
| t <sub>DHS</sub>   | Propagation delay, high-speed mode (EN=1, PMODE=1)  | 20                    | 50   | 200  | ns               |
| t <sub>DLS</sub>   | Propagation delay, low-speed mode (EN=1, PMODE=0)   | 80                    | 250  | 600  | ns               |
|                    | Analog comparator initialization delay <sup>2</sup>   | —                     | —    | 40   | μs               |
| I <sub>DAC6b</sub> | 6-bit DAC current adder (enabled)   | —                     | 7    | —    | μA               |
| INL                | 6-bit DAC integral non-linearity  | -0.5                  | —    | 0.5  | LSB <sup>3</sup> |
| DNL                | 6-bit DAC differential non-linearity  | -0.3                  | —    | 0.3  | LSB              |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V<sub>DD</sub>-0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = V<sub>reference</sub>/64



**Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

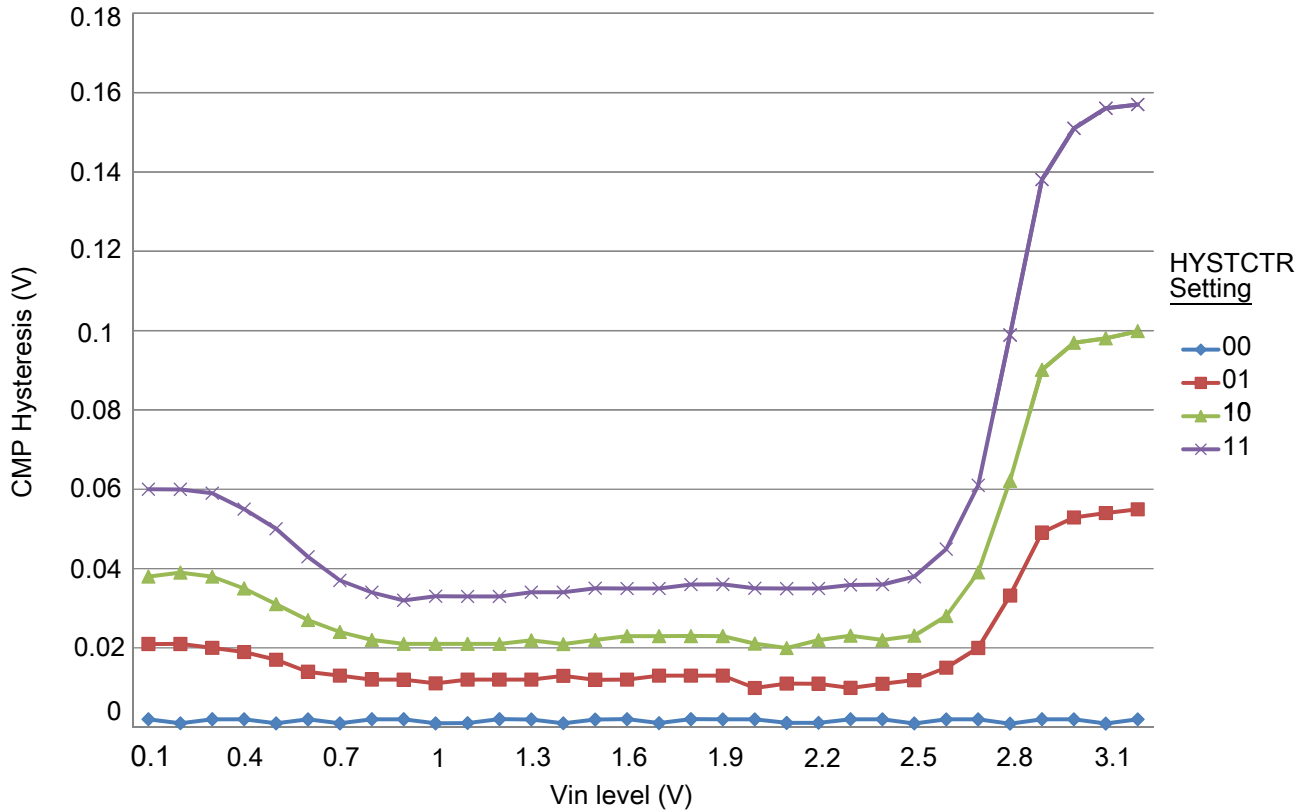


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

### 7.5.6.4 12-bit DAC electrical characteristics

#### 7.5.6.4.1 12-bit DAC operating requirements

Table 39. 12-bit DAC operating requirements

| Symbol     | Description             | Min. | Max. | Unit | Notes |
|------------|-------------------------|------|------|------|-------|
| $V_{DDA}$  | Supply voltage          | 1.71 | 3.6  | V    |       |
| $V_{DACR}$ | Reference voltage       | 1.13 | 3.6  | V    | 1     |
| $C_L$      | Output load capacitance | —    | 100  | pF   | 2     |
| $I_L$      | Output load current     | —    | 1    | mA   |       |

1. The DAC reference can be selected to be  $V_{DDA}$  or  $V_{REF\_OUT}$ .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.



## 7.5.6.4.2 12-bit DAC operating behaviors

Table 40. 12-bit DAC operating behaviors

| Symbol           | Description   | Min.             | Typ.        | Max.       | Unit                   | Notes |
|------------------|---|------------------|-------------|------------|------------------------|-------|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode   | —                | —           | 250        | $\mu\text{A}$          |       |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode  | —                | —           | 900        | $\mu\text{A}$          |       |
| $t_{DACLP}$      | Full-scale settling time (0x080 to 0xF7F) — low-power mode  | —                | 100         | 200        | $\mu\text{s}$          | 1     |
| $t_{DACHP}$      | Full-scale settling time (0x080 to 0xF7F) — high-power mode   | —                | 15          | 30         | $\mu\text{s}$          | 1     |
| $t_{CCDACLP}$    | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode  | —                | 0.7         | 1          | $\mu\text{s}$          | 1     |
| $V_{dacoutl}$    | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000   | —                | —           | 100        | mV                     |       |
| $V_{dacouth}$    | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF   | $V_{DACR} - 100$ | —           | $V_{DACR}$ | mV                     |       |
| INL              | Integral non-linearity error — high speed mode  | —                | —           | $\pm 8$    | LSB                    | 2     |
| DNL              | Differential non-linearity error — $V_{DACR} > 2\text{ V}$  | —                | —           | $\pm 1$    | LSB                    | 3     |
| DNL              | Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$  | —                | —           | $\pm 1$    | LSB                    | 4     |
| $V_{OFFSET}$     | Offset error  | —                | $\pm 0.4$   | $\pm 0.8$  | %FSR                   | 5     |
| $E_G$            | Gain error  | —                | $\pm 0.1$   | $\pm 0.6$  | %FSR                   | 5     |
| PSRR             | Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$   | 60               | —           | 90         | dB                     |       |
| $T_{CO}$         | Temperature coefficient offset voltage  | —                | 3.7         | —          | $\mu\text{V}/\text{C}$ | 6     |
| $T_{GE}$         | Temperature coefficient gain error  | —                | 0.000421    | —          | %FSR/C                 |       |
| $R_{op}$         | Output resistance (load = 3 k $\Omega$ )  | —                | —           | 250        | $\Omega$               |       |
| SR               | Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul> | 1.2<br>0.05      | 1.7<br>0.12 | —<br>—     | V/ $\mu\text{s}$       |       |
| BW               | 3dB bandwidth <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul>               | 550<br>40        | —<br>—      | —<br>—     | kHz                    |       |

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  (DAC<sub>X</sub>\_CO:DACRFS = 1), high power mode (DAC<sub>X</sub>\_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

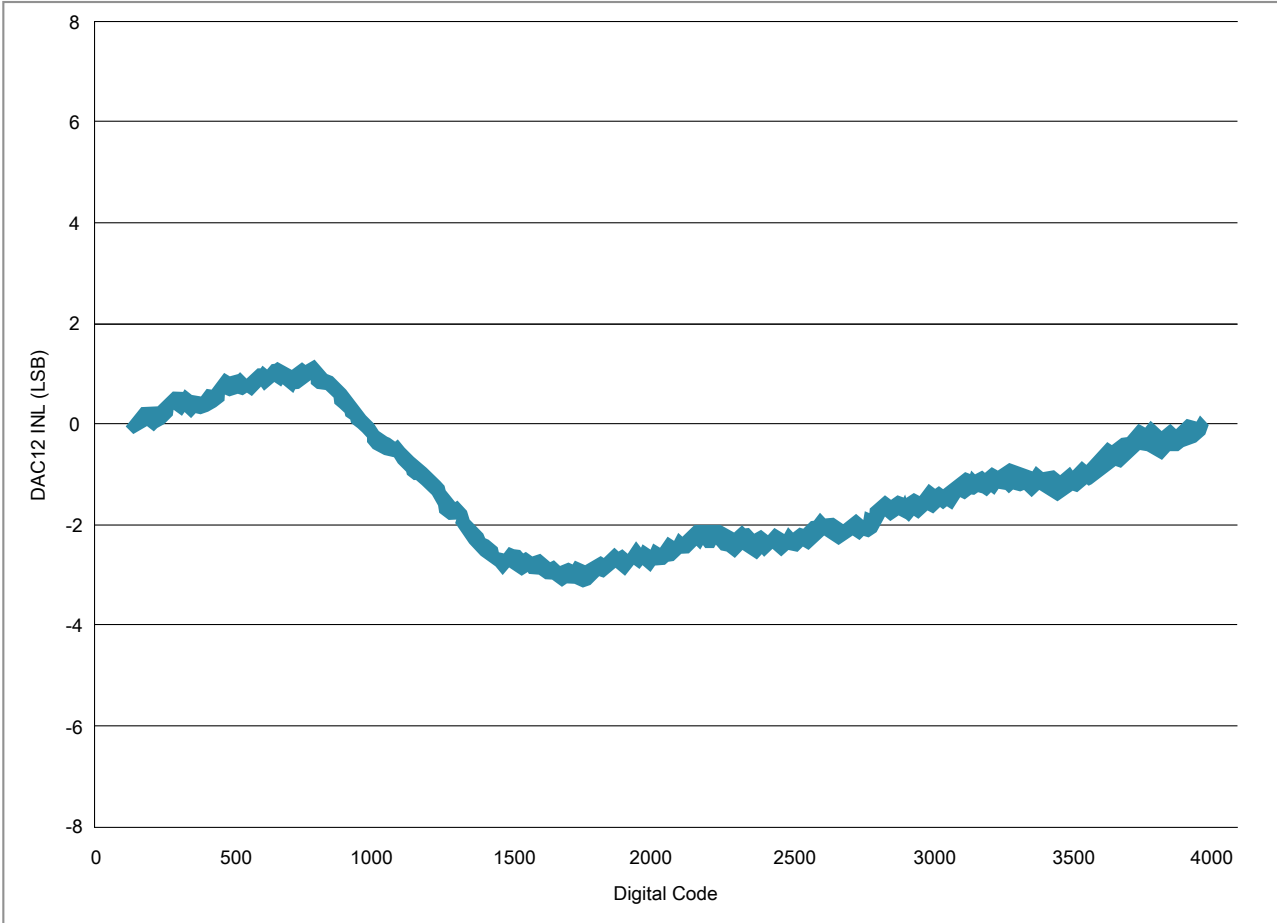
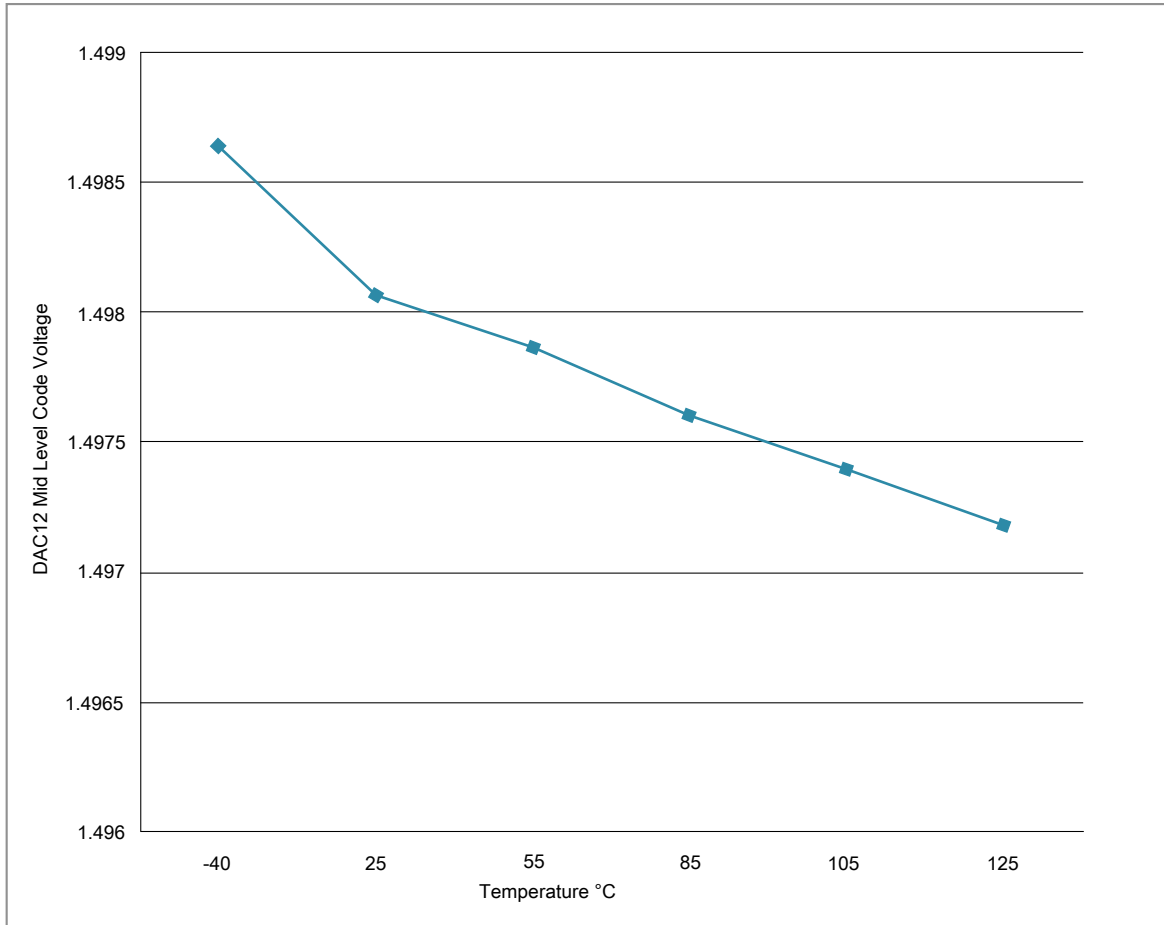


Figure 11. Typical INL error vs. digital code



**Figure 12. Offset at half scale vs. temperature**

## 7.5.7 Timers

See [General switching specifications](#).

## 7.5.8 Communication interfaces

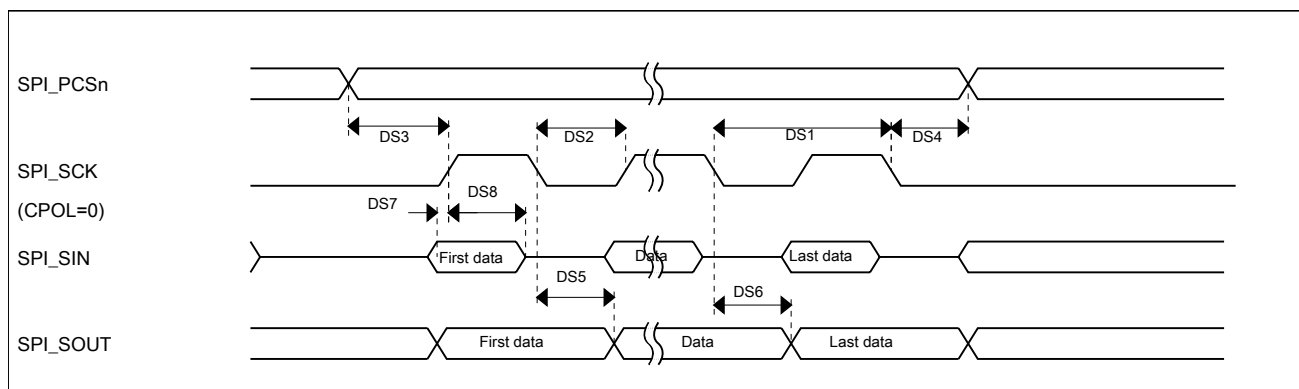
### 7.5.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. See the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 41. Master mode DSPI timing (limited voltage range)**

| Num | Description                         | Min.                     | Max.              | Unit | Notes |
|-----|-------------------------------------|--------------------------|-------------------|------|-------|
|     | Operating voltage                   | 2.7                      | 3.6               | V    |       |
|     | Frequency of operation              | —                        | 12                | MHz  |       |
| DS1 | DSPI_SCK output cycle time          | $2 \times t_{BUS}$       | —                 | ns   |       |
| DS2 | DSPI_SCK output high/low time       | $(t_{SCK}/2) - 2$        | $(t_{SCK}/2) + 2$ | ns   |       |
| DS3 | DSPI_PCSn valid to DSPI_SCK delay   | $(t_{BUS} \times 2) - 2$ | —                 | ns   | 1     |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{BUS} \times 2) - 2$ | —                 | ns   | 2     |
| DS5 | DSPI_SCK to DSPI_SOUT valid         | —                        | 8.5               | ns   |       |
| DS6 | DSPI_SCK to DSPI_SOUT invalid       | -2                       | —                 | ns   |       |
| DS7 | DSPI_SIN to DSPI_SCK input setup    | 16.2                     | —                 | ns   |       |
| DS8 | DSPI_SCK to DSPI_SIN input hold     | 0                        | —                 | ns   |       |

1. The delay is programmable in SPIx\_CTARn[PCSSCK] and SPIx\_CTARn[CSSCK].
2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 13. DSPI classic SPI timing — master mode**

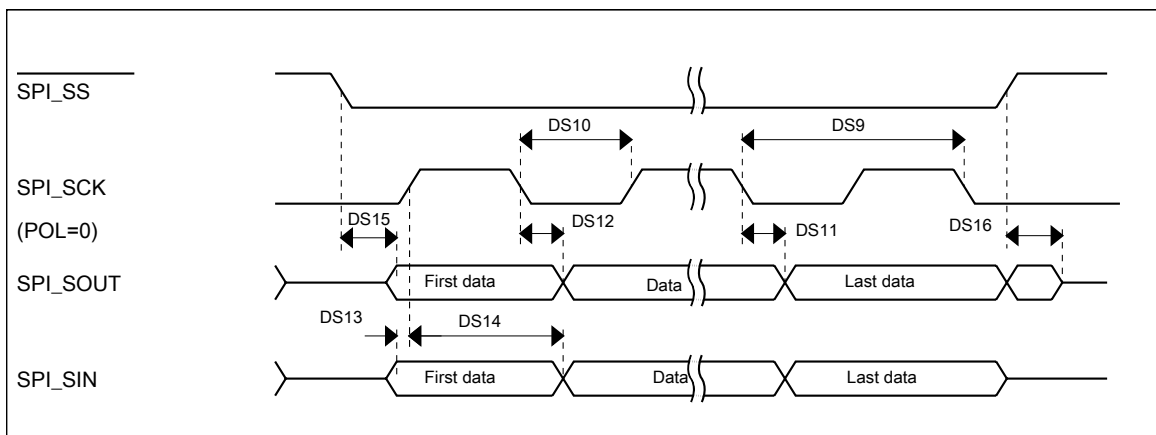
**Table 42. Slave mode DSPI timing (limited voltage range)**

| Num | Description            | Min. | Max. | Unit |
|-----|------------------------|------|------|------|
|     | Operating voltage      | 2.7  | 3.6  | V    |
|     | Frequency of operation |      | 6    | MHz  |

Table continues on the next page...

**Table 42. Slave mode DSPI timing (limited voltage range) (continued)**

| Num  | Description                              | Min.                      | Max.                      | Unit |
|------|--|---------------------------|---------------------------|------|
| DS9  | DSPI_SCK input cycle time                | 4 x t <sub>BUS</sub>      | —                         | ns   |
| DS10 | DSPI_SCK input high/low time             | (t <sub>SCK/2</sub> ) - 2 | (t <sub>SCK/2</sub> ) + 2 | ns   |
| DS11 | DSPI_SCK to DSPI_SOUT valid              | —                         | 21.4                      | ns   |
| DS12 | DSPI_SCK to DSPI_SOUT invalid            | 0                         | —                         | ns   |
| DS13 | DSPI_SIN to DSPI_SCK input setup         | 2.6                       | —                         | ns   |
| DS14 | DSPI_SCK to DSPI_SIN input hold          | 7.0                       | —                         | ns   |
| DS15 | DSPI_SS active to DSPI_SOUT driven       | —                         | 14                        | ns   |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | —                         | 14                        | ns   |



**Figure 14. DSPI classic SPI timing — slave mode**

### 7.5.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. See the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 43. Master mode DSPI timing (full voltage range)**

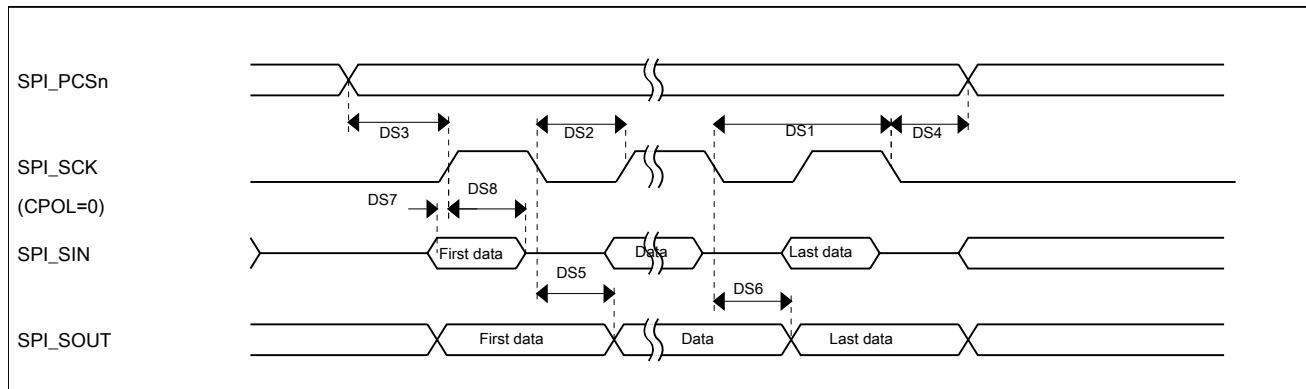
| Num | Description                   | Min.                      | Max.                      | Unit | Notes |
|-----|-------------------------------|---------------------------|---------------------------|------|-------|
|     | Operating voltage             | 1.71                      | 3.6                       | V    | 1     |
|     | Frequency of operation        | —                         | 12                        | MHz  |       |
| DS1 | DSPI_SCK output cycle time    | 2 x t <sub>BUS</sub>      | —                         | ns   |       |
| DS2 | DSPI_SCK output high/low time | (t <sub>SCK/2</sub> ) - 4 | (t <sub>SCK/2</sub> ) + 4 | ns   |       |

*Table continues on the next page...*

**Table 43. Master mode DSPI timing (full voltage range) (continued)**

| Num | Description                         | Min.                     | Max. | Unit | Notes |
|-----|-------------------------------------|--------------------------|------|------|-------|
| DS3 | DSPI_PCSn valid to DSPI_SCK delay   | $(t_{BUS} \times 2) - 4$ | —    | ns   | 2     |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{BUS} \times 2) - 4$ | —    | ns   | 3     |
| DS5 | DSPI_SCK to DSPI_SOUT valid         | —                        | 10   | ns   |       |
| DS6 | DSPI_SCK to DSPI_SOUT invalid       | -1.2                     | —    | ns   |       |
| DS7 | DSPI_SIN to DSPI_SCK input setup    | 23.3                     | —    | ns   |       |
| DS8 | DSPI_SCK to DSPI_SIN input hold     | 0                        | —    | ns   |       |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx\_CTARn[PCSSCK] and SPIx\_CTARn[CSSCK].
3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 15. DSPI classic SPI timing — master mode**

**Table 44. Slave mode DSPI timing (full voltage range)**

| Num  | Description  | Min.               | Max.              | Unit |
|------|--|--------------------|-------------------|------|
|      | Operating voltage                                      | 1.71               | 3.6               | V    |
|      | Frequency of operation                                 | —                  | 6                 | MHz  |
| DS9  | DSPI_SCK input cycle time                              | $4 \times t_{BUS}$ | —                 | ns   |
| DS10 | DSPI_SCK input high/low time                           | $(t_{SCK}/2) - 4$  | $(t_{SCK}/2) + 4$ | ns   |
| DS11 | DSPI_SCK to DSPI_SOUT valid                            | —                  | 29.1              | ns   |
| DS12 | DSPI_SCK to DSPI_SOUT invalid                          | 0                  | —                 | ns   |
| DS13 | DSPI_SIN to DSPI_SCK input setup                       | 3.2                | —                 | ns   |
| DS14 | DSPI_SCK to DSPI_SIN input hold                        | 7.0                | —                 | ns   |
| DS15 | $\overline{DSPI\_SS}$ active to DSPI_SOUT driven       | —                  | 25                | ns   |
| DS16 | $\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven | —                  | 25                | ns   |

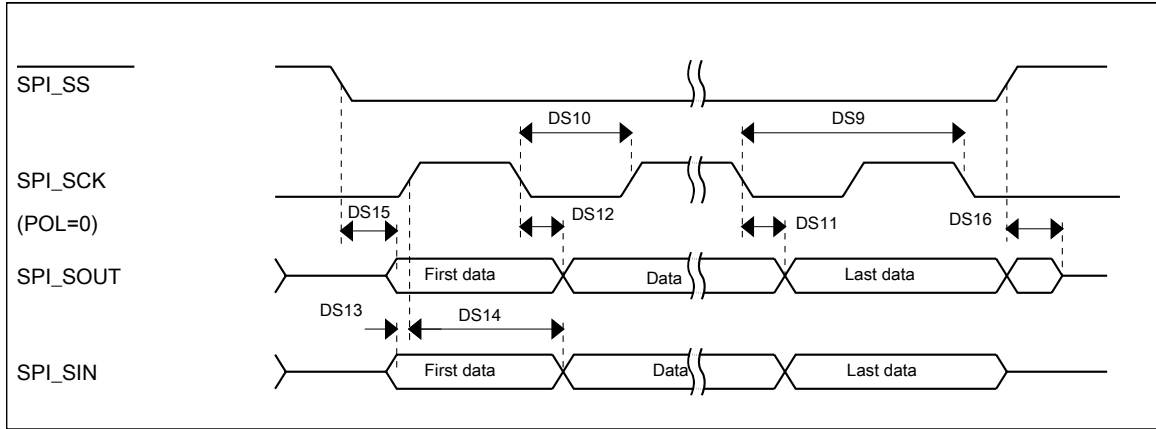


Figure 16. DSPI classic SPI timing — slave mode

### 7.5.8.3 Inter-Integrated Circuit Interface (I<sup>2</sup>C) timing

Table 45. I<sup>2</sup>C timing

| Characteristic   | Symbol        | Standard Mode    |                   | Fast Mode                  |                  | Unit    |
|--|---------------|------------------|-------------------|----------------------------|------------------|---------|
|  |               | Minimum          | Maximum           | Minimum                    | Maximum          |         |
| SCL Clock Frequency  | $f_{SCL}$     | 0                | 100               | 0                          | 400              | kHz     |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}; STA$ | 4                | —                 | 0.6                        | —                | $\mu s$ |
| LOW period of the SCL clock  | $t_{LOW}$     | 4.7              | —                 | 1.3                        | —                | $\mu s$ |
| HIGH period of the SCL clock   | $t_{HIGH}$    | 4                | —                 | 0.6                        | —                | $\mu s$ |
| Set-up time for a repeated START condition   | $t_{SU}; STA$ | 4.7              | —                 | 0.6                        | —                | $\mu s$ |
| Data hold time for I <sup>2</sup> C bus devices  | $t_{HD}; DAT$ | 0 <sup>1</sup>   | 3.45 <sup>2</sup> | 0 <sup>3</sup>             | 0.9 <sup>1</sup> | $\mu s$ |
| Data set-up time   | $t_{SU}; DAT$ | 250 <sup>4</sup> | —                 | 100 <sup>2, 5</sup>        | —                | ns      |
| Rise time of SDA and SCL signals   | $t_r$         | —                | 1000              | $20 + 0.1C_b$ <sup>6</sup> | 300              | ns      |
| Fall time of SDA and SCL signals   | $t_f$         | —                | 300               | $20 + 0.1C_b$ <sup>5</sup> | 300              | ns      |
| Set-up time for STOP condition   | $t_{SU}; STO$ | 4                | —                 | 0.6                        | —                | $\mu s$ |
| Bus free time between STOP and START condition   | $t_{BUF}$     | 4.7              | —                 | 1.3                        | —                | $\mu s$ |
| Pulse width of spikes that must be suppressed by the input filter                            | $t_{SP}$      | N/A              | N/A               | 0                          | 50               | ns      |

1. The master mode I<sup>2</sup>C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum  $t_{HD}; DAT$  must be met only if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF.
4. Set-up time in slave-transmitter mode is 1 IP Bus clock period, if the TX FIFO is empty.
5. A Fast mode I<sup>2</sup>C bus device can be used in a Standard mode I<sup>2</sup>C bus system, but the requirement  $t_{SU}; DAT \geq 250$  ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line  $t_{rmax}$

## MCU Electrical Characteristics

+  $t_{SU; DAT} = 1000 + 250 = 1250$  ns (according to the Standard mode I<sup>2</sup>C bus specification) before the SCL line is released.

6.  $C_b$  = total capacitance of the one bus line in pF.

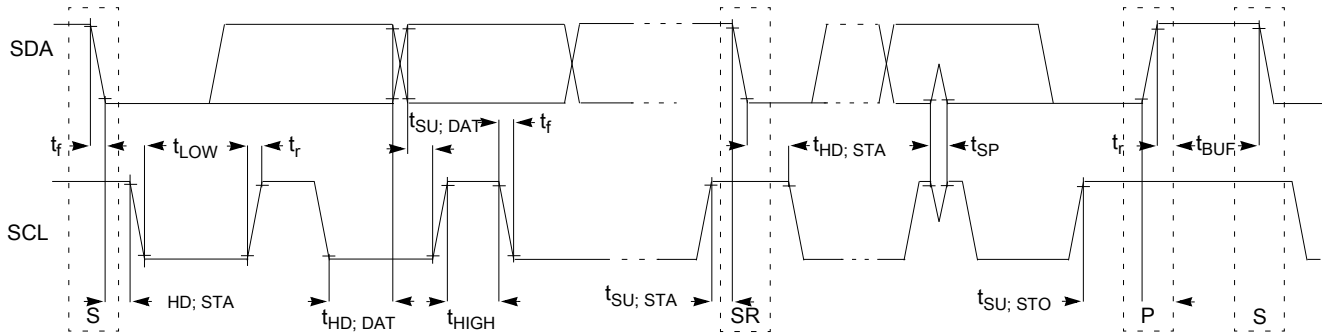


Figure 17. Timing definition for fast and standard mode devices on the I<sup>2</sup>C bus

### 7.5.8.4 LPUART

See [General switching specifications](#).

## 7.5.9 Human-machine interfaces (HMI)

### 7.5.9.1 TSI electrical specifications

Table 46. TSI electrical specifications

| Symbol    | Description  | Min. | Typ. | Max. | Unit |
|-----------|--|------|------|------|------|
| Ta        | Temperature  | -30  | —    | 105  | °C   |
| TSI_RUNF  | Fixed power consumption in run mode  | —    | 100  | —    | µA   |
| TSI_RUNV  | Variable power consumption in run mode (depends on oscillator's current selection) | 1.0  | —    | 128  | µA   |
| TSI_EN    | Power consumption in enable mode   | —    | 100  | —    | µA   |
| TSI_DIS   | Power consumption in disable mode  | —    | 1.2  | —    | µA   |
| TSI_TEN   | TSI analog enable time   | —    | 66   | —    | µs   |
| TSI_CREF  | TSI reference capacitor  | —    | 1.0  | —    | pF   |
| TSI_DVOLT | Voltage variation of VP & VM around nominal values                                 | 0.19 | —    | 1.03 | V    |

### 7.5.9.2 GPIO

The maximum input voltage on PTC0/1/2/3 is  $V_{DD} + 0.3V$ . For rest of the GPIO specification, see [General switching specifications](#).



## 7.6 DC-DC Converter Operating Requirements

**Table 47. DC-DC Converter Recommended operating conditions**

| Characteristic                              | Symbol   | Min              | Typ | Max   | Unit |
|---|--|------------------|-----|-------|------|
| Bypass Mode Supply Voltage (RF and Analog)  | VDD <sub>RF1</sub> ,<br>VDD <sub>RF2</sub> ,<br>VDD <sub>RF3</sub> | 1.425            | —   | 3.6   | Vdc  |
| Bypass Mode Supply Voltage (Digital)        | VDD <sub>X</sub> , V <sub>DCDC_IN</sub> ,<br>VDD <sub>A</sub>      | 1.71             | —   | 3.6   | Vdc  |
| Boost Mode Supply Voltage<br>1              | VDD <sub>DCDC_IN</sub>   | 1.1 <sup>2</sup> | —   | 1.795 | Vdc  |
| Buck Mode Supply Voltage <sup>3, 1, 4</sup> | VDD <sub>DCDC_IN</sub>   | 2.1              | —   | 4.25  | Vdc  |
| External Inductor <sup>5</sup>              | L <sub>DCDC</sub>  | 10               |     |       | uH   |
| Inductor Resistance in Buck Mode            | ESR  | —                | 0.2 | 0.5   | Ohms |
| Inductor Resistance in Boost Mode           | ESR  | —                | —   | 0.2   | Ohms |

- VDD\_1P5 is 1.8 V by default in Boost mode. VDD\_1P8OUT should supply to VDD<sub>1</sub>, VDD<sub>2</sub> and VDD<sub>A</sub>. VDD\_1P5OUT\_PMCIN should supply to VDD<sub>RF1</sub> and VDD<sub>RF2</sub>. VDD<sub>XTAL</sub> can be either supplied by 1.5 V or 1.8 V
- In boost mode, DC-DC converter needs minimum 1.1 V to start, the supply can drop to 0.9 V after the DC-DC converter settles.
- In Buck mode, DC-DC converter needs 2.1 V min to start, the supply can drop to 1.8 V after DC-DC converter settles
- When  $3.6\text{ V} < \text{VDD}_{\text{DCDC\_IN}} / \text{DCDC\_CFG} / \text{PSWITCH} \leq 4.25\text{ V}$ , T<sub>A</sub> and T<sub>J</sub> are constrained to a maximum of +45 °C and +65 °C respectively (typical Li-ion maximum temperatures when charging). When  $\text{VDD}_{\text{DCDC\_IN}} / \text{DCDC\_CFG} / \text{PSWITCH} \leq 3.6\text{ V}$ , T<sub>A</sub> and T<sub>J</sub> are constrained to a maximum of +105 °C and +125 °C respectively.
- In both Buck and Boost modes, LN and LP are connected to external inductor. In boost mode, LP is also shorted to V<sub>DCDC\_IN</sub>.

**Table 48. DC-DC Converter Specifications**

| Characteristics                  | Conditions                          | Symbol          | Min  | Typ              | Max              | Unit |
|----------------------------------|-------------------------------------|-----------------|------|------------------|------------------|------|
| DC-DC Converter Output Power     | Total power output of 1P8V and 1P5V | Pdcdc_out       | —    | —                | 125 <sup>1</sup> | mW   |
| Switching Frequency <sup>2</sup> |                                     | DCDC_FREQ       | —    | 2                | —                | MHz  |
| Half FET Threshold               |                                     | I_half_FET      | —    | 5                | —                | mA   |
| Double FET Threshold             |                                     | I_double_FET    | —    | 40               | —                | mA   |
| Boost Mode                       |                                     |                 |      |                  |                  |      |
| Enable Threshold                 |                                     | EN_THRESH_boost | -    | 50               | -                | mV   |
| DC-DC Conversion Efficiency      |                                     | DCDC_EFF_boost  | -    | 90 %             | -                |      |
| 1.8 V Output Voltage             |                                     | VDD_1P8_boost   | 1.71 | 1.8 <sup>3</sup> | 3.5              | Vdc  |

Table continues on the next page...

**Table 48. DC-DC Converter Specifications (continued)**

| Characteristics                           | Conditions   | Symbol                         | Min                  | Typ                | Max                                     | Unit |
|---|--|--------------------------------|----------------------|--------------------|---|------|
| 1.8 V Output Current <sup>4,5</sup>       | VDD_1P8 = 1.8 V, VDCDC_IN = 1.7 V  | IDDC_1P8_boost<br>1            | —                    | —                  | 45                                      | mA   |
|   | VDD_1P8 = 3.0 V, VDCDC_IN = 1.7 V  | IDDC_1P8_boost<br>2            | —                    | —                  | 27                                      | mA   |
|   | VDD_1P8 = 1.8 V, VDCDC_IN = 0.9 V  | IDDC_1P8_boost<br>3            | —                    | —                  | 20                                      | mA   |
|   | VDD_1P8 = 3.0 V, VDCDC_IN = 0.9 V  | IDDC_1P8_boost<br>4            | —                    | —                  | 10                                      | mA   |
| 1.5V Output Voltage                       |  | VDD_1P5_boost                  | 1.425 <sup>6,7</sup> | 1.8 <sup>6,7</sup> | 2.0                                     | Vdc  |
| 1.5 V Output Current <sup>4,8</sup>       |  | VDD_1P5_boost                  | —                    | —                  | 30                                      | mA   |
| DCDC Transition Operating Behavior        | LSS→Run  | t_DCDCboost_LSS→RUN            | —                    | 50                 | —                                       | us   |
| DCDC Turn on Time                         |  | T <sub>DCDC_ON_boost</sub>     | —                    | 2.3 <sup>9</sup>   | —                                       | ms   |
| DCDC Settling Time for increasing voltage |  | T <sub>DCDC_SETTLE_boost</sub> | —                    | 0.271              | —                                       | ms   |
| DCDC Settling Time for decreasing voltage | C = capacitance attached to the DCDC V1P8 output rail.<br><br>V1 = the initial output voltage of the DCDC.<br><br>V2 = the final output voltage of the DCDC.<br><br>I2 = the load on the DCDC output expressed in Amperes. | T <sub>DCDC_SETTLE_boost</sub> | —                    | $(C*(V1-V2)/I2)$   | —                                       | s    |
| <b>Buck Mode</b>                          |  |                                |                      |                    |   |      |
| DC-DC Conversion Efficiency               |  | DCDC_EFF_buck                  | —                    | 90 %               | —                                       | —    |
| 1.8 V Output Voltage                      |  | VDD_1P8_buck                   | 1.71                 | —                  | min(VDCDC_IN_buck, 3.5) <sup>10,3</sup> | Vdc  |
| 1.8 V Output Current <sup>4,5</sup>       | VDD_1P8 = 1.8 V, VDC_1P5 = 1.5 V   | IDDC_1P8_buck1                 | —                    | —                  | 45                                      | mA   |

Table continues on the next page...

Table 48. DC-DC Converter Specifications (continued)

| Characteristics                           | Conditions   | Symbol                        | Min                 | Typ               | Max  | Unit |
|---|--|-------------------------------|---------------------|-------------------|------|------|
|   | VDD_1P8 = 3.0 V, VDC_1P5 = 1.5 V   | IDD_1P8_buck2                 | —                   | —                 | 27   | mA   |
| 1.5 V Output Voltage                      | Radio section requires 1.5 V   | VDD_1P5_buck                  | 1.425 <sup>11</sup> | 1.5 <sup>11</sup> | 1.65 | Vdc  |
| 1.5 V Output Current <sup>4, 8</sup>      |  | IDD_1P5_buck                  | —                   | —                 | 30   | mA   |
| DCDC Transition Operating Behavior        | LSS→Run  | t_DCDCbuck_LS→RUN             | —                   | 50                | —    | us   |
| DCDC Turn on Time                         |  | T <sub>DCDC_ON_buck</sub>     | —                   | 2.2 <sup>9</sup>  | —    | ms   |
| DCDC Settling Time for increasing voltage |  | T <sub>DCDC_SETTLE_buck</sub> | —                   | 0.371             | —    | ms   |
| DCDC Settling Time for decreasing voltage | C = capacitance attached to the DCDC V1P8 output rail.<br>V1 = the initial output voltage of the DCDC<br>V2 = the final output voltage of the DCDC<br>I2 = the load on the DCDC output expressed in Amperes. | T <sub>DCDC_SETTLE_buck</sub> | —                   | (C*(V1-V2)/I2)    | —    | s    |

1. This is the steady state DC output power. It requires VDCDC\_IN >= 1.7V in boost mode. Excessive transient current load from external device will cause 1p8V and 1P5 output voltage unregulated temporary.
2. This is the frequency that will be observed at LN and LP pins.
3. The voltage output level can be controlled by programming DCDC\_VDD1P8CTRL\_TRG field in DCDC\_REG3.
4. The output current specification in both buck and boost modes represents the maximum current the DC-DC converter can deliver. The KW41Z radio and MCU blocks current consumption is not excluded. Note that the maximum output power of the DC-DC converter is 125mW. The available supply current for external device depends on the energy consumed by the internal peripherals in KW41Z.
5. When using DC-DC in low power mode(pulsed mode), current load must be less than 0.5 mA.
6. The minimum VDD\_1P5\_boost is the maximum of either what is programmed using DCDC\_VDD1P5CTRL\_TRG\_BOOST field in DCDC\_REG3 or VDCDC\_IN\_boost + 0.05V. For example, if VDCDC\_IN = 0.9V, minimum VDD\_1P5 is as programmed in DCDC\_VDD1P5CTRL\_TRG\_BOOST. If VDCDC\_IN = 1.5V, minimum VDD\_1P5 = 1.5 + 0.05V is 1.55V.
7. 1.8 V is the default value of the DC-DC 1.5 V output voltage in boost mode. The user can program DCDC\_VDD1P5CTRL\_TRG\_BOOST field in register DCDC\_REG3 to control 1.5 V output voltage level. For reliable radio operation, a voltage level of 1.425 V is required. VDD\_1P5 must not be programmed higher than VDD\_1P8.
8. 1.5 V is intended to supply power to KW41Z only. It is not designed to supply power to an external device.
9. Turn on time is measured from the application of power (to DCDC\_IN) to when the DCDC\_REG0[DCDC\_STS\_DC\_OK] bit is set. Code execution may begin before the DCDC\_REG0[DCDC\_STS\_DC\_OK] bit is set. Full device specification is not guaranteed until the bit sets.
10. In Buck mode, the maximum VDD\_1P8 output is the minimum of either VDCDC\_IN\_BUCK minus 50 mV or 3.5 V. For example, if VDCDC\_IN = 1.85V, maximum VDD\_1P8 is 1.8V. If VDCDC\_IN = 4.2V, maximum VDD\_1P8 is 3V.

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- 1.5 V is the default value of DCDC\_VDD\_1P5 in buck mode. The user can program DCDC\_VDD1P5CTRL\_TRG\_BUCK field in register DCDC\_REG3 to control 1P5 output voltage level. For Radio operation, minimum 1.425 V is required. VDD\_1P5 must not be programmed higher than VDD\_1P8.

## 7.7 Ratings

### 7.7.1 Thermal handling ratings

Table 49. Thermal handling ratings

| Symbol           | Description                   | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T <sub>STG</sub> | Storage temperature           | -55  | 150  | °C   | 1     |
| T <sub>SDR</sub> | Solder temperature, lead-free | —    | 260  | °C   | 2     |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 7.7.2 Moisture handling ratings

Table 50. Moisture handling ratings

| Symbol | Description                | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL    | Moisture sensitivity level | —    | 3    | —    | 1     |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 7.7.3 ESD handling ratings

Table 51. ESD handling ratings

| Symbol           | Description   | Min.  | Max.  | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V <sub>HBM</sub> | Electrostatic discharge voltage, human body model     | -2000 | +2000 | V    | 1     |
| V <sub>CDM</sub> | Electrostatic discharge voltage, charged-device model | -500  | +500  | V    | 2     |
| I <sub>LAT</sub> | Latch-up current at ambient temperature of 105 °C     | -100  | +100  | mA   | 3     |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 7.7.4 Voltage and current operating ratings

Table 52. Voltage and current operating ratings

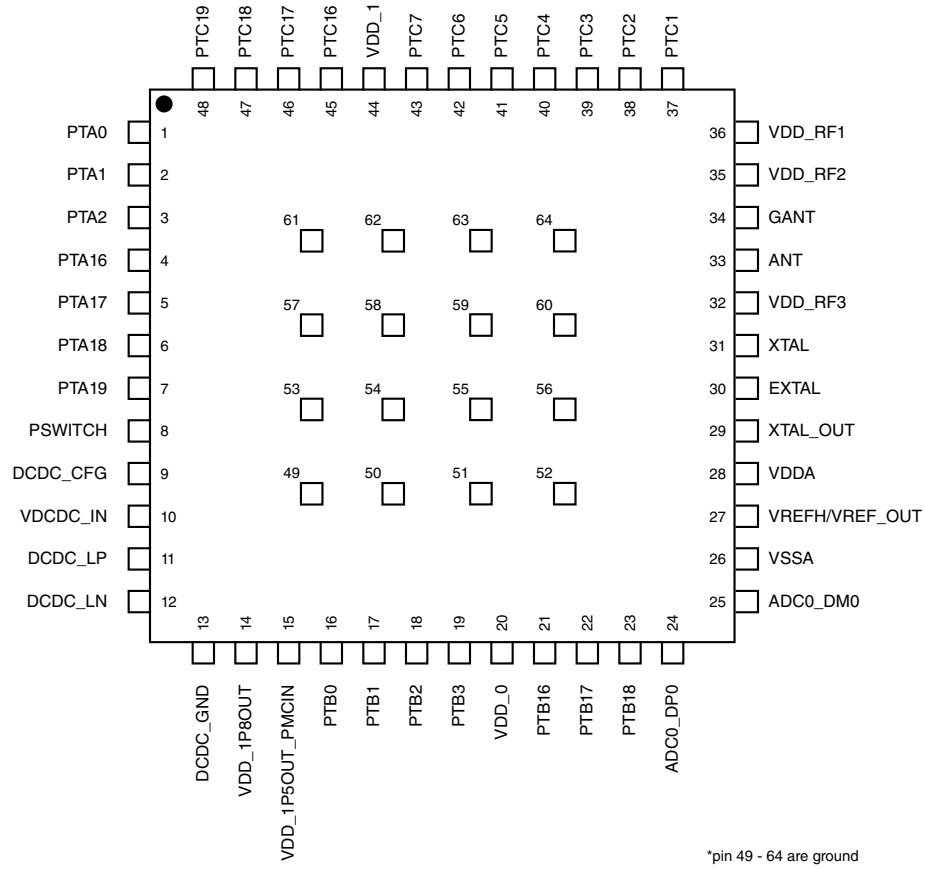
| Symbol         | Description   | Min.           | Max.           | Unit |
|----------------|---|----------------|----------------|------|
| $V_{DD}$       | Digital supply voltage  | -0.3           | 3.8            | V    |
| $I_{DD}$       | Digital supply current  | —              | 120            | mA   |
| $V_{IO}$       | IO pin input voltage  | -0.3           | $V_{DD} + 0.3$ | V    |
| $I_D$          | Instantaneous maximum current single pin limit (applies to all port pins) | -25            | 25             | mA   |
| $V_{DDA}$      | Analog supply voltage   | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V    |
| $V_{IO\_DCDC}$ | IO pins in the DCDC voltage domain (DCDC_CFG and PSWITCH)                 | GND            | VDCDC          | V    |

## 8 Pin Diagrams and Pin Assignments

### 8.1 Pinouts

Device pinout are shown in figures below.

## Pin Diagrams and Pin Assignments



**Figure 18. 48-pin Laminated QFN pinout diagram**

|   | 1        | 2                 | 3       | 4       | 5     | 6     | 7                 | 8               | 9        |
|---|----------|-------------------|---------|---------|-------|-------|-------------------|-----------------|----------|
| A |          |                   |         | VSS     | PTC3  | PTC4  | PTC7              | PTC16           | PTC18    |
| B | GANT     | ANT               | VDD_RF2 | VDD_RF1 | VSS   | PTC2  | PTC6              | PTC17           | PTA1     |
| C | XTAL     | VDD_RF3           | VSS     | VSS     | PTC0  | PTC1  | PTC5              | PTC19           | PTA2     |
| D | EXTAL    | VSS               | VSS     | VSS     | VSS   | VSS   | VDD_1             | PTA0            | PTA17    |
| E | XTAL_OUT | VSS               | VSS     | VSS     | VSS   | VDD_1 | PTA16             | PTA18           | PTA19    |
| F | VDDA     | VREFH_VREF<br>OUT | PTB18   | VSS     | VSS   | VSS   | VSS               | DCDC_CFG        | PSWITCH  |
| G | VSSA     | VSSA              | VSS     | VSS     | PTB3  | PTB2  | VDD_1P8OUT        | DCDC_GND        | VDCDC_IN |
| H | ADC0_DM0 | VSS               | PTB17   | PTB16   | VSS   | PTB1  | VDD_1P5_P<br>MCIN | DCDC_LN         | DCDC_LP  |
| J | ADC0_DP0 | VSS               |         |         | VDD_0 | PTB0  | VSS               | VDD_1P5_C<br>AP |          |

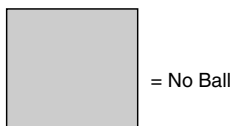


Figure 19. KW41 75-pin WLCSP Pinout Diagram

## 8.2 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and locations of these pins on the packages supported by this device. The Port Control Module is responsible for selecting which ALT functional is available on each PTxy pin.

**NOTE**

On the 75 WLCSP, VDD\_1P5\_CAP and VDD\_1P5\_PMCIN should be tied together external to the device.

**Table 53. KW41Z Pin Assignments**

| KW41 Z(48 LGA / Laminate QFN) | KW41 (WLCSP) | Pin Name         | DEFAULT          | ALT0               | ALT1                   | ALT2      | ALT3 | ALT4 | ALT5       | ALT6 | ALT7    |
|-------------------------------|--------------|------------------|------------------|--------------------|------------------------|-----------|------|------|------------|------|---------|
| 1                             | D8           | PTA0             | SWD_DIO          | TSIO_CH8           | PTA0                   | SPI0_PCS1 |      |      | TPM1_CH0   |      | SWD_DIO |
| 2                             | B9           | PTA1             | SWD_CLK          | TSIO_CH9           | PTA1                   | SPI1_PCS0 |      |      | TPM1_CH1   |      | SWD_CLK |
| 3                             | C9           | PTA2             | RESET_b          |                    | PTA2                   |           |      |      | TPM0_CH3   |      | RESET_b |
| 4                             | E7           | PTA16            | DISABLED         | TSIO_CH10          | PTA16/LLWU_P4          | SPI1_SOUT |      |      | TPM0_CH0   |      |         |
| 5                             | D9           | PTA17            | DISABLED         | TSIO_CH11          | PTA17/LLWU_P5/RF_RESET | SPI1_SIN  |      |      | TPM_CLKIN1 |      |         |
| 6                             | E8           | PTA18            | DISABLED         | TSIO_CH12          | PTA18/LLWU_P6          | SPI1_SCK  |      |      | TPM2_CH0   |      |         |
| 7                             | E9           | PTA19            | DISABLED         | TSIO_CH13/ADC0_SE5 | PTA19/LLWU_P7          | SPI1_PCS0 |      |      | TPM2_CH1   |      |         |
| 8                             | F9           | PSWITCH          | PSWITCH          | PSWITCH            |                        |           |      |      |            |      |         |
| 9                             | F8           | DCDC_CFG         | DCDC_CFG         | DCDC_CFG           |                        |           |      |      |            |      |         |
| 10                            | G9           | VDCDC_IN         | VDCDC_IN         | VDCDC_IN           |                        |           |      |      |            |      |         |
| 11                            | H9           | DCDC_LP          | DCDC_LP          | DCDC_LP            |                        |           |      |      |            |      |         |
| 12                            | H8           | DCDC_LN          | DCDC_LN          | DCDC_LN            |                        |           |      |      |            |      |         |
| 13                            | G8           | DCDC_GND         | DCDC_GND         | DCDC_GND           |                        |           |      |      |            |      |         |
| 14                            | G7           | VDD_1P8OUT       | VDD_1P8OUT       | VDD_1P8OUT         |                        |           |      |      |            |      |         |
| 15                            |              | VDD_1P5OUT_PMCIN | VDD_1P5OUT_PMCIN | VDD_1P5OUT_PMCIN   |                        |           |      |      |            |      |         |

Table continues on the next page...



Table 53. KW41Z Pin Assignments (continued)

| KW41Z(48 LGA / Lamin ate QFN) | KW41 (WLCSP ) | Pin Name       | DEFAULT           | ALT0                       | ALT1                     | ALT2             | ALT3     | ALT4          | ALT5     | ALT6 | ALT7       |
|-------------------------------|---------------|----------------|-------------------|----------------------------|--------------------------|------------------|----------|---------------|----------|------|------------|
|                               | J8            | VDD_1P5_CAP    | VDD_1P5_CAP       | VDD_1P5_CAP                |                          |                  |          |               |          |      |            |
|                               | H7            | VDD_1P5_PMCIN  | VDD_1P5_PMCIN     | VDD_1P5_PMCIN              |                          |                  |          |               |          |      |            |
| 16                            | J6            | PTB0           | DISABLED          |                            | PTB0/LLWU_P8/XTAL_OUT_EN |                  | I2C0_SCL | CMP0_OUT      | TPM0_CH1 |      | CLKOUT     |
| 17                            | H6            | PTB1           | DISABLED          | ADC0_SE1/CMP0_IN5          | PTB1                     | DTM_RX           | I2C0_SDA | LPTM_R0_AL T1 | TPM0_CH2 |      | CMT_IRO    |
| 18                            | G6            | PTB2           | DISABLED          | ADC0_SE3/CMP0_IN3          | PTB2                     | RF_NO T_ALLO WED | DTM_TX   |               | TPM1_CH0 |      |            |
| 19                            | G5            | PTB3           | DISABLED          | ADC0_SE2/CMP0_IN4          | PTB3                     |                  |          | CLKOUT        | TPM1_CH1 |      | RTC_CLKOUT |
| 20                            | J5            | VDD_0          | VDD_0             | VDD_0                      |                          |                  |          |               |          |      |            |
| 21                            | H4            | PTB16          | EXTAL32K          | EXTAL32K                   | PTB16                    |                  | I2C1_SCL |               | TPM2_CH0 |      |            |
| 22                            | H3            | PTB17          | XTAL32K           | XTAL32K                    | PTB17                    |                  | I2C1_SDA |               | TPM2_CH1 |      | BSM_CLK    |
| 23                            | F3            | PTB18          | NMI_b             | DAC0_OUT/ADC0_SE4/CMP0_IN2 | PTB18                    |                  | I2C1_SCL | TPM_CLKIN0    | TPM0_CH0 |      | NMI_b      |
| 24                            | J1            | ADC0_DP0       | ADC0_DP0/CMP0_IN0 | ADC0_DP0/CMP0_IN0          |                          |                  |          |               |          |      |            |
| 25                            | H1            | ADC0_DM0       | ADC0_DM0/CMP0_IN1 | ADC0_DM0/CMP0_IN1          |                          |                  |          |               |          |      |            |
| 26                            | G1, G2        | VSSA           | VSSA              | VSSA                       |                          |                  |          |               |          |      |            |
| 27                            | F2            | VREFH/VREF_OUT | VREFH/VREF_OUT    | VREFH/VREF_OUT             |                          |                  |          |               |          |      |            |
| 28                            | F1            | VDDA           | VDDA              | VDDA                       |                          |                  |          |               |          |      |            |
| 29                            | E1            | XTAL_OUT       | XTAL_OUT          | XTAL_OUT                   |                          |                  |          |               |          |      |            |

Table continues on the next page...

**Table 53. KW41Z Pin Assignments (continued)**

| KW41 Z(48 LGA / Lamin ate QFN) | KW41 (WLCSP ) | Pin Name | DEFAULT   | ALT0             | ALT1                         | ALT2             | ALT3          | ALT4            | ALT 5       | AL T6 | ALT7            |
|--------------------------------|---------------|----------|-----------|------------------|------------------------------|------------------|---------------|-----------------|-------------|-------|-----------------|
| 30                             | D1            | EXTAL    | EXTAL     | EXTAL            |                              |                  |               |                 |             |       |                 |
| 31                             | C1            | XTAL     | XTAL      | XTAL             |                              |                  |               |                 |             |       |                 |
| 32                             | C2            | VDD_RF3  | VDD_RF3   | VDD_RF3          |                              |                  |               |                 |             |       |                 |
| 33                             | B2            | ANT      | ANT       | ANT              |                              |                  |               |                 |             |       |                 |
| 34                             | B1            | GANT     | GANT      | GANT             |                              |                  |               |                 |             |       |                 |
| 35                             | B3            | VDD_RF2  | VDD_RF2   | VDD_RF2          |                              |                  |               |                 |             |       |                 |
| 36                             | B4            | VDD_RF1  | VDD_RF1   | VDD_RF1          |                              |                  |               |                 |             |       |                 |
|                                | C5            | PTC0     | DISABLE D |                  | PTC0/ LLWU_P9                | ANT_A            | I2C0_ SCL     | LPUAR T0_CT S_b | TPM 0_CH 1  |       |                 |
| 37                             | C6            | PTC1     | DISABLE D |                  | PTC1                         | ANT_B            | I2C0_ SDA     | LPUAR T0_RT S_b | TPM 0_CH 2  |       | BLE_ RF_A CTIVE |
| 38                             | B6            | PTC2     | DISABLE D | TSI0_CH14/ DIAG1 | PTC2/ LLWU_P10               | TX_SWI TCH       | I2C1_ SCL     | LPUAR T0_RX     | CMT _IRO    |       | DTM_ RX         |
| 39                             | A5            | PTC3     | DISABLE D | TSI0_CH15/ DIAG2 | PTC3/ LLWU_P11               | RX_SWI TCH       | I2C1_ SDA     | LPUAR T0_TX     | TPM 0_CH 1  |       | DTM_ TX         |
| 40                             | A6            | PTC4     | DISABLE D | TSI0_CH0/ DIAG3  | PTC4/ LLWU_P12               | ANT_A            | EXTR G_IN     | LPUAR T0_CT S_b | TPM 1_CH 0  |       | BSM_ DATA       |
| 41                             | C7            | PTC5     | DISABLE D | TSI0_CH1/ DIAG4  | PTC5/ LLWU_P13               | RF_NO T_ALLO WED | LPTM R0_A LT2 | LPUAR T0_RT S_b | TPM 1_CH 1  |       | BSM_ CLK        |
| 42                             | B7            | PTC6     | DISABLE D | TSI0_CH2         | PTC6/ LLWU_P14/ XTAL_OUT_E N |                  | I2C1_ SCL     | LPUAR T0_RX     | TPM 2_CH 0  |       | BSM_ FRAM E     |
| 43                             | A7            | PTC7     | DISABLE D | TSI0_CH3         | PTC7/ LLWU_P15               | SPI0_P CS2       | I2C1_ SDA     | LPUAR T0_TX     | TPM 2_CH 1  |       | BSM_ DATA       |
| 44                             | E6, D7        | VDD_1    | VDD_1     | VDD_1            |                              |                  |               |                 |             |       |                 |
| 45                             | A8            | PTC16    | DISABLE D | TSI0_CH4         | PTC16/ LLWU_P0               | SPI0_S CK        | I2C0_ SDA     | LPUAR T0_RT S_b | TPM 0_CH 3  |       |                 |
| 46                             | B8            | PTC17    | DISABLE D | TSI0_CH5         | PTC17/ LLWU_P1               | SPI0_S OUT       | I2C1_ SCL     | LPUAR T0_RX     | BSM _FRA ME |       | DTM_ RX         |
| 47                             | A9            | PTC18    | DISABLE D | TSI0_CH6         | PTC18/ LLWU_P2               | SPI0_SI N        | I2C1_ SDA     | LPUAR T0_TX     | BSM _DAT A  |       | DTM_ TX         |

Table continues on the next page...

**Table 53. KW41Z Pin Assignments (continued)**

| KW41Z(48 LGA / Laminate QFN) | KW41 (WLCSP)   | Pin Name | DEFAULT  | ALT0     | ALT1          | ALT2      | ALT3     | ALT4          | ALT5    | ALT6 | ALT7          |
|------------------------------|--|----------|----------|----------|---------------|-----------|----------|---------------|---------|------|---------------|
| 48                           | C8   | PTC19    | DISABLED | TSI0_CH7 | PTC19/LLWU_P3 | SPI0_PCS0 | I2C0_SCL | LPUART0_CTS_b | BSM_CLK |      | BLE_RF_ACTIVE |
| 49-64                        | A4, B5, C3, C4, D2, D3, D4, D5, D6, E2, E3, E4, E5, F4, F5, F6, F7, G3, G4, H2, H5, J2, J7 | Ground   | NA       |          |               |           |          |               |         |      |               |

## 8.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

### 8.3.1 Core Modules

This section contains tables describing the core module signal descriptions.

**Table 54. SWD Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                                      | I/O |
|-----------------|--------------------|--|-----|
| SWD_DIO         | SWD_DIO            | Serial Wire Debug Data Input/Output <sup>1</sup> | I/O |
| SWD_CLK         | SWD_CLK            | Serial Wire Clock <sup>2</sup>                   | I   |

1. Pulled up internally by default
2. Pulled down internally by default

## 8.3.2 Radio Modules

This section contains tables describing the radio signals.

**Table 55. Radio Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description  | I/O |
|-----------------|--------------------|--|-----|
| ANT             | ANT                | Antenna  | O   |
| GANT            | GANT               | Antenna ground   | I   |
| BLE_RF_ACTIVE   | BLE_RF_ACTIVE      | Signal to indicate future BLE activity. Refer <a href="#">BLE Link Layer</a> for more details. | O   |
| RF_NOT_ALLOWED  | RF_NOT_ALLOWED     | Radio off signal, intended for WiFi coexistence control  | I   |
| RF_RESET        | RF_RESET           | Radio reset signal   | I   |
| DTM_RX          | DTM_RX             | Direct Test Mode Receive   | I   |
| DTM_TX          | DTM_TX             | Direct Test Mode Transmit  | O   |
| BSM_CLK         | BSM_CLK            | Bit Streaming Mode (BSM) Clock signal, 802.15.4 packet data stream clock line                  | O   |
| BSM_FRAME       | BSM_FRAME          | Bit Streaming Mode Frame signal, 802.15.4 packet data stream frame line                        | O   |
| BSM_DATA        | BSM_DATA           | Bit Streaming Mode Data signal, 802.15.4 packet data stream data line                          | I/O |
| ANT_A           | ANT_A              | Antenna selection A for Front End Module support   | O   |
| ANT_B           | ANT_B              | Antenna selection B for Front End Module support   | O   |
| TX_SWITCH       | TX_SWITCH          | Front End Module Transmit mode signal  | O   |
| RX_SWITCH       | RX_SWITCH          | Front End Module Receive mode signal   | O   |

## 8.3.3 System Modules

This section contains tables describing the system signals.

**Table 56. System Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                | I/O |
|-----------------|--------------------|----------------------------|-----|
| NMI_b           | —                  | Non-maskable interrupt     | I   |
| RESET_b         | —                  | Reset bidirectional signal | I/O |
| VDD_[1:0]       | VDD                | Power supply               | I   |

*Table continues on the next page...*

**Table 56. System Module Signal Descriptions (continued)**

| SoC Signal Name            | Module Signal Name | Description   | I/O |
|----------------------------|--------------------|---|-----|
| Ground                     | VSS                | Ground  | I   |
| VDD_RF[3:1]                | VDD_RF             | Radio power supply  | I   |
| VDCDC_IN                   | VDCDC_IN           | VDCDC_IN  | I   |
| VDD_1P8OUT                 | VDD_1P8            | DCDC 1.8 V Regulated Output / Input in bypass                 | I/O |
| VDD_1P5OUT_PMCIN           | VDD_1P5/VDD_PMC    | DCDC 1.5 V Regulated Output / PMC Input in bypass (LQFN only) | I/O |
| VDD_1P5_CAP <sup>1</sup>   | VDD_1P5            | DCDC 1.5V Regulated output (WLCSP Only)                       | O   |
| VDD_1P5_PMCIN <sup>1</sup> | VDD_PMC            | PMC Input (WLCSP Only)  | I   |
| PSWITCH                    | PSWITCH            | DCDC enable switch  | I   |
| DCDC_CFG                   | DCDC_CFG           | DCDC switch mode select                                       | I   |
| DCDC_LP                    | DCDC_LP            | DCDC inductor input positive                                  | I/O |
| DCDC_LN                    | DCDC_LN            | DCDC inductor input negative                                  | I/O |
| DCDC_GND                   | DCDC_GND           | DCDC ground   | I   |

1. VDD\_1P5\_CAP and VDD\_1P5\_PMCIN should always be connected together via PCB trace. System designers should take care to ensure this connection is as short as possible.

**Table 57. LLWU Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description   | I/O |
|-----------------|--------------------|---------------|-----|
| LLWU_P[15:0]    | LLWU_P[15:0]       | Wakeup inputs | I   |

### 8.3.4 Clock Modules

This section contains tables for Clock signal descriptions.

**Table 58. Clock Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                                    | I/O |
|-----------------|--------------------|--|-----|
| EXTAL           | EXTAL              | 26 MHz/32 MHz External clock/Oscillator input  | I   |
| XTAL            | XTAL               | 26 MHz/32 MHz Oscillator input                 | I   |
| XTAL_OUT        | XTAL_OUT           | 26 MHz/32 MHz Clock output                     | O   |
| XTAL_OUT_EN     | XTAL_OUT_ENABLE    | 26 MHz/32 MHz Clock output enable for XTAL_OUT | I   |

*Table continues on the next page...*

**Table 58. Clock Module Signal Descriptions (continued)**

| SoC Signal Name | Module Signal Name | Description                                | I/O |
|-----------------|--------------------|--|-----|
| EXTAL32K        | EXTAL32K           | 32 kHz External clock/<br>Oscillator input | I   |
| XTAL32K         | XTAL32K            | 32 kHz Oscillator input                    | I   |
| CLKOUT          | CLKOUT             | Internal clocks monitor                    | O   |

### 8.3.5 Analog Modules

This section contains tables for Analog signal descriptions.

**Table 59. ADC0 Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                                  | I/O |
|-----------------|--------------------|--|-----|
| ADC0_DM0        | DADM0              | ADC Channel 0 Differential<br>Input Negative | I   |
| ADC0_DP0        | DADP0              | ADC Channel 0 Differential<br>Input Positive | I   |
| ADC0_SE[5:1]    | AD[5:1]            | ADC Channel 0 Single-ended<br>Input n        | I   |
| VREFH           | V <sub>REFSH</sub> | Voltage Reference Select<br>High             | I   |
| VDDA            | V <sub>DDA</sub>   | Analog Power Supply                          | I   |
| VSSA            | V <sub>SSA</sub>   | Analog Ground                                | I   |

**Table 60. CMP0 Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description           | I/O |
|-----------------|--------------------|-----------------------|-----|
| CMP0_IN[5:0]    | IN[5:0]            | Analog voltage inputs | I   |
| CMP0_OUT        | CMP0               | Comparator output     | O   |

**Table 61. DAC0 Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|-------------|-----|
| DAC0_OUT        | V <sub>OUT</sub>   | DAC output  | O   |

**Table 62. VREF Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                                      | I/O |
|-----------------|--------------------|--|-----|
| VREF_OUT        | VREF_OUT           | Internally generated voltage<br>reference output | O   |

### 8.3.6 Timer Modules

This section contains tables describing timer module signals.

**Table 63. TPM0 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description    | I/O |
|-----------------|--------------------|----------------|-----|
| TPM_CLKIN[1:0]  | TPM_EXTCLK         | External clock | I   |
| TPM0_CH[3:0]    | TPM_CH[3:0]        | TPM channel    | I/O |

**Table 64. TPM1 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description    | I/O |
|-----------------|--------------------|----------------|-----|
| TPM_CLKIN[1:0]  | TPM_EXTCLK         | External clock | I   |
| TPM1_CH[1:0]    | TPM_CH[1:0]        | TPM channel    | I/O |

**Table 65. TPM2 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description    | I/O |
|-----------------|--------------------|----------------|-----|
| TPM_CLKIN[1:0]  | TPM_EXTCLK         | External clock | I   |
| TPM2_CH[1:0]    | TPM_CH[1:0]        | TPM channel    | I/O |

**Table 66. LPTMR0 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description             | I/O |
|-----------------|--------------------|-------------------------|-----|
| LPTMR0_ALT[2:1] | LPTMR0_ALT[2:1]    | Pulse counter input pin | I   |

**Table 67. RTC Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description             | I/O |
|-----------------|--------------------|-------------------------|-----|
| RTC_CLKOUT      | RTC_CLKOUT         | 1 Hz square-wave output | O   |

### 8.3.7 Communication Interfaces

This section contains tables for the signal descriptions for the communication modules.

**Table 68. SPI0 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description              | I/O |
|-----------------|--------------------|--------------------------|-----|
| SPI0_PCS0       | PCS0/SS            | Chip Select/Slave Select | I/O |
| SPI0_PCS[2:1]   | PCS[2:1]           | Chip Select              | O   |
| SPI0_SCK        | SCK                | Serial Clock             | I/O |
| SPI0_SIN        | SIN                | Data In                  | I   |
| SPI0_SOUT       | SOUT               | Data Out                 | O   |

**Table 69. SPI1 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description              | I/O |
|-----------------|--------------------|--------------------------|-----|
| SPI1_PCS0       | SPI1_PCS0          | Chip Select/Slave Select | I/O |
| SPI1_SCK        | SCK                | Serial Clock             | I/O |
| SPI1_SIN        | SIN                | Data In                  | I   |
| SPI1_SOUT       | SOUT               | Data Out                 | O   |

**Table 70. I2C0 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description           | I/O |
|-----------------|--------------------|-----------------------|-----|
| I2C0_SCL        | SCL                | I2C serial clock line | I/O |
| I2C0_SDA        | SDA                | I2C serial data line  | I/O |

**Table 71. I2C1 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description           | I/O |
|-----------------|--------------------|-----------------------|-----|
| I2C1_SCL        | SCL                | I2C serial clock line | I/O |
| I2C1_SDA        | SDA                | I2C serial data line  | I/O |

**Table 72. LPUART0 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                | I/O |
|-----------------|--------------------|----------------------------|-----|
| LPUART0_CTS_b   | LPUART CTS         | Clear To Send              | I   |
| LPUART0_RTS_b   | LPUART RTS         | Request To Send            | O   |
| LPUART0_RX      | LPUART RxD         | Receive Data               | I   |
| LPUART0_TX      | LPUART TxD         | Transmit Data <sup>1</sup> | I/O |

1. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data



### 8.3.8 Human-Machine Interfaces(HMI)

This section contains tables describing the HMI signals.

**Table 73. GPIO Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                  | I/O |
|-----------------|--------------------|------------------------------|-----|
| PTA[19:16][2:0] | PORTA19-16, 2-0    | General Purpose Input/Output | I/O |
| PTB[18:16][3:0] | PORTB18-16, 3-0    | General Purpose Input/Output | I/O |
| PTC[19:16][7:1] | PORTC19-16, 7-1    | General Purpose Input/Output | I/O |

**Table 74. TSI0 Module Signal Descriptions**

| SoC Signal Name | Module Signal Name | Description                         | I/O |
|-----------------|--------------------|-------------------------------------|-----|
| TSI0_CH[15:0]   | TSI[15:0]          | Touch Sensing Input capacitive pins | I/O |

## 9 Package Information

### 9.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [nxp.com](http://nxp.com) and perform a keyword search for the drawing's document number:

**Table 75. Packaging Dimensions**

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 48-pin Laminate QFN (7x7)                | 98ASA00694D                   |
| 75-pin WLCSP (3.893x3.797)               | 98ASA00956D                   |

## 10 Revision History

**Table 76. MKW41Z Revision History**

| Rev. No. | Date    | Substantial Changes   |
|----------|---------|---|
| 4        | 03/2018 | <ul style="list-style-type: none"> <li>• Added Zigbee 3.0 in supported standards</li> <li>• Updated Flash memory protection features</li> <li>• Updated Table 12 Voltage and current operating behaviors footnotes</li> <li>• Corrected Table 21 typos</li> <li>• Updated Table 26 Reference crystal specifications verbiage</li> <li>• Updated Temperature sensor slow information (Table 33 16-bit ADC characteristics)</li> <li>• Updated DCDC converter operating requirements and specifications</li> <li>• Added DCDC pin voltage operating range to Table 52. Voltage and current operating ratings</li> </ul> |
| Rev 3    | 07/2017 | Added "32 kHz oscillator frequency specifications" table in Clock Modules section.  |
| Rev 2    | 07/2017 | <ul style="list-style-type: none"> <li>• Added WLCSP package details</li> <li>• Updated "DC-DC Converter Specifications" table</li> </ul>   |
| Rev 1    | 10/2016 | Initial Release   |

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