

TSM200N03D

Taiwan Semiconductor

Dual N-Channel MOSFET

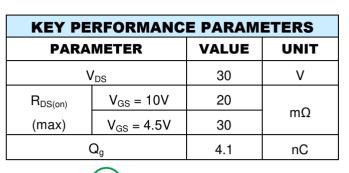
30V, 20A, 20mΩ

FEATURES

- Fast switching
- 100% avalanche tested
- Pb-free plating
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

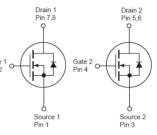
APPLICATIONS

- Power Supply
- Motor Control









Dual N-Channel MOSFET

Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RA	TINGS (T _A = 25°C u	nless otherwise not	ted)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current (Note 1)	$T_{\rm C} = 25^{\circ}{\rm C}$ $T_{\rm C} = 100^{\circ}{\rm C}$	– I _D	20 13	A
Pulsed Drain Current (Note 2)		I _{DM}	80	А
Total Power Dissipation @ $T_C = 25^{\circ}C$		P _{DTOT}	20	W
Single Pulsed Avalanche Energy (Note 3)	E _{AS}	14	mJ
Single Pulsed Avalanche Current (Note 3)		I _{AS}	17	А
Operating Junction and Storage Temperature Range		T _J ,T _{STG}	- 55 to 150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	R _{eJC}	6.4	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air



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PARAMETER	CONDITIONS	SYMBOL	MIN	ТҮР	MAX	UNIT
Static (Note 4)	I					
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV _{DSS}	30			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	V _{GS(TH)}	1.2	1.5	2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	$V_{\text{DS}} = 30V, \ V_{\text{GS}} = 0V$				1	μA
	V _{DS} = 24V, Tc = 125°C	I _{DSS}			10	
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 10A$			17	20	mΩ
	$V_{GS} = 4.5V, \ I_D = 6A$	R _{DS(on)}		23	30	
Forward Transconductance	$V_{DS} = 5V, I_D = 6A$	g _{fs}		13		S
Dynamic (Note 5)		•		•	•	1
Total Gate Charge		Qg		4.1		nC
Gate-Source Charge	$V_{DS} = 15V, I_D = 8A,$	Q _{gs}		1		
Gate-Drain Charge	$V_{GS} = 4.5V$	Q _{gd}		2.1		
Input Capacitance		C _{iss}		345		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	C _{oss}		55		pF
Reverse Transfer Capacitance		C _{rss}		32		
Switching (Note 6)						•
Turn-On Delay Time	$V_{DD} = 15V, I_D = 1A,$ $R_{GEN}=6\Omega$	t _{d(on)}		2.8		
Turn-On Rise Time		tr		7.2		
Turn-Off Delay Time		t _{d(off)}		15.8		ns
Turn-Off Fall Time		t _f		4.6		
Source-Drain Diode (Note 4)						•
Maximum Continuous Drain-Source Diode Forward Current	Integral reverse diode in the MOSFET	Is			20	A
Maximum Pulse Drain-Source Diode Forward Current		I _{SM}			80	А
Diode-Source Forward Voltage	$V_{GS} = 0V, I_{S} = 1A$	V _{SD}			1	V

Notes:

1. Current limited by package

2. Pulse width limited by the maximum junction temperature

3. L = 0.1mH, I_{AS} = 17A, V_{DD} = 25V, R_G = 25 Ω , Starting T_J = 25 $^{\circ}$ C

4. Pulse test: PW \leq 300µs, duty cycle \leq 2%

5. For DESIGN AID ONLY, not subject to production testing.

6. Switching time is essentially independent of operating temperature.



ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM200N03DPQ33 RGG	PDFN33 Dual	5Kpcs / 13"Reel

Note:

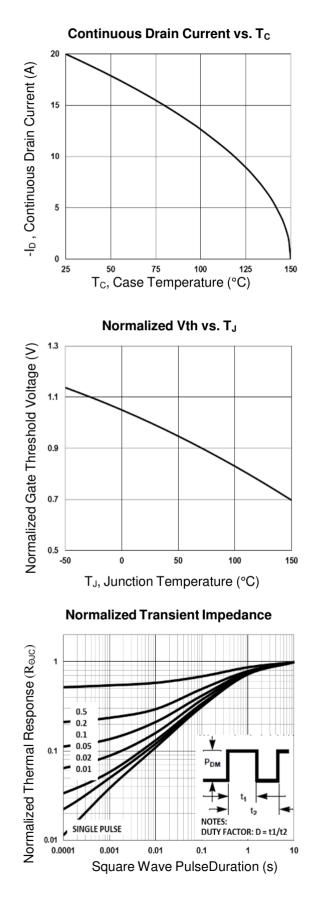
1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC

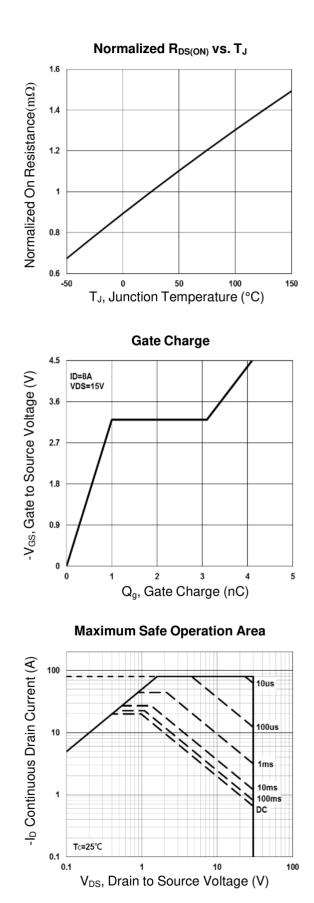
2. Halogen-free according to IEC 61249-2-21 definition



CHARACTERISTICS CURVES

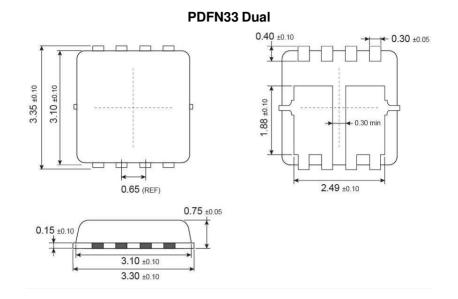
 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$



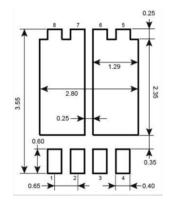




PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM

Μ



Y	= Year Code
T	= real Coue

- = Month Code for Halogen Free Product O =Jan P =Feb Q =Mar R =Apr S =May T =Jun U =Jul V =Aug W =Sep X =Oct Y =Nov Z =Dec
- L = Lot Code (1~9, A~Z)



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