ClearClockTM Oscillator Family | Ultra-Low Jitter | 3.2x2.5mm XO

AK3A

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3.2 x 2.5 x 1.0 mm RoHS/RoHS II Compliant

MSL Level = N/A

Features

- Exceptionally Low RMS Jitter: 83fs Typ (LVDS @ 156.25MHz)
- Available in industry standard frequencies between 100MHz & 212.5MHz
- ± 25 ppm stability over industrial operating temperature (-40°C to +85°C)
- 2.5V, 3.3V, 2.25V to 3.63V Continuous supply voltage options
- LVPECL, LVDS, HCSL differential output logic
- Industry standard 3.2 x 2.5 x 1.0 mm footprint
- Based on 3rd overtone, quartz crystal technology
- Available in Abracon's global distribution network
- Output Enable (Pad 1 or Pad 2 Active High) options available

Applications

• Optical Transceivers and Modules

ESD Sensitive (Pb)

- Data Centers, Storage, and Servers
- Networking switches and gateways
- 100G/200G/400G/800G Ethernet
- Fibre Channel/SONET/SDH/PCIe
- Industrial and FPGA applications
- Test & measurement

Key Electrical Specifications

Parameters		Min.	Typ.	Max.	Unit	Notes
Frequency Range		100		212.5	MHz	
Standard Available Frequencies		100.000, 114.285, 122.880, 125.000, 148.500, 150.000, 155.520, 156.250, 200.000, & 212.500		MHz	Contact Abracon for availability of frequencies not listed	
Supply Voltage (Vdd) [Note 1]		2.97	3.3	3.63		Option "A"
		2.375	2.5	2.625	V	Option "B"
		2.375		3.63		Option "D"
	LVPECL		40	60		@ 200MHz; @ Vdd=3.3V
Supply Current (Idd)	LVDS		17	35	mA	@ 200MHz; @ Vdd=3.3V
	HCSL		27	40		@ 200MHz; @ Vdd=3.3V
Operating Temperature Rang	e	-20		70	°C	Option "D"
1 0 1		-40		85		Option "F" or "Q"
Storage Temperature		-55		125	°C	
Frequency Tolerance [Note 2]		-10	< ±5	10	ppm	
Frequency Stability over [Note	: 3,4]	-15	<±10	15	ppm	Option "D" (-20°C to +70°C)
Operating Temperature Rang		-20	<±15	20		Option "Q" (-40°C to +85°C)
		-25	<±20	25		Option "F" (-40°C to +85°C)
First Year Aging		-3		3	ppm	At 25°C
All-Inclusive Frequency Acc	uracy	-40		40		Option "D" (-20°C to +70°C)
(Total Stability) [Notes 5]		-45		45	ppm	Option "Q" (-40°C to +85°C)
[Notes 5]		-50		50		Option "F" (-40°C to +85°C)
	LVPECL		0.2	0.4		@ Vdd=3.3V, R _L =50Ω
Rise (Tr) / Fall (Tf) Time [Notes 6]	LVDS		0.2	0.4		@ Vdd=3.3V, R_L =100 Ω
	LVDS		0.2	0.4	ns	@ Vdd=2.5V, R _L =100Ω
	HCSL		0.5	0.8		@ Vdd=3.3V, R_L =50 Ω to GND
	HCSL		0.5	0.8		@ Vdd=2.5V, R_L =50 Ω to GND
Duty Cycle		45		55	%	
Start-up Time [Note 3]			< 2	5	ms	

Note 1: Supply voltage (Vdd) = 2.5V and $2.375 \sim 3.63$ V options not available with LVPECL output

Note 2: Frequency Accuracy (Initial Set-Tolerance), at time of shipment (pre-reflow), relative to carrier frequency, @ +25°C

Note 3: Relative to initial measured frequency @ +25°C

Note 4: Option Q only available in select frequencies. Please contact Abracon for availability

Note 5: Includes post reflow frequency accuracy, temperature stability, load pulling, power supply variation, and 10-year aging

Note 6: Measured over 20% to 80% of waveform



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3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**





MSL Level = N/A

Parameters			Min.	Тур.	Max.	Unit	Notes	
	LVPECL	Voh	V _{dd} -1.025	V _{dd} -0.95	V _{dd} -0.88	V	$R_I = 50\Omega$ to $V_{dd} = 2.0V$	
Differential		Vol	V _{dd} -1.81	V _{dd} -1.7	V _{dd} -1.62		KL-30 52 to V dd-2.0 V	
Output High Voltage (VOH)	LVDS	Voh		1.43	1.60		R _L =100Ω between	
Output Low Voltage (VOL)		Vol	0.90	1.10			both outputs	
	HCSL	V_{OH}	0.50	0.74	0.85		R_L =50 Ω to ground	
		Vol	-0.15	0.00	0.15		on each output	
,			0.400				LVPECL	
Output Voltage Swing (Vopp)	Output Voltage Swing (Vopp)			0.350	0.450	V	LVDS	
			0.500	0.700	0.850		HCSL	
Output Enable & Disable Control			0.7*(V _{dd})			V	Output Enable or No Connect	
					0.3*(V _{dd})		Output Disable (High Impedance)	
Output Enable Time				< 1	5.0	ms		
Output Disable Time					0.2	μs		
Output Disable Current Consumption					10	μΑ	OE ≤ 0.3 V	
RMS Phase Jitter (12kHz to 20MHz from Carrier)			See Table 1 below			Vdd, output logic type and Carrier frequency dependent		

Table 1 RMS Phase Jitter 12kHz - 20MHz BW, Vdd=3.3V [Note 7, 8, 9]

INTO THASE SILLET TERMS — ZOTTITE DVV, Vuu 3.5 V						
Frequency (MHz)	Output	RMS Jitter				
Frequency (MIIIZ)	Output	Typ. (fs)	Max (fs)			
	LVDS	184	200			
100	LVPECL	166	200			
	HCSL	152	175			
	LVDS	118	150			
125	LVPECL	94	125			
	HCSL	90	115			
	LVDS	83	125			
156.25	LVPECL	64	100			
	HCSL	71	100			
	LVDS	55	100			
200	LVPECL	75	100			
	HCSL	70	100			
	LVDS	54	100			
212.5	LVPECL	72	100			
	HCSL	70	100			

Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs

Note 8: Phase jitter measured with Keysight E5052B Signal Source Analyzer

Note 9: Refer to the next section for phase noise test setup and representative phase noise plots



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3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**

MSL Level = N/A

ESD Sensitive Pb



Absolute Maximum Ratings [Note 10]

Parameters	Min.	Тур.	Max.	Unit	Notes
Supply Voltage	Vss-0.5		5	V	
Input Voltage	Vdd-0.5		$V_{DD}+0.5$	V	
Output Voltage	Vdd-0.5		V _{DD} +0.5	V	
Maximum Junction Operating Temperature			150	°C	
Ambient Operating Temperature Range	-40		85	°C	Industrial
Ambient Operating Temperature Range	-20		70	°C	Extended Commercial
Reflow Temperature			260	°C	See Reflow Profile
ESD Protection 4k		I, 300V MM,	2kV CDM		

Note 10: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.



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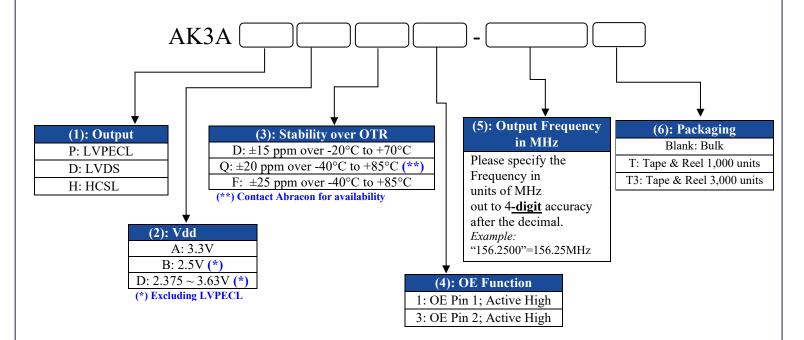
ESD Sensitive (Pb)



3.2 x 2.5 x 1.0 mm RoHS/RoHS II Compliant

MSL Level = N/A

Options and Part Identification [Note 11]



Part Number Example:

AK3APAF1-156.2500 AK3APAF1-156.2500T AK3APAF1-156.2500T3

Note 11: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal



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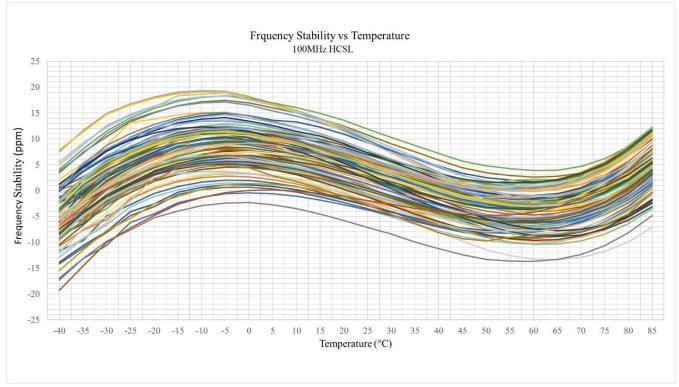
ESD Sensitive (Pb)

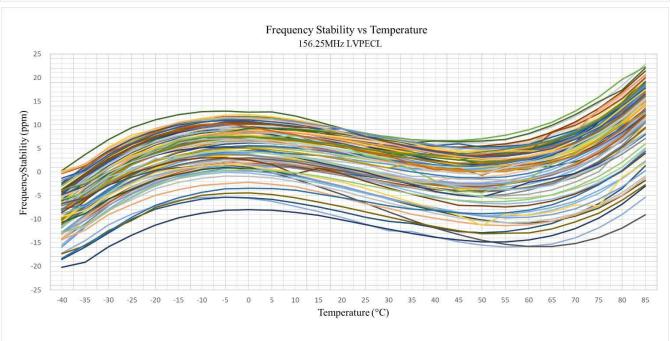


3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**

MSL Level = N/A

Typical Frequency vs. Temperature Characteristics







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Check Inventory (S)

ESD Sensitive (Pb)

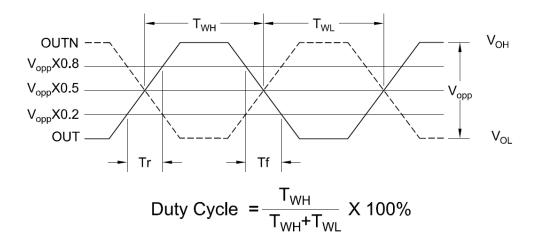


3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**

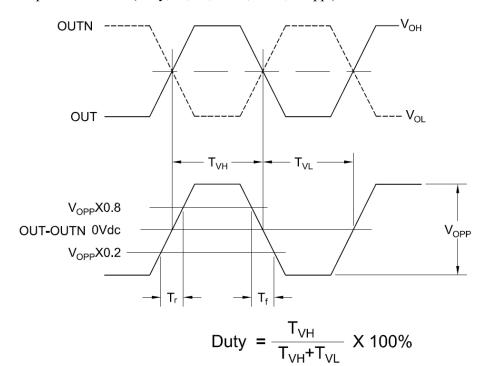
MSL Level = N/A

Differential Output Waveform

LVPECL: Output Wave Form (Duty, Tr, Tf)



LVDS: Output Wave Form (Duty, Tr, Tf, VOH, VOL, VOpp)





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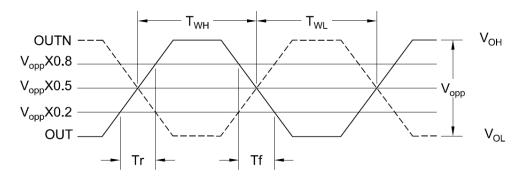


3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**

MSL Level = N/A

ESD Sensitive

HCSL: Output Wave Form (Duty, Tr, Tf, VOH, VOL, VOpp)



Duty Cycle =
$$\frac{T_{WH}}{T_{WH} + T_{WL}} \times 100\%$$



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Check Inventory



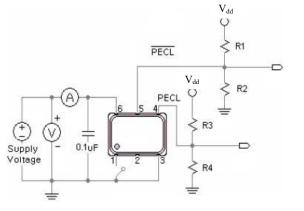
3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant** MSL Level = N/A

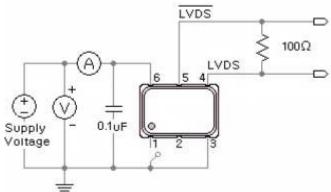
ESD Sensitive

Recommended Test Circuit [Note 12]

LVPECL

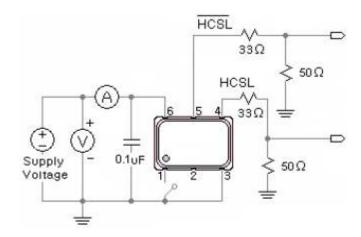
LVDS





 $Vdd= 3.3V: R1=R3=127\Omega; R2=R4=82.5\Omega$

HCSL



Note 12: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.



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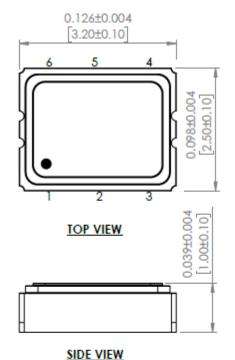
3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**

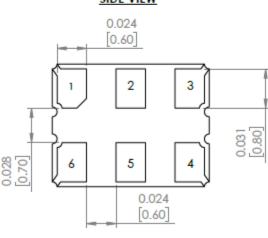
MSL Level = N/A

ESD Sensitive (Pb)



Mechanical Dimensions





BOTTOM VIEW

Recommended Land Pattern 0.035 0.012 0.90 0.30 0.094 2.40

<u>Case 1</u> Pin #1=Output Enable/Disable Function where OE is Active HIGH		Case 2 Pin #2=Output Enable/Disable Function where OE is Active HIGH		
Pin Description		Pin	Description	
# 1	Output Enable = Logic High, "1", Vdd	# 1	No Connect	
# 1	Output Disable = Logic Low, "0", GND	# 2	Output Enable = Logic High, "1", Vdd	
# 2	No Connect	# 2	Output Enable = Logic Low, "0", GND	
# 3	GND	# 3	GND	
# 4	Output	# 4	Output	
# 5	Complementary output	# 5	Complementary output	
# 6	Supply Voltage (Vdd)	# 6	Supply Voltage (Vdd)	

Dimensions: inches [mm]



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ESD Sensitive (Pb)



3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**

MSL Level = N/A

Reflow Profile [JEDEC J-STD-020]

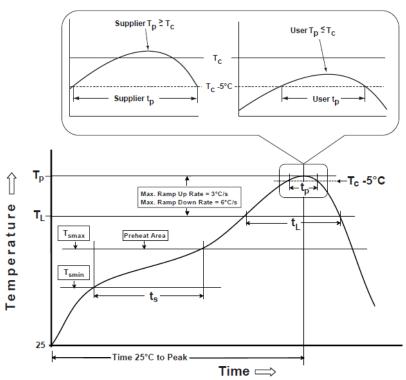


Table 1 **SnPb Eutectic Process** Classification Temperatures (Tc) Volume mm³ Package Thickness <350 <u>></u>350 <2.5 mm 235 °C 220 °C ≥2.5 mm 220 °C 220 °C

Table 2 Pb-Free Process Classification Temperatures (Tc)						
Package Thickness	Volume mm³ <350	Volume mm ³ 350-2000	Volume mm³ >2000			
<1.6 mm	260 °C	260 °C	260 °C			
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C			
>2.5 mm	250 °C	245 °C	245 °C			

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		•
Temperature minimum (T _{smin})	100°C	150°C
Temperature maximum (T _{smax})	150°C	200°C
Time (T _{smin} to T _{smax}) (t _s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T _{smax} to T _P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T _L)	183°C	217°C
Time at liquidous (t _L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T _P)*	see Table 1	see Table 2
Time (t _p)** within 5°C of the specified classification temperature (T _C)	20 sec.	30 sec.
Ramp-down rate (T _p to T _{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

^{*}Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.



^{**}Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

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ESD Sensitive (Pb)



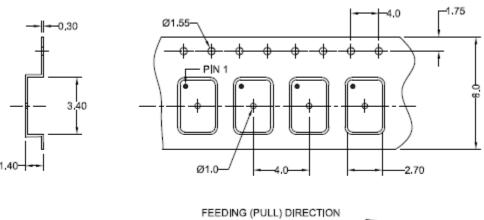
3.2 x 2.5 x 1.0 mm **RoHS/RoHS II Compliant**

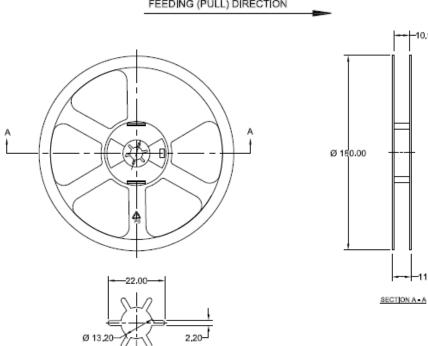
MSL Level = N/A

10,90

Packaging

Blank = BulkT = Tape & Reel 1,000 units/reel T3= Tape & Reel 3,000 units/reel





Dimensions: mm

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