NCP5680

High Efficiency White LED Driver

The NCP5680 product is a High Power charge pump driver dedicated to the recycling of a large Super Cap capacitor.

The built−in DC/DC converter is based on a high efficient charge pump structure with 1X, 1.5X and 2X operating modes. It supports double power flash LED and torch operation. The controller is designed to properly drives large external NMOS device with accurate control of the peak current flowing into the LED. Also, the chip includes Open Load and Overload Detection circuit to protect the system against faults at Vout or LED level.

Features

- 2.7 to 5.5 V Input Voltage Range
- Dual Power Flash LED Capability
- Integrated Overload Protection
- Selectable Flash/Torch Mode of Operation
- Programmable SuperCAP Re−cycling Current
- Capable to Share the DC Voltage to Supply Peripheral Circuits
- Indicator LED Function
- Integrated Photo Sense Function
- Support Camera Strobe
- Built−in Short Circuit Protection
- Selectable Flash Time Out Safety Timing
- Support External NMOS up to 10 A Load Capability
- Embedded SuperCAP Vbias
- Fully I2C Protocol Compliant
- Support GSM Synchronization
- Built−in LED Test Function
- This is a Halide−Free Device
- This is a Pb−Free Device

Typical Applications

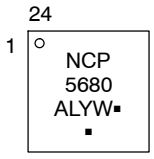
- Portable Photo Flash
- Digital Cellular Phone Camera Photo Flash

ON Semiconductor®

http://onsemi.com

UQFN24
MU SUFFIX
CASE 523AG

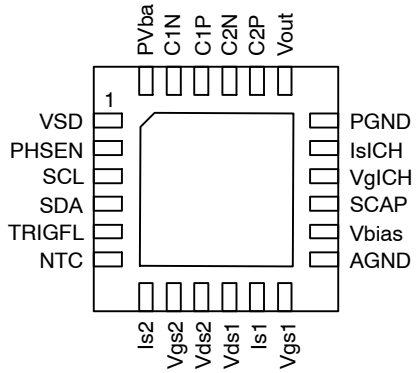
MARKING DIAGRAM



NCP5680 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP5680MUTXG	UQFN24 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

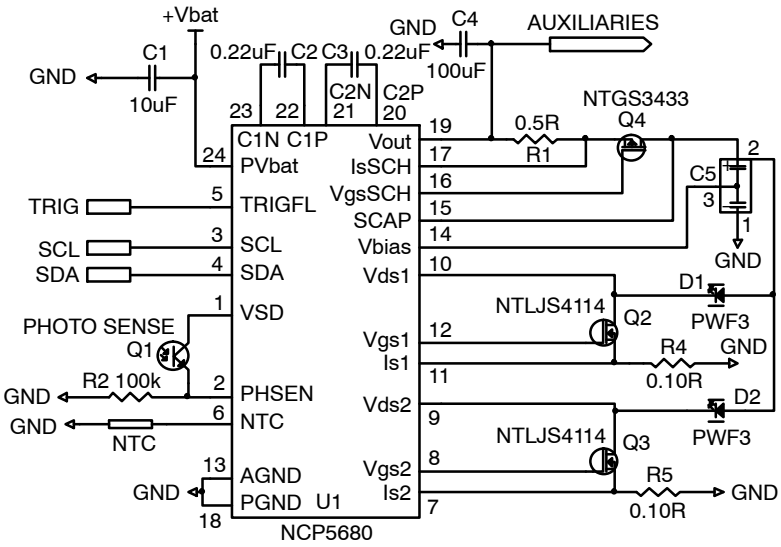


Figure 1. Typical Dual White LED Driver

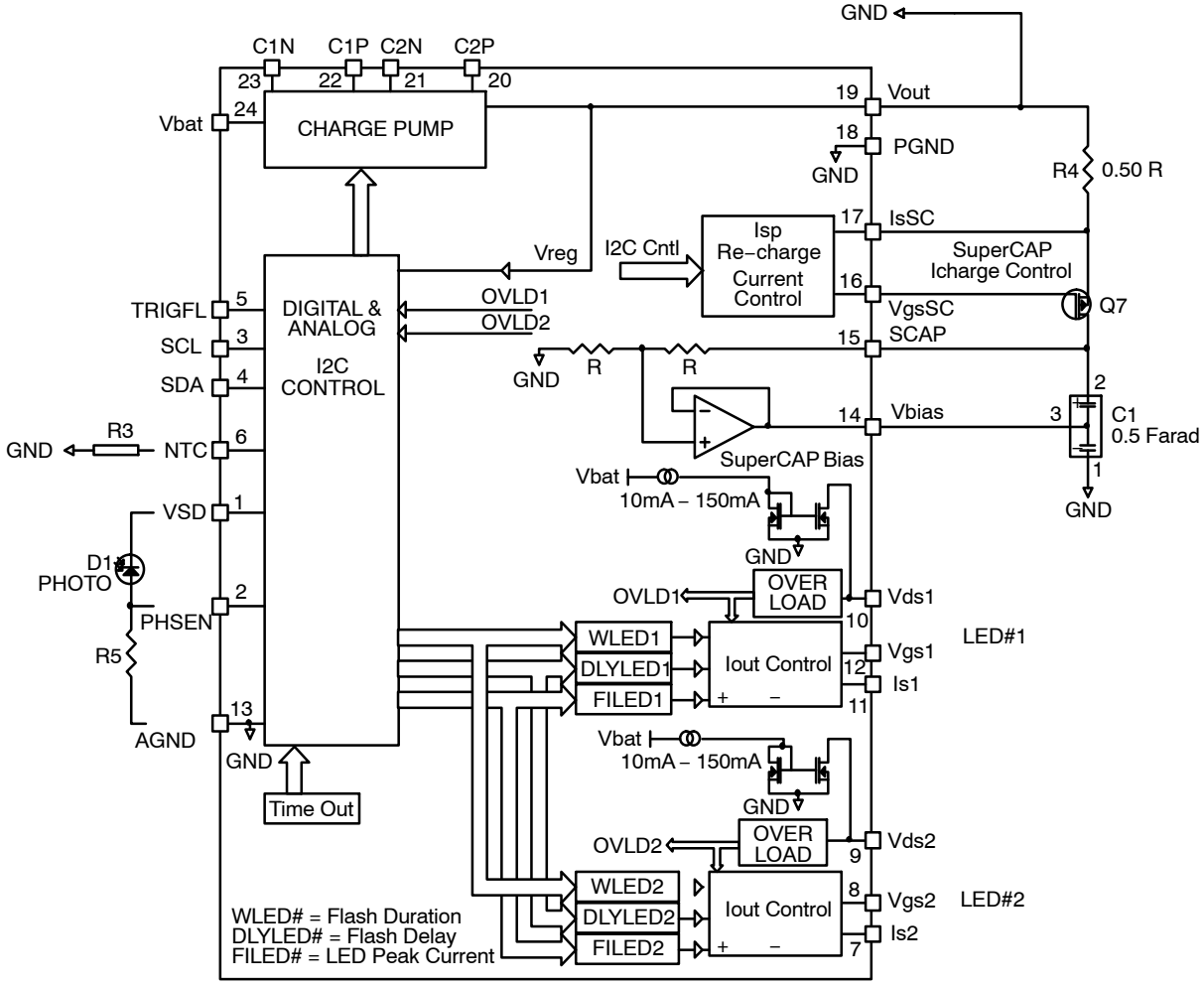


Figure 2. Simplified Block Diagram

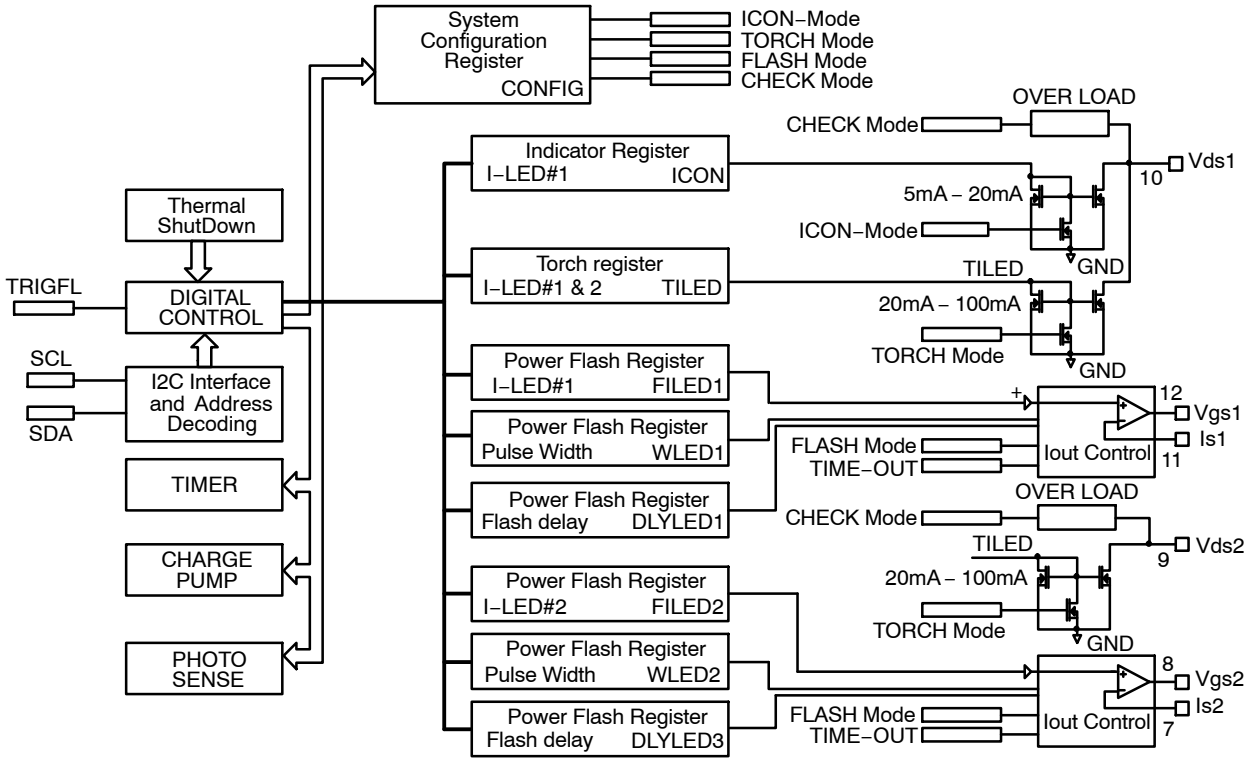


Figure 3. Simplified NCP5680 Concept

PIN DESCRIPTIONS

Pin	Name	Type	Description
1	VSD	OUTPUT, POWER	This pin provides the 2.5 V Photo sense bias voltage. The bias voltage is connected when either a flash sequence has been selected, or the ENPH bit, in the CONFIG0 register, is set High. The output current is limited to 1 mA. The same pin is used to synchronize the charge pump operation by an external digital signal (see Figure 6).
2	PHSEN	INPUT, ANALOG	This pin fulfills two functions: PHOTO SENSE FUNCTION: the pin is connected to the external photo transistor. The operating voltage is limited in the 0 V to 1.7 V range. The voltage signal developed across that pin and ground during a flash sequence is compared with the PHREF voltage (encoded in one I2C data byte) to stop the flash pulse when the illumination is completed. This function is activated by the ENPH bit of the CONFIG0 register: ENPH = 0 → the Photo sense is not activated, the flash time depends solely upon the TRIGFL pulse width, but is automatically limited by the Time out. ENPH = 1 → the Photo sense is activated, the flash time depends upon the TRIGFL duration and the amount of light reflected by the scene, but limited by the Time Out. The PHREF reference is setup by the external MCU and stored into a built−in register through the I2C lines. CHARGE PUMP SYNC: the charge pump is de−activated when an external DC voltage (V_{MSK}), in the 2.1 V to 2.5 V range, is applied to the PHSEN pin, whatever be the status of the photo sense transistor. The PHSEN resumes to the normal operation when the V_{MSK} voltage is disconnected from the pin.
3	SCL	INPUT, DIGITAL	This pin carries the I2C clock to control the DC/DC converter and to set up the output current. The SCL clock is associated with the SDA signal.
4	SDA	INPUT, DIGITAL	This pin carries the data provided by the I2C protocol. A normal I2C sequence must send the I2C address plus a pair of SDA byte to properly program the embedded registers.
5	TRIGFL	INPUT, DIGITAL	This pin supports the digital signal coming from an external peripheral to trig the flash pulse. The duration of this positive pulse drives the LED, the photo sense being a way to accurately control the illumination of the scene. The TRIGFL signal is independent from the I2C interface, assuming the supercap has been properly charged to the appropriate voltage prior to launch the flash trigger. The built−in time out makes sure the flash duration does not extend the programmed limit (ranging from 2 ms to 200 ms). In addition, an internal pull−down resistor (100 kΩ typical) makes sure the pin is not floating when it is not connected to an external network.
6	NTC	INPUT, ANALOG	This pin monitors the external Negative Temperature Coefficient resistor. A programmable constant current is provided by the pin (10 μA typical) and the internal structure compares the resulting voltage against the programmed limit, the result being a stop of the power current when V_{NTC} is lower than Vlimit.
7	Is2	INPUT, ANALOG	This pin, associated to Vgs2 and the Vout pin, returns the sense voltage, developed across the external shunt resistor, to the LED#2 current control loop. Care must be observed to avoid noise, stray capacitance and parasitic ohmic element between the shunt resistor and this point to minimize the parasitic pulses on the LED output current.
8	Vgs2	OUTPUT, POWER	This pin controls the gate of the external NMOS device and the LED is activated when the bit BLED1=1 in the Select Register byte. Care must be observed to minimize the routing between this pin and the gate of the external device. Similarly, the PCB track shall be designed to sustain the relative high current pulse flowing into the Ciss during the normal operation. The built−in driver structure is capable to control 10 A rated NMOS device with Ciss up to 2500 pF.
9	Vds2	INPUT, ANALOG	This pin fulfils two functions: − support the I−LED when the Torch mode is activated. In this case, the Gate drive Vgs1 and Vgs2 signals are deactivated. The internal current mirror, programmed by the I2C port, limits the ILED1 to 100 mA maximum. − sense the Drain voltage across the external NMOS #2 to detect the overload condition: see Table 2.

1. Using low ESR ceramic capacitor, X5R type, is mandatory to optimize the Charge Pump efficiency and to reduce the EMI. Care must be observed to prevent large influence of the ceramic capacitor DC bias: using 10 V rated capacitor, 0805 or 0603 size, is recommended.
2. Total DC/DC output current is limited to 500 mA

PIN DESCRIPTIONS

Pin	Name	Type	Description
10	Vds1	INPUT, ANALOG	This pin fulfils three functions: – support the I–LED when the Torch mode is activated. In this case, the Gate drive Vgs1and Vgs2 signals are deactivated. The internal current mirror, programmed by the I2C port, limits the ILED2 to 100 mA maximum – support the Indicator LED current when this mode is activated. In this case, the Vgs1 and Vgs2 signals are deactivated. The internal current mirror, programmed by the I2C port, limits the ILED1 to 20 mA maximum – sense the Drain voltage across the external NMOS #2 to detect the overload condition: see Table 2.
11	Is1	INPUT, ANALOG	This pin, associated to Vgs1 and the Vout pin, returns the sense voltage, developed across the external shunt resistor, to the LED#1 current control loop. Care must be observed to avoid noise, stray capacitance and parasitic ohmic element between shunt resistor and this point to minimize the parasitic pulses on the LED output current.
12	Vgs1	OUTPUT, POWER	This pin controls the gate of the external NMOS device and the LED is activated when the bit BLED0=1 in the Select Register byte. Care must be observed to minimize the routing between this pin and the gate of the external device. Similarly, the PCB track shall be designed to sustain the relative high current pulse flowing into the Ciss during the normal operation. The built–in driver structure is capable to control 10A rated NMOS device with Ciss up to 2500 pF.
13	AGND	OUTPUT, POWER	This pin carries the return to ground of the analog and digital blocks and must be connected to the external ground plane.
14	Vbias	OUTPUT, Bias	This pin provides the bias voltage necessary to drive the supercap capacitor. The Vbias voltage is equal to Vout/2 and shall not be overloaded.
15	SCAP	INPUT, ANALOG	This pin senses the voltage developed across the external SuperCAP. This voltage is fed back to the Vbias network to maintain the appropriate bias voltage at the superCAP mid point.
16	Vg_{ICH}	OUTPUT, ANALOG	This pin drives the gate of the external PMOS associated to the superCAP current control loop. Such a function might be omitted when not necessary in the final application. In this case, a direct contact can be set–up between the Vout pin and the external SuperCAP capacitor, the current being limited to 500 mA maximum.
17	Is_{ICH}	INPUT, ANALOG	This pin, associated with the Vg_{ICH} signal, is the return of the SuperCAP charge current sense. An external shunt resistor shall be connected between Vout and the external PMOS drain to monitor the superCAP charge current.
18	PGND	OUTPUT, POWER	These pins carry the ground return of the DC/DC converter and must be connected to the external ground plane. Since this pin provides the current charge path for the external Super Cap capacitor, cares must be observed to minimize both the ESR and the ESL parasitic elements between the Super cap negative electrode and these pins. Using ground plane technique is highly recommended.
19	Vout	OUTPUT, POWER	This pin provides the output voltage supplied by the DC/DC converter and must be bypassed by a 10 μF ceramic capacitor minimum located as close as possible to the pin. The circuit shall not operate without such bypass capacitor properly connected to the Vout pin. The converter supplies 500 mA maximum continuous current to total external load. Consequently, the re–cycling time depends upon the Super Cap capacitance value, the operating Vbat input supply voltage and the programmed I_{ICH}. The output voltage is internally clamped to 5.5 V maximum in the event of no load situation. On the other hand, the output current is limited to 100 mA (maximum) in the event of a short circuit to ground.
20	C2P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2N pin.
21	C2N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2P.
22	C1P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1N pin.
23	C1N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1P.
24	Vbat	INPUT, POWER	This pin is connected to the input Battery voltage to supply all the built–in blocks. The pin must be connected to the Power plane and decoupled to ground by a 10 μF ceramic capacitor minimum.

1. Using low ESR ceramic capacitor, X5R type, is mandatory to optimize the Charge Pump efficiency and to reduce the EMI. Care must be observed to prevent large influence of the ceramic capacitor DC bias: using 10 V rated capacitor, 0805 or 0603 size, is recommended.
2. Total DC/DC output current is limited to 500 mA

MAXIMUM RATINGS (Note 3)

Symbol	Rating	Value	Unit
V_{BAT}	Power Supply	−0.3 < Vbat < 7.0	V
Vout	Output Power Supply	6.0	V
SCL, SDA, TRIGFL	Digital Input Voltage Digital Input Current	−0.3 < V < V_{BAT} 1	V mA
ESD	Machine Model (Note 4)	200	V
P_D $R_{\theta jc}$ $R_{\theta ja}$	UQFN24 package − Power Dissipation @ T_A = +85°C (Note 5) − Thermal Resistance Junction to Case − Thermal Resistance Junction to Air	40 11 160	mW °C/W °C/W
T_A	Operating Ambient Temperature Range	−40 to +85	°C
T_J	Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature Range	−65 to + 150	°C
	Latch−up current maximum rating per JEDEC standard: JESD78.	±100	mA

3. Maximum electrical ratings define the values beyond which permanent damage(s) may occur internally to the chip whatever be the operating temperature
4. This device series contains ESD protection and exceeds the following tests:
   Standard ESD protections must be used when handling any integrated circuit.
   Appropriate ESD techniques must be observed to avoid damage to the device
   Machine Model (MM) ±200V per JEDEC standard: JESD22−A115
5. The maximum package power dissipation limit must not be exceeded.
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

POWER SUPPLY SECTION: (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < V_{bat} < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
24	V_{bat}	Power Supply	2.7		5.5	V
19	I_{out}	Continuous DC Current in the Load @ 3.0 V < V_{bat} < 3.2 V (Note 12) @ 3.6 V < V_{bat} < 5.5 V (Note 12)			220 400	mA
19	I_{scL} I_{scH}	Continuous Output Short Circuit Current		50 100		mA
19	V_{out}	Output Voltage Regulation (4.5 V < V_{out} < 5.3 V) (See Table 5)	−100		+100	mV
19	Tcy	DC/DC Re−Cycling Time (Cout = 0.50 Farad), V_{bat} = 4.2 V, I_{ICH} = 500 mA. From the end of the previous flash to the full load operation		2		s
24	I_{stdb}	Stand By Current, V_{bat} = 3.6 V, I_{out} = 0 mA, DC/DC = Off, V_{bias} = Off			1.0	μA
24	I_{op}	Operating Current, @ I_{out} = 0 mA, V_{bat} = 3.6 V following a reset state		0.6		mA
7, 11	I_{FTOL}	Power Flash Output Current Tolerance: −25°C < T_A < 85°C (Note 8) @V_{bat} = 3.8 V, I_{LED} ≥ 500 mA (See Figure 10)	 −5		 +5	%
9, 10	I_{TTOL}	Torch Output Current Tolerance I Torch @ Vds1 (Note 10) I Torch @ Vds2 (Note 10)	−15 10 10		+15 100 100	% mA mA
10	I_{IND}	Indicator LED Current − Indicator Mode @ Vds1 (Note 11)	−25 0.1		+25 6.3	% mA
	Fpwr	Clock Operating Frequency @ T_A = 25°C	0.85	1.0	1.15	MHz

7. The external shunt resistor shall be ±1% tolerance or better
8. The external sense resistor shall be ±1% tolerance or better
9. The maximum LED current depends upon the external NMOS device
10. The Vgs1 and Vgs2 pins are deactivated when the Torch mode is operating
11. The Vgs1 and Vgs2 pins are deactivated when the Indicator mode is operating
12. Parameter characterized, not tested in production, guaranteed by design.

PROGRAMMABLE AND POWER UP PRESET CONDITION SECTION

Pin	Symbol	Rating	Min	Typ	Max	Unit
19	I_{ICH}	Programmable SuperCAP Re−Charge Current Range A ±8% tolerance applies to each step of the five steps (Note 7)	100		500	mA
7, 11	I_{FLSH}	Programmable Flash Output Current Range (Note 8) See Figure 10	0.4		6.3	A
7, 11	Tpfl	Programmable Power Flash Width Range	0.01		255	ms
7, 11	Tout	Automatically Preset Power Flash Security Time Out @ Power Up		50		ms

ANALOG SECTION: (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < V_{bat} < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
14	I_{bias}	Super Cap Bias Voltage Current Capability (V_{bias} = V_{CC}/2)	1.0			mA
1	V_{VSD}	Photo Sense Supply @ Iph = 2 mA	2.5			V
2	V_{PHSEN}	Input Photo Sense Voltage			1.7	V
6	V_{NTC}	Input Negative Coefficient Sensor Voltage (See NTCREG Register)			2.0	V
2	V_{MSK}	Input Synchronization Transmit Mask	2.1		2.5	V
5	R_{TRG}	Internal Pull−Down Resistor		100		kΩ
7, 11	V_{iref}	Input Voltage to Current Conversion across the Shunt Resistor during a Flash Sequence @ R_{sense} = 0.1 Ω (Notes 12 and 13)	95	100	105	mV/A
	T_{SD}	Thermal Shutdown		145		°C
	T_{SDh}	Thermal Shutdown Hysteresis		20		°C

13. The overall output current tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.

DIGITAL PARAMETERS SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < V_{bat} < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
3	F_{SCL}	Input I2C Clock Frequency (Note 12)			400	kHz
3, 4	V_{IH}	Positive going Input High Voltage Threshold, TRIGFL, SDA & SCL signals	1.6		V_{bat}	V
3, 4	V_{IL}	Negative going Input Low Voltage Threshold, TRIGFL, SDA & SCL signals	0		0.4	V

14. Maximum efficient power flash duration T_{FW} depends upon the reservoir capacitor and the LED current.

NOTE: Digital inputs undershoot < − 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{bat}

REGISTER SELECTION BITS

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0	
0	00	0	0	0	0	0	0	0	0	SDN Shut Down command
1	01	0	0	0	0	0	0	0	1	CONFIG0
2	02	0	0	0	0	0	0	1	0	CONFIG1 register
3	03	0	0	0	0	0	0	1	1	FILED1: set up the Power Flash LED1
4	04	0	0	0	0	0	1	0	0	FILED2: set up the Power Flash LED2
5	05	0	0	0	0	0	1	0	1	RFU
6	06	0	0	0	0	0	1	1	0	TILED: set up the Video/Torch LED current (LED1 = LED2)
7	07	0	0	0	0	0	1	1	1	FLDLY1: set up the time delay Start to LED1
8	08	0	0	0	0	1	0	0	0	FLDLY2: set up the time delay LED1 to LED2
9	09	0	0	0	0	1	0	0	1	RFU
10	0A	0	0	0	0	1	0	1	0	FLWID1: set up the Power Flash pulse width LED1
11	0B	0	0	0	0	1	0	1	1	FLWID2: set up the Power Flash pulse width LED2
12	0C	0	0	0	0	1	1	0	0	RFU
13	0D	0	0	0	0	1	1	0	1	PHSEN: set up the Photo sense range
14	0E	0	0	0	0	1	1	1	0	PHGAIN: set up the input amplifier gain
15	0F	0	0	0	0	1	1	1	1	VOUTREG: set up the Vout voltage
16	10	0	0	0	1	0	0	0	0	INMDE: set up the Indicator mode (ICON)
17	11	0	0	0	1	0	0	0	1	NTCREG: set up the NTC low limit
18	12	0	0	0	1	0	0	1	0	NTCBIAS: set up the DC bias current to NTC
19	13	0	0	0	1	0	0	1	1	ICHG: set up the superCAP re−charge current
20	14	0	0	0	1	0	1	0	0	TOUT: set up the Power flash time out
21	15	0	0	0	1	0	1	0	1	RFU
22	16	0	0	0	1	0	1	1	0	RFU
23	17	0	0	0	1	0	1	1	1	STATUS
24	18	0	0	0	1	1	0	0	0	RFU
25	19	0	0	0	1	1	0	0	1	Reserved for manufacturing test: *do not access*

NOTE: All register addresses beyond $18 are reserved for ON Semiconductor manufacturing tests and shall not be R/W in the application.

FUNCTIONS PROGRAMMING REGISTERS

$00 – SDN Shut Down command
$01 – CONFIG0
$02 – CONFIG1 register
$03 – FILED1 : set up the Power Flash LED1
$04 – FILED2 : set up the Power Flash LED2
$06 – TILED : set up the Video/Torch LED current
$07 – FLDLY1: set up the time delay Start to LED1
$08 – FLDLY2 : set up the time delay Start to LED2
$0A – FLWID1: set up the Power Flash pulse width LED1
$0B – FLWID2: set up the Power Flash pulse width LED2
$0D – PHSEN: set up the Photo sense range
$0E – PHGAIN : set up the input amplifier gain
$0F – VOUTREG: set up the Vout voltage
$10 – INMDE: set up the Indicator mode (ICON)
$11 – NTCREG : set up the NTC low limit
$12 – NTCBIAS : set up the DC bias current to NTC
$13 – ICHG: set up the superCAP re−charge current
$14 – TOUT : set up the Power flash time out
$17 – STATUS

																		COMMENTS
Shutdown																	X	send %0000 0000
RESET															X			send % 1xxx xxxx
Set Pre Charge															X			send %xxxx xx1x
Set Charge Pump															X			send %xxxx x1xx
Set Vout						X												send %0000 0000 to %0000 0111
SetUp ICHG superCAP			X															send %0000 0000 to %0000 0111
Set up the NTC bias current				X														send %0000 0000 to %0011 1111
Set up the NTC reference voltage					X													send %0000 0000 to %0001 1111
Enable/Disable the NTC function																X		send % xx1x xxxx
Select Flash mode															X			send % xx1x xxx0
Select Torch/Video mode															X			send % xx0x xxx0
Select Indicator/Icon mode															X			send % xx0x xxx1
SetUp ILED indicator						X												send %0000 0000 to %0011 1111
SetUp IFLASH#1														X				send %0000 0000 to %0011 1111
SetUp IFLASH#2													X					send %0000 0000 to %0011 1111
Enable LED#1																X		send % xxxx xxx1
Enable LED#2																X		send % xxxx xx1x
Set Time Out	X																	send %0000 0000 to %0111 1111
Set Pulse Width LED#1										X								send %0000 0000 to %1111 1111
Set Pulse Width LED#2									X									send %0000 0000 to %1111 1111
Set Delay Flash LED#1												X						send %0000 0000 to %1111 1111
Set Delay Flash LED#2											X							send %0000 0000 to %1111 1111
Set Flash Trigger :I2C/External															X			Send % xxx1 xxxx
SetUp ITORCH													X					send %0000 0000 to %0011 1111
Activate/Deactivate Photo Sense																X		Send% xxx1 xxxx
SetUp Photo Sense Refrence								X										send %0000 0000 to %1111 1111
SetUp Check Sequence																X		
Read STATUS register	X																	

Table 1. Functions Programming Table

INTERNAL REGISTERS DESCRIPTION

SDN[7..0] Shut Down command $00

	B7	B6	B5	B4	B3	B2	B1	B0
RESET	0	0	0	0	0	0	0	0

SDN[7:0] = → NCP5680 is in Shut Down mode, all the LED are switched to the OFF state, the previously programmed parameters are stored into their respective registers. The Vout voltage is no longer controlled by the chip and the SuperCap is disconnected from the Vbat. The SuperCap voltage bias is maintained until the Vout voltage is below 2 V.

Although the third byte could carry any data when an SDN command is transmitted, it is preferred to force all the 8 bits to zero. Consequently, a typical shut down command shall be: $I2C Address – $00 – $00.

Note: there is no internal structure to rapidly discharge the SuperCap: it is up to the external circuit to take whatever action is necessary to cope with the end application.

CONFIG0[7..0] Configuration register $01

	B7	B6	B5	B4	B3	B2	B1	B0
	TPLGT	ENTC	ICHG	ENPH	CKPLS	CKPRC	BKL2	BKL1
RESET	0	0	0	0	0	0	0	0

TPLGT: activate the 200 ms time out associated to the Picture Light function.

TPLGT = 0 → the 200 ms is de−activated

TPLGT = 1 → the 200 ms time out is activated and apply to the Picture Light only.

Note: the 200 ms time out is automatically asserted when the TILED current is higher than 100 mA.

ENTC: control the NTC input function

ENTC = 0 → the external NTC is de−activated and no action is forwarded to the Power Flash current block.

ENTC = 1 → the external NTC is biased by the internal current and the Power flash current is switched OFF when the NTC drops below the minimum level defined by the NTCREG register

ICHG: control the superCAP charging current during a start up sequence

ICHG = 0 → the charging current is limited to 250 mA maximum (125 mA typical)

ICHG = 1 → the charging current is limited to 350 mA maximum (250 mA typical)

ENPH: control the photo sense

ENPH = 0 → the photo sense is de−activated

ENPH = 1 → the photo sense is activated

CKPLS: this bit controls the LED1 & LED2 internal check during a flash sequence

CKPLS = 0 → no LED check performed during a flash sequence

CKPRC = 1 → the LED check are automatically performed, during a flash sequence, the results can be read from the STATUS register. If a fault is detected at any time during a flash pulse, the flash sequence is immediately stopped.

CKPRC: this bit controls the LED1 & LED2 internal check out of a flash sequence.

CKPRC = 0 → no LED check performed

CKPRC = 1 → the LED check are automatically performed (both LED1 and LED2), the results can be read from the STATUS register.

BKL1: = LED2 control

BKL = 0 → LED2 de−activated

BKL = 1 → LED2 activated

BKL0: = LED1 control

BKL = 0 → LED1 de−activated

BKL = 1 → LED1 activated

CONFIG1[7..0] Configuration register $02

	B7	B6	B5	B4	B3	B2	B1	B0
	RESET	CPFL	SELFL	I2CTRG	EXTRG	CPACT	SACT	ENIND
RESET	0	0	0	0	0	0	0	0

RESET:

B7 = 1 → unconditionally clear all the registers to their respective zero state.

CPFL:

B6 = 0 → the charge pump is de−activated when a power flash sequence is on going

B6 = 1 → the charge pump is fully active during a power flash sequence.

SELFL:

B5 = 0 → the Torch / Video mode is engaged, the flash cannot be fired, the ILED current is limited to 100 mA/LED.

B5 = 1 → the Flash mode is engaged, the flash can be fired.

I2CTRG:

B4 = 0 → when an I2C flash sequence is on going, the flash is immediately stopped by this I2C command.

B4 = 1 → The flash is immediately launched by the I2C when this bit is High, unless the EXTRG bit is high. In this case, the external Trigger pulse has the highest priority.

EXTRG:

B3 = 0 → The TRGFL pin is de−activated, the flash can be launched by the I2C port only

B3 = 1 → The Photo Flash sequence is activated by the positive going pulse applied to the TRGFL pin, the duration of the Flash Pulse being identical to the TRGFL pulse width. The Time out is activated. The two LED are simultaneously powered, unless one of the two LED is not activated, according to the CONFIG0 register setup.

CPACT:

B2 = 0 → the charge pump is de−activated

B2 = 1 → the NCP5680 and the Charge Pump are active. The Vout voltage is equal to the programmed value stored into VOUTREG register. All the LED are biased as defined in the previous or next programming sequence. A flash can be launched.

SACT:

B1 = 0 → the NCP5680 is active, but the pre−charge is de−activated. If the CPACT is Low, the Vout voltage will be low. If the CPACT bit is High, then the Vout voltage will be equal to the programmed value.

B1 = 1 → the NCP5680 is active, the pre−charge is activated. The Vout voltage is equal to the Vbat voltage, unless the Charge pump is activated (CPACT = 1). All the LED are biased as defined in the previous or next programming sequence. A power limited flash can be launched.

ENIND:

B0 = 0 → the Indicator function is de−activated

B0 = 1 → the Indicator function is activated.

FILED1[7..0] Power Flash LED1 ILED register $03

	B7	B6	B5	B4	B3	B2	B1	B0
mA	0	0	3200	1600	800	400	200	100
RESET	0	0	0	0	0	0	0	0

FILED2 [7..0] Power Flash LED2 ILED register $04

	B7	B6	B5	B4	B3	B2	B1	B0
mA	0	0	3200	1600	800	400	200	100
RESET	0	0	0	0	0	0	0	0

TILED [7..0] Torch / Video / Picture View/ View Finder LED1 & LED2 register $06

	B7	B6	B5	B4	B3	B2	B1	B0
mA	0	128	64	32	16	8	4	2
RESET	0	0	0	0	0	0	0	0

NOTE: The 200 ms time out is automatically asserted when TILED is higher than 100 mA. The TILED current is maintained constant when TILED is equal or lower than 100 mA.

FLDLY1[7..0] Power flash Delay #1 register $07

	B7	B6	B5	B4	B3	B2	B1	B0
ms	256	128	64	32	16	8	4	2
RESET	0	0	0	0	0	0	0	0

NOTE: Tolerance of the Fpwr Clock parameter applies to the timing parameters.

FLDLY2[7..0] Power flash Delay #2 register $08

	B7	B6	B5	B4	B3	B2	B1	B0
ms	256	128	64	32	16	8	4	2
RESET	0	0	0	0	0	0	0	0

NOTE: Tolerance of the Fpwr Clock parameter applies to the timing parameters.

FLWID1[7..0] Power flash LED1 width register $0A

	B7	B6	B5	B4	B3	B2	B1	B0
ms	128	64	32	16	8	4	2	1
RESET	0	0	0	0	0	0	0	0

NOTE: Tolerance of the Fpwr Clock parameter applies to the timing parameters.

FLWID2[7..0] Power flash LED2 width register $0B

	B7	B6	B5	B4	B3	B2	B1	B0
ms	128	64	32	16	8	4	2	1
RESET	0	0	0	0	0	0	0	0

NOTE: Tolerance of the Fpwr Clock parameter applies to the timing parameters.

PHSEN[7..0] Photo Sense Reference register $0D

	B7	B6	B5	B4	B3	B2	B1	B0
mV	1280	640	320	160	80	40	20	10
RESET	0	0	0	0	0	0	0	0

NOTE: a ±12.5% tolerance applies to each bit of the PHSEN register

PHGAIN[7..0] Photo Sense Input Amplifier gain register $0E

	B7	B6	B5	B4	B3	B2	B1	B0
gain	0	8	4	2	1	0.5	0.25	0.125
RESET	0	0	0	0	0	0	0	0

NOTE: a ±10% tolerance applies to each bit of the PHGAIN register

VOUTREG[7..0] Vout Adjustment register $0F

	B7	B6	B5	B4	B3	B2	B1	B0
mV	0	0	0	0	0	800	400	200
RESET	0	0	0	0	0	0	0	0

NOTE: The Vout voltage must be reduced to the minimum value when the Torch/Video mode is activated: see the Torch/Video paragraph and the Thermal Consideration note.

INMDE[7..0] Indicator mode register $10

	B7	B6	B5	B4	B3	B2	B1	B0
μA	0	0	3200	1600	800	400	200	100
RESET	0	0	0	0	0	0	0	0

NTCREG[7..0] External NTC low limit register $11

	B7	B6	B5	B4	B3	B2	B1	B0
mV	CNTC	0	0	1600	800	400	200	100
RESET	0	0	0	0	0	0	0	0

CNTC: a positive going pulse clears the NTC high temperature limit and clear the STATUS[NTC] bit. The bit shall be Low to resume NTC normal operation.

NOTE: a ±15% tolerance applies to each bit of the NTCREG register

NTCBIAS[7..0] NTC current bias register $12

	B7	B6	B5	B4	B3	B2	B1	B0
μA	0	0	320	160	80	40	20	10
RESET	0	0	0	0	0	0	0	0

NOTE: a ±10% tolerance, measured at V_{bat} = 3.6 V, applies to each bit of the NTCBIAS register

ICHG[7..0] SuperCAP re−charge current register $13

	B7	B6	B5	B4	B3	B2	B1	B0
	TOUTDIS2	TOUTDIS1	0	0	0	400 mA	200 mA	100 mA
RESET	0	0	0	0	0	0	0	0

NOTE: TOUTDIS1 & TOUTDIS2: these two bits are used to disconnect the Time Out function when B7 and B6 are High:
B7 or B6 = 0 --> the Time Out function is active and operate normally.
B7 = B6 = 1 --> the Time Out function is de-activated

STATUS[7..0] System LED check READ register $17

	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	0	SLED2	SLED1	RFU	VDS2	VDS1
READ only	RDY	NTC	0	0	0	0	0	0

RDY: Output Capacitor status:
0 → Output capacitor not fully charged yet
1 → Output capacitor fully charged to the programmed voltage

NTC: external thermal sensor flag
0 → a high temperature has been sensed by the NTC. All the power blocks are de−activated (Charge pump, flash and Torch/Video)
1 → normal operation, no high temperature detected.
B5 = RFU

SLED2: LED#2 Check 0 → LED#2 A/K Short Circuited
1 → Pin OK

SLED1: LED#1 Check 0 → LED#1 A/K Short Circuited
1 → Pin OK
B2 = RFU

VDS2: LED#2 Check 0 → Pin connection or LED#2 OPEN
1 → Pin OK

VDS1: LED#1 Check 0 → Pin connection or LED#1 OPEN
1 → Pin OK

TOUT[7..0] Time Out register $14

	B7	B6	B5	B4	B3	B2	B1	B0
ms	256	128	64	32	16	8	4	2
RESET	0	0	0	1	1	0	0	1

The minimum time out is preset at 50 ms.

NOTE: Tolerance of the Fpwr Clock parameter applies to the timing parameters.

“The Time Out function can be de-activated to generate the infinite operation requested by the Video mode. To achieve such a function, the here below logic conditions must be met:

– ICHG register: bits B7 = B6 = 1

– CONFIG1 register: bit B3 = 1 (external trigger flash only)

– FILED1 and FILED2 must be lower or equal to 500 mA each

The Time out is maintained is any of the three conditions is not fulfilled.”

DC/DC Operation

The converter is based on a charge pump technique to generate a constant DC voltage capable to either re−charge the external Super Cap, or to drive the LED in the torch mode. The system regulates the current flowing into the LED by means of an internal current mirror associated with the external shunt resistor and the external power NMOS. The output voltage is adjusted and regulated in the range 4.5 V to 5.5 V across the external Super Cap reservoir, the NMOS device being used as a current controlled source to drive the LED. When the DC/DC is not active, the voltage across the external reservoir capacitor is either zero or equal to the voltage present at the Vbat pin, depending upon the operation defined by the SACT bit in the CONFIG1 register.

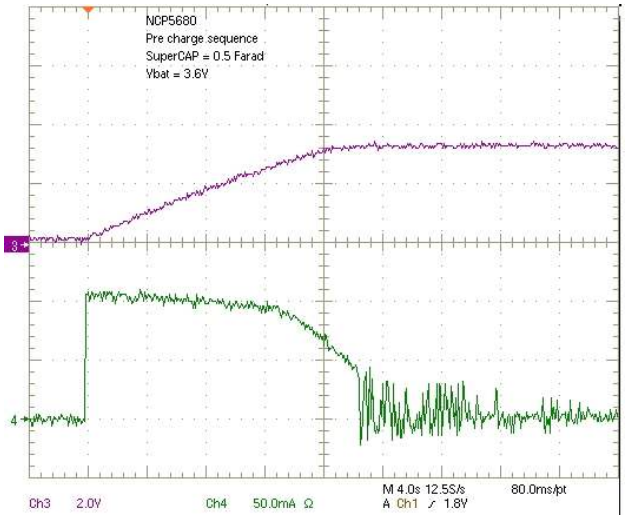


Figure 4. Typical Pre Charge Sequence

The output current is setup by the external reference resistor connected between Vout and the LED. With a 100 mV drop across the shunt resistor, the forward current into the LED being: ILed = 0.10/R. The shunt resistor must be sized to sustain the amount of current flowing during the operation.

The Vout voltage is continuously monitored and the charge pump stops when the voltage is above the maximum programmed value. The converter resumes to normal operation when the voltage drops below the programmed value (there is no fault latched since the converter operates in the hysteretic regulation mode). Consequently, the chip can operate under no load conditions during any test procedures with no risk in term of OVP situation.

However, when the check routine is activated, the voltage present at the drain of the external NMOS is monitored to detect fault condition that might develop in the power flash structure according to Table 2.

Table 2. LED Drive Overload Detection Conditions

Vds	NCP5680 status	Fault
0 V	Standby	LED open or Cathode to ground shorted
0 V	Pulsed Flash	LED open or Cathode to ground shorted
0 V < Vds < Vout	Standby	Normal operation, no fault
= Vout	Standby	Anode to Cathode LED shorted
> 2.0 V	Pulsed Flash	Anode to Cathode LED shorted, Charge pump de−activated, flash de−activated

When the check routine is activated, the result is stored into the STATUS register and can be read back by the I2C port.

On the other hand, the external SuperCAP re−charge current can be programmed, through the I2C port, to better handle the total energy demand. The three bits present in the ICHG register makes possible the adjustment of the re−charge current from 100 mA to 500 mA, keeping in mind that the charge pump is designed to supply up to 500 mA maximum.

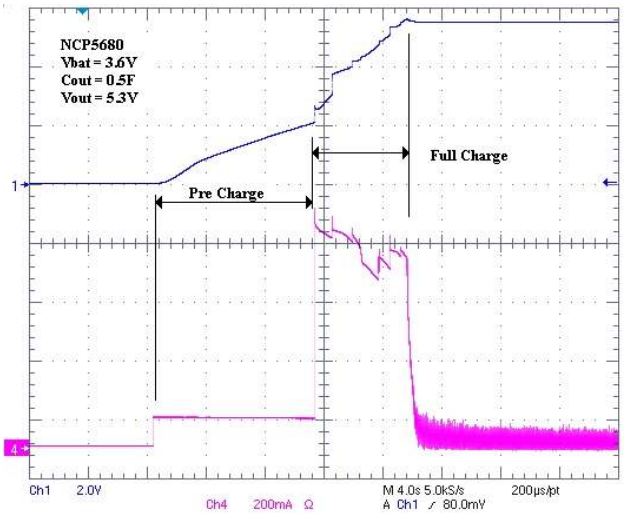


Figure 5. Typical Pre Charge and Full Charge Sequence

Finally, the charge pump can be de−activated, upon command from the MCU, during a transmit burst pulse applied to the PHSEN pin: see typical schematic Figure 6. In this case, any on going flash keeps going, but no energy is absorbed from the battery as depicted in Figures 7 and 8.

Similarly, the burst function can be used to smooth the input battery current as depicted in Figure 9.

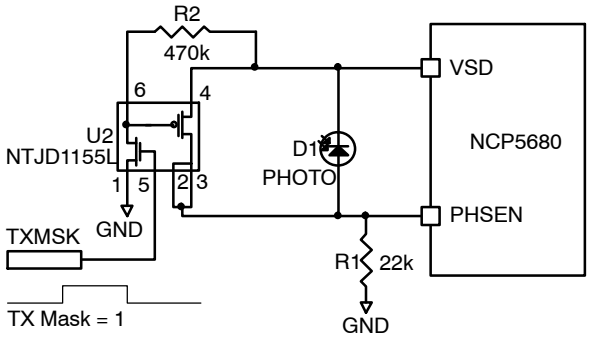


Figure 6. Typical Transmit Burst Mask

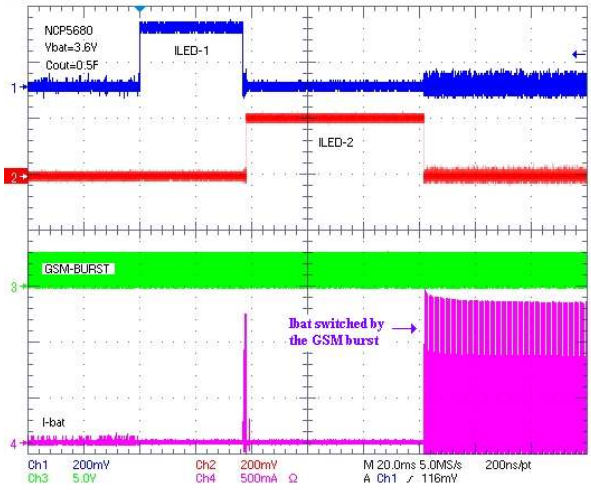


Figure 7. GSM Burst during the Re−charge of the SuperCAP

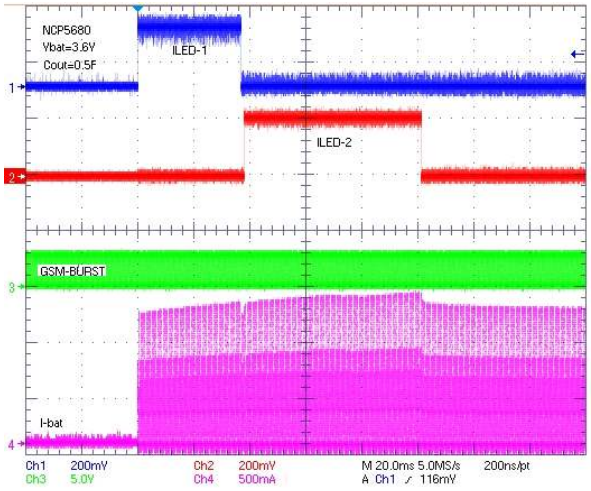


Figure 8. GSM Burst during a Flash and Re−charge Sequence

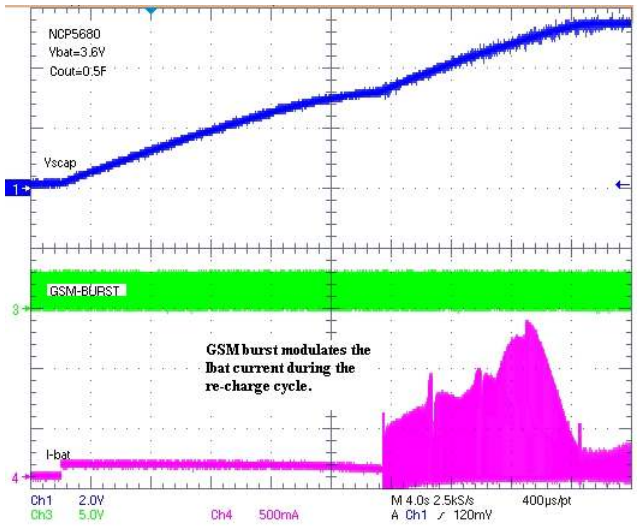


Figure 9. GSM Active during a Re−charge Cycle

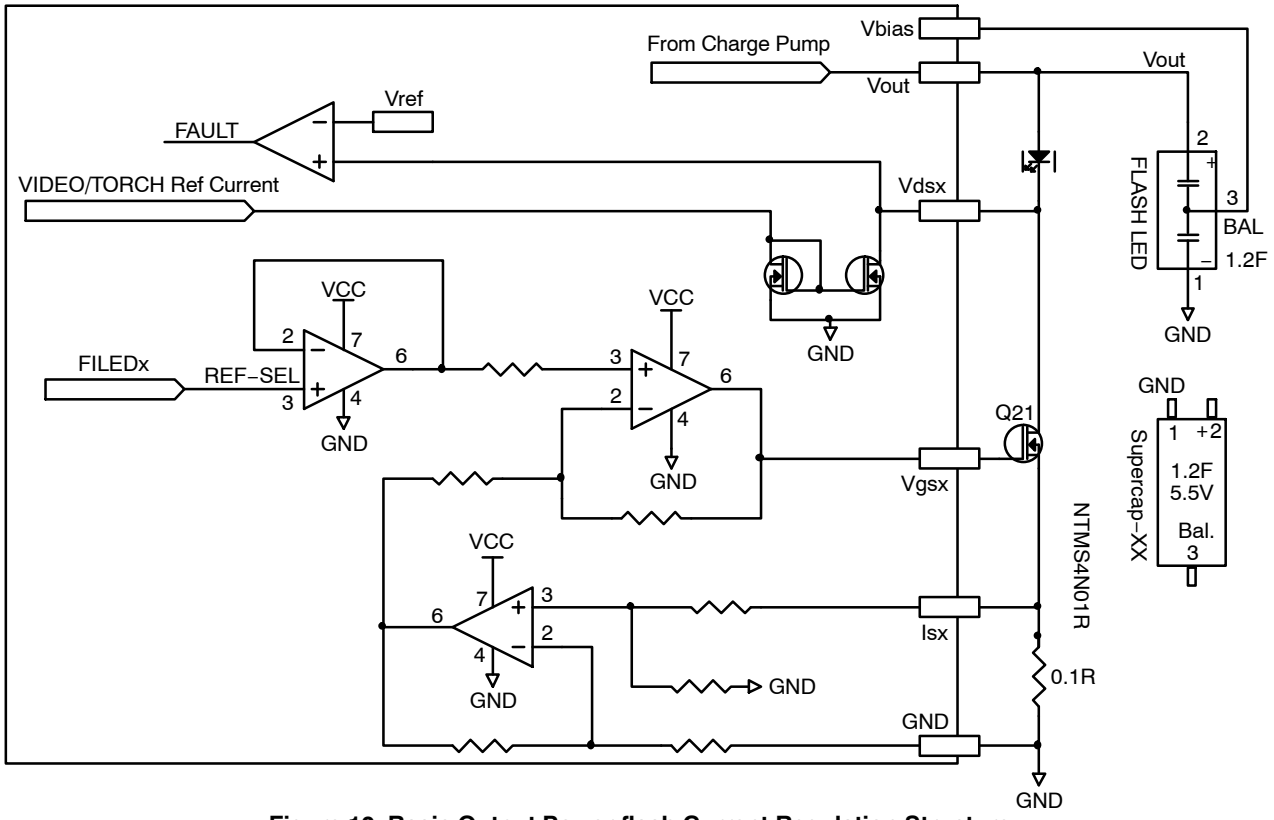


Figure 10. Basic Output Power flash Current Regulation Structure with Video/Torch loop and Overload detection

Table 3. Recommended SuperCAP Products

Manufacturer	Part Number
CAP−XX	HA230F
CAP−XX	HW207F
CAP−XX	HS206F
TDK	EDLC122344−551−2F−30(E)
TDK	EDLC272020−501−2F−50(E)

Table 4. Maximum External MOS Transistor Input Capacitance

CcissN	External NMOS input capacitance	TBD		2500	pF
CcgdN	External NMOS Gate / Drain capacitance	TBD		TBD	pF
CcissP	External PMOS input capacitance			2500	pF

Output Voltage Regulation

The output voltage −Vout− can be adjusted by the I2C port within the 4.5 V to 5.5 V range (200 mV/step), as depicted in Table 5. It is preset at 4.5 V upon a Power On Reset or a RESET command.

Table 5. Output Voltage Adjustment

B7	B6	B5	B4	B3	B2	B1	B0	Vout
0	0	0	0	0	0	0	0	4.5 V
0	0	0	0	0	0	0	1	4.7 V
0	0	0	0	0	0	1	0	4.9 V
0	0	0	0	0	0	1	1	5.1 V
0	0	0	0	0	1	0	0	5.3 V
0	0	0	0	0	1	0	1	5.5 V

Load Connection

The primary function of the NCP5680 chip is to control two high power LED arranged in the photo flash structure. The LED are independently activated or de−activated by means of the I2C command.

In addition, the chip is capable to drive the Torch mode or the Indicator function, the output LED current being monitored by the associated current mirrors. Although it is possible to connect several LED in parallel to share the output current, such solution is discouraged since the matching between the LED can no longer be guaranteed.

However, using a dual NMOS device in the same package provides a way to drive up to four LEDs with full flash current capability per LED, as depicted in Figure 11.

LED Programming Operation

All the electrical biases of each LED are set up by means of an hexadecimal byte coming from the I2C port. The Iout peak current, the flash pulse duration and the flash delays are stored into registers associated to each LED. Consequently, each LED can have a different amplitude, duration and delay during a single photo flash sequence.

The mode of operation − either Video torch or Flash, or Picture Light or ICON − is selected by the I2C command. In addition, the photo flash sequence can be activated either by the appropriate I2C command, or by means of the dedicated TRGFL pin, assuming the chip has been previously activated (the TRGFL signal has no effect if NCP5680 is in shut down mode). The Time out is automatically asserted when a pulsed flash is activated.

Power Flash

The I−LED flash current is regulated by means of the analog loop built with the external NMOS device associated to the external shunt resistor: see Figure 10. The internal operational amplifier uses the reference voltages, as defined by the contain of register FILED1 and FILED2, to monitor the current flowing in the loop. Basically, the Voltage to current ratio is 100 mV/A: a 100 mΩ resistor will force a 1 A I−LED current with 100 mV programmed at the FILED1 or FILED2 register. Of course, different value for the shunt resistor can be implemented, but care must be observed as it might be difficult to extract a low drop voltage in a noisy environment.

The power flash sequence can be activated in two ways:

1. Using the I2C command associated to the CONFIG1register: the positive going of the bit I2CTRG signal fires the pulsed flash (the pulse width depends upon the contain of FLWID1 & FLWID2 registers), the delays are activated, depending upon the contain of FLDY1 & FLDY2 registers, the time out is engaged, the output current is forced to the values previously stored into the FILED1 and FILED2 registers. The flash can be as short as 100 μs, with 255 ms as a maximum duration (see TOUT register). The I2CTRG bit in the CONFIG1 register is automatically reset to Low when the flash pulse is completed.
2. Using a direct command through the TRGFL pin, assuming the EXTRG bit in the CONFIG1 register is set to High. In this case, the time out is activated but the timers and the pulse width registers are de−activated since the duration of the pulsed flash depends solely upon the duration of the signal present at the TRGFL pin.

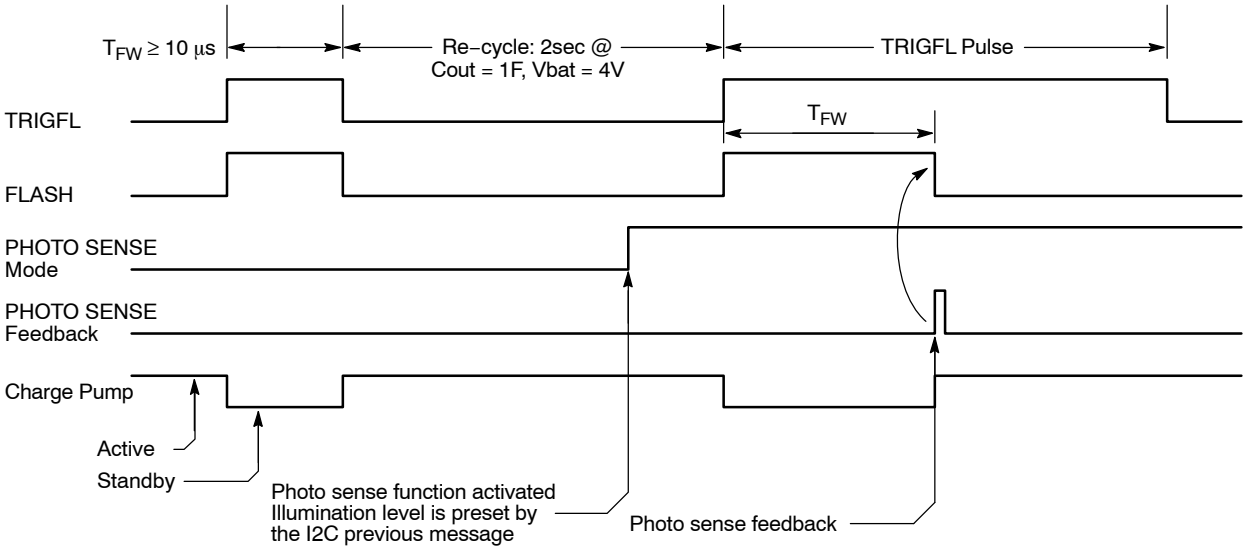


Figure 11. Basic Operation Timings

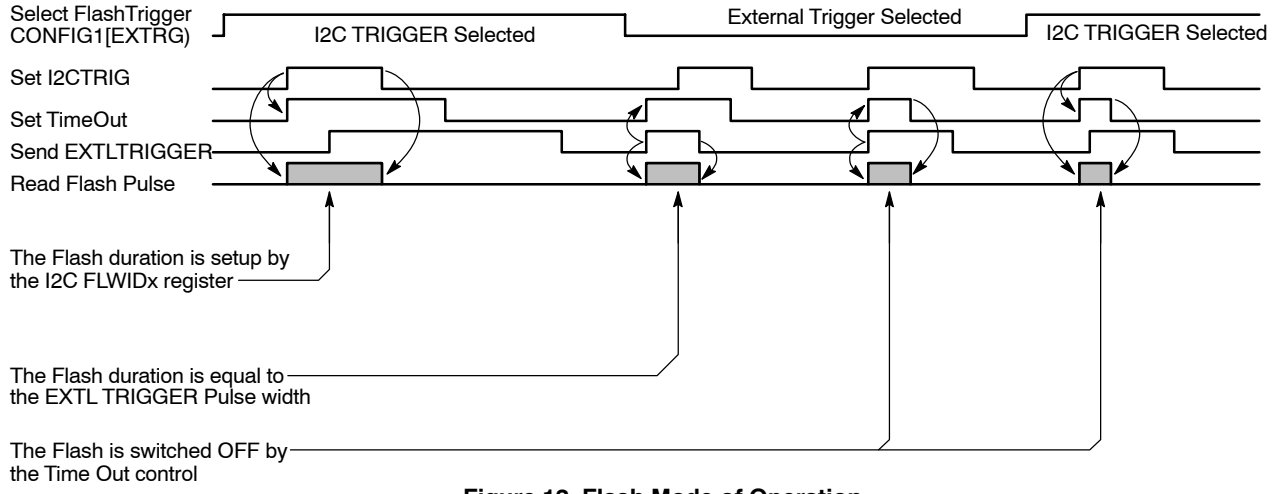


Figure 12. Flash Mode of Operation

When the power flash is activated, the default Time out is preset to 50 ms typical and can be set up to a different timing through an I2C command. Although the NCP5680 can sustain a 255 ms time out, care must be observed, at system level, that both the external NMOS transistors and the LED are capable to absorb the increase of temperature coming from the extra heat developed during a larger time out sequence.

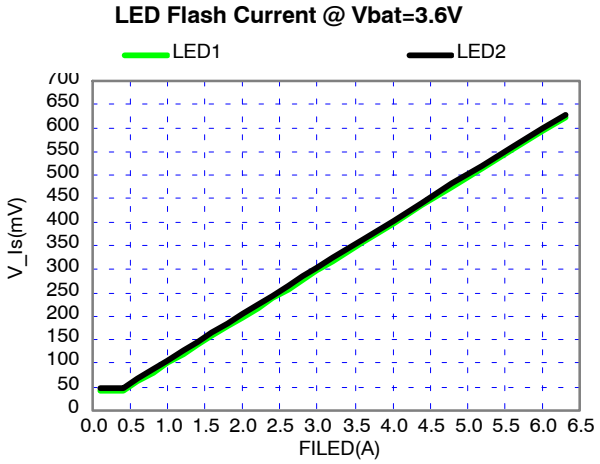


Figure 13. Flash ILED Current vs. Vsense

Flash Configuration

To generate a flash pulse, several registers must be preset before a flash takes place:

FILED1 = $03 → LED1 set up the peak current
FILED1 = $04 → LED2 set up the peak current
FLDLY1 = $07 → LED1 set up the delay time
FLDLY2 = $08 → LED2 set up the delay time
FLWID1 = $0A → LED1 set up the pulse width time
FLWID2 = $0B → LED2 set up the pulse width time
VOUTREG = $0F → set up the output voltage value
TOUT = $14 → set up the time out

A typical sequence is depicted here below:

- Set up the configuration registers to control the flash sequence
- Set up the pulse width, the amplitude and the delay time

CONFIG0	B7	B6	B5	B4	B3	B2	B1	B0
Select the Photo Sense Mode of Operation	–	–	1/0	–	–	–	–	–
Select the Automatic LED check during a pulse	–	–	–	1/0	–	–	–	–
Select LED2	–	–	–	–	–	–	1/0	–
Select LED1	–	–	–	–	–	–	–	1/0

Typical Sequence:

– send the I2C address $7C
– select the CONFIG0 register $01
– activate LED1 and LED2 $03

CONFIG1	B7	B6	B5	B4	B3	B2	B1	B0
Select the Charge Pump Mode of Operation: 0 → charge pump de−activated during a flash pulse 1 → charge pump activated during a flash pulse	–	1/0	–	–	–	–	–	–
Select the Flash mode	–	–	1	–	–	–	–	–
Control a flash sequence from the I2C port: 0 → the I2C trigger is de−activated, clear previous sequence 1 → the I2C trigger is activated and the flash pulse is forced on the positive going pulse	–	–	–	1/0	–	–	–	–
Control the charge pump: 0 → charge pump de−activated 1 → charge pump activated	–	–	–	–	–	1/0	–	–
Control the pre charge mode: 0 → pre charge pump de−activated 1 → pre charge pump activated	–	–	–	–	–	–	1/0	–

Typical Sequence:

– send the I2C address $7C
– setup the Output Voltage $0F, $xx
– setup the LED1 current amplitude $03, $xx
– setup the LED1 pulse width $0A,$xx
– setup the LED1 delay $07, $xx
– send the I2C address $7C
– setup the LED2 current amplitude $04, $xx
– setup the LED2 pulse width $0B, $xx
– setup the LED2 delay $08, $xx
– send the I2C address $7C
– select the CONFIG1 register $02
– Activate the charge pump during a flash pulse & %0110 0110
Activate the charge pump &
Select the flash Mode &
Clear previous sequence
– send the I2C address $7C
– select the CONFIG1 register $02
– Activate the charge pump during a flash pulse & %0111 0110
Activate the charge pump &
Select the flash Mode &
Send I2C Flash trigger

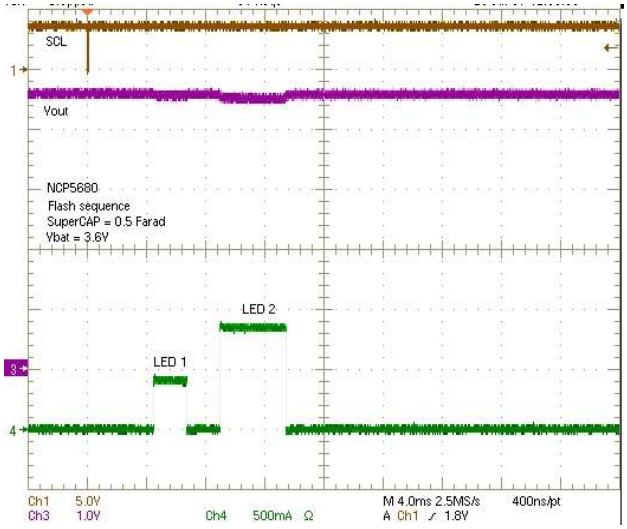


Figure 14. Typical Flash Pulses Sequence

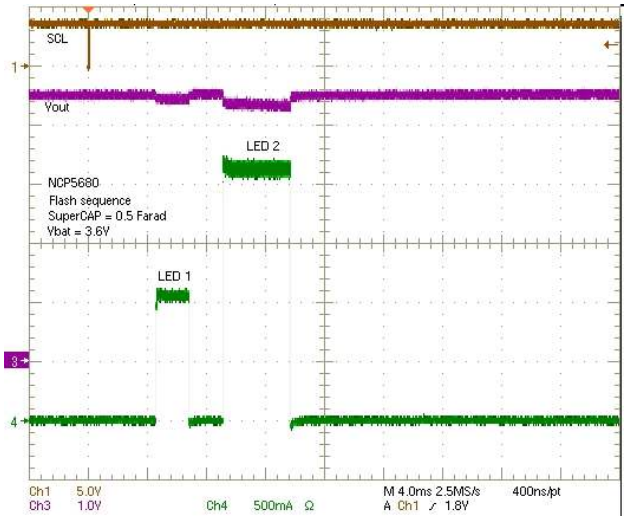


Figure 15. Typical Flash Pulses with 2A peak in LED2

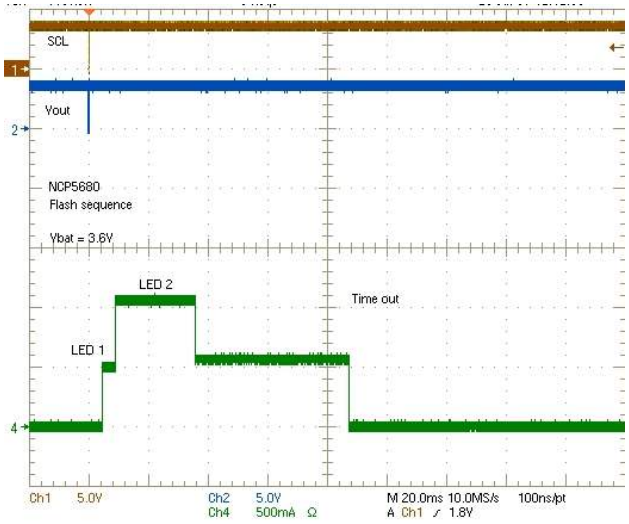


Figure 16. Typical Flash pulse with Time Out Engaged

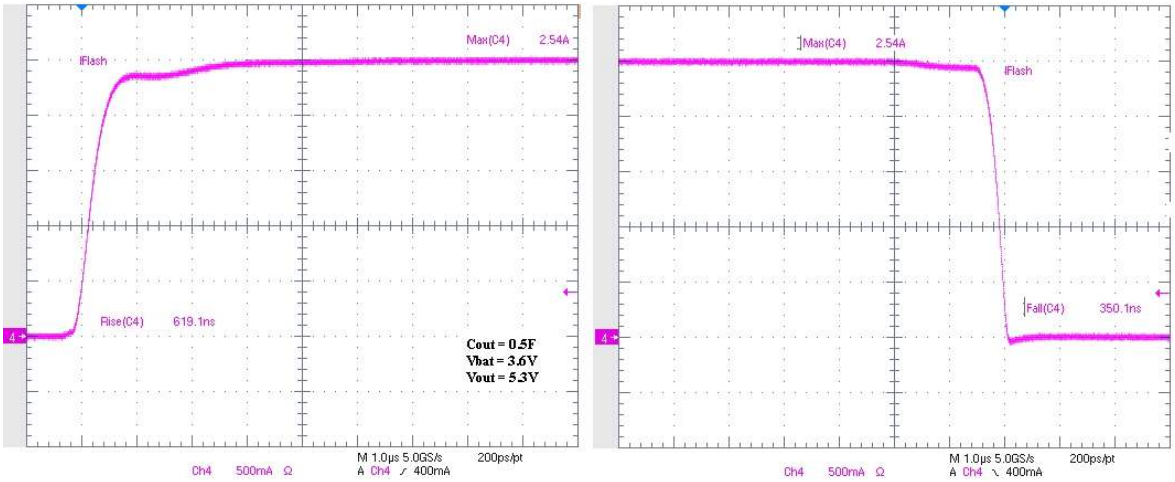


Figure 17. Typical ILED Rise & Fall Time

Torch / Video

The torch/video mode is activated when the SELFL bit is low. In this case, the pulse width and delays registers are irrelevant, the time out is de−activated. The output current is setup by the contain of the TILED register. In addition, the time out is immediately activated if the contain of the TILED register exceeds $3F.

Similarly, the external NMOS are deactivated (Vgs1 = Vgs2 = 0) and the ILED current is controlled by the built−in current mirrors, the maximum current being 100 mA per LED.

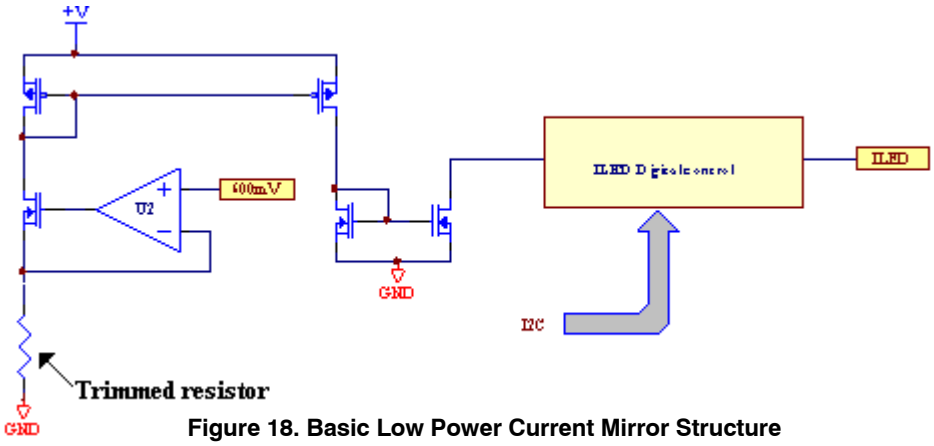


Figure 18. Basic Low Power Current Mirror Structure

Auxiliary Operation

The power capability of the built-in charge pump makes possible the use of a permanent load connected at the Vout pin with a 100 mA continuous load current. Two situations shall be considered:

a - the auxiliary load is ripple sensitive and fully active when the power flash is triggered: using the extra PMOS transistor is mandatory to isolate the auxiliary load from the power LED. In this case, a minimum 100 μF/6.3 V capacitor is required to maintain the Vout voltage constant during the operation.

b - the auxiliary load is de-activated during a flash sequence : using the PMOS transistor is not mandatory and the auxiliary can be powered from the SuperCAP.

Thermal Consideration

Based on the data sheet published by the LED manufacturers', the forward drop of these LED can be 3 V or less when the forward current is 100 mA and below. Assuming that such a device is connected in the system, a relative large amount of power will be dissipated into the current mirrors built inside the NCP5680. Let assume that Vf = 3.0 V @ If = 100 mA and consider the Vout was programmed at 5.5 V. The voltage across the current mirror will be:

Vom = Vout – Vf

Vom = 5.5 – 3 = 2.5 V

The power dissipated into the current mirror will be

Pom = Vom * If

Pom = 2.5 * 0.1 = 0.25 W

Assuming that the two LED are activated simultaneously, the total power dissipated by the current mirror will be 0.50 W. In addition, the charge pump is active during this operation to maintain Vout at the programmed value, and an extra 400 mW will be added to the losses. On the other hand, it is unlikely possible to increase the PCB area large enough to significantly reduce the thermal resistance between the QFN package and the ambient air: generally speaking, the Rthj−a is in the range of 40°C/W, assuming the Rthj−c negligible in comparison to the Rthc−a. Taking all these parameters into account, the die temperature can be calculated :

$\Delta Tj = SP \times Rthj-c$

$\Delta Tj = (0.5 + 0.4) * 40 = 36°C$

Assuming that the system operates under +85°C ambient temperature, then the chip will be at 85+36 = 121°C, very close to the maximum rating.

To avoid any long term fault with the system, it is strongly recommended to reduce the Vout voltage to the minimum value when the Torch/Video mode is activated. In this case, the net voltage across the current mirror will be limited to 4.5 – 3.0 = 1.5 V, the losses will decrease accordingly, yielding a 113°C maximum junction temperature under the same environment as depicted before.

To control the Torch/Video mode, several registers must be preset before a flash takes place. A typical sequence is depicted here:

CONFIG0	B7	B6	B5	B4	B3	B2	B1	B0
Select LED2	–	–	–	–	–	–	1/0	–
Select LED1	–	–	–	–	–	–	–	1/0

Typical Sequence:

– send the I2C address $7C

– select the CONFIG0 register $01

– activate LED1 and LED2 $03

CONFIG1	B7	B6	B5	B4	B3	B2	B1	B0
Select the Charge Pump Mode of Operation: 0 → charge pump de−activated during a flash pulse 1 → charge pump activated during a flash pulse	–	1	–	–	–	–	–	–
Select the Torch/Video mode	–	–	0	–	–	–	–	–
Control the charge pump: 0 → charge pump de−activated 1 → charge pump activated	–	–	–	–	–	1	–	–
Control the pre charge mode: 0 → pre charge pump de−activated 1 → pre charge pump activated	–	–	–	–	–	–	1	–

Indicator

The indicator mode is activated when the ENIND bit in the CONFIG1 register is High. The pulse width and timer registers are irrelevant, the time out is de−activated. The indicator function applies solely to LED 1. The Torch/Video mode is bypassed if it was active in the previous phase and resumes to the previous situation when ENIND = Low.

The external NMOS are deactivated (Vgs1 = Vgs2 = 0) and the ILED current is controlled by the built−in current mirror, the maximum current being 6.3 mA.

The indicator might be activated permanently, both the power flash or the video/torch mode having an automatic highest priority: the indicator current for LED1 is summed with the main current coming from either the flash or the video/torch circuits.

Photo Sense

When the photo sense is activated (bit PHEN = 1 in the CONFIG0 register), the duration of the flash is automatically reduced when enough light back from the photo target is sensed through the external sensor. The analog signal present at the PHSEN pin is amplified (depending upon the gain setup by the MCU) and compared with the reference programmed by the MCU: the photo flash pulse is switched OFF when the input signal is higher than the content of the PHSEN register (see Figure 19). The built−in flip flop makes sure that a single pulse is generated when the light feedback has been acknowledged by the sensor. The flip flop is reset to the armed position upon a new trigger flash command (coming from either the I2C or from the TRGFL pin).

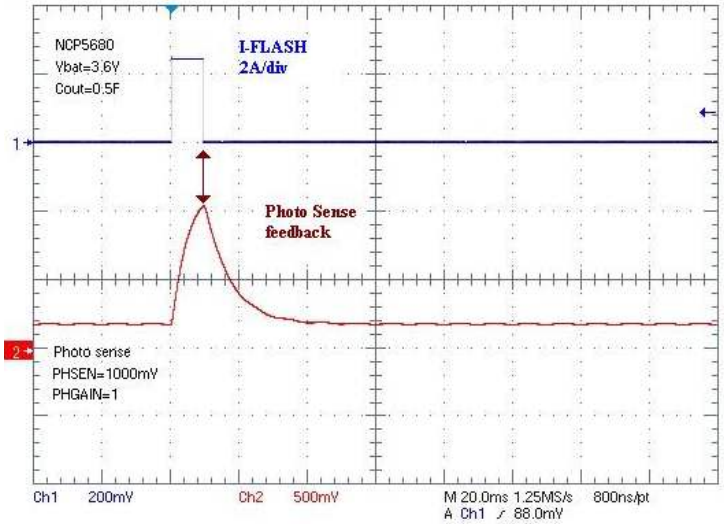


Figure 19. Typical Flash Pulses with Photo Sense Engaged

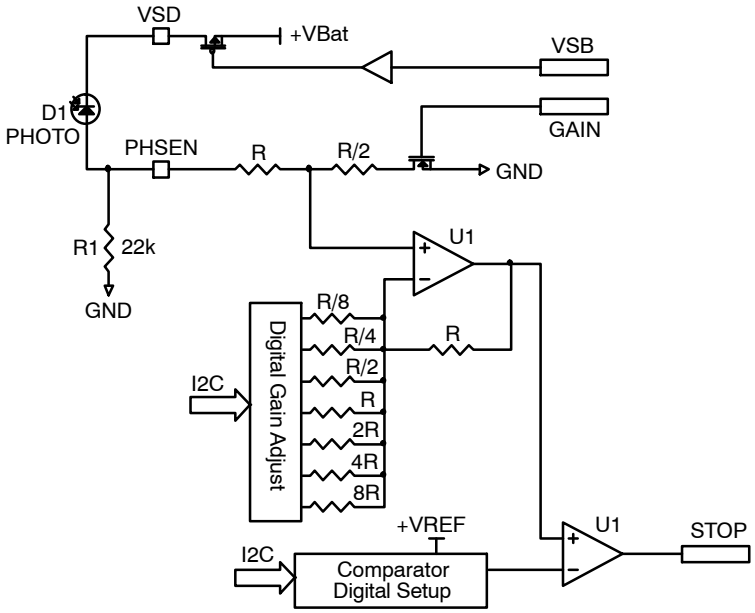


Figure 20. Basic Photo Sense Structure

On the other hand, the VSD bias voltage is activated when either the charge pump is active, or the ENPH bit in the CONFIG0 register is High.

In order to minimize the influence of voltage offset, operating the Photo Sense trigger level in the 360 mV to 1500 mV range is recommended.

Picture Light

The Picture Light current share the same internal current mirror used to support the Torch/ Video function. The level of current is controlled by the TILED register. In addition, a 200 ms time out is automatically activated when the TILED current is higher than 100 mA. On the other hand,

the 200 ms time out can be activated by forcing the TPLGT bit to high in the CONFIG0 register. The Picture Light cannot be combined with a power flash pulse.

NTC Sensor

The external NTC element is controlled by the ENTC bit in the CONFIG0 register. When the function is activated, the external NTC element is biased by a programmable constant current (in the 10 μA to 630 μA range), the voltage developed across the NTC pin and GND being compared to the reference voltage stored into the NTCREG register. When the NTC voltage drops below the minimum level (setup by the NTCREG register), the charge is de−activated and both the flash and the torch mode are automatically switched OFF, reducing the power dissipated into the LED to almost zero. The associated flip flop is reset to the normal mode when a power OFF/ON sequence is forced, or by pulsed Hi/Lo the NTCREG[CNTC] bit. In both case, the NTC temperature must be cool enough to enable the power current flow into the LED.

Time Out Security

When an extra security is requested by the end application, and external structure shall be implemented to handle the worst but rare case condition, i.e. when the NCP5680 built−in timer and time out fail simultaneously. To handle such conditions, an external circuit will switch off the two NMOS transistor when the time extend the maximum 200 ms time out defined by the passive component. There is no software associated with the security circuit, the activation being automatically done when any of the two NMOS is used to generate a power flash pulse. The typical circuit is depicted in Figure 21.

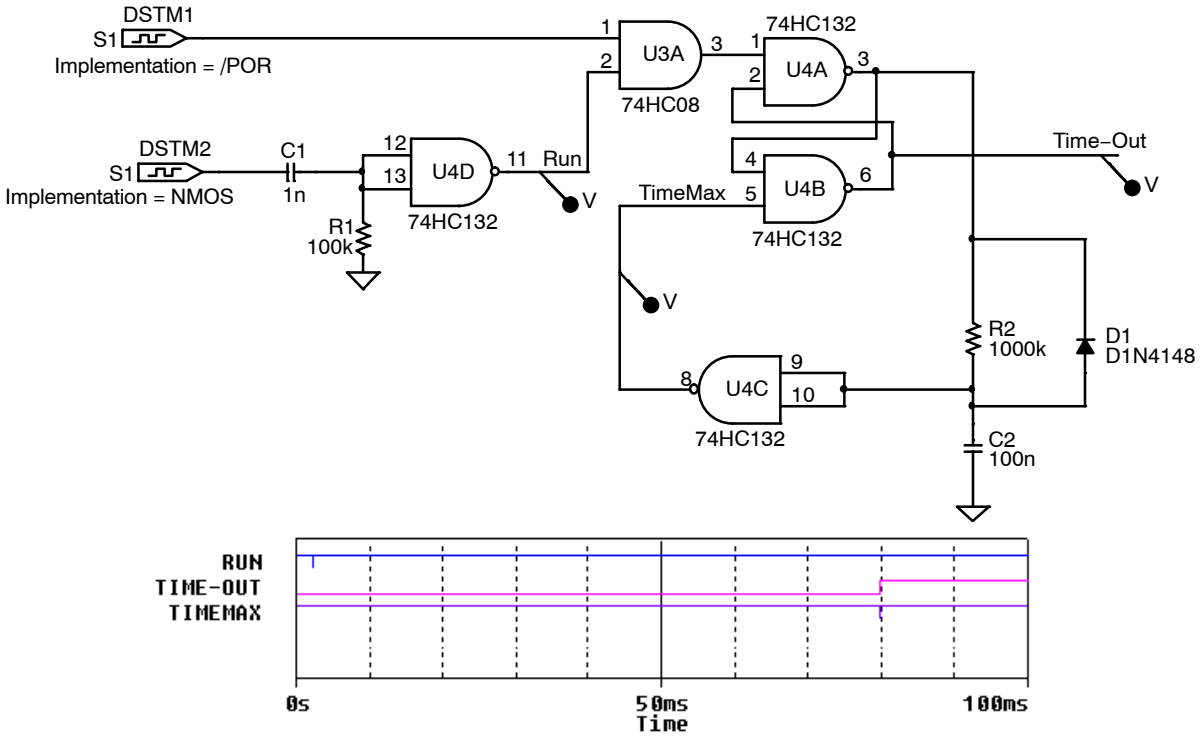


Figure 21. Basic External Hardware Time Out Security Circuit

The NMOS signal is derived from the gate drive voltage applied to the external NMOS transistor: this signal is fully synchronized with a photo flash pulse. The positive going slope generates a negative pulse at the RESET input of the flip flop built with two NAND gate which, in turn, activates the delay built with the RC network connected to a single inverter. The flip−flop is set when the RC timing ends (a negative going pulse is present at the SET input), turning ON the external NMOS transistor which, in turn, will force to ground the gate of the power transistor. At this point, the ILED current is disconnected and no more power is dissipated in the circuit. To flip flop is reset by sending a new photo flash sequence, or using any kind of MCU controlled signal.

I2C Protocol

The NCP5680 is considered as a Slave system, with no possibility to take control of the bus, programmed by means of the standard I2C protocol driven by the external MCU. In addition, the internal STATUS register can be read back upon request coming from the external MCU.

To program one particular register, the communication takes place with three serial bytes:

– Byte#1 → physical I2C address = %0111 1100 (Write) / %0111 1101 (Read)

– Byte#2 → select the internal register to read

– Byte#3 → Data stored into the selected register.

Note: the STATUS register is Read only and no byte can be stored from the I2C port into this register.

Table 6. I2C Physical address byte (first byte is $7C if Write or $7D is Read)

B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	1	1	1	0	R/W

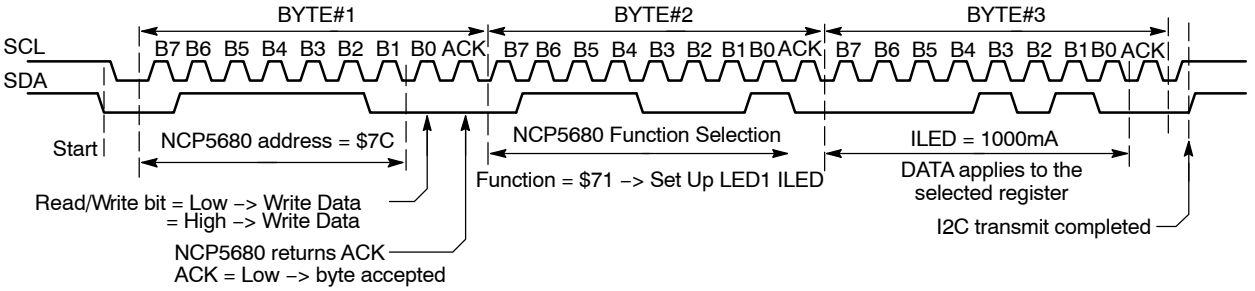


Figure 22. Typical I2C programming Sequence

Example: select the NCP5680 interface ($7C), then select LED1 output current register, then send the value to be stored into the LED1 register.

To read the STATUS register, the protocol is slightly different and five I2C cycles are necessary:

– Byte#1 → physical I2C address = %0111 1100 (Write) to write the STATUS register

– Byte#2 select the STATUS register to read = $17

– Byte#3 → send an irrelevant data byte ($FF)

– Force a STOP condition

– Force a START condition

– Byte#4 → physical I2C address = %0111 1101 (Read) to read the STATUS register

– Byte#5→ the NCP5680 returns the STATUS contain on the SDA line. The MCU must maintain the SCL signal active.

LED Checking Function

Although the power transistors are external to the NCP5680 chip, provisions have been made, at silicon level, to protect the system against fault developed during operation.

The first element, in regard to the power flash, is an automatic time out sequence engaged when a flash is activated. Such protection will automatically switch off the output current if the pulse width exceeds the time out limit (maximum 255 ms). Similarly, the time out function is automatically de−activated when the Torch/Video mode of operation is selected by software. In this case, the continuous current is limited to 100 mA maximum per LED.

Beside the thermal shutdown procedure embedded into the silicon, the second protection feature is the Vout to Ground short circuit protection: the output current is automatically reduced to 60 mA typical, (100 mA max) when such a short is developed across the output voltage pin and ground.

According to the power LED manufacturers, an Anode to Cathode short might develop in case of failure: such a situation is detected by the NCP5680 and the associated current loop is automatically disconnected. The test procedure shall be launched by forcing the CKPRC bit in the CONFIG0 register and the procedure is activated upon the positive going slope of this bit. During the check, a 1 mA / 20 μs width typical bias current is forced through the LED. To send a new check sequence, the CKPRC bit must be forced back to low and a new positive edge can be sensed by forcing CKPRC high.

Finally, the system permanently monitor the Drain/ Ground voltage of each external NMOS to detect any fault condition in the power flash circuit.

A specific command shall be send by the I2C to check the circuit without any on going sequence. The system makes sure the LED is connected to the Vds pin and that no short circuit exist between Vout and Vds (no A/K short−circuit). Such a command over ride the BKL1 and BKL2 status and the check is carried out even when the BKL1 & BKL2 bits are low. In case of failure, the chip de−activate the offender pin and returns the fault bit into the register. The MCU can read the STATUS register content by means of the I2C protocol.

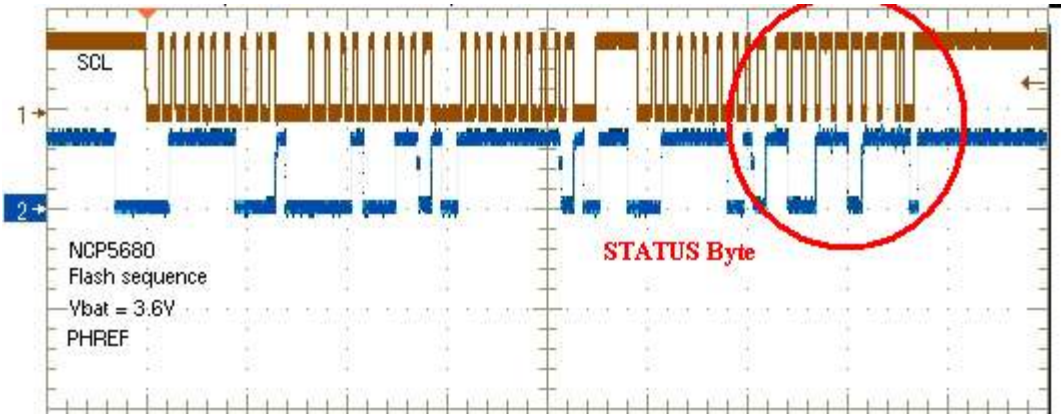


Figure 23. Basic I2C Read Sequence to Extract the STATUS Register

Thermal Shutdown

When the thermal shutdown is engaged, the charge pump is fully de−activated and neither the torch/video, nor the flash can be launched. The rest of the chip is maintained active in order to keep a full control of the operation, in particular the SuperCAP bias voltage is active and regulated.

Basic I/O Protection Structure

All the pins of the NCP5680 device are ESD protected by built in diode structure as depicted in Figure 24. Since a diode is attached between the I/O pin and the supply pin, the voltage at the I/O pin shall not extend the V_{CC} voltage plus one Vf drop.

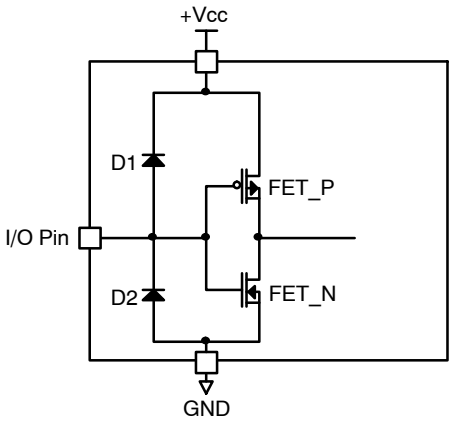


Figure 24. Typical ESD Pin Protection Structure

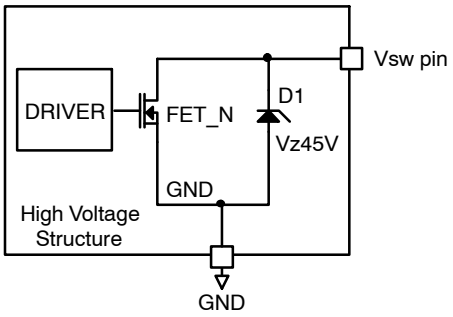


Figure 25. Basic ESD Protection Dedicated to Power Pin.

Different structures might apply to protect specific pins, in particular the power related functions. In this case, a single diode based clamp structure can be wired to sustain the ESD specifications as depicted in Figure 25.

Typical Application Schematic Diagram

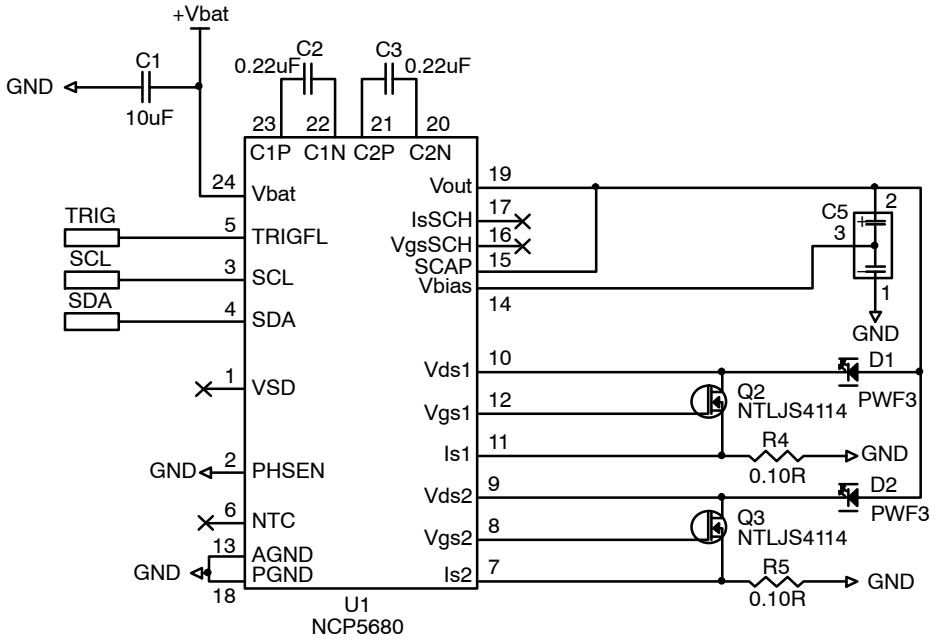


Figure 26. Basic Power Flash Application

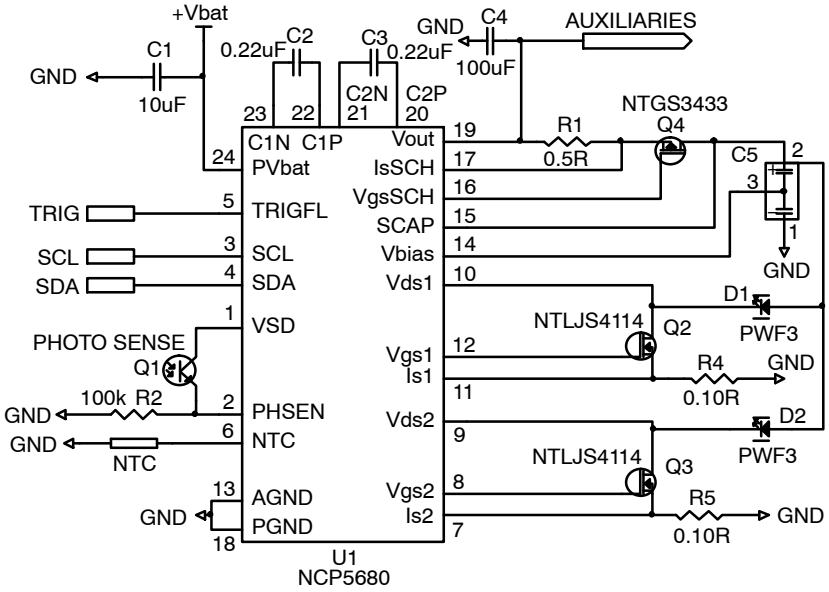


Figure 27. Full Functions Typical Application

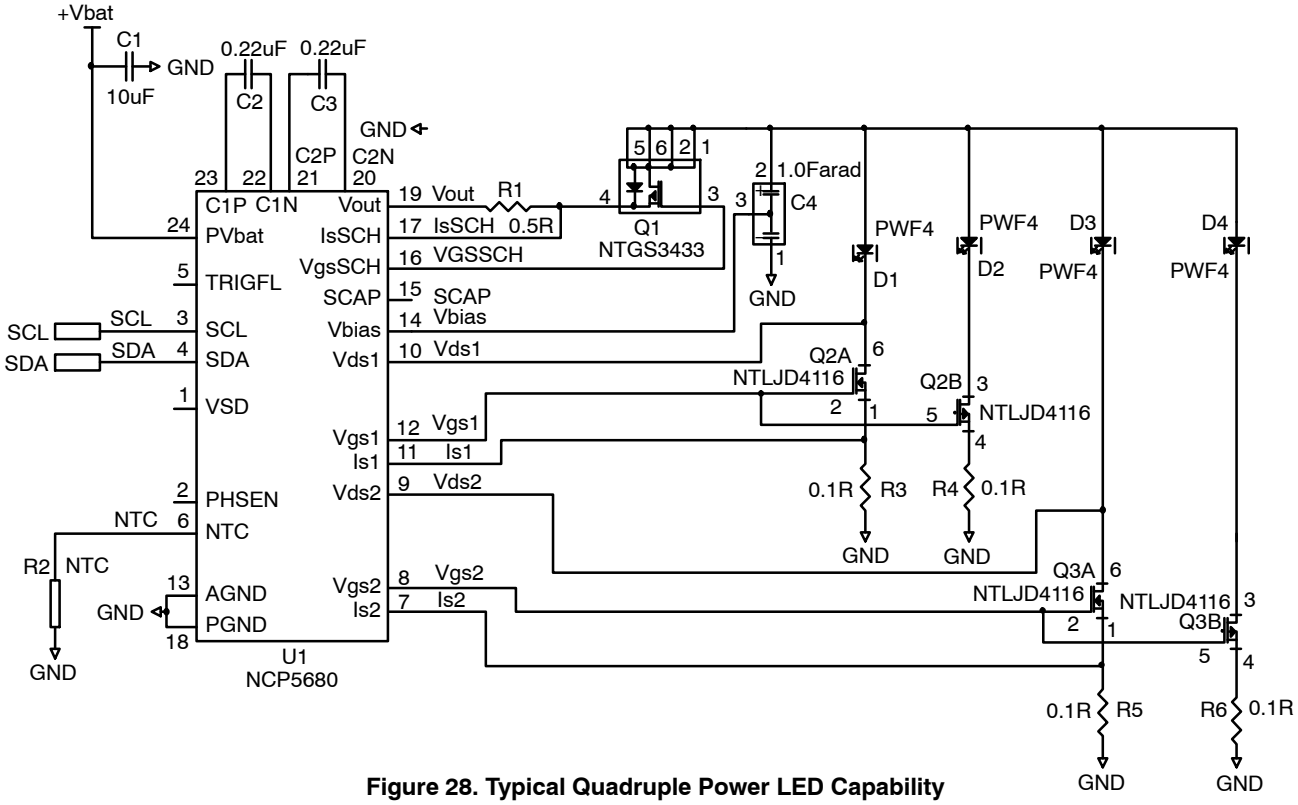
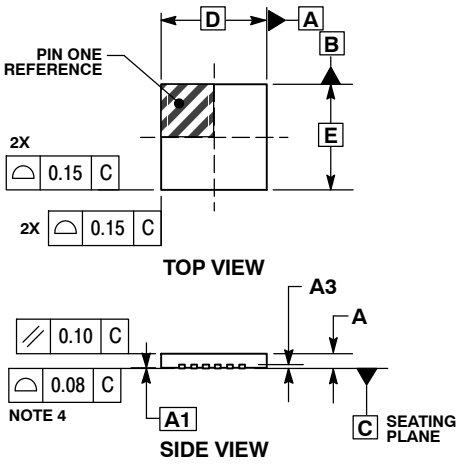


Figure 28. Typical Quadruple Power LED Capability

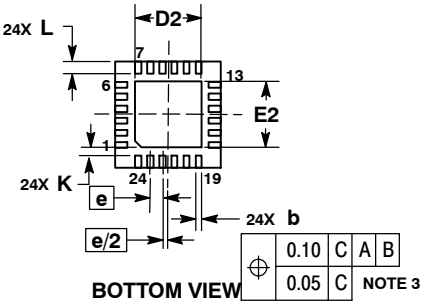
PACKAGE DIMENSIONS

UQFN24 3.5x3.5, 0.4P
CASE 523AG−01
ISSUE O

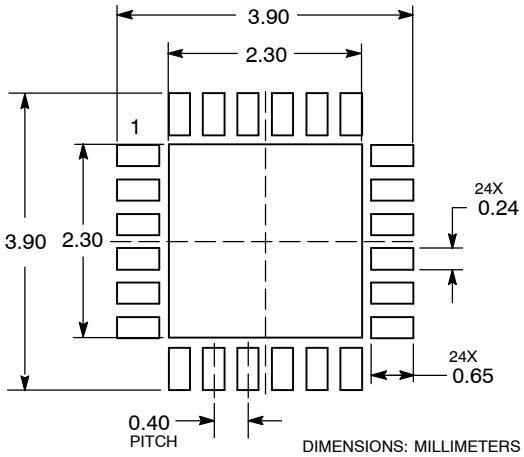


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.50 BSC	
D2	2.10	2.30
E	3.50 BSC	
E2	2.10	2.30
e	0.40 BSC	
L	0.30	0.50
K	0.20	−−−



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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