

## MM74HC4316 Quad Analog Switch with Level Translator

### General Description

The MM74HC4316 devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "ON" resistance and low "OFF" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the MM74HC4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels. The MM74HC4316 also has a common enable input in addition to each switch's control which when LOW will disable all switches to their OFF state. All analog inputs

and outputs and digital inputs are protected from electrostatic damage by diodes to  $V_{CC}$  and ground.

### Features

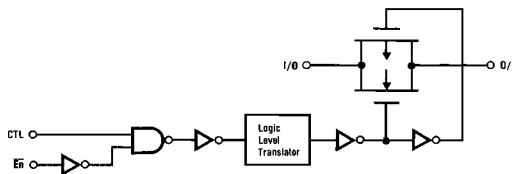
- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "ON" resistance:  
50 typ. ( $V_{CC}-V_{EE} = 4.5V$ ) 30 typ. ( $V_{CC}-V_{EE} = 9V$ )
- Low quiescent current: 80  $\mu A$  maximum (74HC)
- Matched switch characteristics
- Individual switch controls plus a common enable

### Ordering Code:

Order Number	Package Number	Package Description
MM74HC4316M	M16A	16-Lead Small Outline Integrated Package (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4316SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4316MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-1536, 4.4mm Wide
MM74HC4316N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

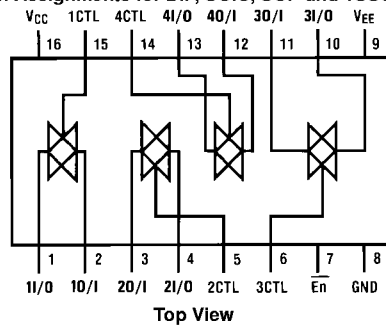
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Diagram



### Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



### Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

Absolute Maximum Ratings <sup>(Note 1)</sup>		Recommended Operating Conditions		
(Note 2)				
Supply Voltage ( $V_{CC}$ )	-0.5 to +7.5V	Min	Max	Units
Supply Voltage ( $V_{EE}$ )	+0.5 to -7.5V	2	6	V
DC Control Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$	0	-6	V
DC Switch I/O Voltage ( $V_{IO}$ )	$V_{EE} - 0.5$ to $V_{CC} + 0.5V$	DC Input or Output Voltage		
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA	0	$V_{CC}$	V
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA	Operating Temperature Range ( $T_A$ )		
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA	-40	+85	$^{\circ}C$
Storage Temperature Range ( $T_{STG}$ )	-65 $^{\circ}C$ to +150 $^{\circ}C$	Input Rise or Fall Times		
Power Dissipation ( $P_D$ )		( $t_r, t_f$ ) $V_{CC} = 2.0V$	1000	ns
(Note 3)	600 mW	$V_{CC} = 4.5V$	500	ns
S.O. Package only	500 mW	$V_{CC} = 6.0V$	400	ns
Lead Temperature ( $T_L$ )		$V_{CC} = 12.0V$	250	ns
(Soldering 10 seconds)	260 $^{\circ}C$	<p><b>Note 1:</b> Absolute Maximum Ratings are those values beyond which damage to the device may occur.</p> <p><b>Note 2:</b> Unless otherwise specified all voltages are referenced to ground.</p> <p><b>Note 3:</b> Power Dissipation temperature derating — plastic "N" package: — 12 mW/<math>^{\circ}C</math> from 65<math>^{\circ}C</math> to 85<math>^{\circ}C</math>.</p>		

### DC Electrical Characteristics <sup>(Note 4)</sup>

Symbol	Parameter	Conditions	$V_{EE}$	$V_{CC}$	$T_A = 25^{\circ}C$		$T_A = -40$ to $85^{\circ}C$		$T_A = -55$ to $125^{\circ}C$		Units
					Typ	Guaranteed Limits					
$V_{IH}$	Minimum HIGH Level Input Voltage			2.0V	1.5	1.5	1.5	V			
				4.5V	3.15	3.15	3.15	V			
				6.0V	4.2	4.2	4.2	V			
$V_{IL}$	Maximum LOW Level Input Voltage			2.0V	0.5	0.5	0.5	V			
				4.5V	1.35	1.35	1.35	V			
				6.0V	1.8	1.8	1.8	V			
$R_{ON}$	Minimum "ON" Resistance (Note 5)	$V_{CTL} = V_{IH}, I_S = 2.0$ mA	GND	4.5V	100	170	200	220	$\Omega$		
				4.5V	40	85	105	110	$\Omega$		
				6.0V	30	70	85	90	$\Omega$		
		$V_{IS} = V_{CC}$ or $V_{EE}$ (Figure 1)	GND	2.0V	100	180	215	240	$\Omega$		
				4.5V	40	80	100	120	$\Omega$		
				6.0V	20	40	60	70	$\Omega$		
$R_{ON}$	Maximum "ON" Resistance Matching	$V_{CTL} = V_{IH}$ $V_{IS} = V_{CC}$ to $V_{EE}$	GND	4.5V	10	15	20	20	$\Omega$		
				4.5V	5	10	15	15	$\Omega$		
				6.0V	5	10	15	15	$\Omega$		
$I_{IN}$	Maximum Control Input Current	$V_{IN} = V_{CC}$ or GND	GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$		
$I_{IZ}$	Maximum Switch "OFF" Leakage Current	$V_{OS} = V_{CC}$ or $V_{EE}$ $V_{IS} = V_{EE}$ or $V_{CC}$ $V_{CTL} = V_{IL}$ (Figure 2)	GND	6.0V		$\pm 60$	$\pm 600$	$\pm 600$	nA		
				6.0V		$\pm 100$	$\pm 1000$	$\pm 1000$	nA		
$I_{IZ}$	Maximum Switch "ON" Leakage Current	$V_{IS} = V_{CC}$ to $V_{EE}$ $V_{CTL} = V_{IH}, V_{OS} = OPEN$ (Figure 3)	GND	6.0V		$\pm 40$	$\pm 150$	$\pm 150$	nA		
				6.0V		$\pm 60$	$\pm 300$	$\pm 300$	nA		
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ $\mu A$	GND	6.0V		2.0	20	40	$\mu A$		
				6.0V		8.0	80	160	$\mu A$		

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case on resistances ( $R_{ON}$ ) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

**Note 5:** At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics									
V <sub>CC</sub> = 2.0V–6.0V, V <sub>EE</sub> = 0V–6V, C <sub>L</sub> = 50 pF (unless otherwise specified)									
Symbol	Parameter	Conditions	V <sub>EE</sub>	V <sub>CC</sub>	T <sub>A</sub> = +25°C		T <sub>A</sub> = –40°C to +85°C	T <sub>A</sub> = –55°C to +125°C	Units
					Typ	Guaranteed Limits			
t <sub>PHL</sub>	Maximum Propagation		GND	2.0V	25	50	63	75	ns
t <sub>PLH</sub>	Delay Switch In to Out		GND	4.5V	5	10	13	15	ns
			–4.5V	4.5V	4	8	12	14	ns
			–6.0V	6.0V	3	7	11	13	ns
t <sub>PZL</sub>	Maximum Switch Turn "ON" Delay (Control)	R <sub>L</sub> = 1 kΩ	GND	2.0V	30	165	206	250	ns
t <sub>PZH</sub>			GND	4.5V	20	35	43	53	ns
			–4.5V	4.5V	15	32	39	48	ns
			–6.0V	6.0V	14	30	37	45	ns
t <sub>PHZ</sub>	Maximum Switch Turn "OFF" Delay (Control)	R <sub>L</sub> = 1 kΩ	GND	2.0V	45	250	312	375	ns
t <sub>PLZ</sub>			GND	4.5V	25	50	63	75	ns
			–4.5V	4.5V	20	44	55	66	ns
			–6.0V	6.0V	20	44	55	66	ns
t <sub>PZL</sub>	Maximum Switch Turn "ON" Delay (Enable)		GND	2.0V	35	205	256	308	ns
t <sub>PZH</sub>			GND	4.5V	20	41	52	62	ns
			–4.5V	4.5V	19	38	48	57	ns
			–6.0V	6.0V	18	36	45	54	ns
t <sub>PLZ</sub>	Maximum Switch Turn "OFF" Delay (Enable)		GND	2.0V	58	265	330	400	ns
t <sub>PHZ</sub>			GND	4.5V	28	53	67	79	ns
			–4.5V	4.5V	23	47	59	70	ns
			–6.0V	6.0V	21	47	59	70	ns
f <sub>MAX</sub>	Minimum Frequency Response (Figure 7)	R <sub>L</sub> = 600Ω, V <sub>IS</sub> = 2V <sub>PP</sub> at (V <sub>CC</sub> –V <sub>EE</sub> )/2 (Note 6) (Note 7)	0V	4.5V	40				MHz
	20 log (V <sub>OS</sub> /V <sub>IS</sub> ) = –3 dB		–4.5V	4.5V	100				MHz
	Control to Switch Feedthrough Noise (Figure 8)	R <sub>L</sub> = 600Ω, F = 1 MHz C <sub>L</sub> = 50 pF (Note 7) (Note 8)	0V	4.5V	100				mV
			–4.5V	4.5V	250				mV
	Crosstalk Between any Two Switches (Figure 9)	R <sub>L</sub> = 600Ω, F = 1 MHz	0V	4.5V	–52				dB
			–4.5V	4.5V	–50				dB
	Switch OFF Signal Feedthrough Isolation (Figure 10)	R <sub>L</sub> = 600Ω, F = 1 MHz V <sub>CTL</sub> = V <sub>L</sub> (Note 7) (Note 8)	0V	4.5V	–42				dB
			–4.5V	4.5V	–44				dB
THD	Sinewave Harmonic Distortion (Figure 11)	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF, F = 1 KHz							
		V <sub>IS</sub> = 4V <sub>PP</sub>	0V	4.5V	0.013				%
		V <sub>IS</sub> = 8V <sub>PP</sub>	–4.5V	4.5V	0.008				%
C <sub>IN</sub>	Maximum Control Input Capacitance				5				pF
C <sub>IN</sub>	Maximum Switch Input Capacitance				35				pF
C <sub>IN</sub>	Maximum Feedthrough Capacitance	V <sub>CTL</sub> = GND			0.5				pF
C <sub>PD</sub>	Power Dissipation Capacitance				15				pF

**Note 6:** Adjust 0 dBm for F = 1 KHz (Null R<sub>L</sub>/R<sub>on</sub> Attenuation).

**Note 7:** V<sub>IS</sub> is centered at V<sub>CC</sub>–V<sub>EE</sub>/2.

**Note 8:** Adjust for 0 dBm.

AC Test Circuits and Switching Time Waveforms

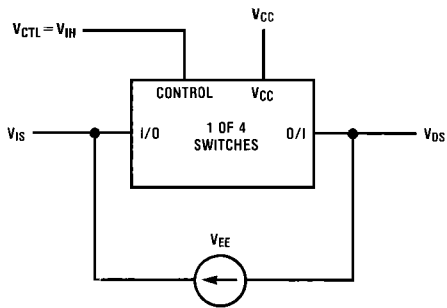


FIGURE 1. "ON" Resistance

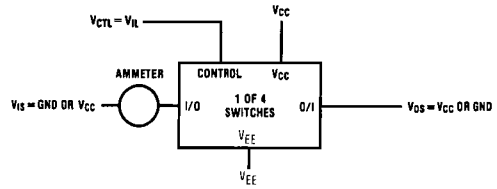


FIGURE 2. "OFF" Channel Leakage Current

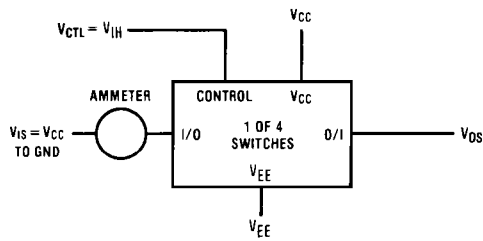


FIGURE 3. "ON" Channel Leakage Current

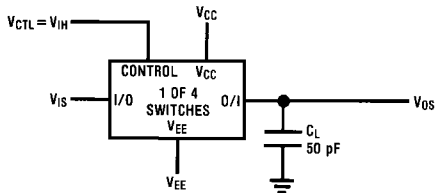


FIGURE 4.  $t_{PHL}$ ,  $t_{PLH}$  Propagation Delay Time Signal Input to Signal Output

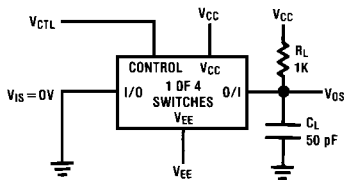
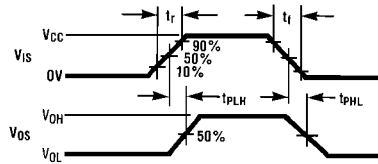


FIGURE 5.  $t_{PZL}$ ,  $t_{PLZ}$  Propagation Delay Time Control to Signal Output

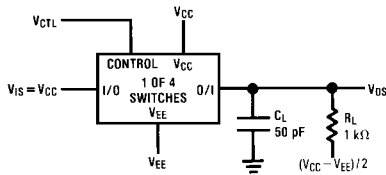
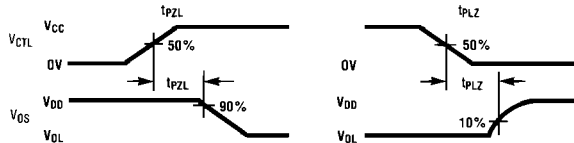
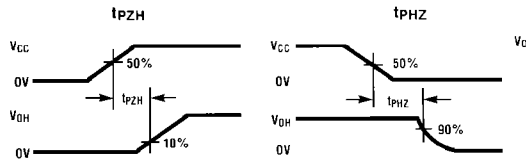


FIGURE 6.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output



AC Test Circuits and Switching Time Waveforms (Continued)

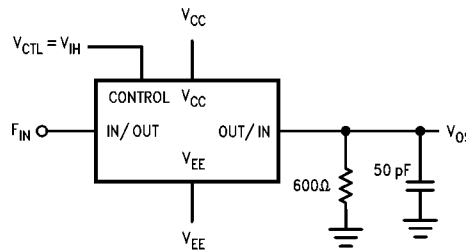


FIGURE 7. Frequency Response

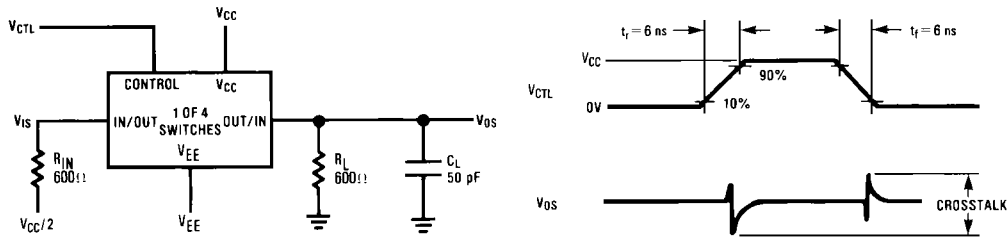


FIGURE 8. Crosstalk: Control Input to Signal Output

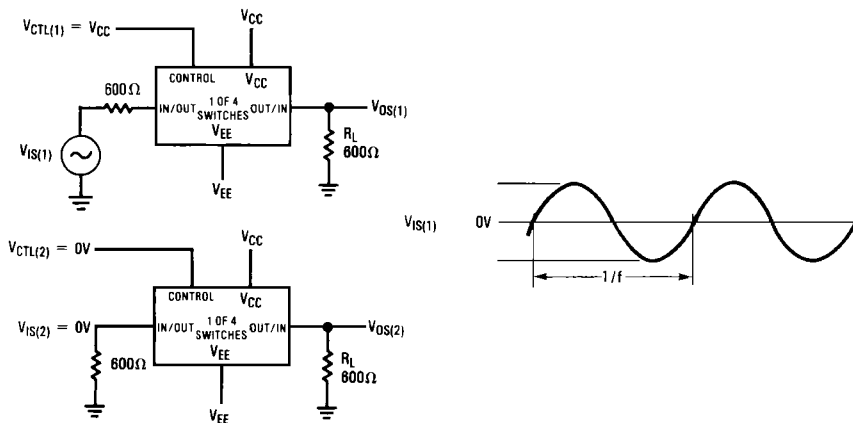


FIGURE 9. : Crosstalk Between Any Two Switches

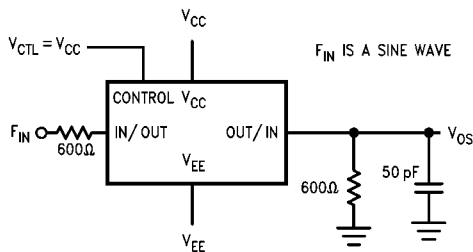


FIGURE 10. Switch OFF Signal Feedthrough Isolation

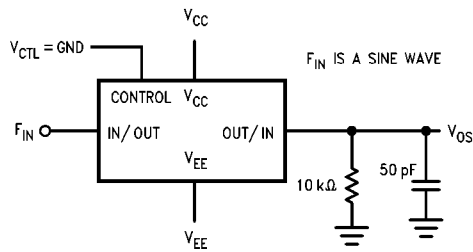
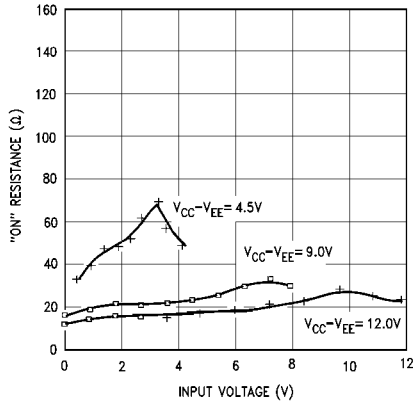


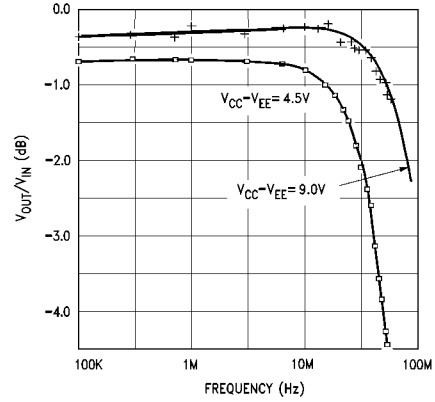
FIGURE 11. Sinewave Distortion

## Typical Performance Characteristics

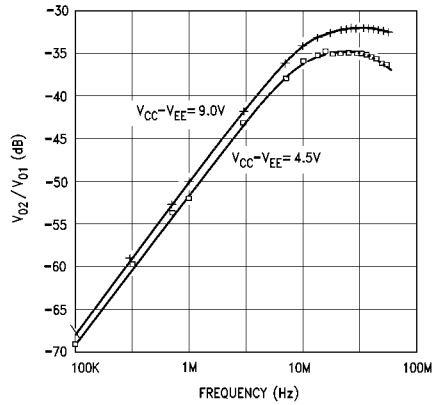
Typical "ON" Resistance



Typical Crosstalk Between Any Two Switches



Typical Frequency Response

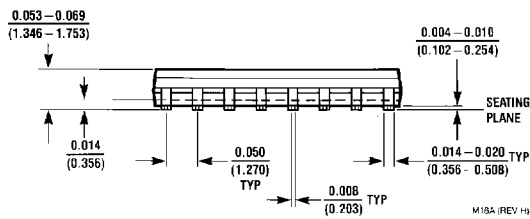
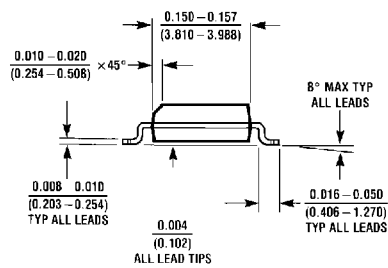
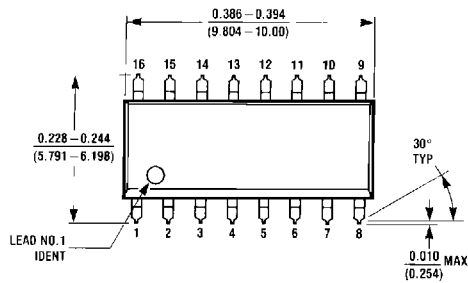


## Special Considerations

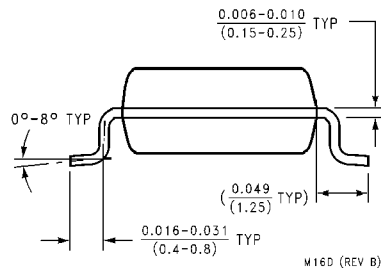
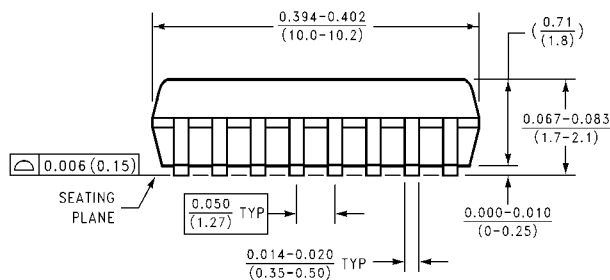
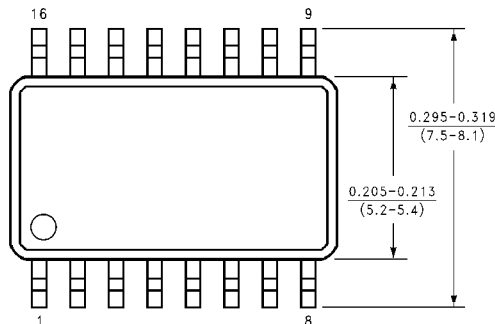
In certain applications the external load-resistor current may include both  $V_{CC}$  and signal line components. To avoid drawing  $V_{CC}$  current when switch current flows into

the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

**Physical Dimensions** inches (millimeters) unless otherwise noted

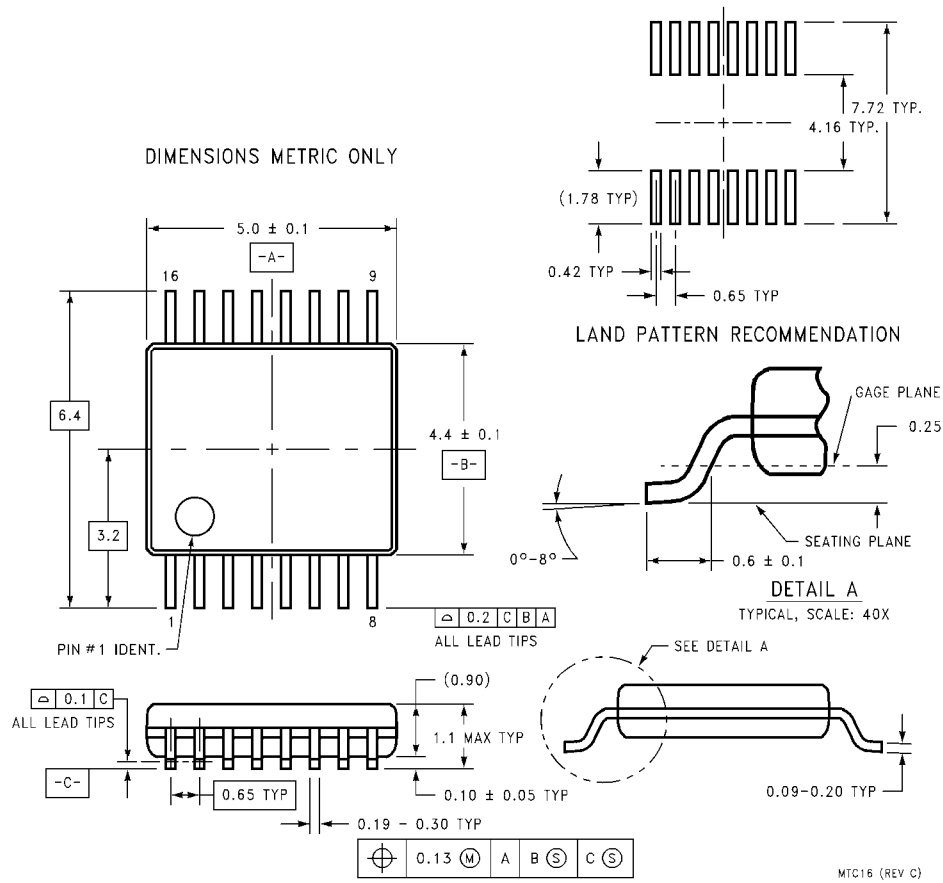


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**



**16-Lead small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

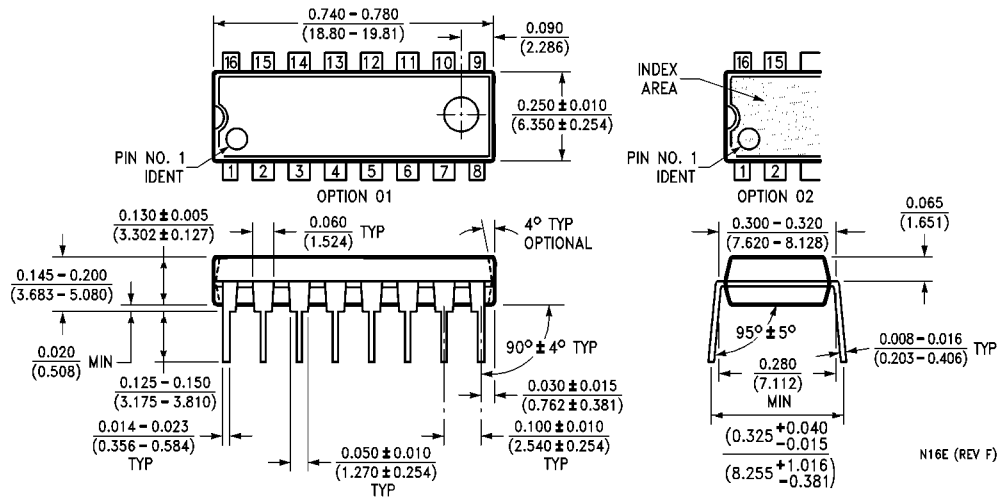
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

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