TS3A27518E-Q1 6-bit, 1-of-2 Multiplexer or Demultiplexer With Integrated IEC L-4 ESD and 1.8-V Logic Compatible Control Inputs

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 2: –40°C to 105°C ambient operating temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C3B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 1.65-V to 3.6-V single-supply operation
- Powered-off protection (isolation in powerdown mode, Hi-Z when $V_+ = 0$)
- Low capacitance switches, 21.5 pF (typical)
- Bandwidth up to 240 MHz for high-speed rail-to-rail signal handling
- Crosstalk and off isolation of −62 dB
- 1.8-V logic threshold compatibility for control inputs
- 3.6-V tolerant control inputs
- ESD performance: NC/NO ports
  - ±6-kV contact discharge (IEC 61000-4-2)
- 24-pin TSSOP (7.80 mm × 4.40 mm) and 24-pin QFN (4.00 mm × 4.00 mm) package

2 Applications

- SD/SDIO and MMC two port MUX
- PC VGA video MUX/video systems
- Audio and video signal routing

3 Description

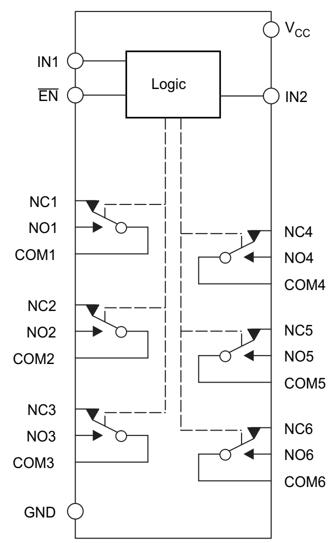
The TS3A27518E-Q1 is a 6-bit 1-of-2 multiplexer-demultiplexer designed to operate from 1.65 V to 3.6 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction. The TS3A27518E-Q1 has two control pins, each controlling three 1-of-2 muxes at the same time, and an enable pin that is used to put all outputs in high-impedance mode. The control pins are compatible with 1.8-V logic thresholds and are backward compatible with 2.5-V and 3.3-V logic thresholds as well.

The TS3A27518E-Q1 allows any SD, SDIO, and multimedia card host controllers to be expanded out to multiple cards or peripherals because the SDIO interface consists of 6-bits: CMD, CLK, and Data[0:3] signals. The TS3A27518E-Q1 has two control pins that give additional flexibility to the user, for example, the ability to mux two different audio-video signals in equipment such as an LCD television, an LCD monitor, or a notebook docking station.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A27518E-Q1	RTW (WQFN, 24)	4.00 mm × 4.00 mm
	PW (TSSOP, 24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2019) to Revision D (November 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document......1
- Added functional safety-capable information to the *Features* section......1

Changes from Revision B (May 2012) to Revision C (January 2019) **Page**

- Added *Device Information* table, *ESD Ratings* table, *Recommended Operating Conditions* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section......1
- Updated the numbering format for tables, figures, and cross-references throughout the document......1

Changes from Revision A (March 2012) to Revision B (May 2012) **Page**

- Changed device temp grade from 1 to 2, removed maximum withstand voltage info, changed C3B2 to C3B.. 1
- Added extra row to ordering information table......1
- Changed T_A = –40°C to 85°C to T_A = –40°C to 105°C......5
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C and limits -7.5 to 7.5......5
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C with limits 68......5
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C with limits 70......5
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C with limits 5 μA......5
- Changed T_A = –40°C to 85°C to T_A = –40°C to 105°C......7
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C with limits 38.4......7
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C with limits 3......7
- Changed T_A = –40°C to 85°C to T_A = –40°C to 105°C......9
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C and limits –5.8 to 5.8......9
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C with limits 35.2......9
- Changed Full to –40°C to 85°C and added extra row with 85°C to 105°C with limits 2.5......9

5 Pin Configuration and Functions

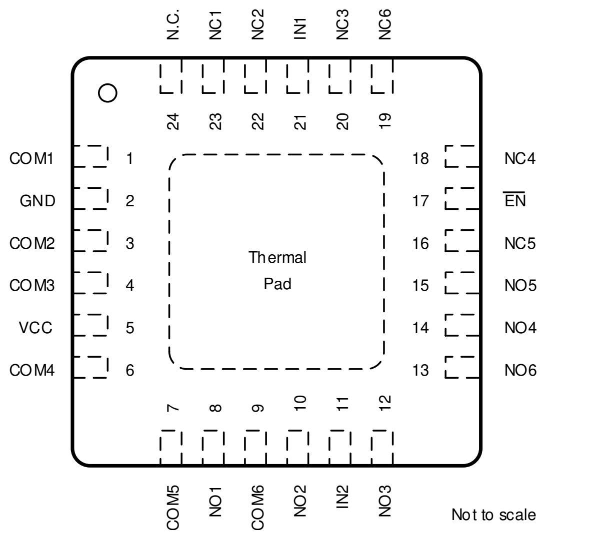


Figure 5-1. RTW Package, 24-Pin WQFN (Top View)

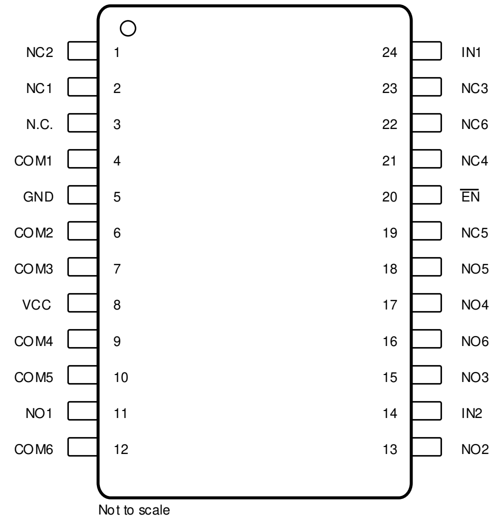


Figure 5-2. PW Package, 24-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	RTW	PW		
COM1	1	4	I/O	Common-signal path
COM2	3	6	I/O	Common-signal path
COM3	4	7	I/O	Common-signal path
COM4	6	9	I/O	Common-signal path
COM5	7	10	I/O	Common-signal path
COM6	9	12	I/O	Common-signal path
$\overline{EN}$	17	20	I	Digital control to enable or disable all signal paths
GND	2	5	—	Ground.
IN1	21	24	I	Digital control to connect COM to NC or NO
IN2	11	14	I	Digital control to connect COM to NC or NO
N.C.	24	3	—	Not connected
NC1	23	2	I/O	Normally closed-signal path
NC2	22	1	I/O	Normally closed-signal path
NC3	20	23	I/O	Normally closed-signal path
NC4	18	21	I/O	Normally closed-signal path
NC5	16	19	I/O	Normally closed-signal path
NC6	19	22	I/O	Normally closed-signal path
NO1	8	11	I/O	Normally open-signal path
NO2	10	13	I/O	Normally open-signal path
NO3	12	15	I/O	Normally open-signal path
NO4	14	17	I/O	Normally open-signal path
NO5	15	18	I/O	Normally open-signal path
NO6	13	16	I/O	Normally open-signal path
V_{CC}	5	8	—	Voltage supply

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_+	Supply voltage range[(2)]		–0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range[(2) (3) (4)]		–0.5	4.6	V
I_K	Analog port diode current[(5)]	$V_+ < V_{NC}, V_{NO}, V_{COM} < 0$	–50		mA
I_{NC} I_{NO} I_{COM}	ON-state switch current[(6)]	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–50	50	mA
V_I	Digital input voltage range[(2) (3)]		–0.5	4.6	V
I_{IK}	Digital input clamp current[(2) (3)]	$V_{IO} < V_I < 0$	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) Requires clamp diodes on analog port to V_+.
(6) Pulse at 1-ms duration <10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] AEC-Q100 Classification Level H2	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)] AEC-Q100 Classification Level C3B	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process..
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	1.65	3.6	V
Analog signal voltage	V_{NC}	0	V_{CC}	V
	V_{NO}			
	V_{COM}			
Digital input voltage	V_I	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC (1)		TS3A27518E PW (TSSOP) 24 PINS	TS3A27518E RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	42.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.1	19.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
ON-state resistance	r_{on}	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –32 mA,	Switch ON, See Figure 7-1	25°C	3 V		4.4	6.2	Ω
				Full				7.6	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 2.1 V, I_{COM} = –32 mA,	Switch ON, See Figure 7-1	25°C	3 V		0.3	0.7	Ω
				Full				0.8	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –32 mA,	Switch ON, See Figure 7-2	25°C	3 V		0.95	2.1	Ω
				Full				2.3	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 7-2	25°C	3.6 V	–0.5	0.05	0.5	µA
				Full		–7		7	
	$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$	V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0, or V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,		25°C	0 V	–1	0.05	1	
				Full		–12		12	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V, or V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V,	Switch OFF, See Figure 7-2	25°C	3.6 V	–1	0.01	1	µA
				Full		–2		2	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V, or V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–1	0.02	1	
				Full		–12		12	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 7-3	25°C	3.6 V	–2.5	0.04	2.2	µA
				–40°C to 85°C		–7		7	
				85°C to 105°C		–7.5		7.5	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 7-3	25°C	3.6 V	–2	0.03	2	µA
				Full		–7		7	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(1)									
Input logic high	V_{IH}			Full	3.6 V	1.2		3.6	V
Input logic low	V_{IL}			Full	3.6 V	0		0.65	V

6.5 Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Input leakage current	I_{IH}, I_{IL}	$V_I = V_+$ or 0		25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–2.5		2.5	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	3.3 V		18.1	59	ns
				–40°C to 85°C	3 V to 3.6 V			60	
				85°C to 105°C				68	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	3.3 V		25.4	60.6	ns
				–40°C to 85°C	3 V to 3.6 V			61	
				85°C to 105°C				70	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-6	25°C	3.3 V	4	11.1	22.7	ns
				Full	3 V to 3.6 V			28	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 7-10	25°C	3.3 V		0.81		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 7-4	25°C	3.3 V		13		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 7-4		3.3 V		8.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 7-4	25°C	3.3 V		21.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 7-4	25°C	3.3 V		21.5		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND	See Figure 7-4	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 7-6	25°C	3.3 V		240		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 7-8	25°C	3.3 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 7-9	25°C	3.3 V		–62		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 7-9	25°C	3.3 V		–71		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 7-11	25°C	3.3 V		0.05		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		0.04	0.3	µA
				–40°C to 85°C				3	
				85°C to 105°C				5	

(1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.6 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
ON-state resistance	r_{on}	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 7-1	25°C	2.3 V		5.5	9.6	Ω
				Full				11.5	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.6 V, I_{COM} = –32 mA,	Switch ON, See Figure 7-1	25°C	2.3 V		0.3	0.8	Ω
				Full				0.9	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 7-2	25°C	2.3 V		0.91	2.2	Ω
				Full				2.3	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 7-2	25°C	2.7 V	–0.3	0.04	0.3	µA
				Full		–6		6	
	$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$	V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} =2.7 V to 0, or V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V,		25°C	0 V	–0.6	0.02	0.6	
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 7-2	25°C	2.7 V	–0.7	0.02	0.7	µA
				Full		–1		1	
	$I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V, or V_{NC} or V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,		25°C	0 V	–0.7	0.02	0.7	
				Full		–7.2		7.2	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NC} or V_{NO} = 0.5 V or 2.3 V, V_{COM} = Open,	Switch ON, See Figure 7-3	25°C	2.7 V	–2.1	0.03	2.1	µA
				Full		–6		6	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.3 V,	Switch ON, See Figure 7-3	25°C	2.7 V	–2	0.02	2	µA
				Full		–5.7		5.7	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(1)									
Input logic high	V_{IH}	V_I = V_+ or GND		Full	2.7 V	1.15		3.6	V
Input logic low	V_{IL}			Full	2.7 V	0		0.55	V
Input leakage current	I_{IH}, I_{IL}	V_I = V_+ or 0		25°C	2.7 V	-0.1	0.01	0.1	µA
				Full		–2.1		2.1	
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	2.5 V		17.2	36.8	ns
				Full	2.3 V to 2.7 V			42.5	
Turn-off time	t_{OFF}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	2.5 V		17.1	29.8	ns
				–40°C to 85°C	2.3 V to 2.7 V			34.4	
				85°C to 105°C				38.4	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = $V_+/2$, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-6	25°C	2.5 V	4.5	13	30	ns
				Full	2.3 V to 2.7 V			33.3	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 7-10	25°C	2.5 V		0.47		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 7-4	25°C	2.5 V		13.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 7-4		2.5 V		9		pF

6.6 Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 7-4	25°C	2.5 V		22		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 7-4	25°C	2.5 V		22		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 7-4	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 7-6	25°C	2.5 V		240		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 7-8	25°C	2.5 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 7-9	25°C	2.5 V		–62		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 7-9	25°C	2.5 V		–71		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 7-11	25°C	2.5 V		0.06		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.01	0.1	µA
				–40°C to 85°C				2	
				85°C to 105°C				3	

(1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.7 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
ON-state resistance	r_{on}	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA, Switch ON, See Figure 7-1	25°C	1.65 V		7.1	14.4	Ω
			Full				16.3	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –32 mA, Switch ON, See Figure 7-1	25°C	1.65 V		0.3	1	Ω
			Full				1.2	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA, Switch ON, See Figure 7-2	25°C	1.65 V		2.7	5.5	Ω
			Full				7.3	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V; Switch OFF, See Figure 7-2	25°C	1.95 V	–0.25	0.03	0.25	µA
			Full		–5		5	
	$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V, or V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0; Switch OFF, See Figure 7-2	25°C	0 V	–0.4	0.01	0.4	µA
			Full		–7.2		7.2	
COM OFF leakage current	$I_{COM(OFF)}$, $I_{COM(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V; Switch OFF, See Figure 7-2	25°C	1.95 V	–0.4	0.02	0.4	µA
			Full		–0.9		0.9	
	$I_{COM(PWROFF)}$, $I_{COM(PWROFF)}$	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V, or V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0; Switch OFF, See Figure 7-2	25°C	0 V	–0.4	0.02	0.4	µA
			–40°C to 85°C		–5		5	
			85°C to 105°C		–5.8		5.8	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open; Switch ON, See Figure 7-3	25°C	1.95 V	–2	0.02	2	µA
			Full		–5.2		5.2	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V; Switch ON, See Figure 7-3	25°C	1.95 V	–2	0.02	2	µA
			Full		–5.2		5.2	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(1)								
Input logic high	V_{IH}	V_I = V_+ or GND	Full	1.95 V	1		3.6	V
Input logic low	V_{IL}		Full	1.95 V	0		0.4	V
Input leakage current	I_{IH}, I_{IL}	V_I = V_+ or 0	25°C	1.95 V	-0.1	0.01	0.1	µA
			Full		-2.1		2.1	
Dynamic								
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω, C_L = 35 pF, See Figure 7-5	25°C	1.8 V		14.1	49.3	ns
			Full	1.65 V to 1.95 V			56.7	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω, C_L = 35 pF, See Figure 7-5	25°C	1.8 V		16.1	26.5	ns
			–40°C to 85°C	1.65 V to 1.95 V			31.2	
			85°C to 105°C				35.2	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω, C_L = 35 pF, See Figure 7-6	25°C	1.8 V	5.3	18.4	58	ns
			Full	1.65 V to 1.95 V			58	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 7-10	25°C	1.8 V		0.21		pC

6.7 Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 7-4	25°C	1.8 V		9		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 7-4	25°C	1.8 V		22		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 7-4	25°C	1.8 V		22		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 7-4	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 7-6	25°C	1.8 V		240		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 7-8	25°C	1.8 V		-60		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 7-9	25°C	1.8 V		-60		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 7-9	25°C	1.8 V		-71		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 7-11	25°C	1.8 V		0.1		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.01	0.1	μA
				–40°C to 85°C				1.5	
				85°C to 105°C				2.5	

(1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.8 Typical Characteristics

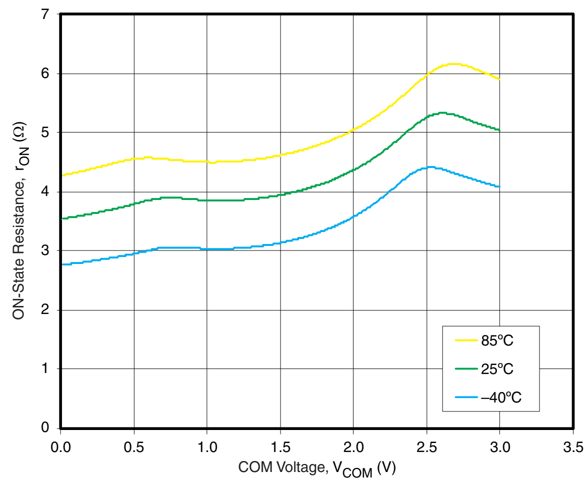


Figure 6-1. ON-State Resistance vs COM Voltage (V_{CC} = 3 V)

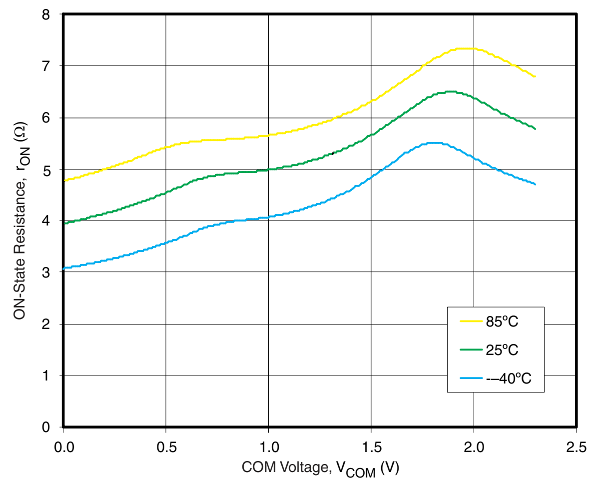


Figure 6-2. ON-State Resistance vs COM Voltage (V_{CC} = 2.3 V)

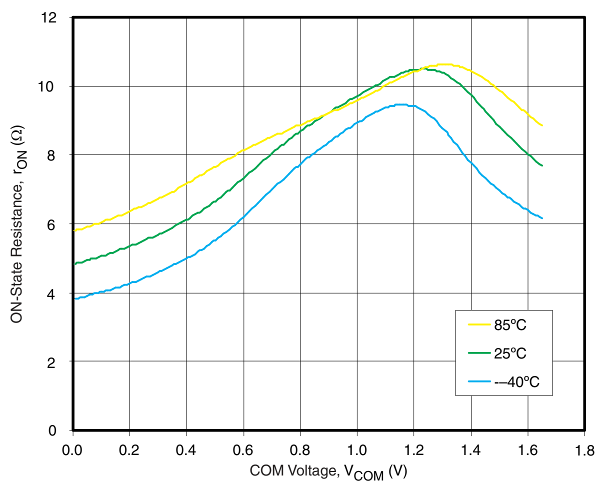


Figure 6-3. ON-State Resistance vs COM Voltage (V_{CC} = 1.65 V)

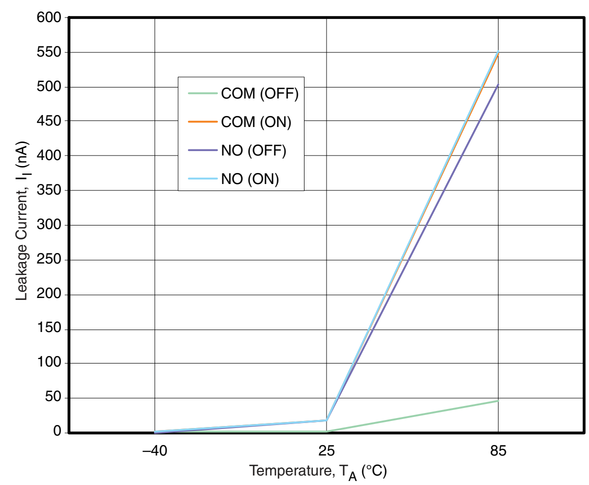


Figure 6-4. Leakage Current vs Temperature (V_{CC} = 3.3 V)

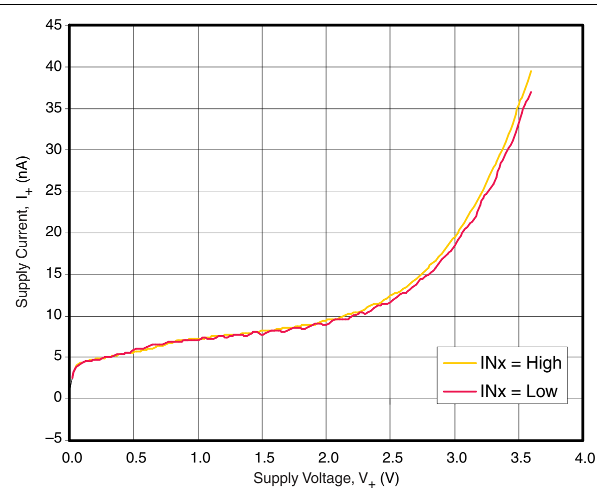


Figure 6-5. Supply Current vs Supply Voltage

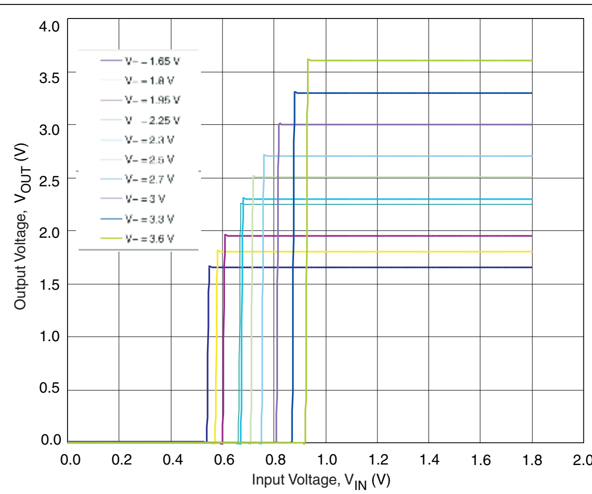


Figure 6-6. Control Input Thresholds (IN1, T_A = 25°C)

6.8 Typical Characteristics (continued)

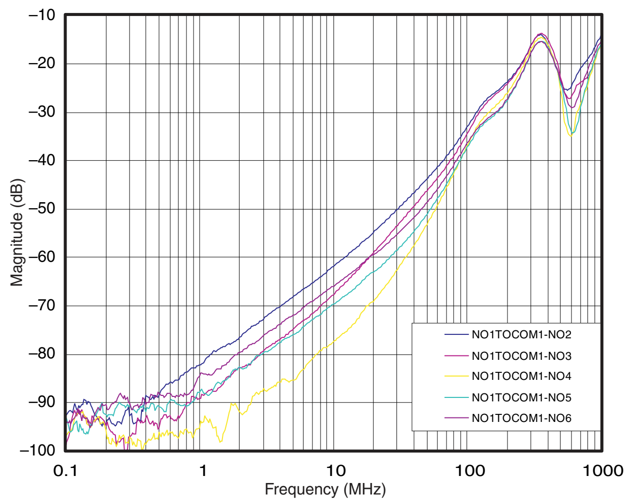


Figure 6-7. Crosstalk Adjacent

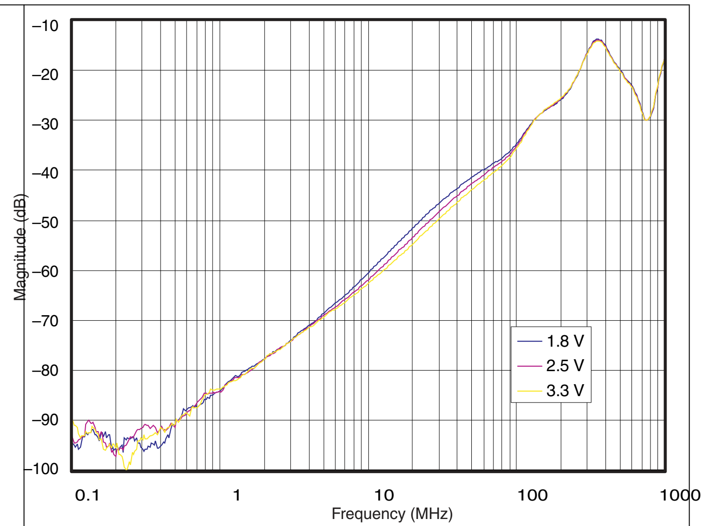


Figure 6-8. Crosstalk

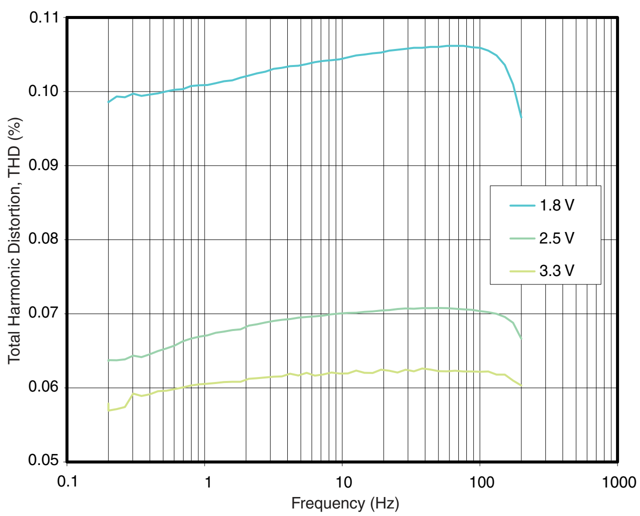


Figure 6-9. Total Harmonic Distortion vs Frequency

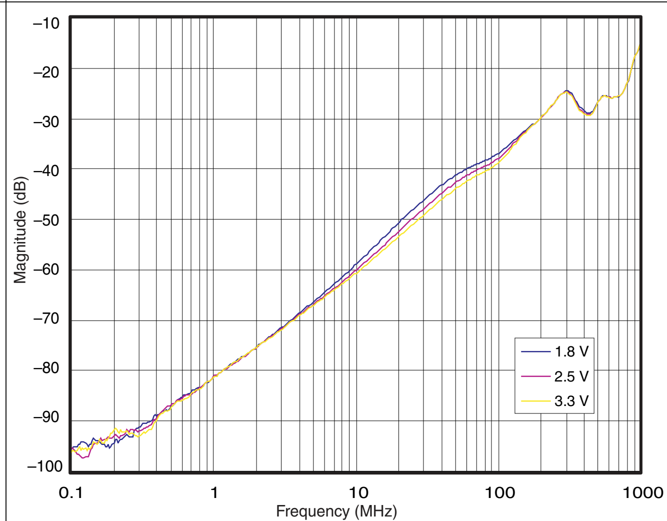


Figure 6-10. OFF Isolation

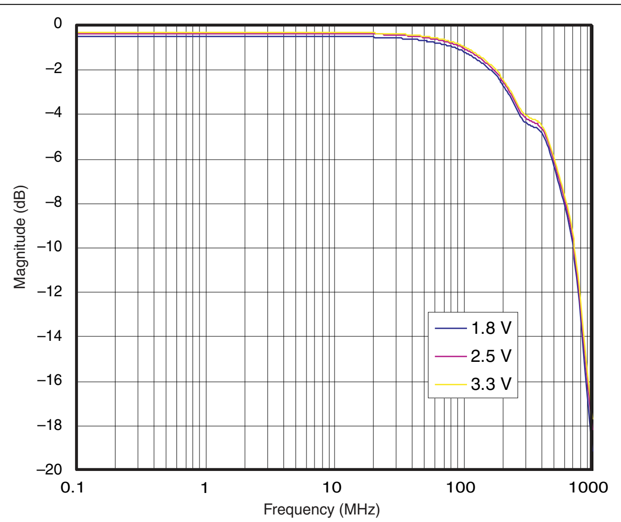


Figure 6-11. Insertion Loss

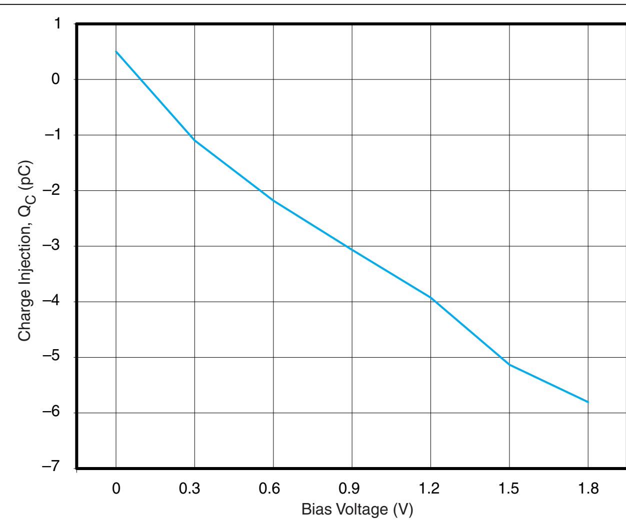


Figure 6-12. Charge Injection vs Bias Voltage (1.8 V)

6.8 Typical Characteristics (continued)

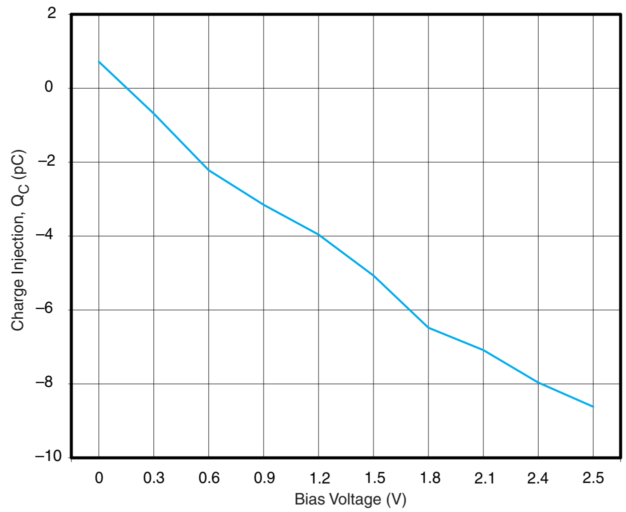


Figure 6-13. Charge Injection vs Bias Voltage (2.5 V)

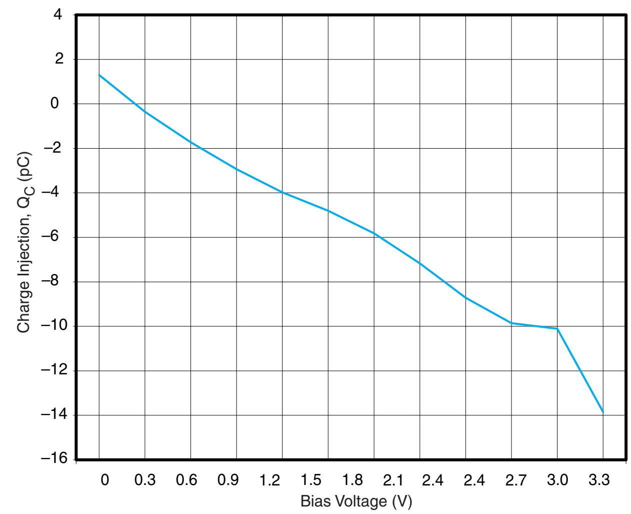


Figure 6-14. Charge Injection vs Bias Voltage (3.3 V)

7 Parameter Measurement Information

Table 7-1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output NC or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(OFF)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN, $\overline{EN}$)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2) .This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

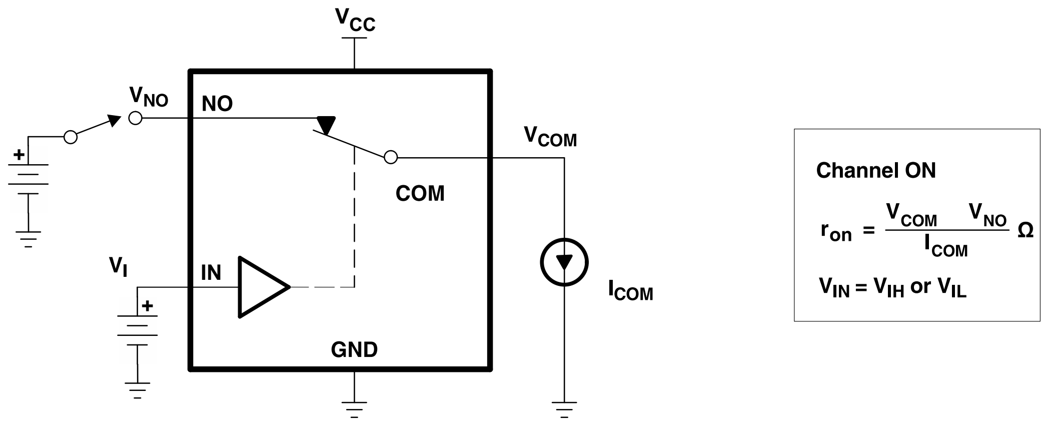


Figure 7-1. ON-state Resistance (r_{ON})

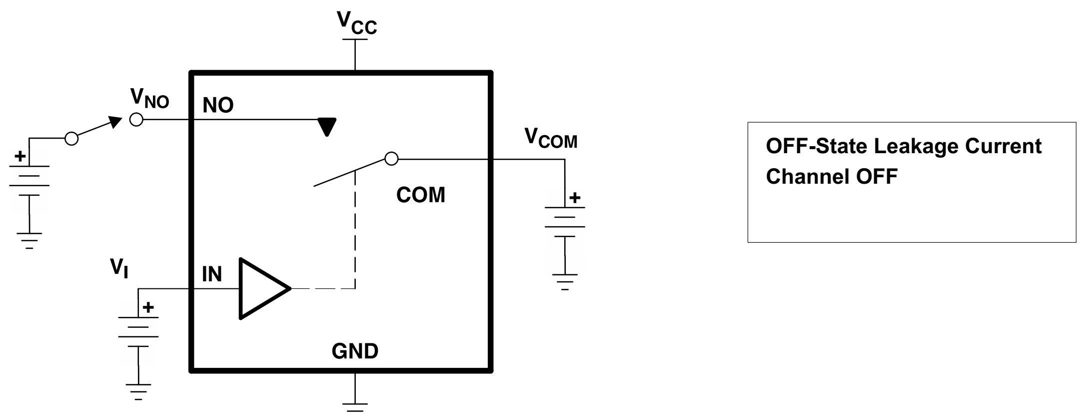


Figure 7-2. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

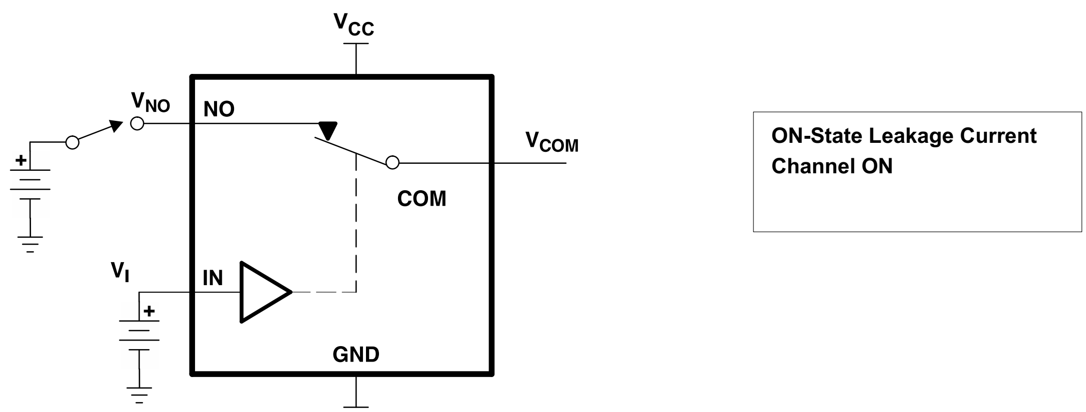


Figure 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

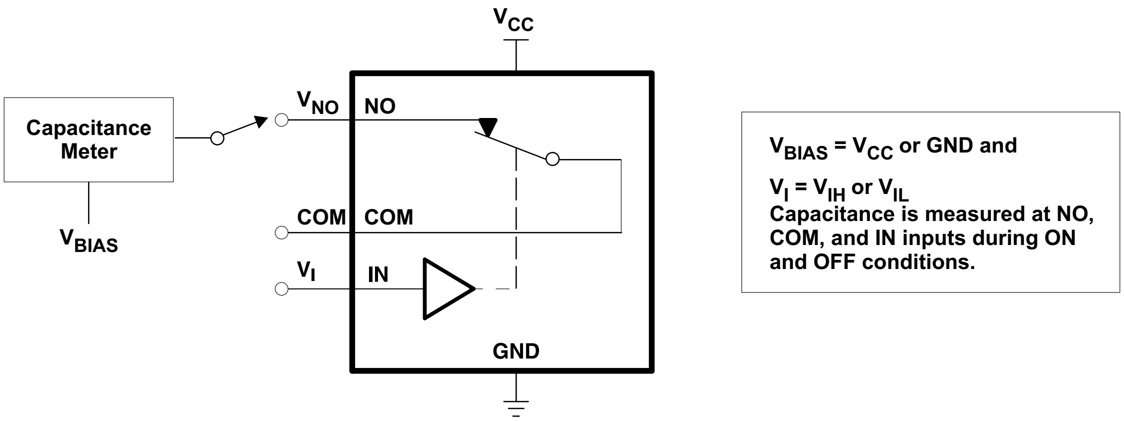
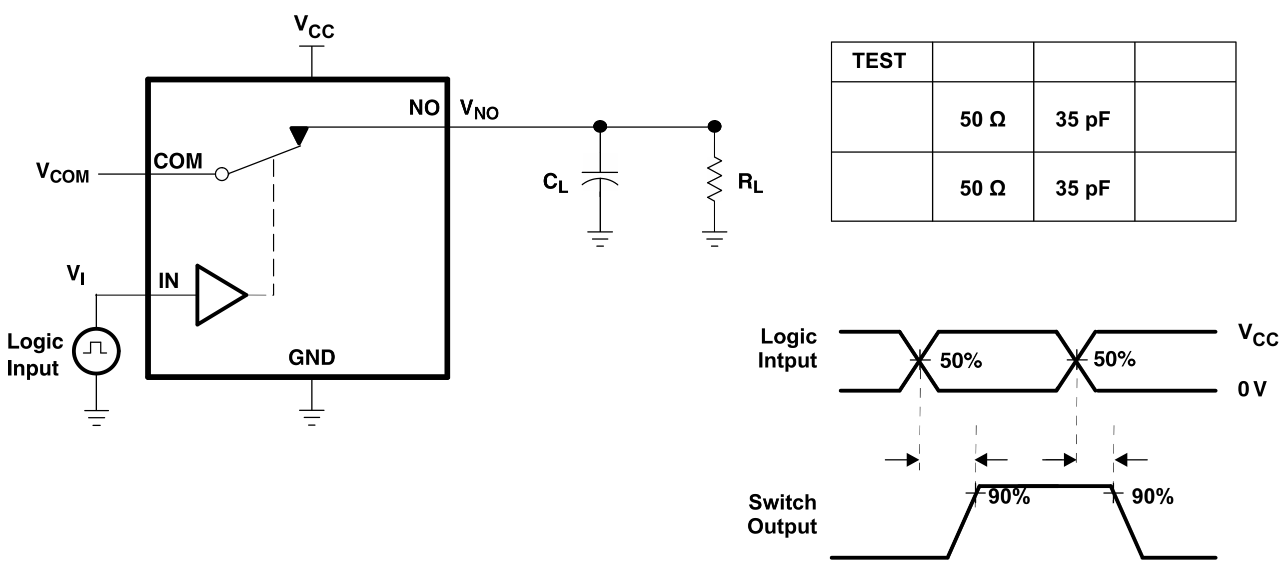


Figure 7-4. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)

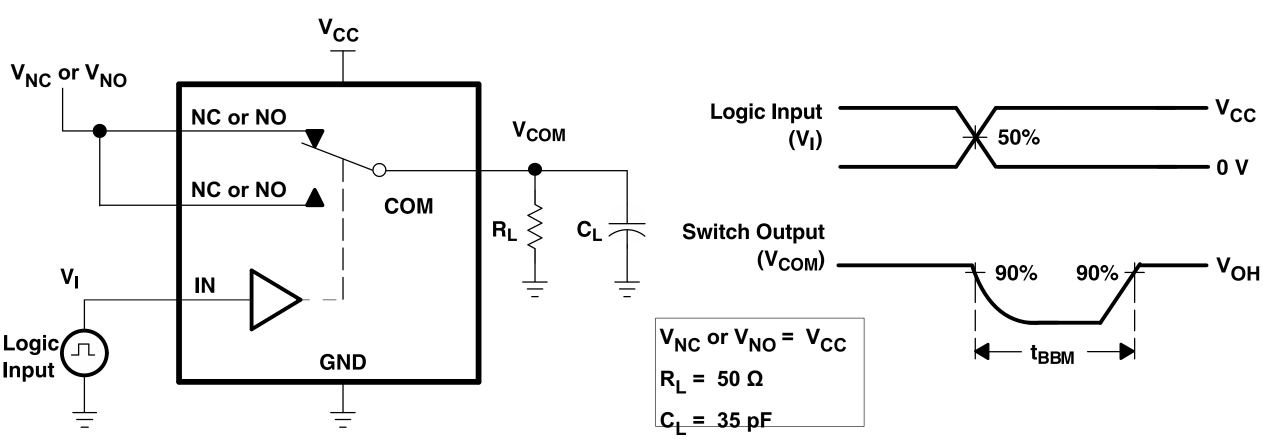


TEST			
	50 Ω	35 pF	
	50 Ω	35 pF	

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 7-5. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 7-6. Break-Before-Make Time (t_{BBM})

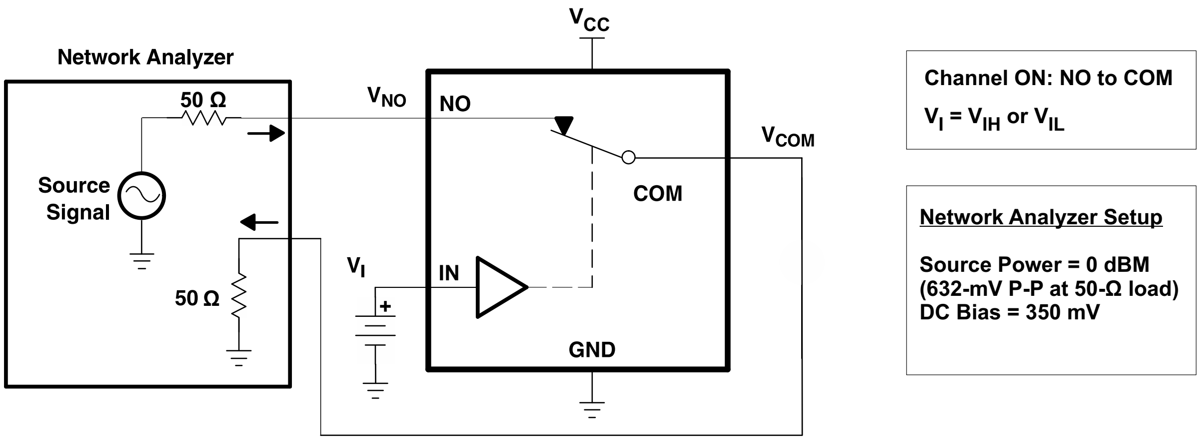


Figure 7-7. Bandwidth (BW)

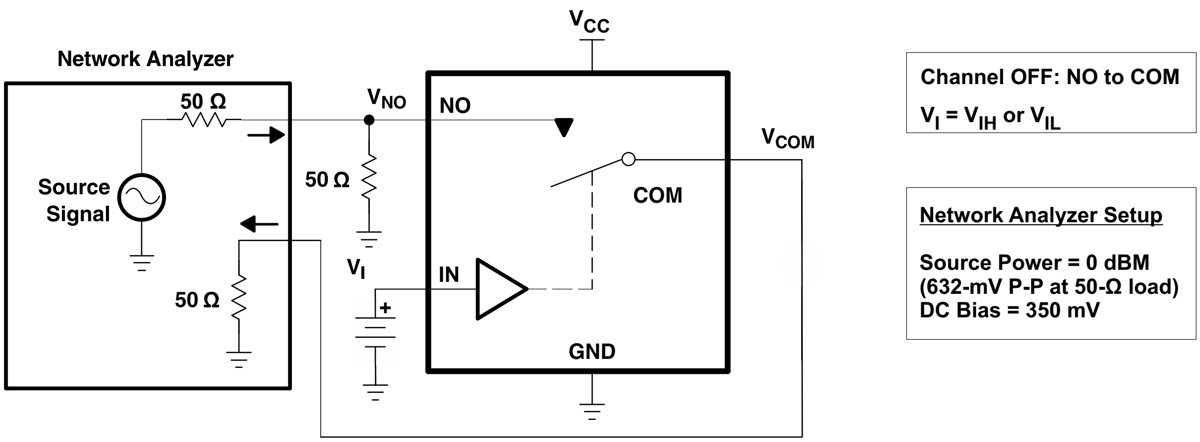


Figure 7-8. OFF Isolation (O_{ISO})

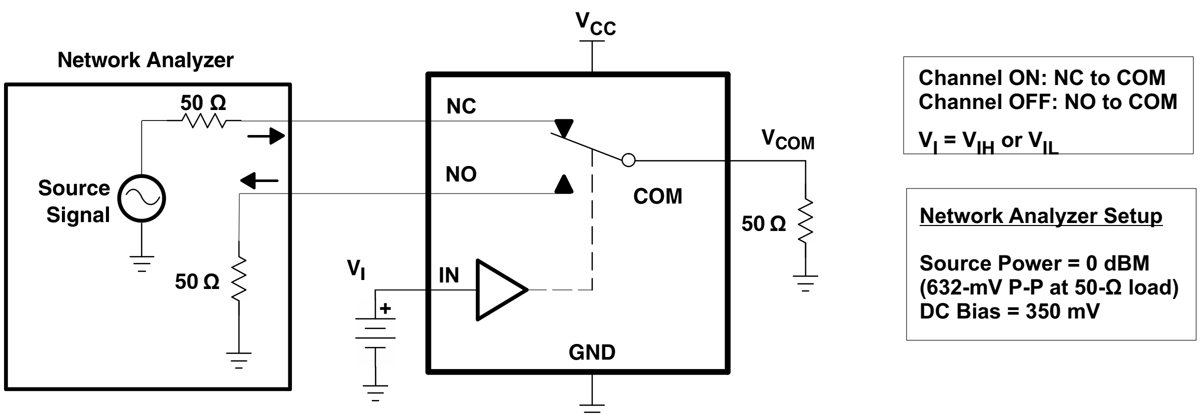
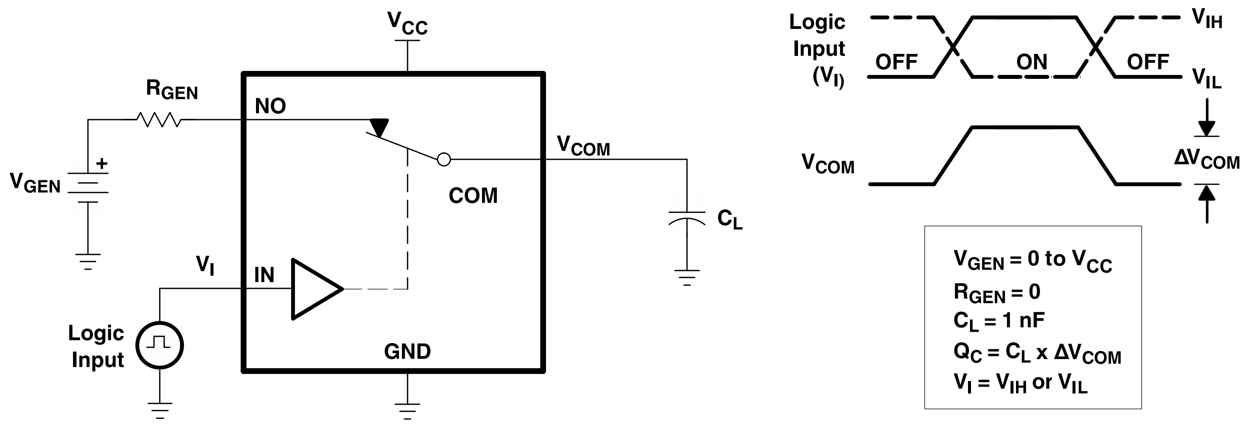


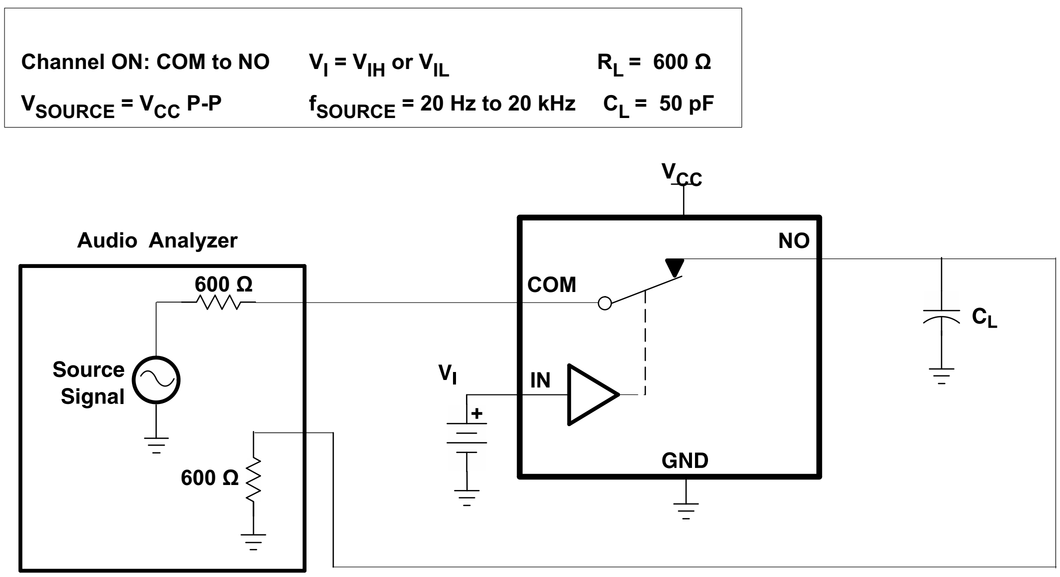
Figure 7-9. Crosstalk (X_{TALK})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 7-10. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

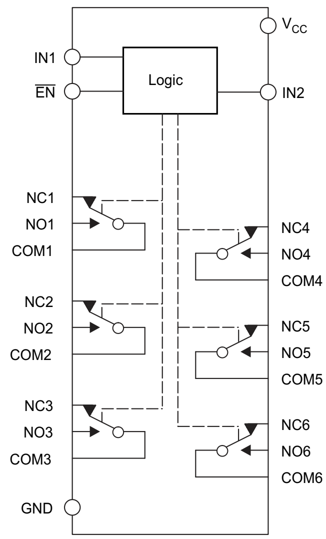
Figure 7-11. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A27518E-Q1 is a bidirectional, 6-channel, 1:2 multiplexer-demultiplexer designed to operate from 1.65 V to 3.6 V. This device can handle both digital and analog signals, and can transmit signals up to V_{CC} in either direction. The TS3A27518E-Q1 has two control pins, each controlling three 1:2 muxes at the same time, and an enable pin that puts all outputs in high-impedance mode. The control pins are compatible with 1.8-V logic thresholds and are backward compatible with 2.5-V and 3.3-V logic thresholds.

8.2 Functional Block Diagram



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8.3 Feature Description

The isolation in power-down mode, V_{CC} = 0 feature places all switch paths in high-impedance state (High-Z) when the supply voltage equals 0 V.

8.4 Device Functional Modes

The TS3A27518E-Q1 is a bidirectional device that has two sets of three single-pole double-throw switches. Two digital signals control the 6 channels of the switch; one digital control for each set of three single-pole, double-throw switches. Digital input pin IN1 controls switches 1, 2, and 3, while pin IN2 controls switches 4, 5, and 6.

The TS3A27518E-Q1 has an $\overline{EN}$ pin that when set to logic high, it places all channels into a high-impedance or HIGH-Z state. Table 8-1 lists the functions of TS3A27518E-Q1.

Table 8-1. Function Table

$\overline{EN}$	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

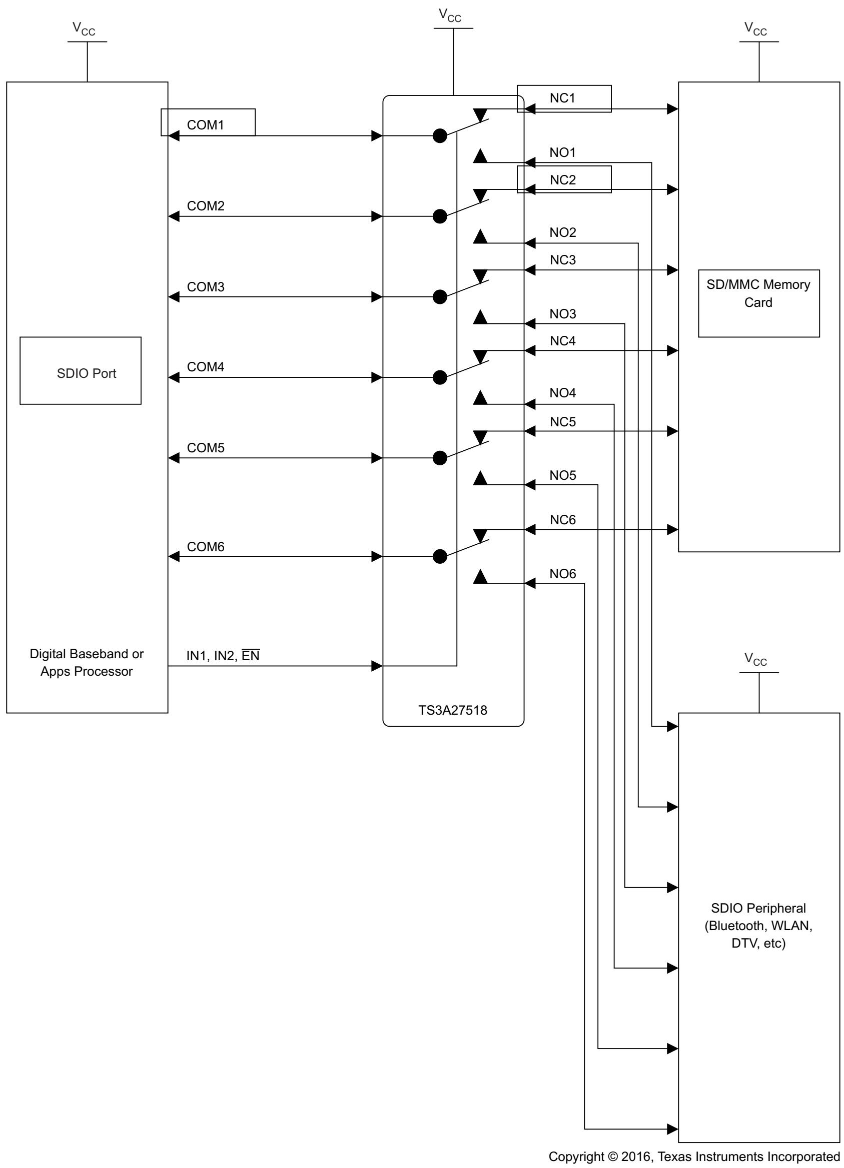

Figure 9-1. SDIO Expander Application Block Diagram

9.2.1 Design Requirement

Ensure that all of the signals passing through the switch are within the recommended operating ranges to ensure proper performance. For more information, see *Section 6.3*.

9.2.2 Detailed Design Procedure

The TS3A27518E-Q1 can operate properly without any external components. However, TI recommends connecting unused pins to the ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends that the digital control pins (INX) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

For the RTW package connect the thermal pad to ground.

9.2.3 Application Curves

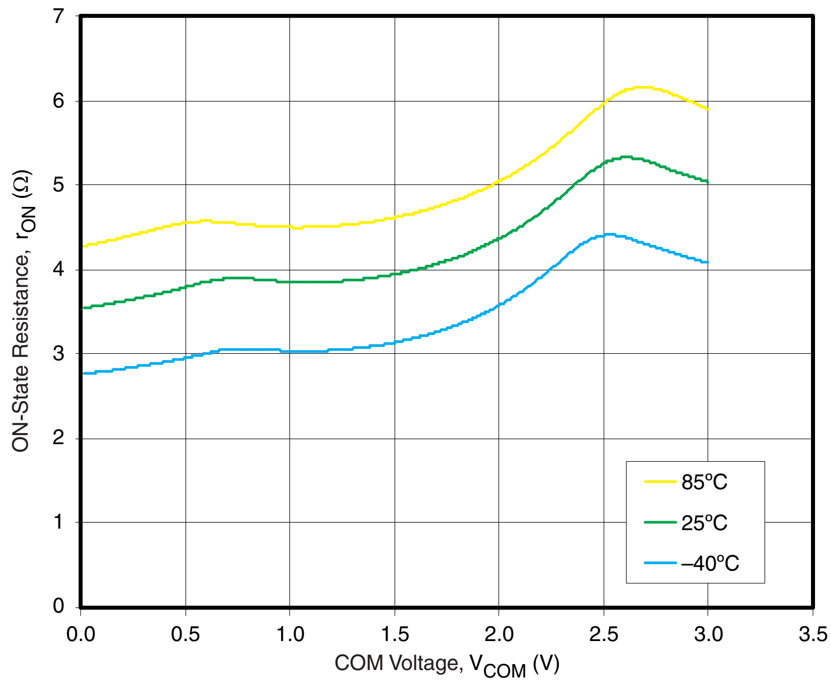

Figure 9-2. ON-State Resistance vs COM Voltage (V_{CC} = 3 V)

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_{CC} on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1-μF capacitor is adequate for most applications, if connected from V_{CC} to GND.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following these common printed-circuit board layout guidelines:

- Bypass capacitors should be used on power supplies, and should be placed as close as possible to the V_{CC} pin
- Short trace-lengths should be used to avoid excessive loading
- For the RTW package, connect the thermal pad to ground

11.2 Layout Example

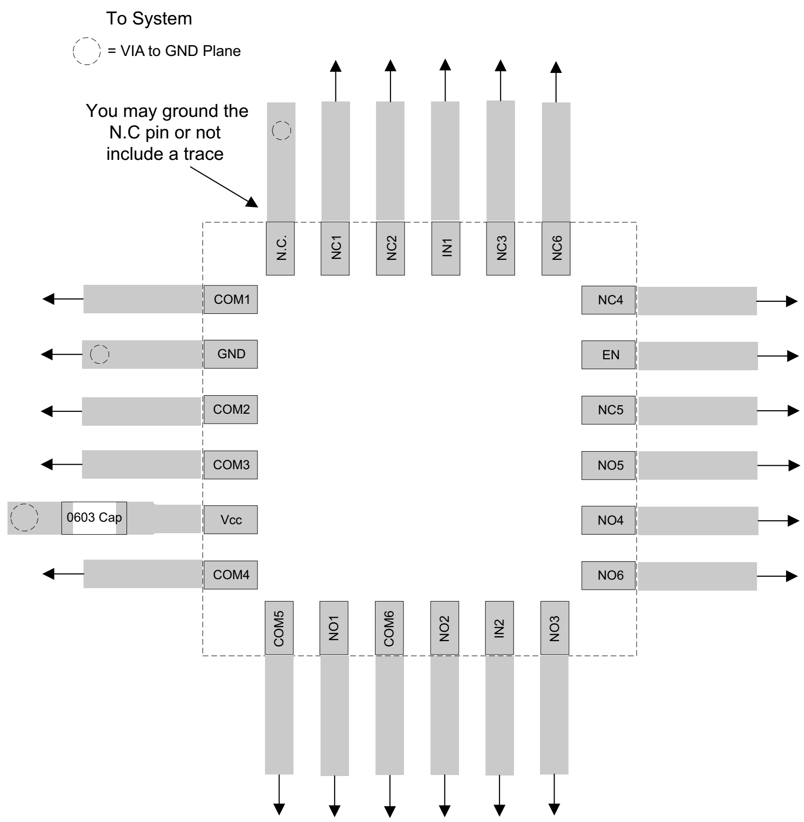

Figure 11-1. WQFN Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TS3A27518E-Q1 Functional Safety FIT Rate, FMD and Pin FMA* report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A27518EIPWRQ1	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	YL518EQ1	Samples
TS3A27518EIRTWRQ1	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	27518EI	Samples
TS3A27518ETRTWRQ1	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	27518ET	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS3A27518E-Q1 :

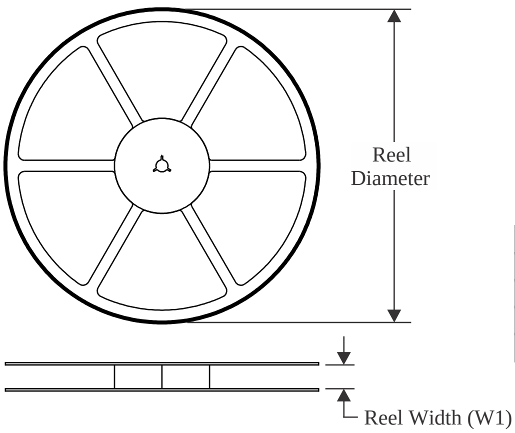
- Catalog : TS3A27518E

NOTE: Qualified Version Definitions:

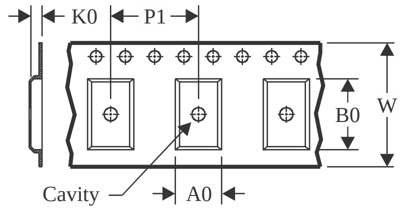
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

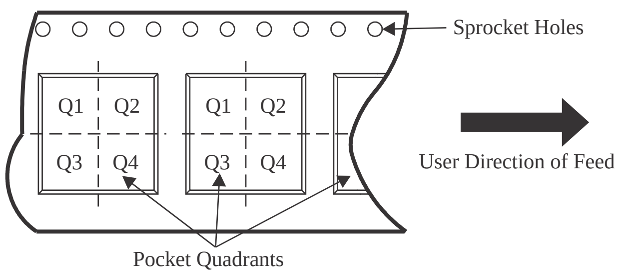


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

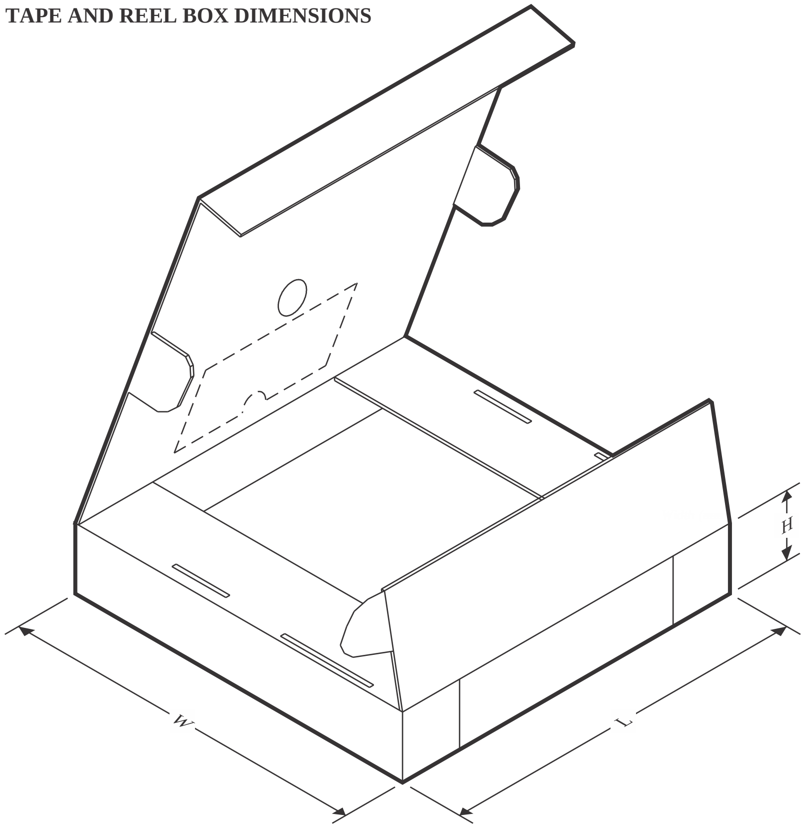
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

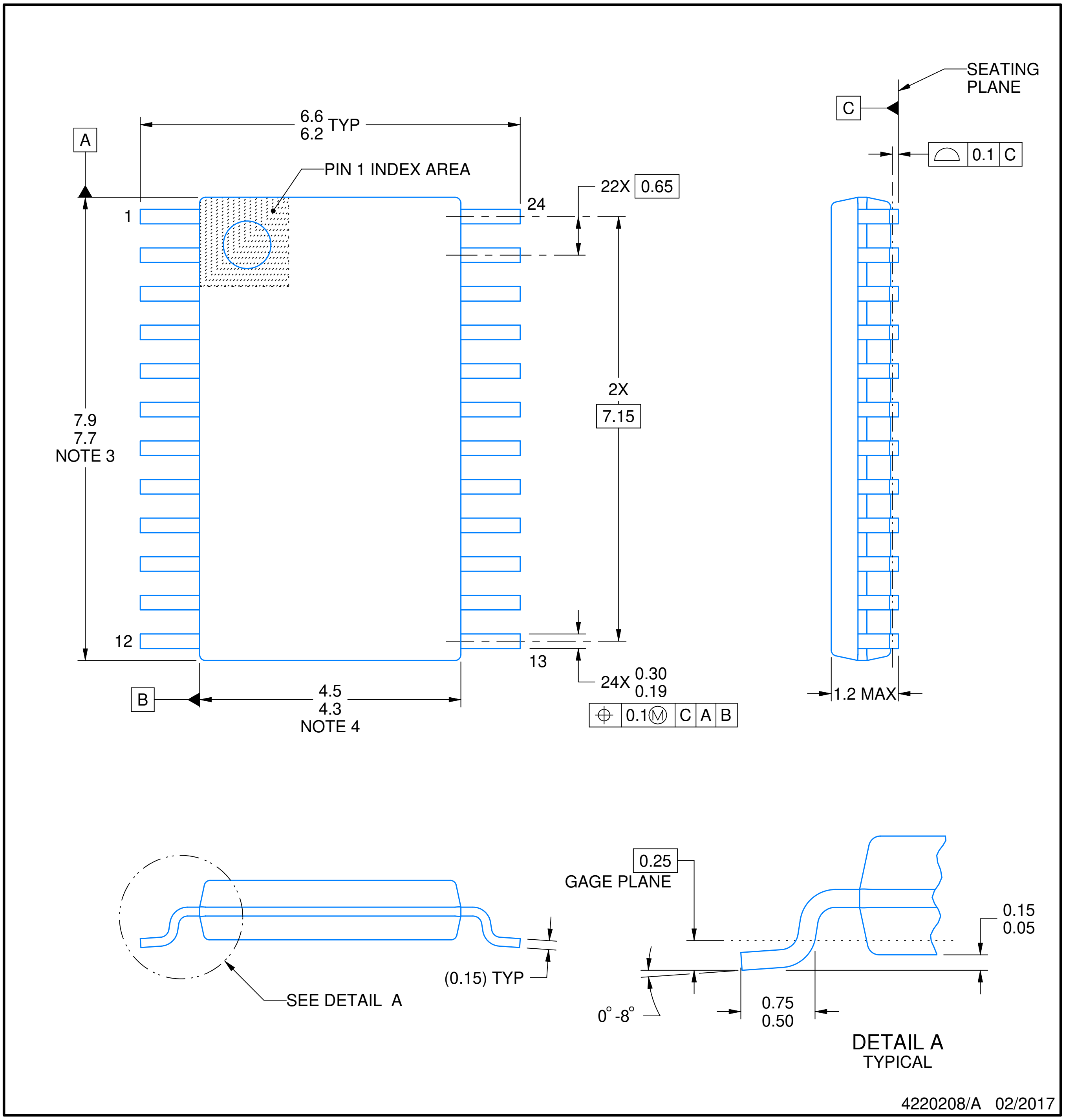
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A27518EIPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TS3A27518EIRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TS3A27518ETRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



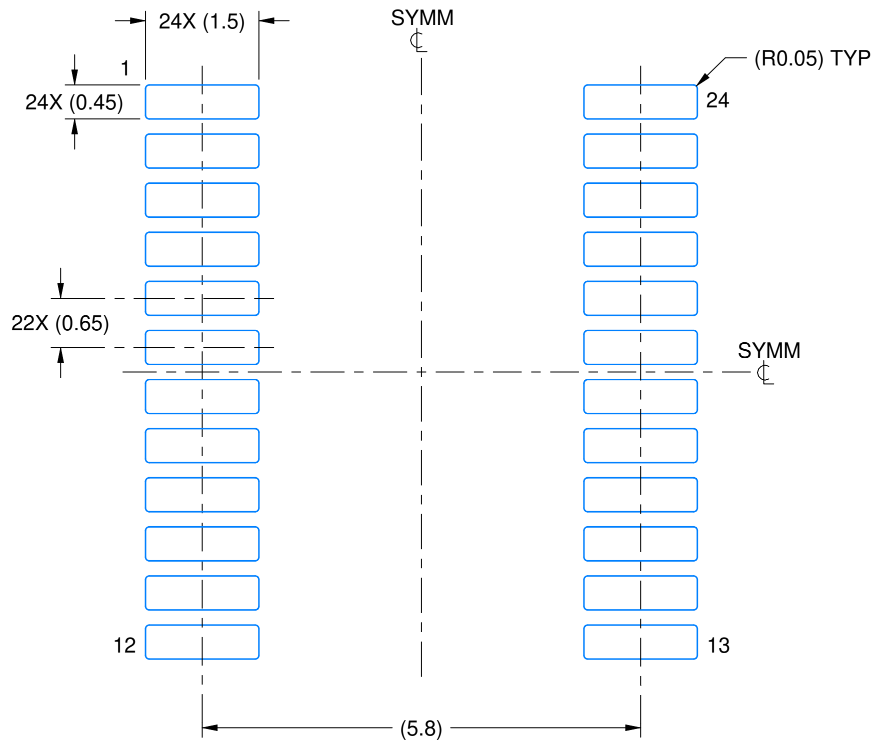
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A27518EIPWRQ1	TSSOP	PW	24	2000	356.0	356.0	35.0
TS3A27518EIRTWRQ1	WQFN	RTW	24	3000	356.0	356.0	35.0
TS3A27518ETRTWRQ1	WQFN	RTW	24	3000	356.0	356.0	35.0

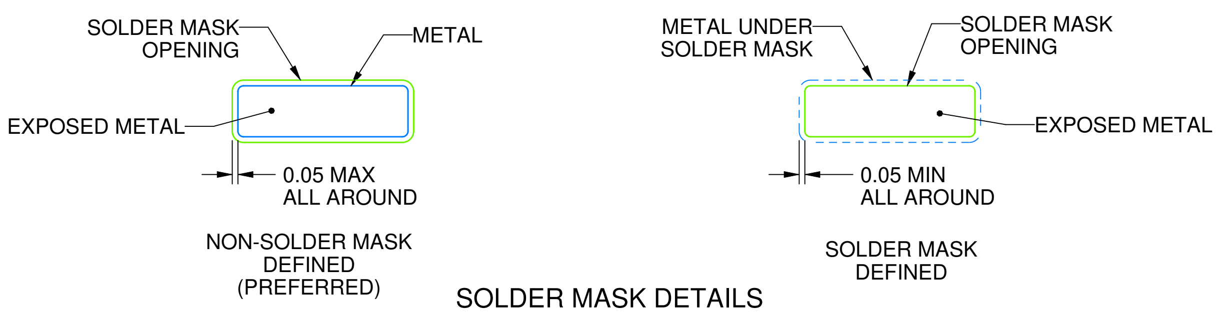


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

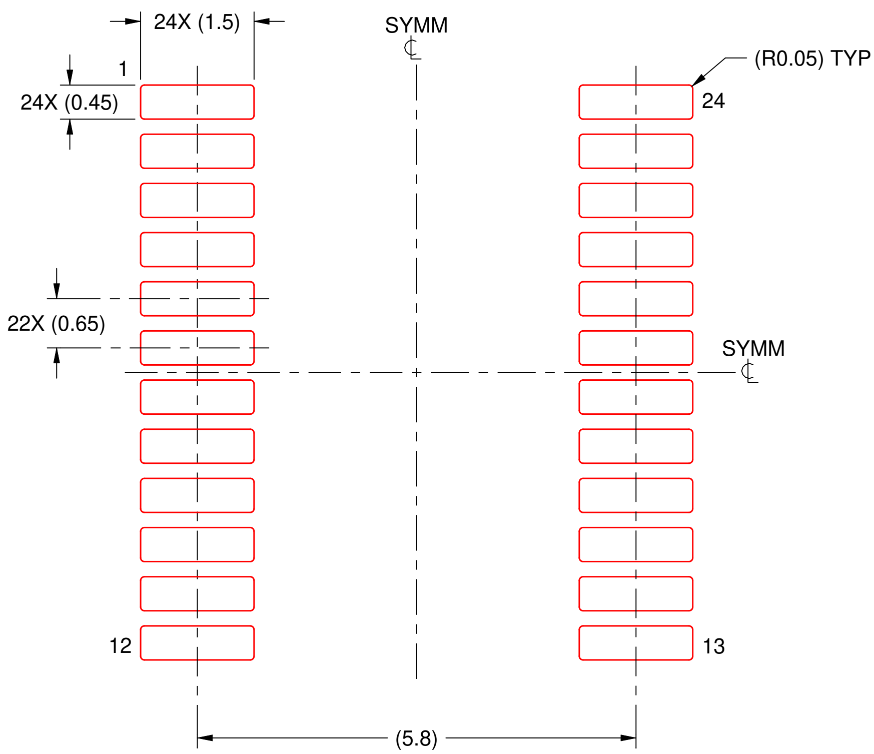


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



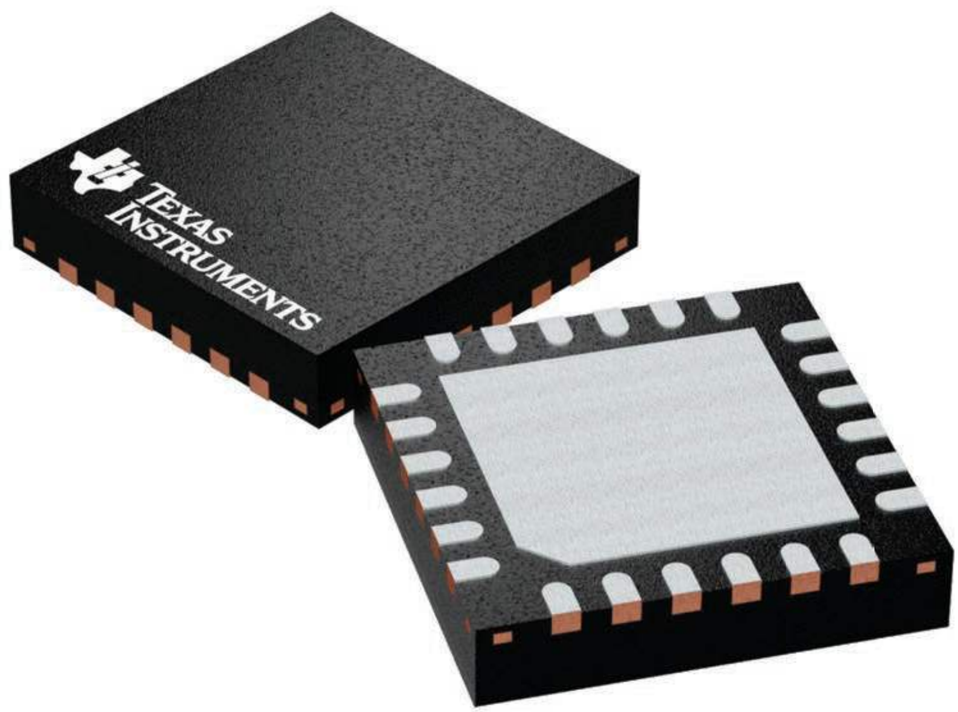
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

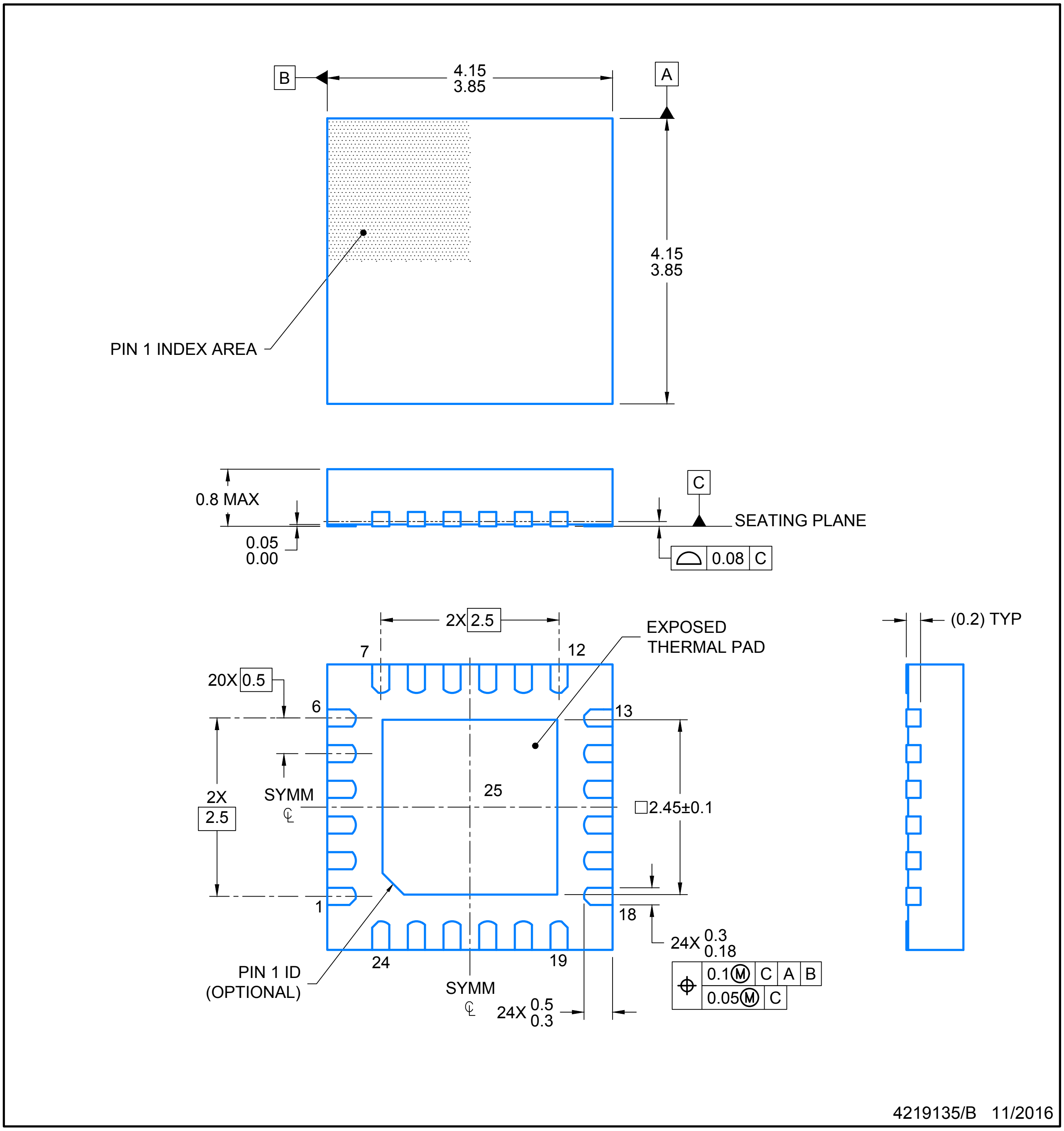
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

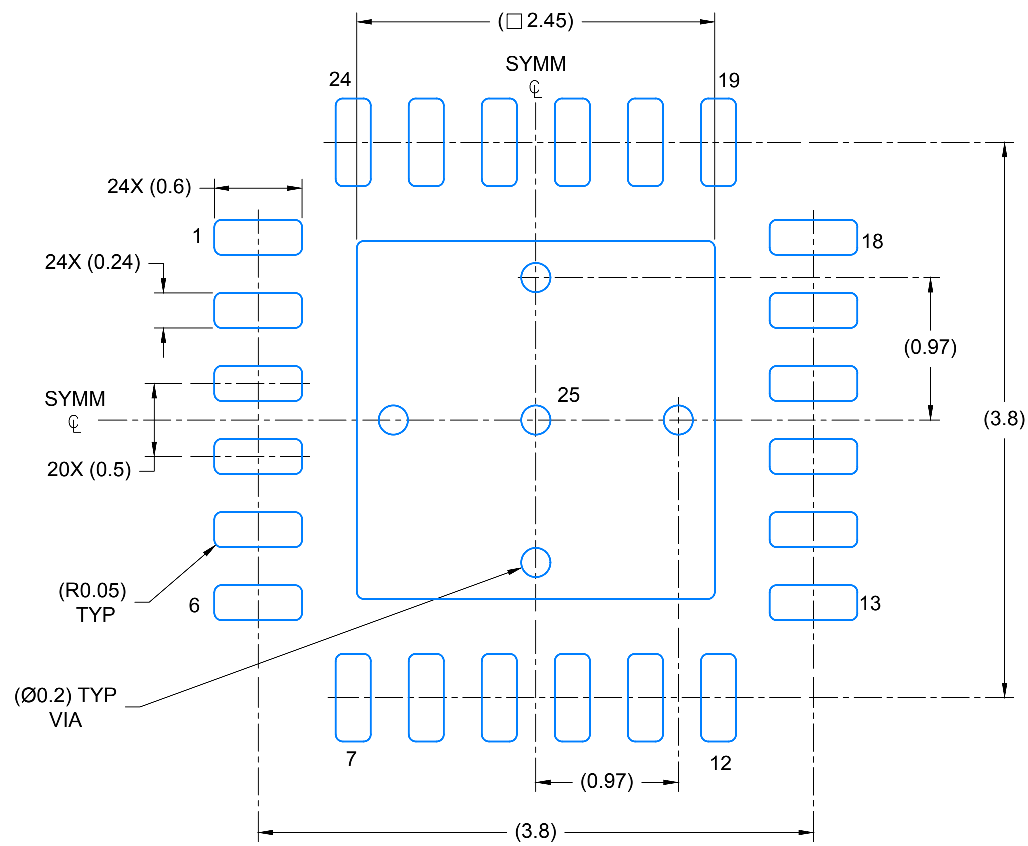


4224801/A

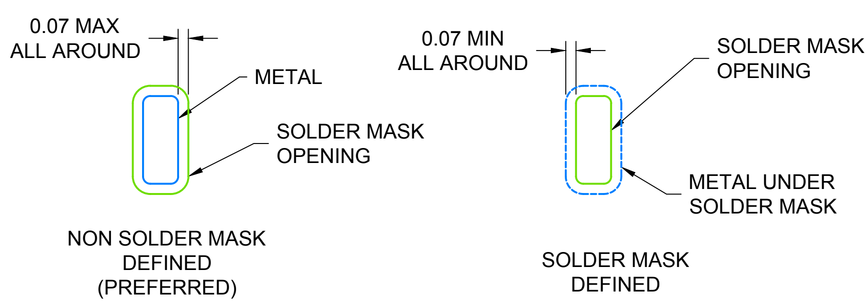


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 20X

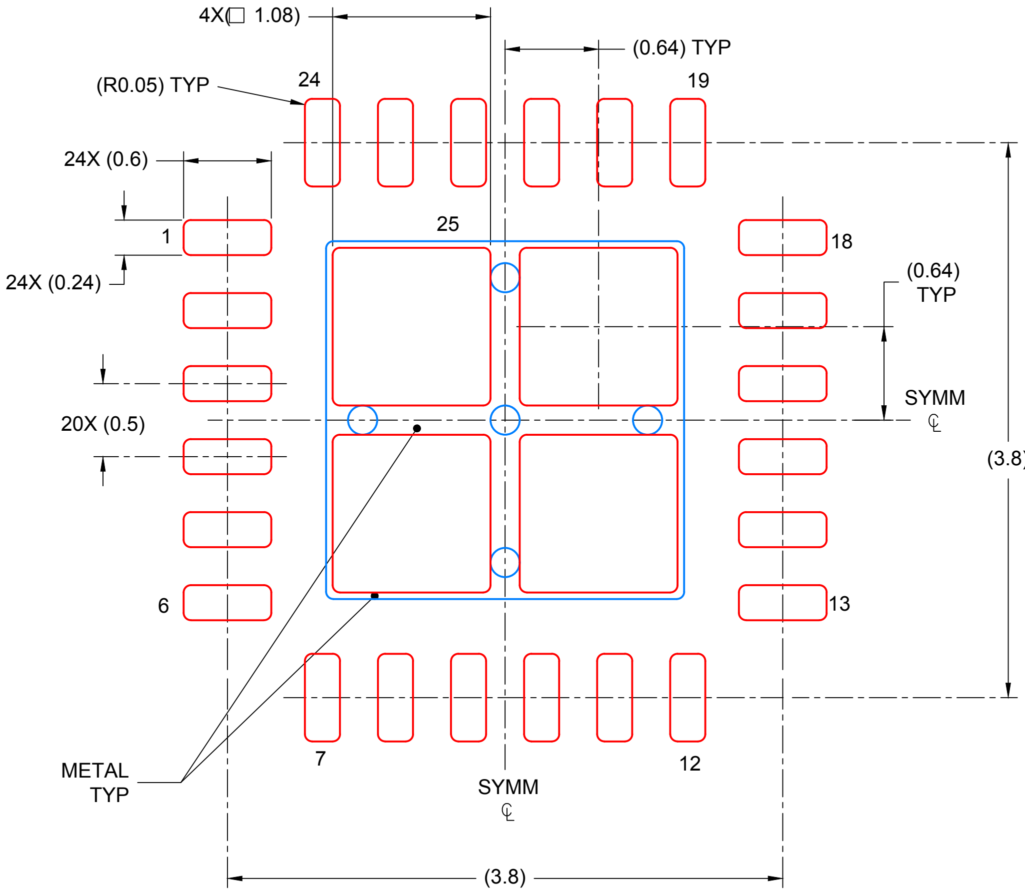


SOLDER MASK DETAILS

4219135/B 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED COVERAGE BY AREA UNDER PACKAGE
SCALE: 20X

4219135/B 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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