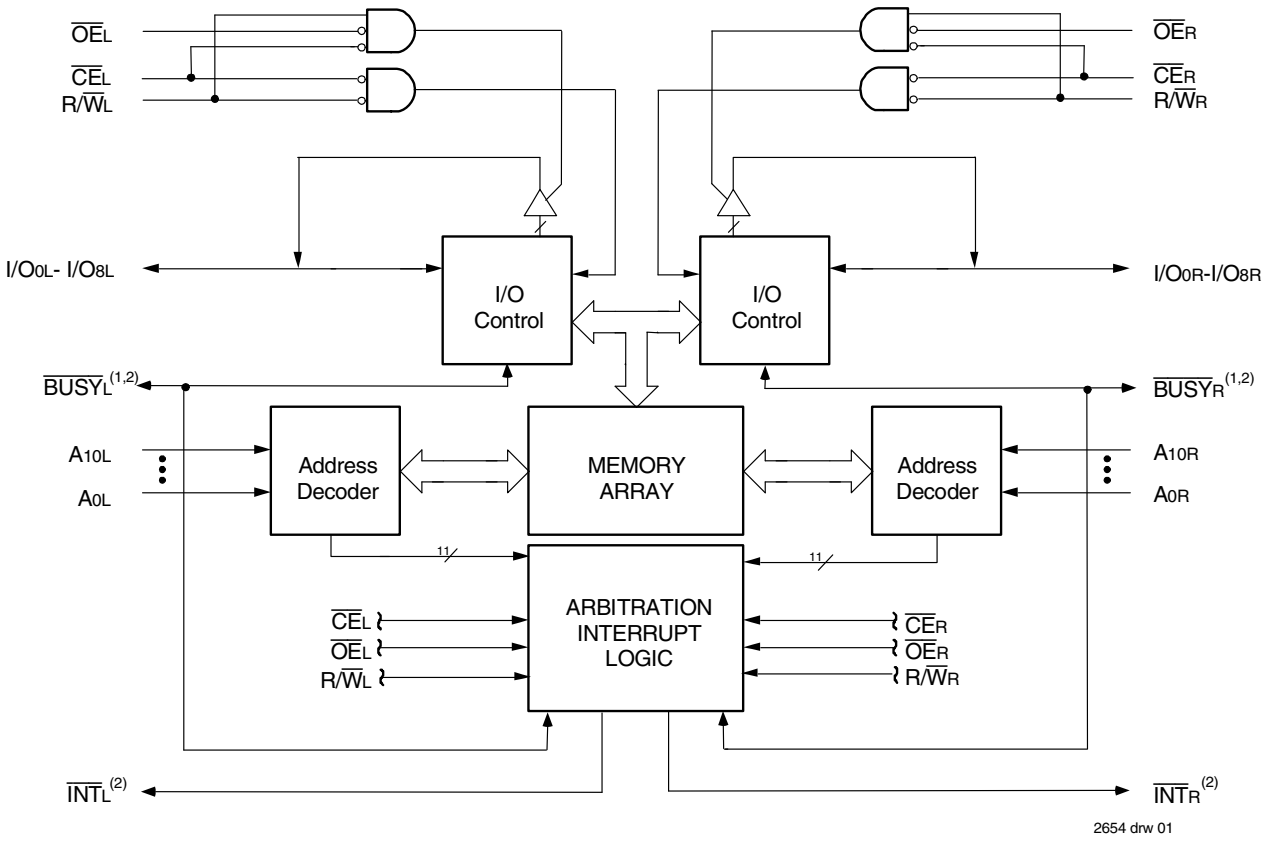
HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

70121L
70125L

Features

- High-speed access
  - *Commercial: 25ns (max.)*
- Low-power operation
  - *IDT70121/70125L*
    Active: 675mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- Fully asychronous operation from either port
- On-chip port arbitration logic (IDT70121 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Battery backup operation—2V data retention
- TTL-compatible, signal 5V (±10%) power supply
- Available in 52-pin PLCC
- Green parts available, see ordering information

Functional Block Diagram



NOTES:
1. 70121 (MASTER): $\overline{BUSY}$ is non-tri-stated push-pull output.
   70125 (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is non-tri-stated push-pull output.

SEPTEMBER 2019

Description

The IDT70121/IDT70125 are high-speed 2K x 9 Dual-Port Static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT70125 "SLAVE" Dual-Port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 18-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

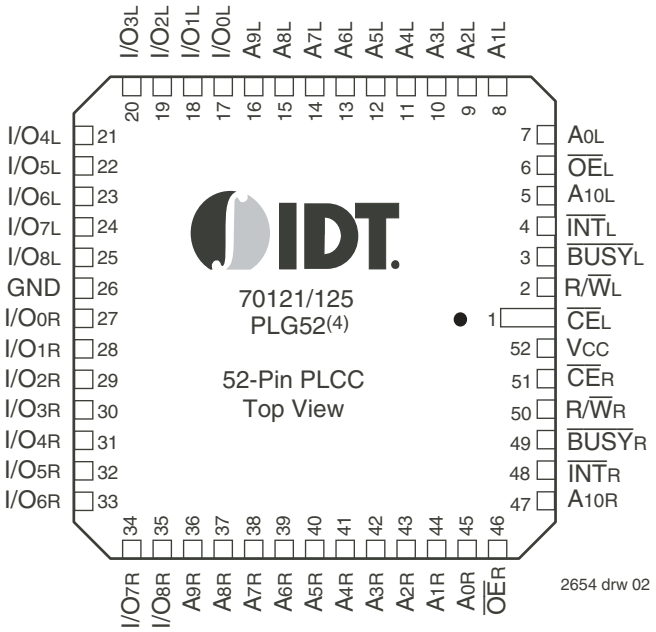
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121/IDT70125 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using CMOS high-performance technology, these devices typically operate on only 675mW of power. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µ W from a 2V battery.

The IDT70121/IDT70125 devices are packaged in a 52-pin PLCC.

Pin Configurations[1,2,3]



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately .75 in x .75 in x .17 in.
4. This package code is used to reference the package diagram.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

2654 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 10%.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2654 tbl 02

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2654 tbl 03

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions(1)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2654 tbl 04

NOTE:
1. This parameter is determined by device characterization but is not production tested.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	70121S 70125S		70121L 70125L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2654 tbl 05

NOTE:
1. At Vcc ≤ 2.0V leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,4] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		70121X25 70125X25 Com'l Only Typ.	70121X25 70125X25 Com'l Only Max.	70121X35 70125X35 Com'l & Ind Typ.	70121X35 70125X35 Com'l & Ind Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled f = f_{MAX}[2]	COM'L	S	135	260	135	250	mA
				L	135	220	135	210	
			IND	S	—	—	135	275	
				L	—	—	135	250	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}$"A" = $\overline{CE}$"B" = V_{IH} f = f_{MAX}[2]	COM'L	S	30	65	30	65	mA
				L	30	45	30	45	
			IND	S	—	—	30	80	
				L	—	—	30	65	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[2]	COM'L	S	80	175	80	165	mA
				L	80	145	80	135	
			IND	S	—	—	80	190	
				L	—	—	80	165	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}$"A" and $\overline{CE}$"B" ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[3]	COM'L	S	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	
			IND	S	—	—	1.0	15	
				L	—	—	0.2	5	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled, f = f_{MAX}[2]	COM'L	S	70	170	70	160	mA
				L	70	140	70	130	
			IND	S	—	—	70	185	
				L	—	—	70	160	

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Symbol	Parameter	Test Condition	Version		70121X55 70125X55 Com'l Only Typ.	70121X55 70125X55 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled f = f_{MAX}[2]	COM'L	S	135	240	mA
				L	135	200	
			IND	S	—	—	
				L	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}$"A" = $\overline{CE}$"B" = V_{IH} f = f_{MAX}[2]	COM'L	S	30	65	mA
				L	30	45	
			IND	S	—	—	
				L	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[2]	COM'L	S	80	155	mA
				L	80	125	
			IND	S	—	—	
				L	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}$"A" and $\overline{CE}$"B" ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[3]	COM'L	S	1.0	15	mA
				L	0.2	5	
			IND	S	—	—	
				L	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled, f = f_{MAX}[2]	COM'L	S	70	150	mA
				L	70	120	
			IND	S	—	—	
				L	—	—	

2654 tbl 06b

NOTES:

1. 'X' in part numbers indicates power rating (S or L).
2. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
3. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
4. V_{CC}=5V, T_A=+25°C for Typ, and is not production tested.
5. Port "A" may be either left or right port. Port "B" is opposite from port "A".

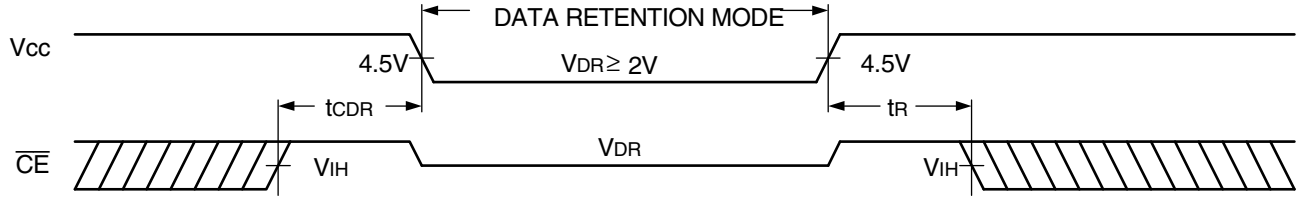
Data Retention Characteristics (L Version Only)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V, $\overline{CE} \geq V_{CC}$ - 0.2V	IND.	—	100	4000	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2	COM'L.	—	100	1500	
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	V

2654 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but is not production tested.

Data Retention Waveform



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AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2654 tbl 08

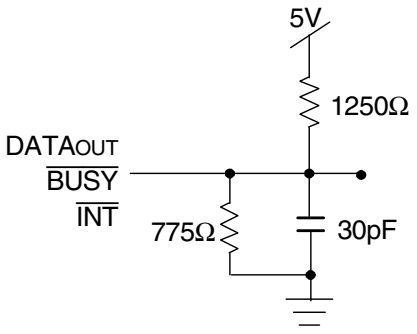

Figure 1. AC Output Test Load

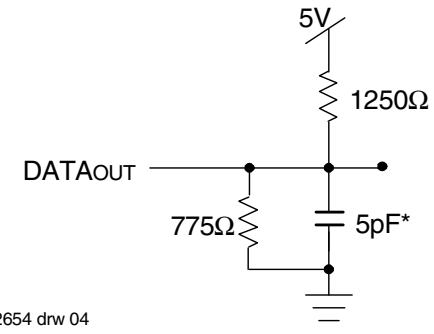

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Figure 2. Output Test Load
(For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(3)

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	25	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	12	—	25	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	ns
t_{LZ}	Output Low-Z Time(1,2)	0	—	0	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	15	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	50	—	50	ns

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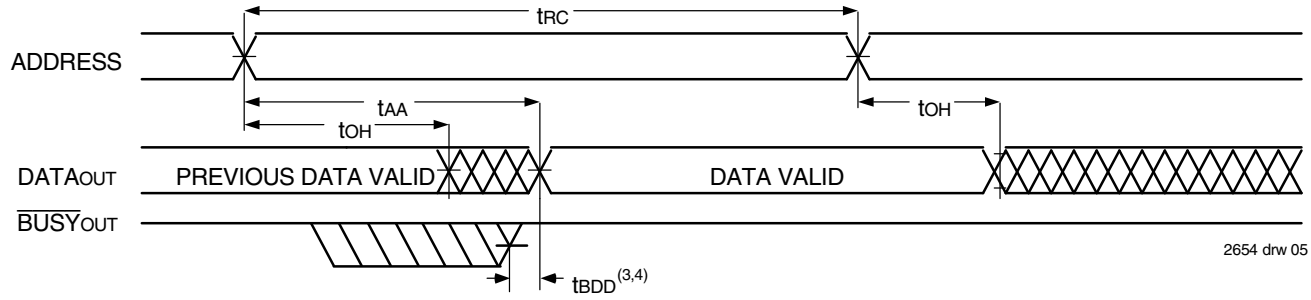
Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	55	—	ns
t_{AA}	Address Access Time	—	55	ns
t_{ACE}	Chip Enable Access Time	—	55	ns
t_{AOE}	Output Enable Access Time	—	35	ns
t_{OH}	Output Hold from Address Change	0	—	ns
t_{LZ}	Output Low-Z Time(1,2)	0	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	30	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	50	ns

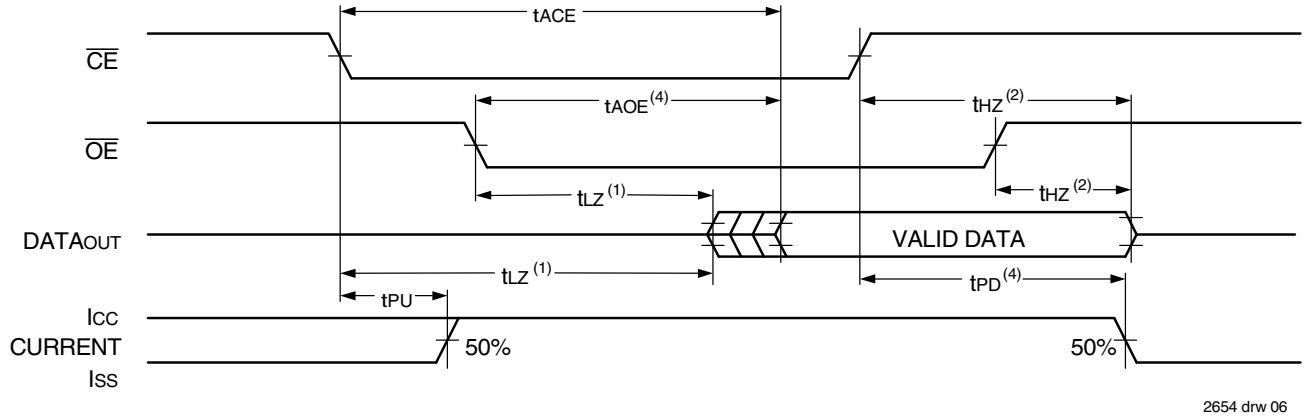
2654 tbl 09b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Read Cycle No. 1, Either Side(1,2,4)



Timing Waveform of Read Cycle No. 2, Either Side(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. t_{BDD} delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, t_{AOE}, t_{ACE}, t_{AA}, or t_{BDD}.
5. R/$\overline{W}$ = V_{IH}, $\overline{CE}$ = V_{IL}, and $\overline{OE}$ = V_{IL}, and the address is valid prior to other coincidental with $\overline{CE}$ transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4]

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time [4]	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width[6]	20	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	20	—	ns
t_{HZ}	Output High-Z Time[1,2,3]	—	10	—	15	ns
t_{DH}	Data Hold Time[5]	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,3]	—	10	—	15	ns
t_{OW}	Output Active from End-of-Write[1,2,3,5]	0	—	0	—	ns

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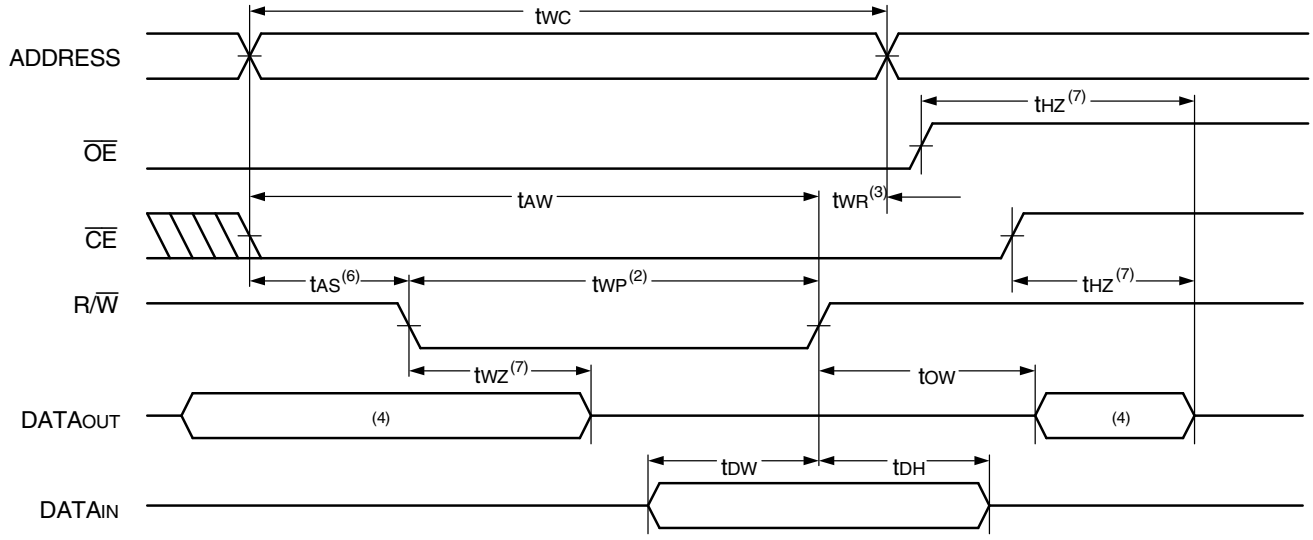
Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
WRITE CYCLE				
t_{WC}	Write Cycle Time[4]	55	—	ns
t_{EW}	Chip Enable to End-of-Write	40	—	ns
t_{AW}	Address Valid to End-of-Write	40	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WP}	Write Pulse Width[6]	40	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	ns
t_{HZ}	Output High-Z Time[1,2,3]	—	30	ns
t_{DH}	Data Hold Time[5]	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,3]	—	30	ns
t_{OW}	Output Active from End-of-Write[1,2,3,5]	0	—	ns

2654 tbl 10b

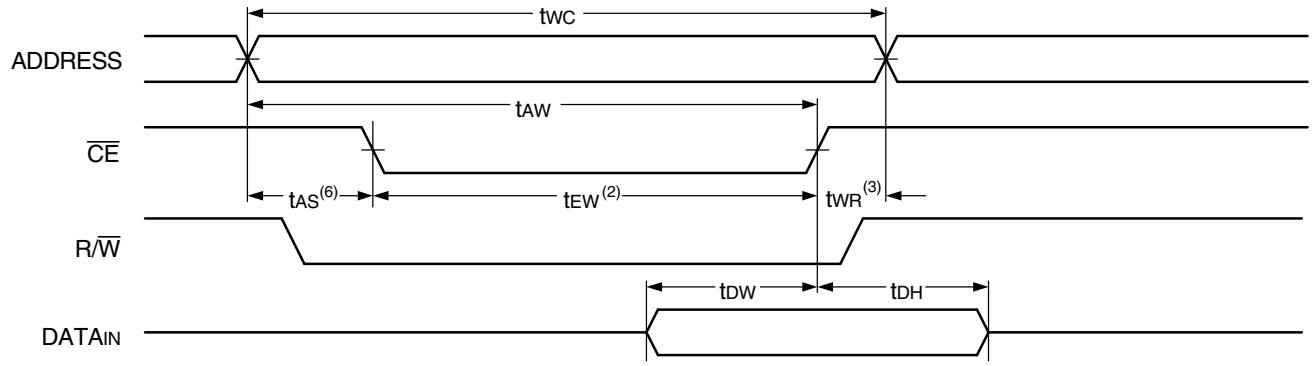
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$, since R/$\overline{W}$ = V_{IL} must occur after t_{BAA} .
4. 'X' in part numbers indicates power rating (S or L).
5. The specified t_{DH} must be met by the device supplying write date to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature. The actual t_{DH} will always be smaller than the actual t_{OW}.
6. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



2654 drw 07

Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,5)



2654 drw 08

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and a R/$\overline{W}$ = V_{IL}
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(6)

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (For MASTER IDT70121)						
t_{BAA}	BUSY Access Time from Address	—	20	—	20	ns
t_{BDA}	BUSY Disable Time from Address	—	20	—	20	ns
t_{BAC}	BUSY Access Time from Chip Enable	—	20	—	20	ns
t_{BDC}	BUSY Disable Time from Chip Enable	—	20	—	20	ns
t_{WDD}	Write Pulse to Data Delay(1)		50		60	
t_{DDD}	Write Data Valid to Read Data Delay(1)		35		45	
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	BUSY Disable to Valid Data(3)	—	30	—	30	ns
t_{WH}	Write Hold After BUSY(5)	15	—	20	—	ns
BUSY INPUT TIMING (For SLAVE IDT70125)						
t_{WB}	Write to BUSY Input(4)	0	—	0	—	ns
t_{WH}	Write Hold After BUSY(5)	15	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	45	ns

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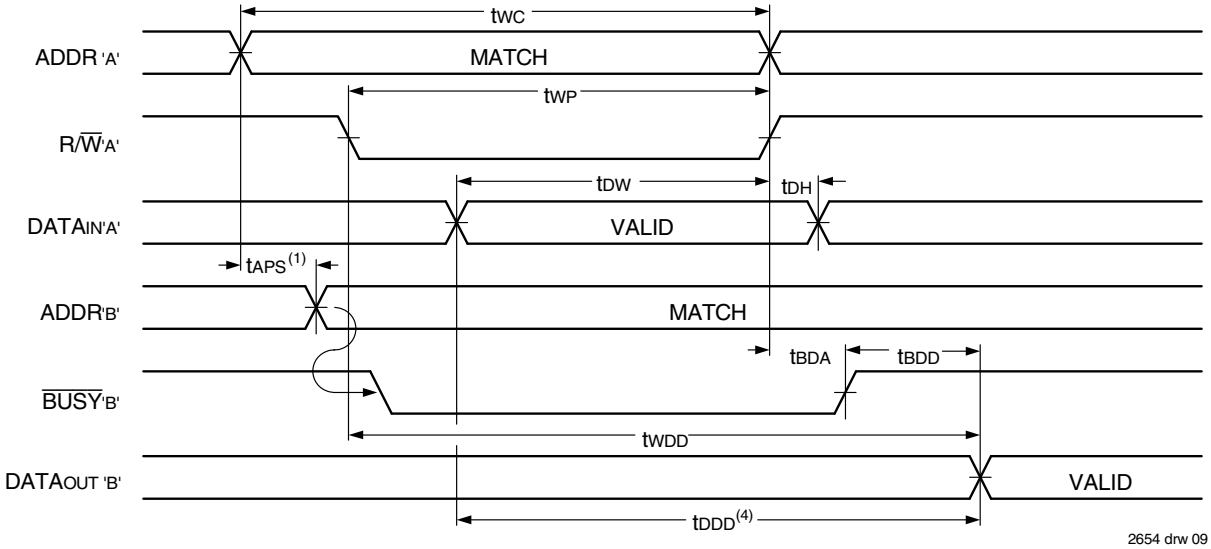
Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
BUSY TIMING (For MASTER IDT 70121)				
t_{BAA}	BUSY Access Time from Address	—	30	ns
t_{BDA}	BUSY Disable Time from Address	—	30	ns
t_{BAC}	BUSY Access Time from Chip Enable	—	30	ns
t_{BDC}	BUSY Disable Time from Chip Enable	—	30	ns
t_{WDD}	Write Pulse to Data Delay(1)		80	
t_{DDD}	Write Data Valid to Read Data Delay(1)		65	
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	ns
t_{BDD}	BUSY Disable to Valid Data(3)	—	45	ns
t_{WH}	Write Hold After BUSY(5)	20	—	ns
BUSY INPUT TIMING (For SLAVE IDT 70125)				
t_{WB}	Write to BUSY Input(4)	0	—	ns
t_{WH}	Write Hold After BUSY(5)	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	65	ns

2654 tbl 11b

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY.
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
5. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
6. 'X' in part numbers indicates power rating (S or L).

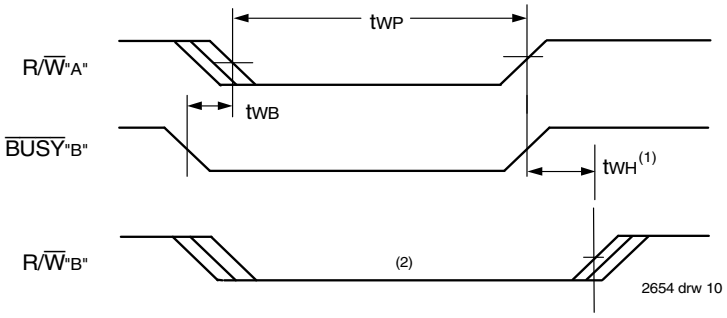
Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (1,2,3)



2654 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for Slave (IDT70125).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

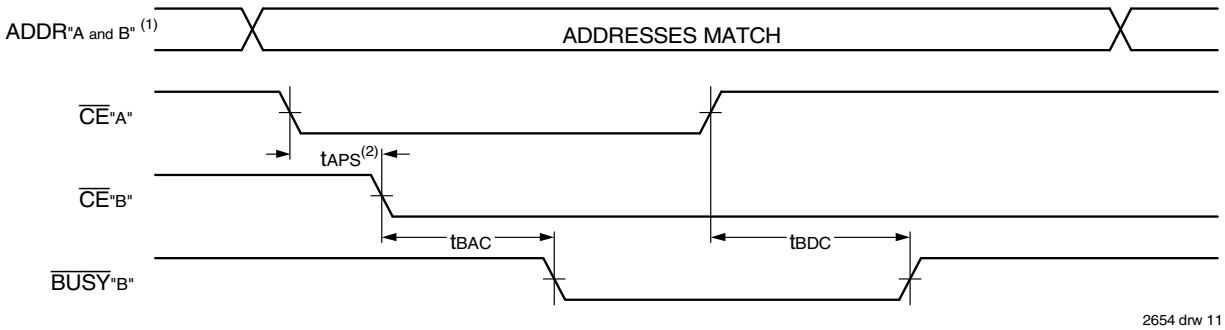
Timing Waveform of Write with $\overline{BUSY}$ (3)



2654 drw 10

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) and output (master).
2. $\overline{BUSY}$ is asserted on port 'B' blocking R/$\overline{W}$'B', until $\overline{BUSY}$'B' goes HIGH.
3. All timing is the same for left and right ports. Port"A" may be either left or right port. Port "B" is the opposite from port "A".

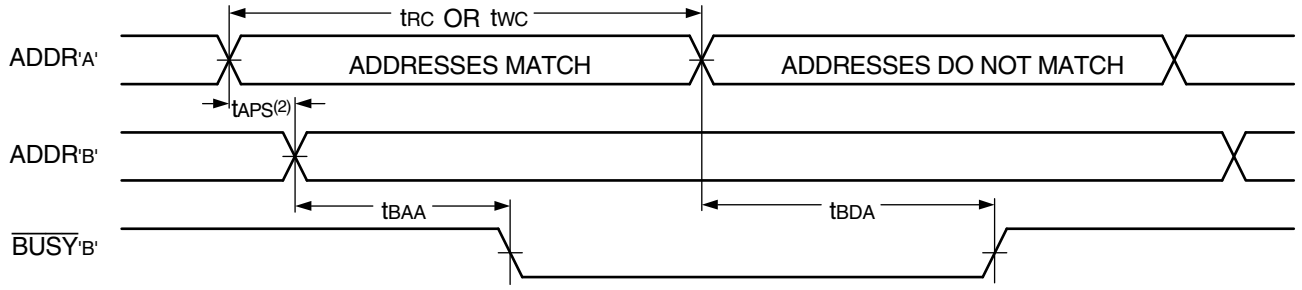
Timing Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing (1)



2654 drw 11

NOTES:
1. All timing is the same for left and right ports. Port “A” may be either left or right port. Port “B” is the opposite from port “A”.
2. If tAPS is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (70121 only).

Timing Waveform of $\overline{BUSY}$ Arbitration Controlled by Address(1)



2654 drw 12

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If t_{APS} is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (70121 only).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
INTERRUPT TIMING						
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	35	ns
t_{INR}	Interrupt Reset Time	—	25	—	35	ns

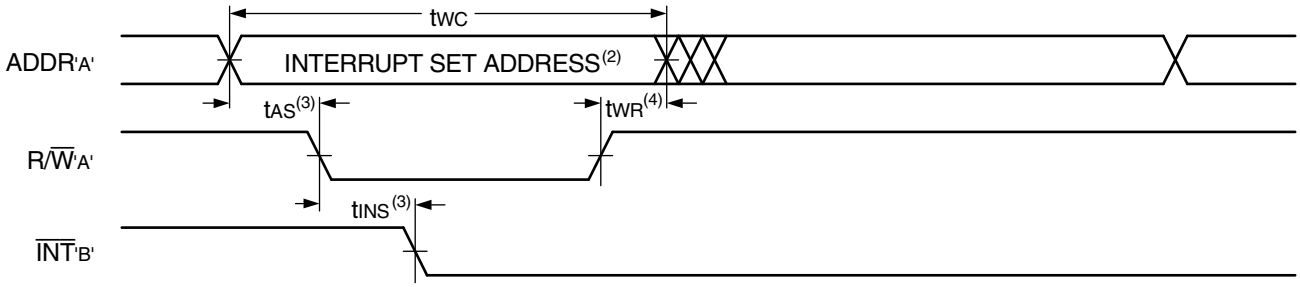
2654 tbl 12a

Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
INTERRUPT TIMING				
t_{AS}	Address Set-up Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{INS}	Interrupt Set Time	—	45	ns
t_{INR}	Interrupt Reset Time	—	45	ns

2654 tbl 12b

NOTES:
1. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Interrupt Mode(1)



2654 drw 13

NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

Truth Tables

Truth Table I. Non-Contention Read/Write Control(4)

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disable and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power-DownMode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory(2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port(3)
H	L	H	Z	High-Impedance Outputs

2654 tbl 13

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

Truth Table II. Interrupt Flag(1,4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{10L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{10R}-A_{0R}	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2654 tbl 14

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = V_{IH}
2. If $BUSY_L$ = V_{IL}, then No Change.
3. If $BUSY_R$ = V_{IL}, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

Functional Description

The IDT70121/125 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70121/125 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per Truth Table II. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag (INT_R) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag (INT_R), the right port must access the memory location 7FF. The message (9 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “busy”. The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of $\overline{BUSY}$ logic is not desirable, the $\overline{BUSY}$ logic can be disabled by using the IDT70125 (SLAVE). In the IDT70125, the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT70121/125 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array requires the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70121/125 RAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the RAM array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT70121 RAM the $\overline{BUSY}$ pin is an output of the part, and the BUSY pin is an input of the IDT70125 as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{BUSY}$ on one side of the array and another master indicating $\overline{BUSY}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and

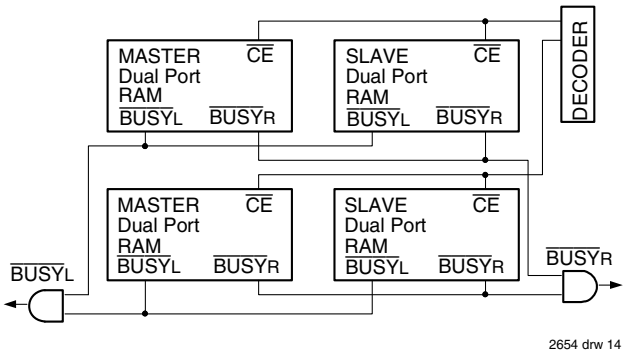
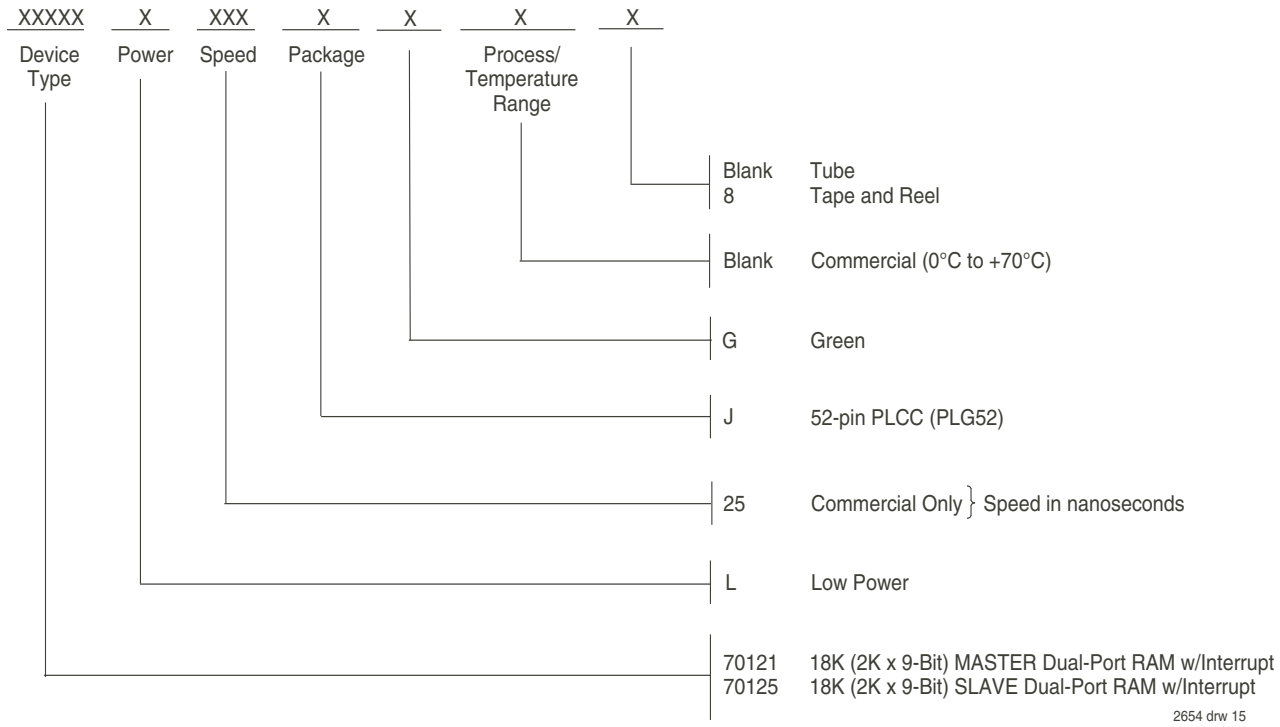


Figure 3. Busy and chip enable routing for both width and depth expansion with 70121 (Master) and 70125 (Slave) RAMs.

inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Ordering Information



NOTES:

LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02.

Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
25	70121L25JG	PLG52	PLCC	C
	70121L25JG8	PLG52	PLCC	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
25	70125L25JG	PLG52	PLCC	C
	70125L25JG8	PLG52	PLCC	C

Datasheet Document History

01/06/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
	Pages 2 and 3	Added additional notes to pin configurations
06/03/99:		Changed drawing format
	Page 1	Corrected DSC number
05/28/04:	Page 3	Changed storage temperature parameter from -55 to +125 to -65 to +150
		Clarified T_A parameter footnote
	Page 4	DC Electrical parameters–changed test condition wording from "open" to "disabled"
	Page 9	Changed ±500mV to 0mV in notes
	Page 2	Added date revision for pin configuration
	Page 4, 6, 8,10&12	Added Industrial temp to column headings for 35ns speed to DC and AC Electrical Characteristics
	Page 4	Removed Industrial temp from 25, 45 & 55ns speeds from DC Electrical Characteristics
	Page 3, 4, 6, 8,10&12	Removed Industrial temp footnote from all tables
	Page 10	Corrected error in AC $\overline{BUSY}$ timing tables changing 71V33 to 70121 and changing 71V43 to 70125
	Page 15	Added Industrial temp offering to 35ns ordering information
	Page 1 & 15	Replaced old ™ logo with new ™ logo
	Page 6	Footnote reference 5 removed from AC Electrical Characteristics READ table
	Page 1	Changed wording of footnote 1 from "$\overline{INT}$ is totem-pole output" to "$\overline{INT}$ is non-tr-stated push-pull output"
	Page 5	Updated AC Test Conditions Input Rise/Fall Times from 5ns to 3ns
04/05/06:	Page 1	Added green availability to features
	Page 15	Added green indicator to ordering information
10/21/08:	Page 15	Removed "IDT" from orderable part number
08/05/14:	Page 1	Added green availability to Features
	Page 15	Added green indicator to Ordering Information
	Page 2 &15	The package code for the J52-1 changed to J52 to match standard package code
	Page 15	Added Tape and Reel to Ordering Information
08/27/14:	Page 1	Removed 45ns commercial speed grade from Features High-speed access information
	Page 1-16	Removed 45ns commercial speed grade throughout the datasheet to correct a discrepancy in IDT's product catalog
	Page 4	Specifically including the DC Chars table
	Page 6,8,10&12	Specifically including the AC Chars tables
	Page 15	Removed 45ns commercial speed grade from the Ordering Information
10/10/17:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
09/16/19:	Page 1 & 15	Deleted obsolete Commercial speed grades 35/55ns and Industrial speed grade 35ns
	Page 2	Rotated PLG52 PLCC pin configuration to accurately reflect pin 1 orientation
	Page 15	Added Orderable Part Information table

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

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