

74HC00; 74HCT00

Quad 2-input NAND gate

Rev. 9 — 22 October 2021

Product data sheet

1. General description

The 74HC00; 74HCT00 is a quad 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
 - For 74HC00: CMOS level
 - For 74HCT00: TTL level
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC00D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT00D				
74HC00PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT00PW				
74HC00BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT00BQ				

4. Functional diagram

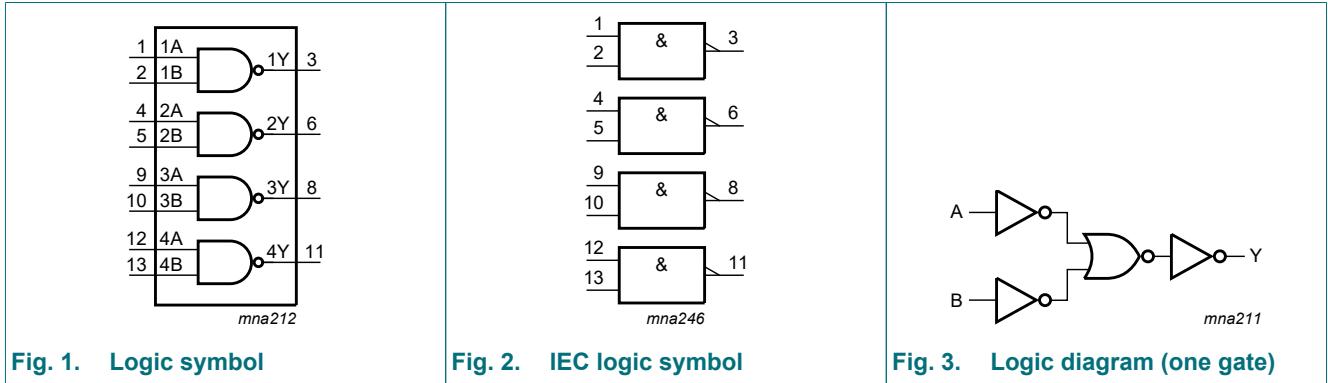


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one gate)

5. Pinning information

5.1. Pinning

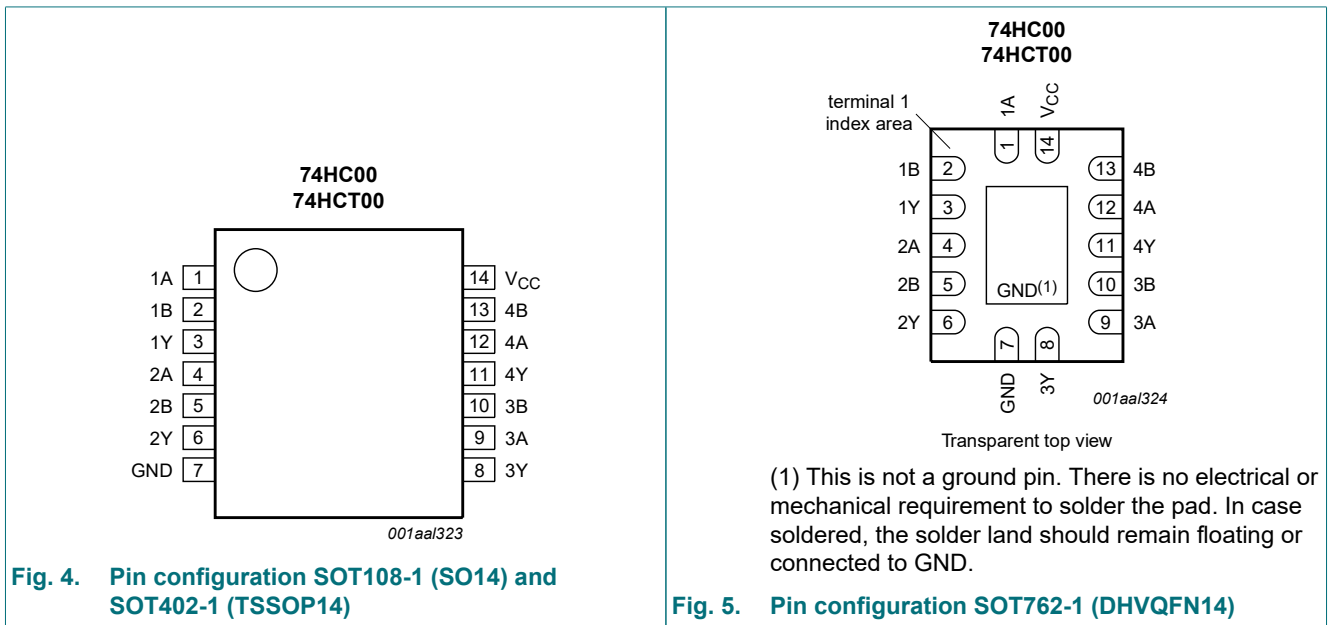


Fig. 4. Pin configuration SOT108-1 (SO14) and SOT402-1 (TSSOP14)

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC00			74HCT00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC00										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	-	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	-	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	-	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	-	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	-	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	-	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	-	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	-	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	-	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	-	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	-	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	-	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	-	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	-	-	±1	-	±1	μA
		V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	-	-	20	-	40	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT00										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	-	4.5	-	4.4	-	4.4	-	V
V _{OL}	LOW-level output voltage	I _O = -4.0 mA	-	4.32	-	3.84	-	3.7	-	V
		V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
V _{OL}	LOW-level output voltage	I _O = 20 μA	-	0	-	-	0.1	-	0.1	V
		I _O = 4 mA	-	0.15	-	-	0.33	-	0.4	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	-	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	-	-	20	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	150	-	-	675	-	735	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC00										
t _{pd}	propagation delay	nA, nB to nY; see Fig. 6 [1]								
		V _{CC} = 2.0 V	-	25	-	-	115	-	135	ns
		V _{CC} = 4.5 V	-	9	-	-	23	-	27	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	7	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	7	-	-	20	-	23	ns
t _t	transition time	see Fig. 6 [2]								
		V _{CC} = 2.0 V	-	19	-	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	-	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	-	-	16	-	19	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	22	-	-	-	-	-	pF
74HCT00										
t _{pd}	propagation delay	nA, nB to nY; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	12	-	-	24	-	29	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	10	-	-	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see Fig. 6 [2]	-	-	-	-	29	-	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V [3]	-	22	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑ (C_L × V_{CC}² × f_o) = sum of outputs.

10.1. Waveforms and test circuit

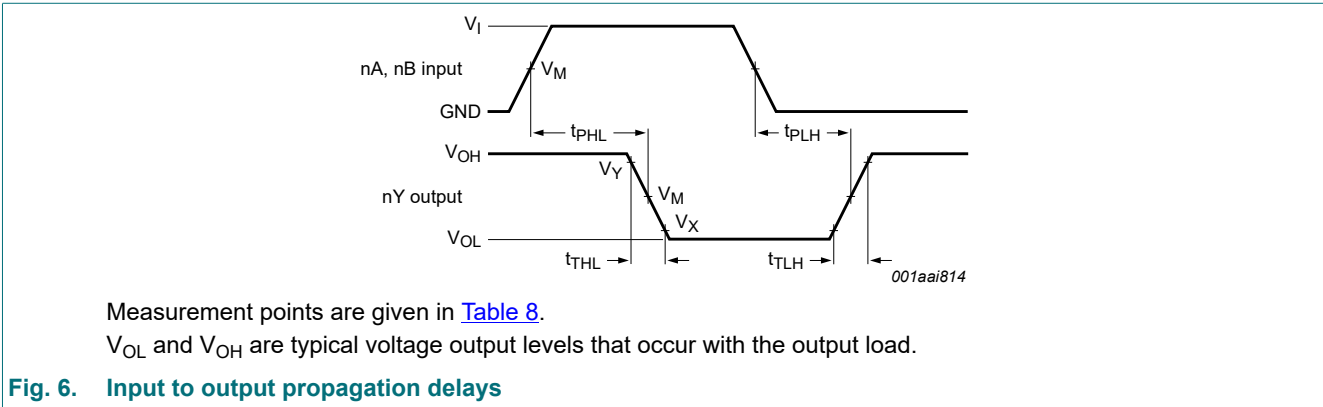


Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC00	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT00	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

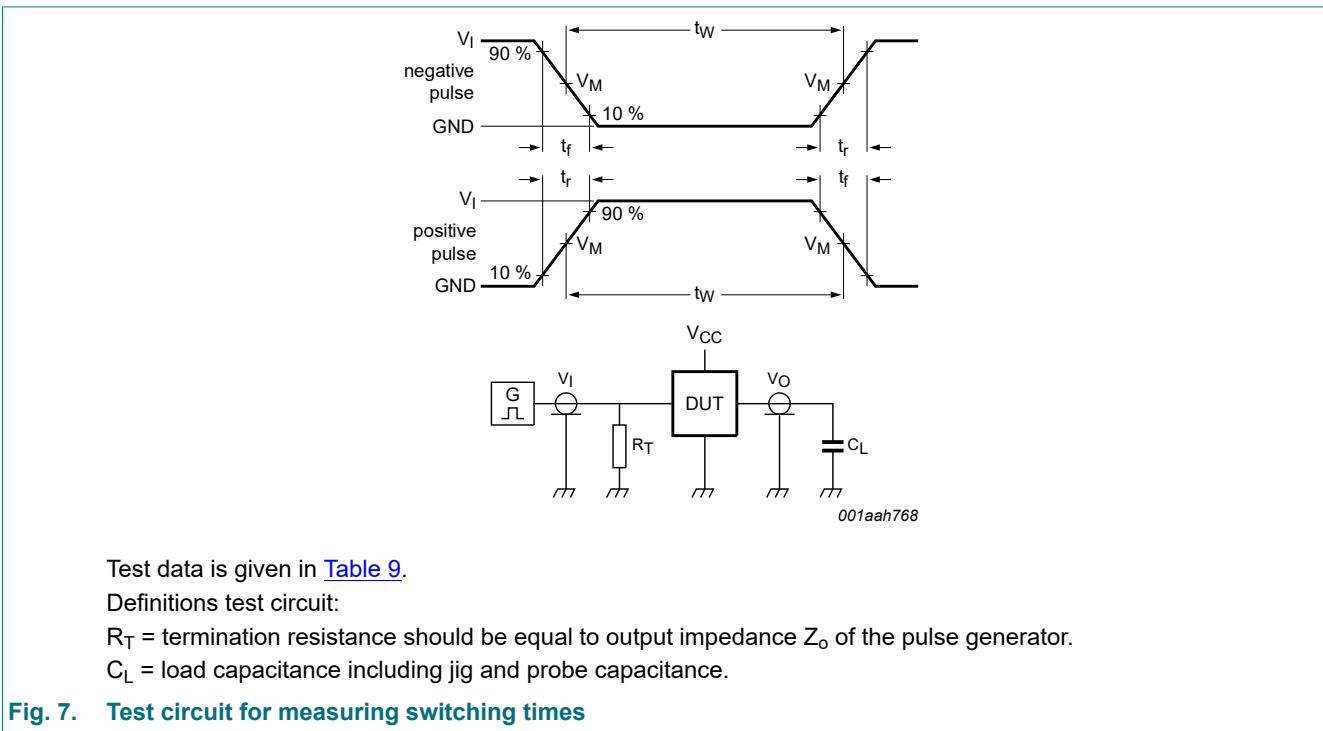


Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC00	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT00	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

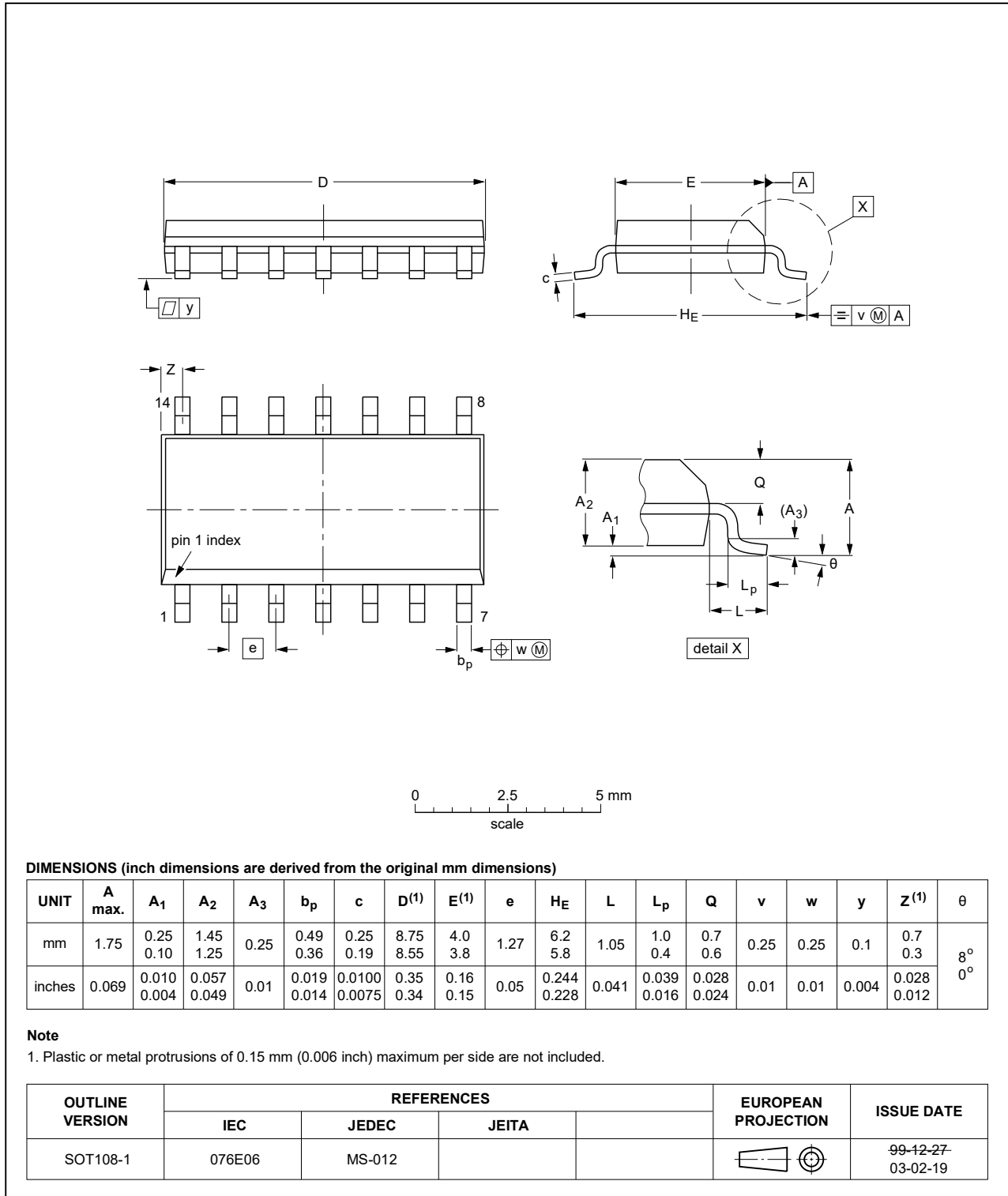


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

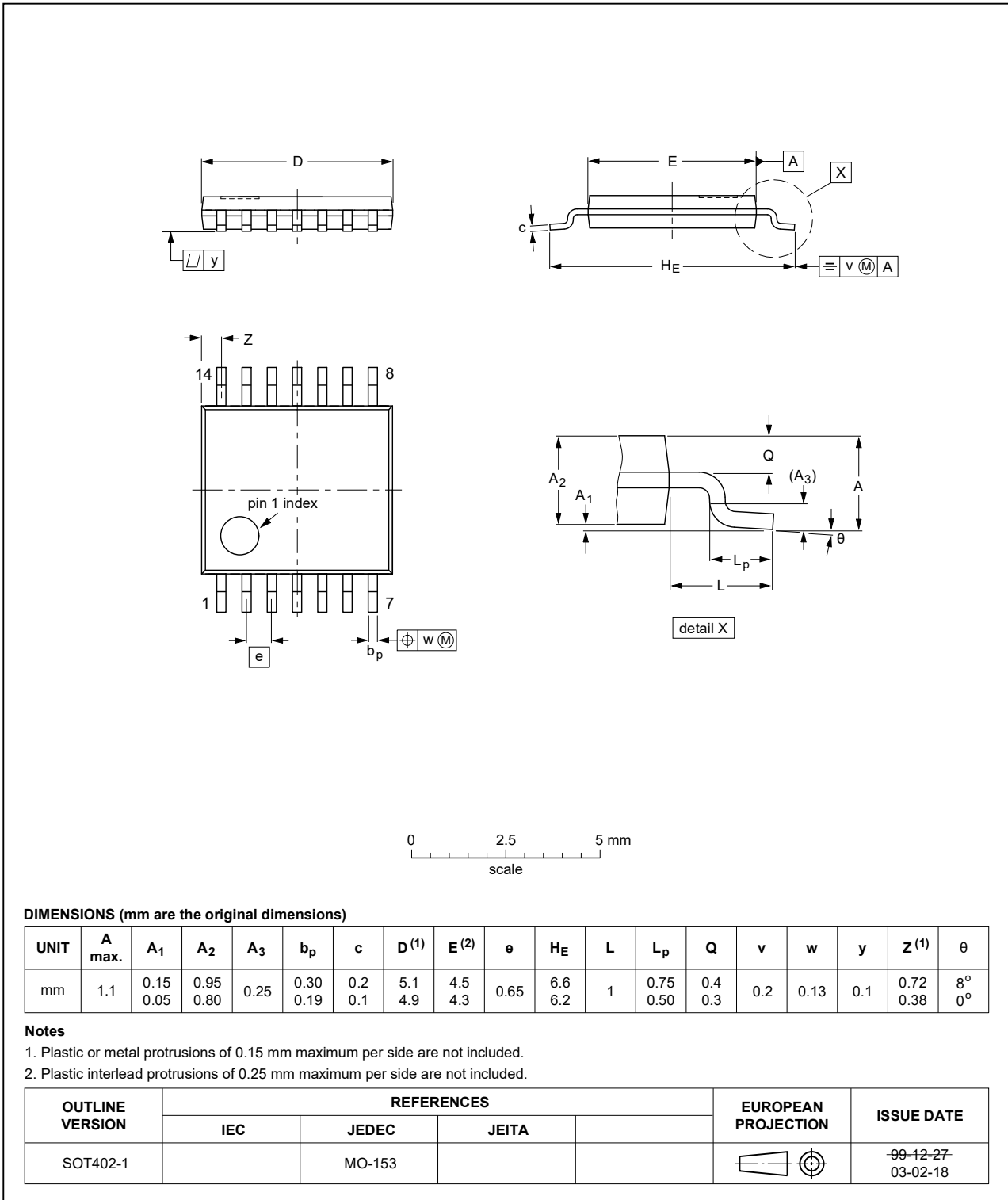


Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

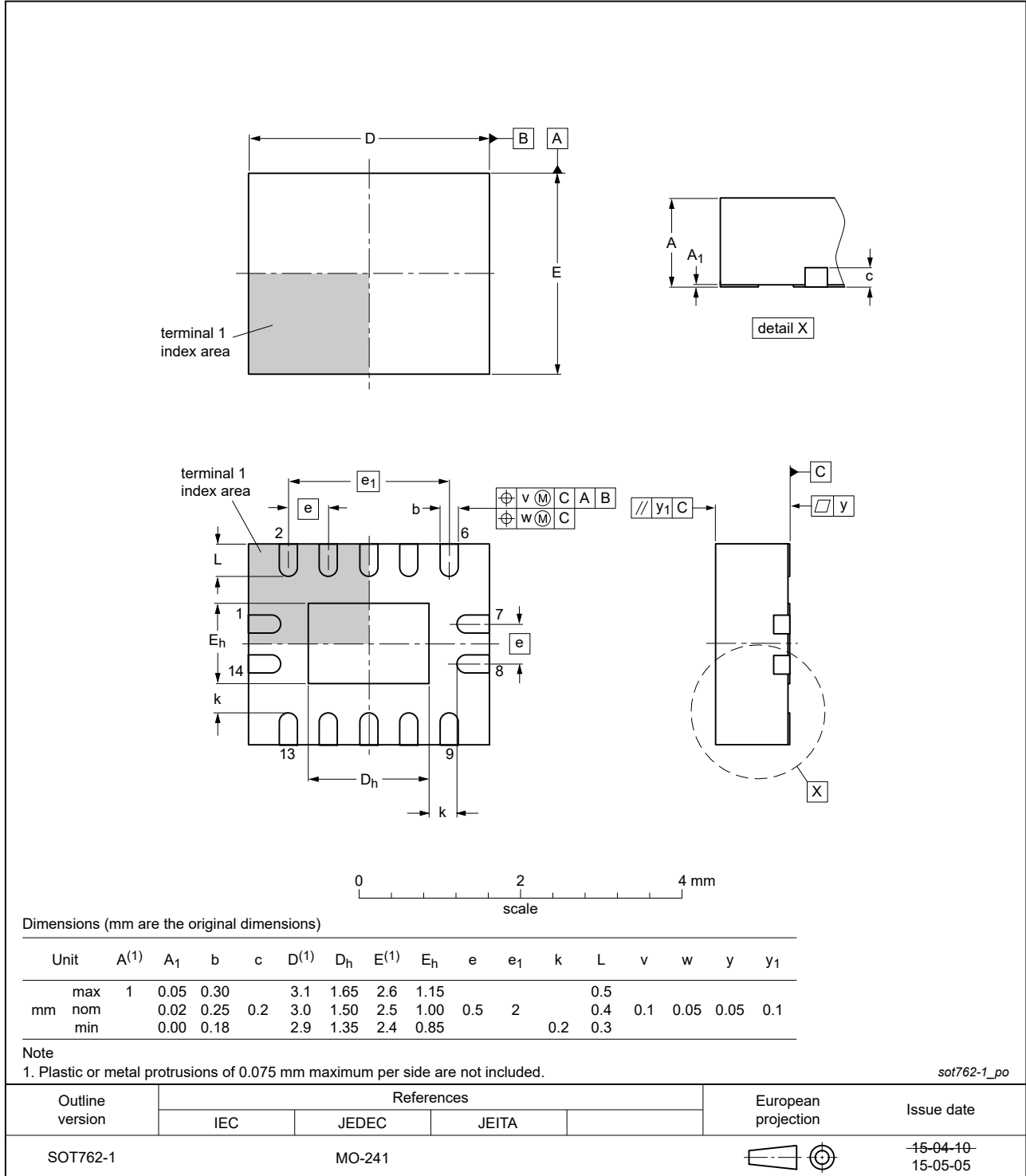


Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT00 v.9	20211022	Product data sheet	-	74HC_HCT00 v.8
Modifications:	<ul style="list-style-type: none"> • Section 9: V_{OL} condition for 74HCT00 corrected. (Errata) 			
74HC_HCT00 v.8	20210810	Product data sheet	-	74HC_HCT00 v.7
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC00DB and 74HCT00DB (SOT337-1/SSOP14) removed. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation have been updated. 			
74HC_HCT00 v.7	20151125	Product data sheet	-	74HC_HCT00 v.6
Modifications:	<ul style="list-style-type: none"> • Type numbers 74HC00N and 74HCT00N (SOT27-1) removed. 			
74HC_HCT00 v.6	20111214	Product data sheet	-	74HC_HCT00 v.5
Modifications:	<ul style="list-style-type: none"> • Legal pages updated. 			
74HC_HCT00 v.5	20101125	Product data sheet	-	74HC_HCT00 v.4
74HC_HCT00 v.4	20100111	Product data sheet	-	74HC_HCT00 v.3
74HC_HCT00 v.3	20030630	Product data sheet	-	74HC_HCT00_CNV v.2
74HC_HCT00_CNV v.2	19970826	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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